A new possible MSADC Carrier Board

1. **Main Data Processing Device:** *Plain FPGA, SOC-FPGA or MPSOC-FPGA?*

2. **Hardware Design Approach:** *Single board or Carrier + System on Module?*

3. ***A survey of inspiring commercial products***

Selection of Main Data Processing Device

Main considerations

- **Required Functionalities:** Peripheral ports and Connectivity, External memory, Booting options, . . .
- **uP performance:** nr of cores, bus width, clock freq, cache, DMA, interrupts, . . .
- **Logic resources**: CLB, memory blocks, DSP blocks, IOs, High Speed Links, . . .
- **Cost:** per unit, and total system cost including associated components (RAM, ROM, Clock gen, Volt regs, . . .)
- **Power consumption and dissipation:** average, peak, max temperature, heat dissipator, fan, . . .
- **Design time and Complexity:** HDL, Embedded uP Operating System, SW programming, Debugging, . . .
- **EDA Tools and Support:** Paid/free licenses, third party IP cores, Libraries, open ref designs, . . .
- **Obsolescence and Maintenance:** EDA tools, Embedded Operative System, SW design environment, . . .
- **Scalability and Upgradeability:** Pin compatibility with larger devices, Memory expansion, . . .
- **Portability:** Porting of HDL design and software programs to other FPGA vendor or device families, . . .

Hardware Design

Main considerations

- **Modularity**: Single Board vs Carrier & SOM, Onboard Memory (soldered vs SODIMM)
- **Size**, **Power Supply** (V ranges and I max), connectors, Over Volt/Current protections, shielding
- **Main Services**: Remote control, Voltage/Temp monitoring, SMD Card, Debugging facilities, Cooling,
- **Connectors**: Power, Ethernet, Optical links, JTAG, USB, Data specific, General purpose, . . .
- **PCB Technology**: Nr of layers, Thickness, Min trace width, Buried vias, Impedance control,
- **Performance**: Max working frequency, Trace equalization, Mechanical robustness,
- **Budget**: Prototyping, Small volume, and Mass production, Possible redesigns & iterations
- **Design time and complexity**: Schematics, Layout, PCB production, Debugging, Components availability
- **Software EDA Tools and Support:** Commercial, Open source, Cost free, CAD and Libraries,
- **Obsolescence and Maintenance:** Components life cycle, Repairing,
- **Expandability and Versatility:** Adaptability and reutilization in other contexts or for other applications

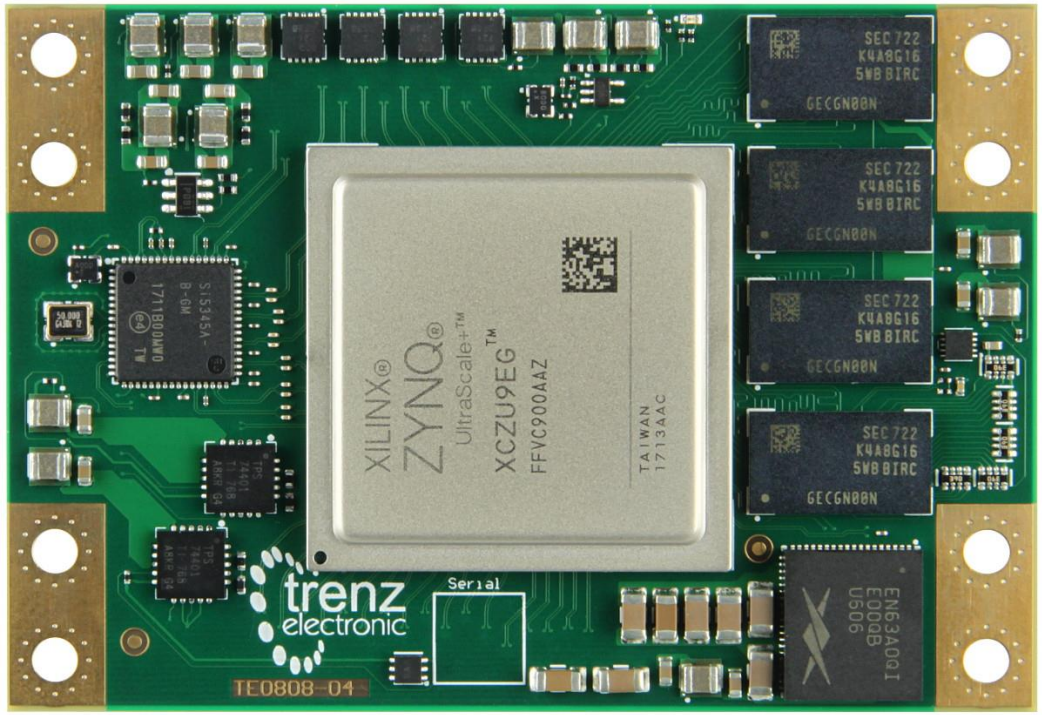
FPGA SOC System On Module

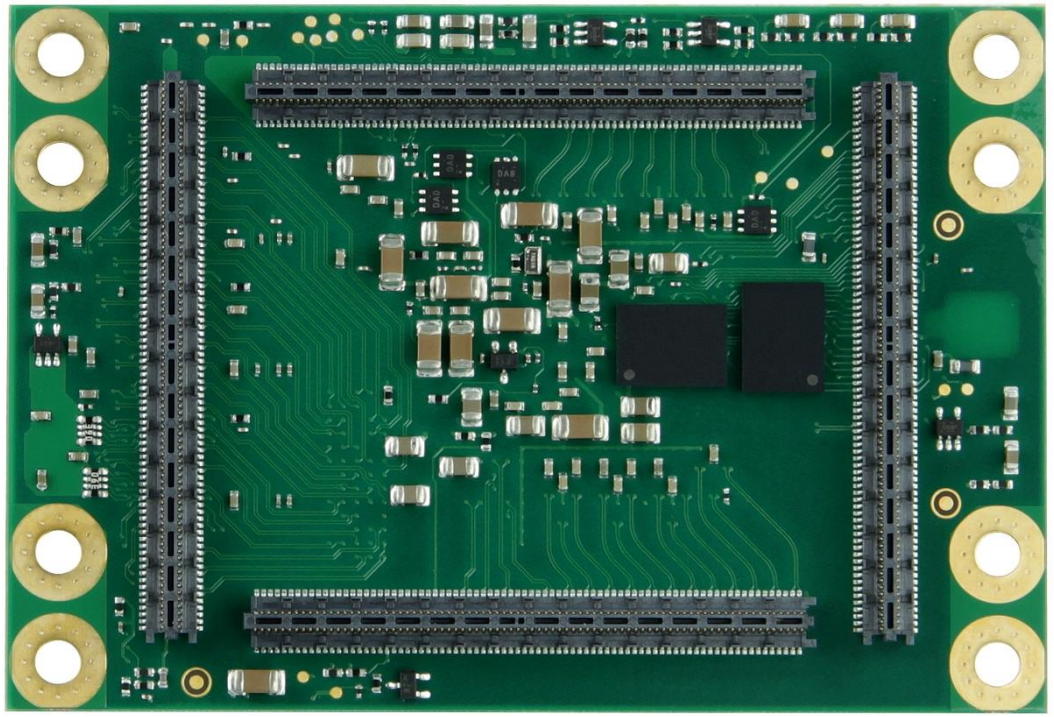
- Positive aspects
  - To encapsulate a complex SoC FPGA along with essential common components in order to facilitate the design of large hardware systems avoiding risk of errors related to critical interconnections such as between SoC FPGA and DDR memories.
  - To standardize a board to board connection to facilitate hardware upgradeability, partial replacement and interchangeability.
  - To allow the HW designer to concentrate the efforts on the application specific aspects, relaying on an error-free partial system module.
  - Availability of several affordable commercial solutions and design support.

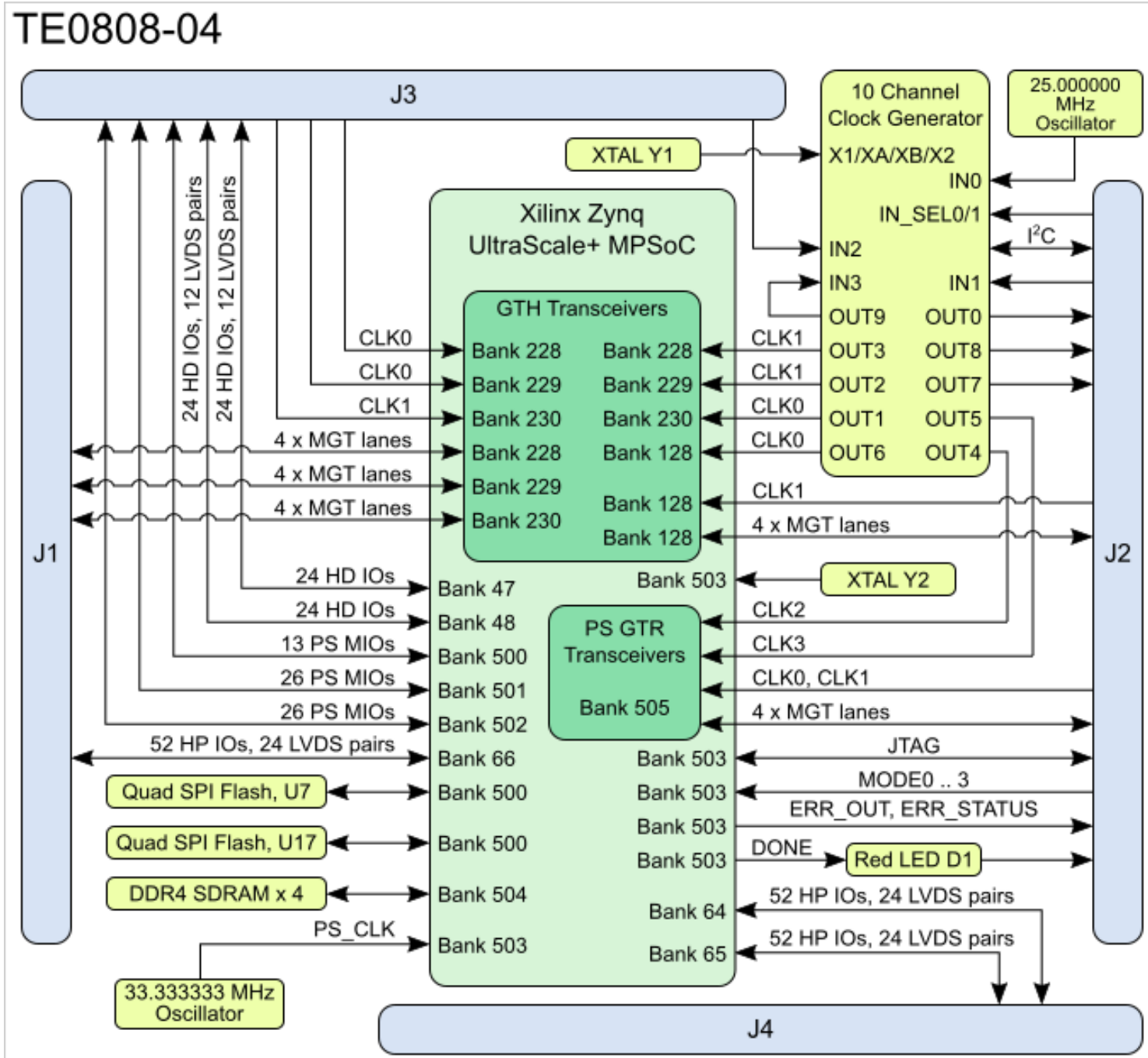
- Potential issues due to the quality of the board-to-board connectors
  - Some signals may experience speed degradation
  - Some extra cost
  - Electrical connection reliability
  - Precise and reliable mechanical mounting may need securing screws.

Commercial SoC FPGA SOM

UltraSOM+ MPSoC Module with Zynq UltraScale+ XCZU9EG-1FFVC900E, 4 GByte DDR4
(€1,064.00)





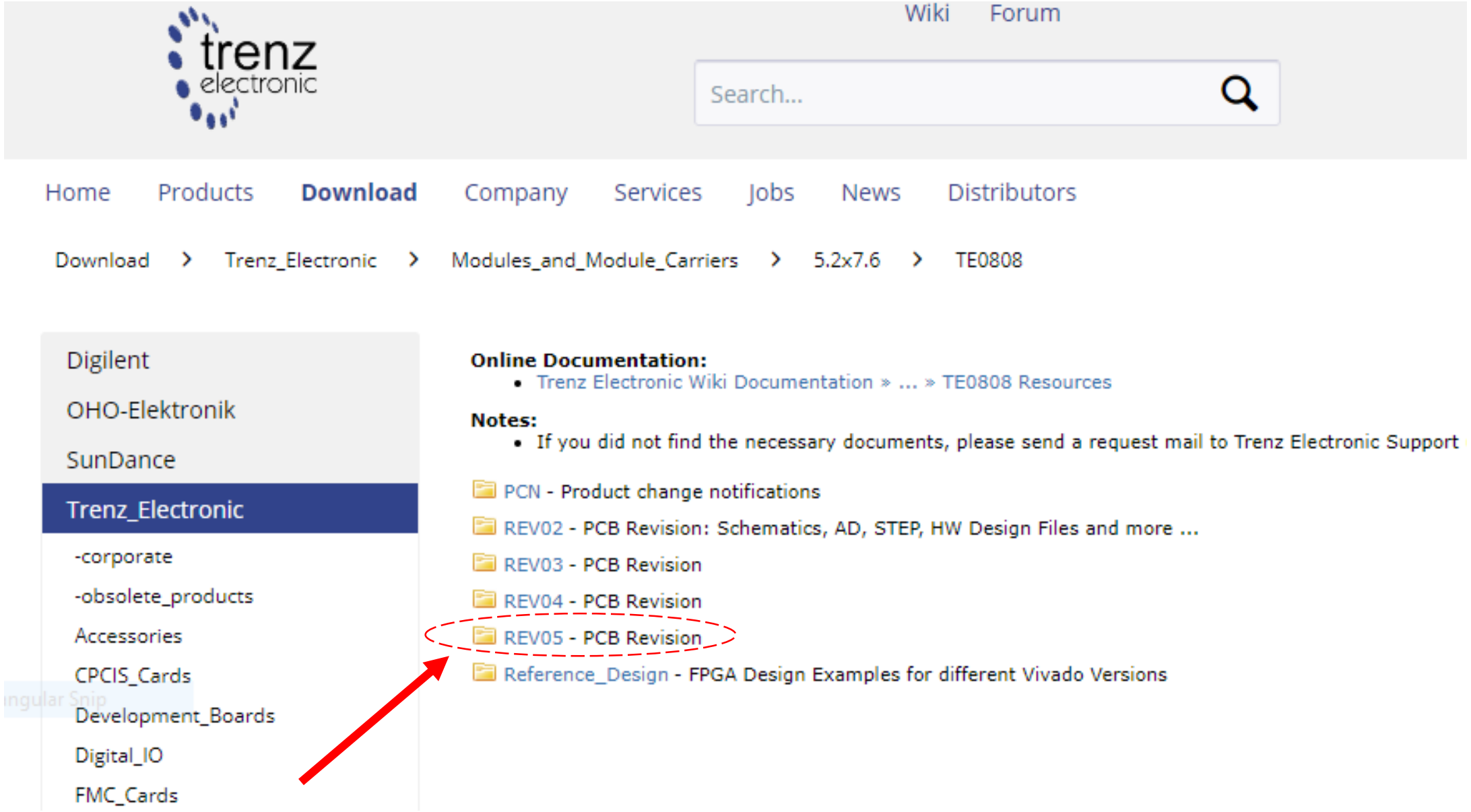

TE0808-04
J3
J1
J2
J4
10 Channel
Clock Generator
X1/XA/XB/X2
IN0
IN_SEL0/1
IN2
IN3
IN1
OUT9
OUT0
OUT3
OUT8
OUT2
OUT7
OUT1
OUT5
OUT6
OUT4
25.000000
MHz
Oscillator
XTAL Y1
XTAL Y2
I2C
Xilinx Zynq
UltraScale+ MPSoC
GTH Transceivers
Bank 228
Bank 229
Bank 230
Bank 128
PS GTR
Transceivers
Bank 505
Bank 47
Bank 48
Bank 500
Bank 501
Bank 502
Bank 66
Bank 503
Bank 504
Bank 64
Bank 65
24 HD IOs, 12 LVDS pairs
CLK0
CLK1
4 x MGT lanes
24 HD IOs
13 PS MIOs
26 PS MIOs
52 HP IOs, 24 LVDS pairs
CLK2
CLK3
CLK0, CLK1
JTAG
MODE0 .. 3
ERR_OUT, ERR_STATUS
DONE
Red LED D1
Quad SPI Flash, U7
Quad SPI Flash, U17
DDR4 SDRAM x 4
PS_CLK
33.333333 MHz
Oscillator

Main components description

Figure 2: TE0808 MPSoC module.

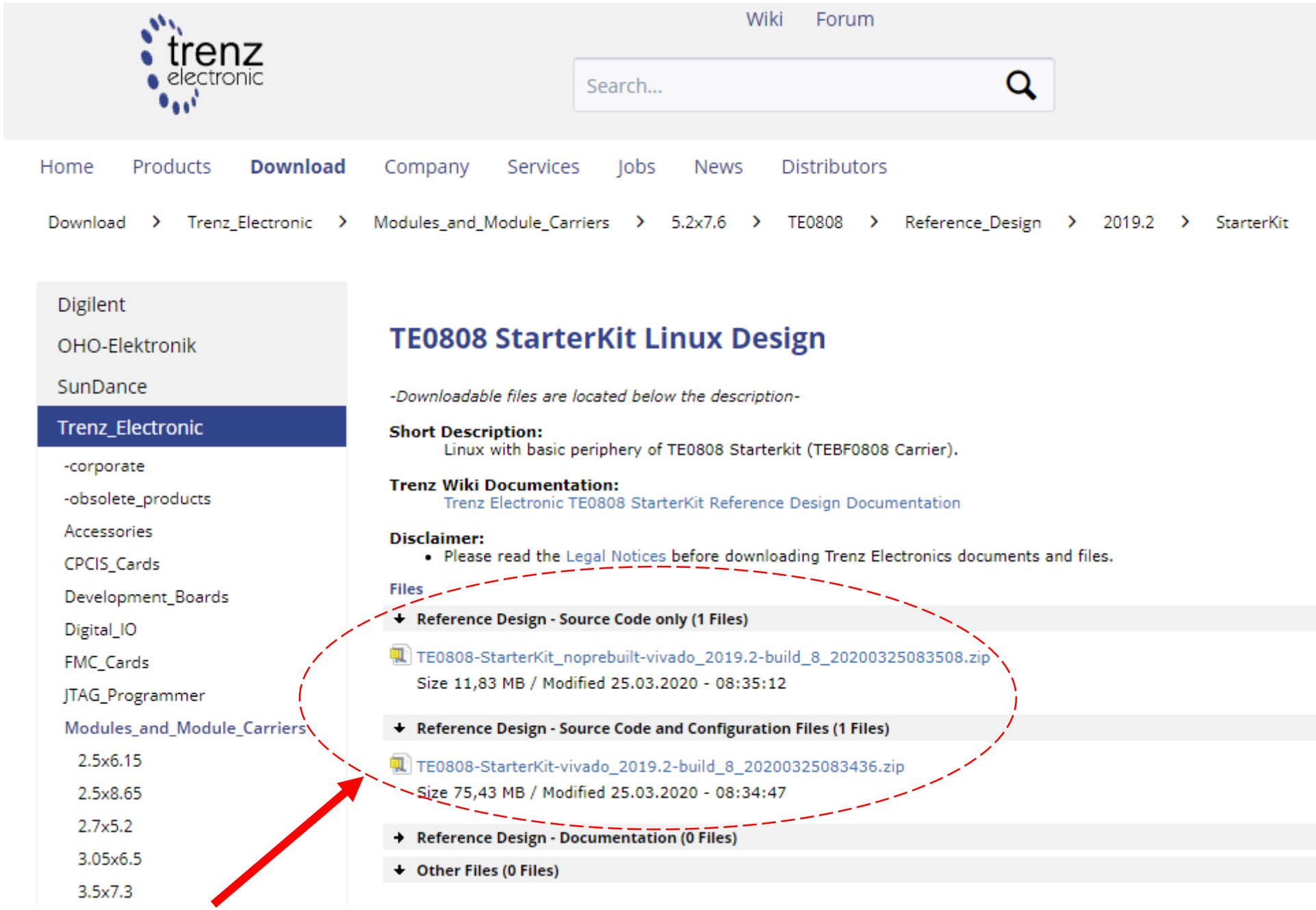
1. Xilinx ZYNQ UltraScale+ XCZU9EG MPSoC, U1
2. Low-power programmable oscillator @ 33.333333 MHz (PS_CLK), U32
3. Red LED (DONE), D1
4. 256Mx16 DDR4-2400 SDRAM, U12
5. 256Mx16 DDR4-2400 SDRAM, U9
6. 256Mx16 DDR4-2400 SDRAM, U2
7. 256Mx16 DDR4-2400 SDRAM, U3
8. 12A PowerSoC DC-DC converter, U4
9. Quartz crystal, Y1
10. Low-power programmable oscillator @ 25.000000 MHz (IN0 for U5), U25
11. 10-channel programmable PLL clock generator, U5
12. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J4
13. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J2
14. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J3
15. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J1
16. Quartz crystal, Y2
17. 256 Mbit serial NOR Flash memory, U7
18. 256 Mbit serial NOR Flash memory, U17

Design complexity



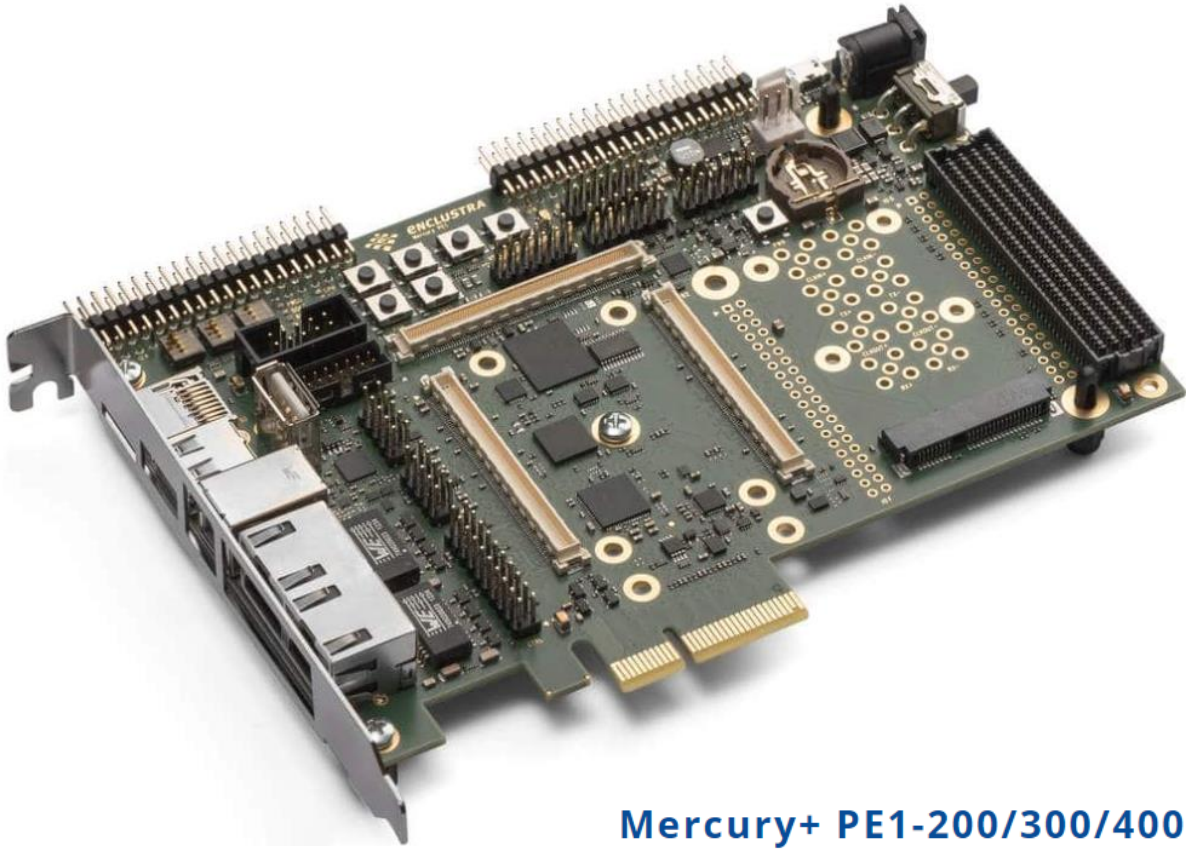
SW/Design Support

Availability of reference designs



SOM carrier board

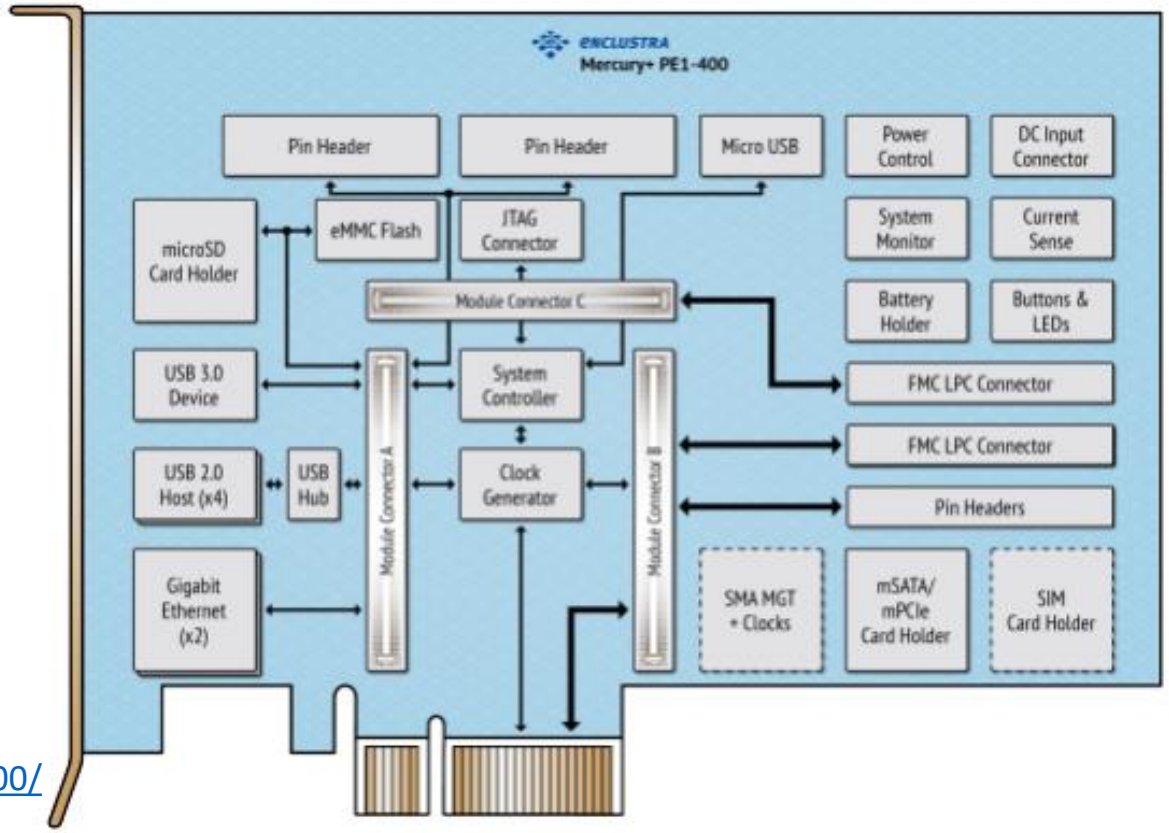
Base Board for Mercury/Mercury+ FPGA Modules



Mercury+ PE1-200/300/400

Board Architecture

Show board variant: PE1-200 - PE1-300 - **PE1-400**



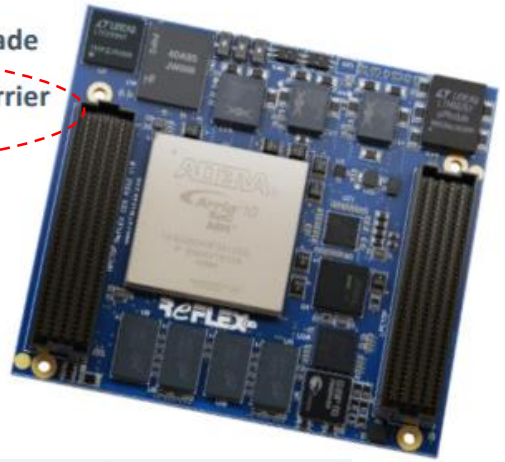
https://www.enclustra.com/en/products/base-boards/mercury-pe1-200-300-400/

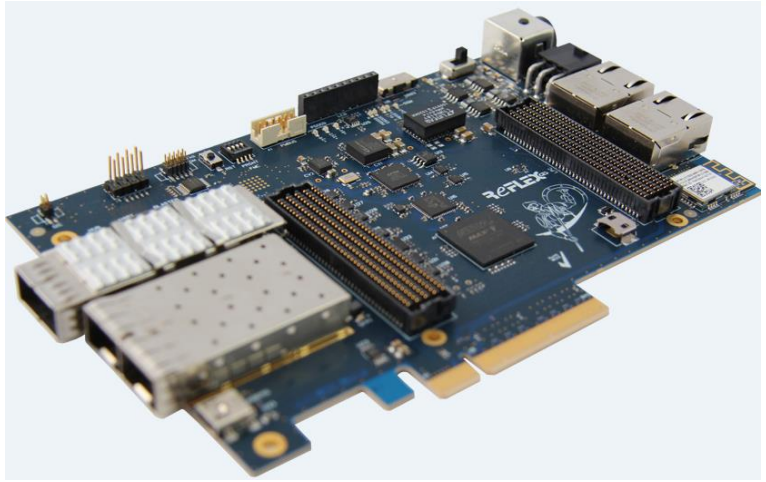
A commercial FPGA SOC SOM with FMC connectors (I)

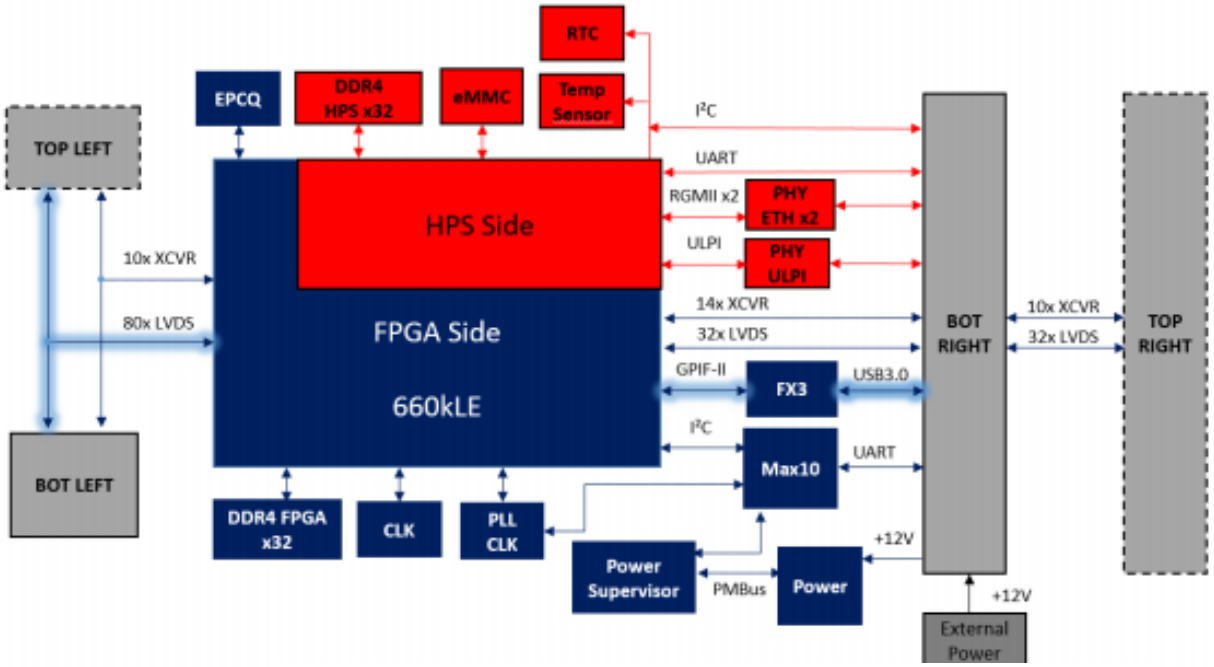
Arria 10 SoC SoM

System-on-Module featuring

- Highly integrated Altera Arria10 SoC Module
- 270 or 660 KLE, Commercial or Industrial Temp grade
- Dual mode as a **System-on-module** or FMC carrier board
- 2x Gbit Ethernet HPS, USB 2.0 OTG, USB 3.0
- DDR4 HPS and FPGA
- eMMC Flash Memory
- PCIe Gen3 x8
- Dual FMC Capability



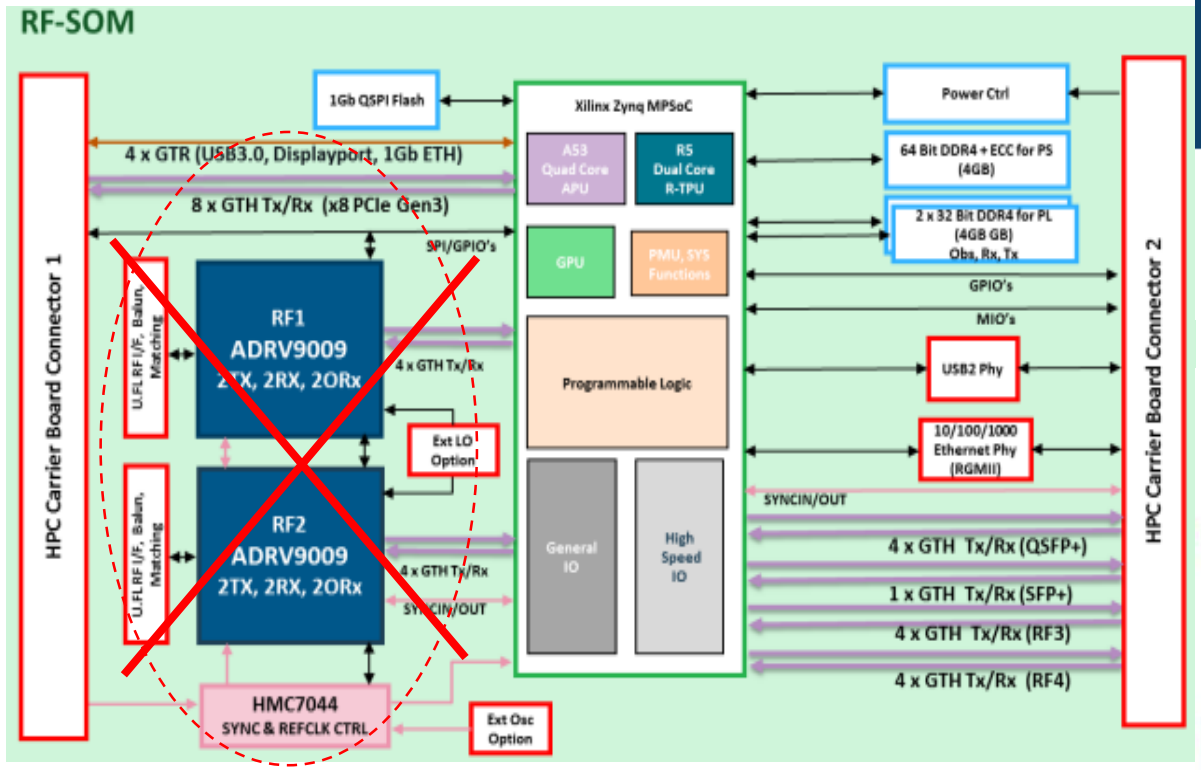




Prezzi (EUR)

Qtà	Prezzo Unitario	Prezzo esteso
1	837,72 €	837,72 €
1	1.680,12 €	1.680,12 €

A commercial FPGA SOC SOM with FMC connectors (II)

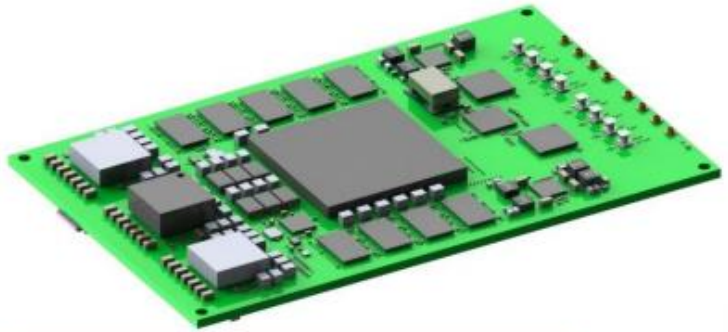


ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

ADRV9009-ZU11EG RF System-on-Module

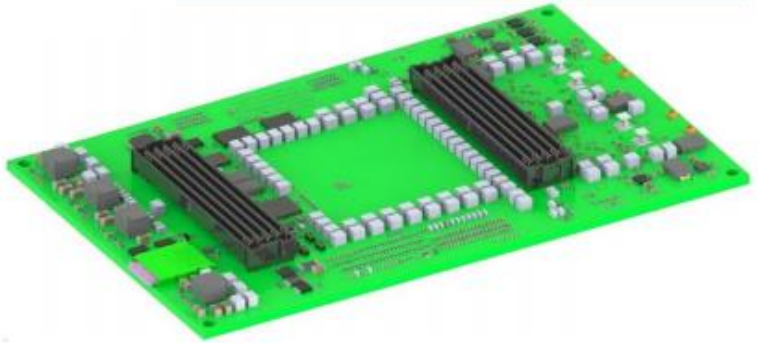
Production Ready Hardware for Prototyping and Systems Development
With open source software for industry standard development platforms

The ADRV9009-ZU11EG is highly customisable and offers wide bandwidth and tuning range for a broad range of applications. It contains 2x Wideband ADRV9009 Dual Transceivers and Quad-core ARM® Cortex™-A53 MPCore™. 4GB of DDR4 (with ECC) is dedicated to the Programming System and 2x2GB Banks are dedicated for Programmable Logic giving much flexibility for developing custom applications. 1Gb of flash is provided for image storage, with an additional option to boot over USB or from a removable SD-Card.

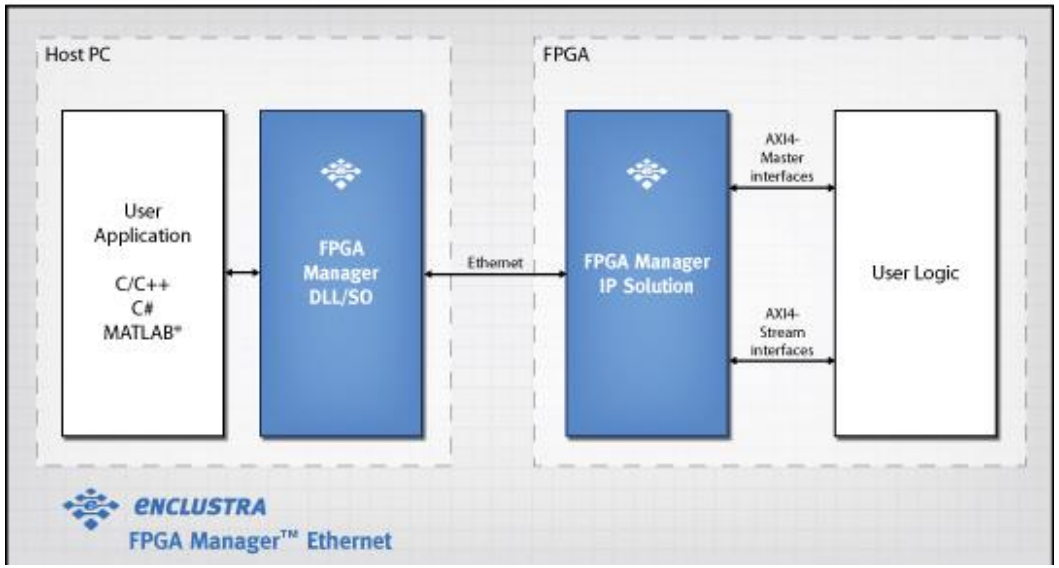


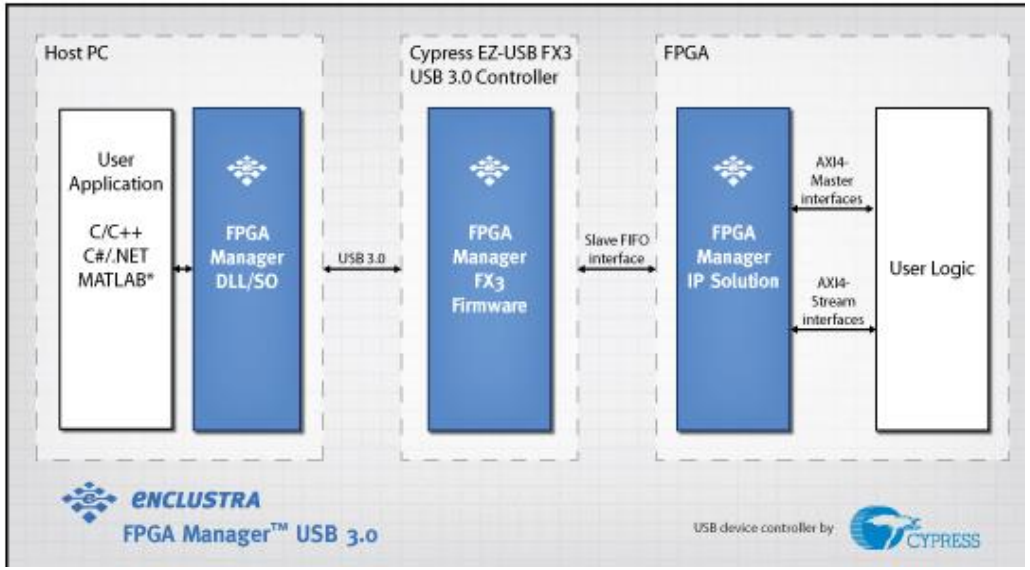
- Wide tuning range 75MHz to 6GHz
- Max receiver BW 200MHz
- Max transmitter synthesis BW 450MHz
- Max observation receiver BW 450MHz
- Integrated LO and Phase synch between all channels

- Platform development environment support includes Industry standard Linux Industrial I/O Applications, MATLAB®, Simulink®, and GNU Radio, and streaming interfaces for custom C, C++, python, and C# applications
- HDL reference designs and drivers to allow zero day development



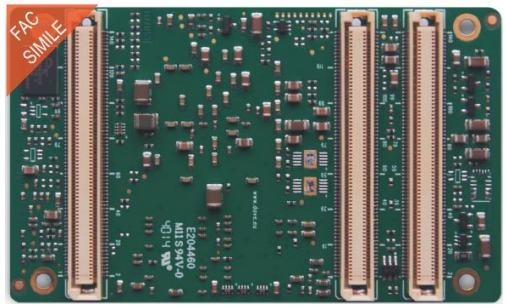
A modular approach for an FPGA–PC Communication System

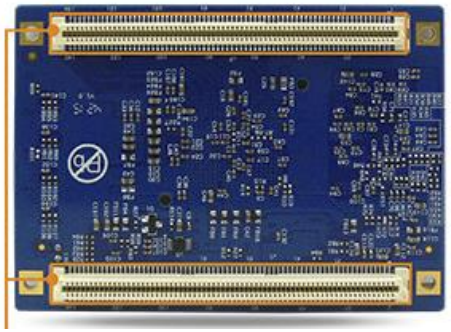


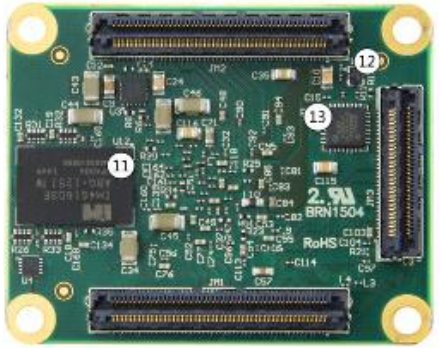


https://www.enclustra.com/en/products/fpga-manager/fpga-manager-ethernet/
https://www.enclustra.com/en/products/fpga-manager/fpga-manager-usb3/

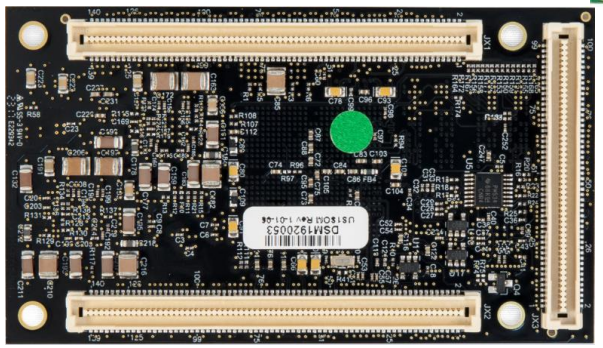
So far no standard sockets for SOM based on FPGA-SOC

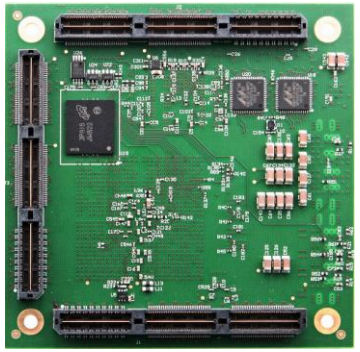


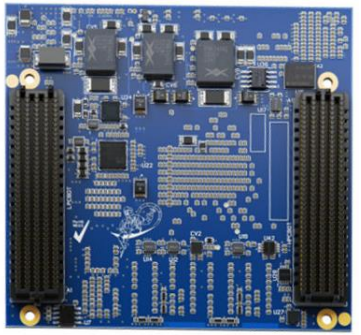




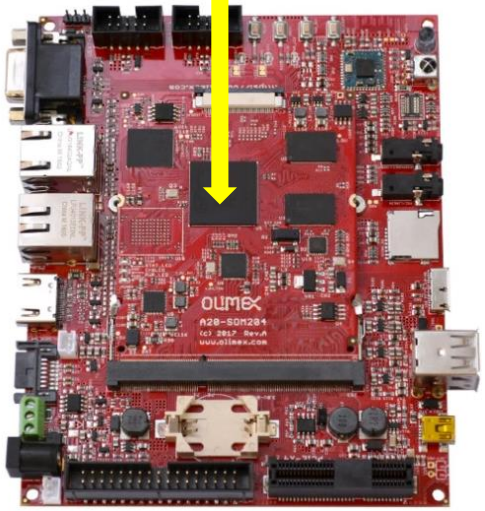
SODIMM SOM

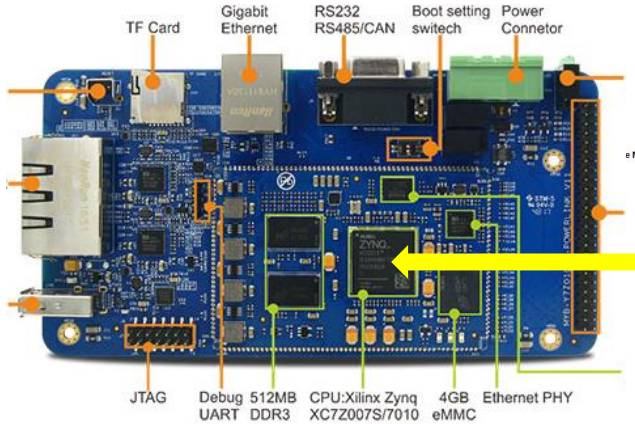






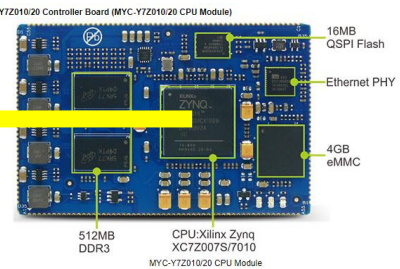
Soldered SOM



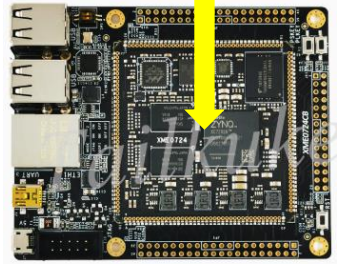


MYD-Y7Z010/20 Development Board

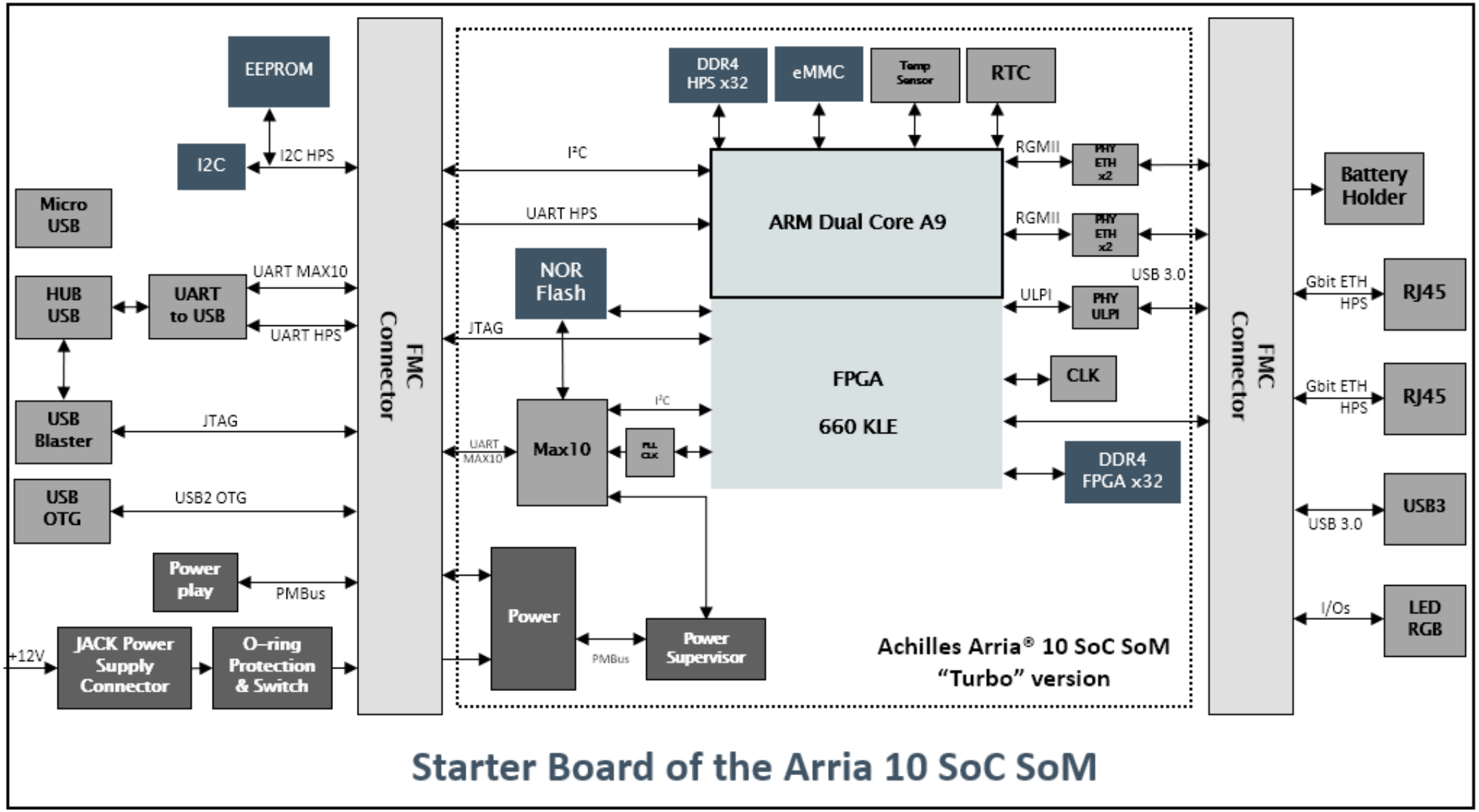
Soldered SOM



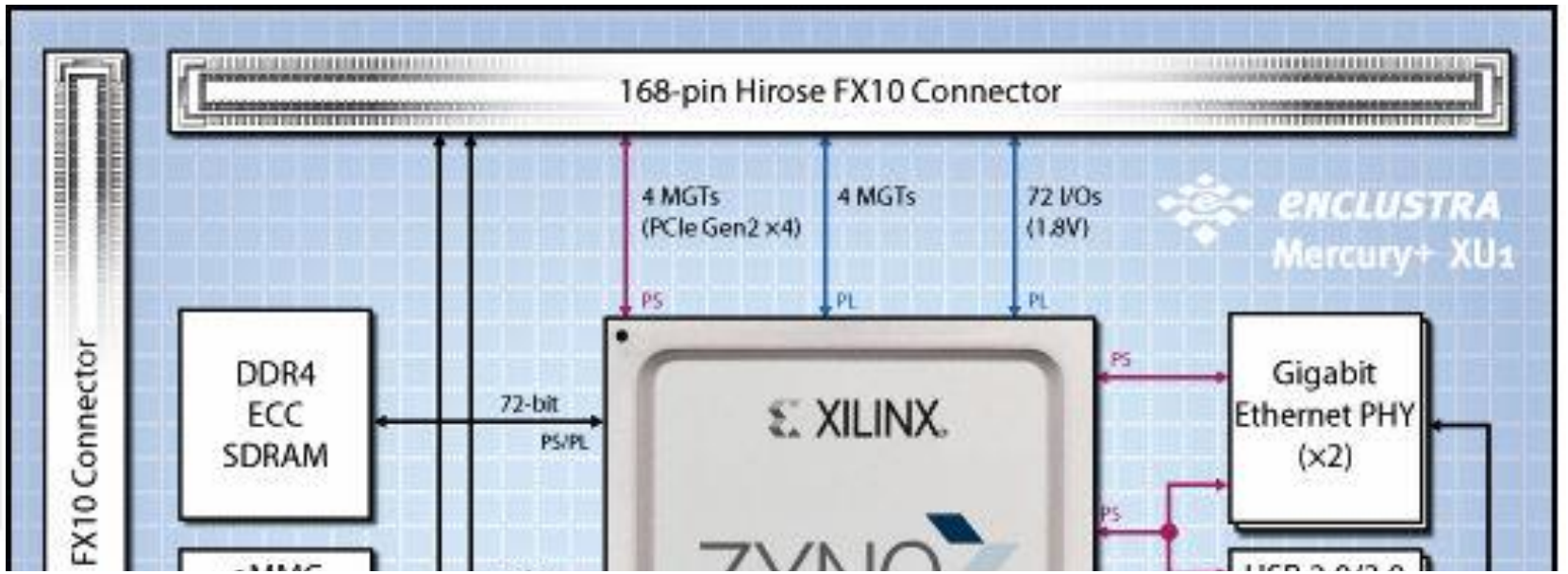
MYC-Y7Z010/20 CPU Module



What it should be in the SOM and the carrier? (example I)



What it should be in the module? (example II)



FAMILY OVERVIEW

VITA 57.4 FMC+ is the latest Standard in the popular VITA FMC family. This specification increases the performance of VITA 57.1 FMC Standard by extending the total number of Gigabit Transceivers to 32 and increasing the maximum data rate to 28 Gbps. Both are important developments for embedded computing designs using FPGAs and high-speed I/O. In addition, backward compatibility was achieved by using new connectors that allow FMC+ carriers to accept original FMC mezzanines.

What it should be in the module? (example III)

Arria 10 SOC FPGA System On Module (SOM) Highlights:

•Arria10 SX SOC & GX FPGA compatibility
- SX270, SX320, SX480, SX570, SX660
- GX270, GX320, GX480, GX570, GX660

•24 high speed transceivers @ 17.4Gbps
•Up to 76LVDS/152SE FPGA IOs
•64-Bit DDR4 support for FPGA
•Variable IO voltage support
•Industrial Grade operation

The specifications of Arria 10 SOC FPGA System On Module (SOM) :

•**SoC:**Arria10 SoC
- Dual Core, ARM Cortex – A9 CPU @ 1.5GHz
- SX270 (10AS027) FPGA Fabric
- 35mm x 35mm F34 Package

•**Memory:**
- 1GB DDR4 with optional ECC for HPS
- 1GB SLC NAND Flash for HPS
- Optional 64-bit DDR4 for FPGA*
- QSPI Flash for FPGA (Optional)

•**Communication:**
- 10/100/100 Ethernet PHY For HPS

•**Arria10 SoC FPGA IO interfaces:**
- 24 high-speed transceivers
- 76LVDS/152SE FPGA
- 8LVDS/8SE General purpose clock outputs
- 7LVDS/7SE General purpose clock inputs

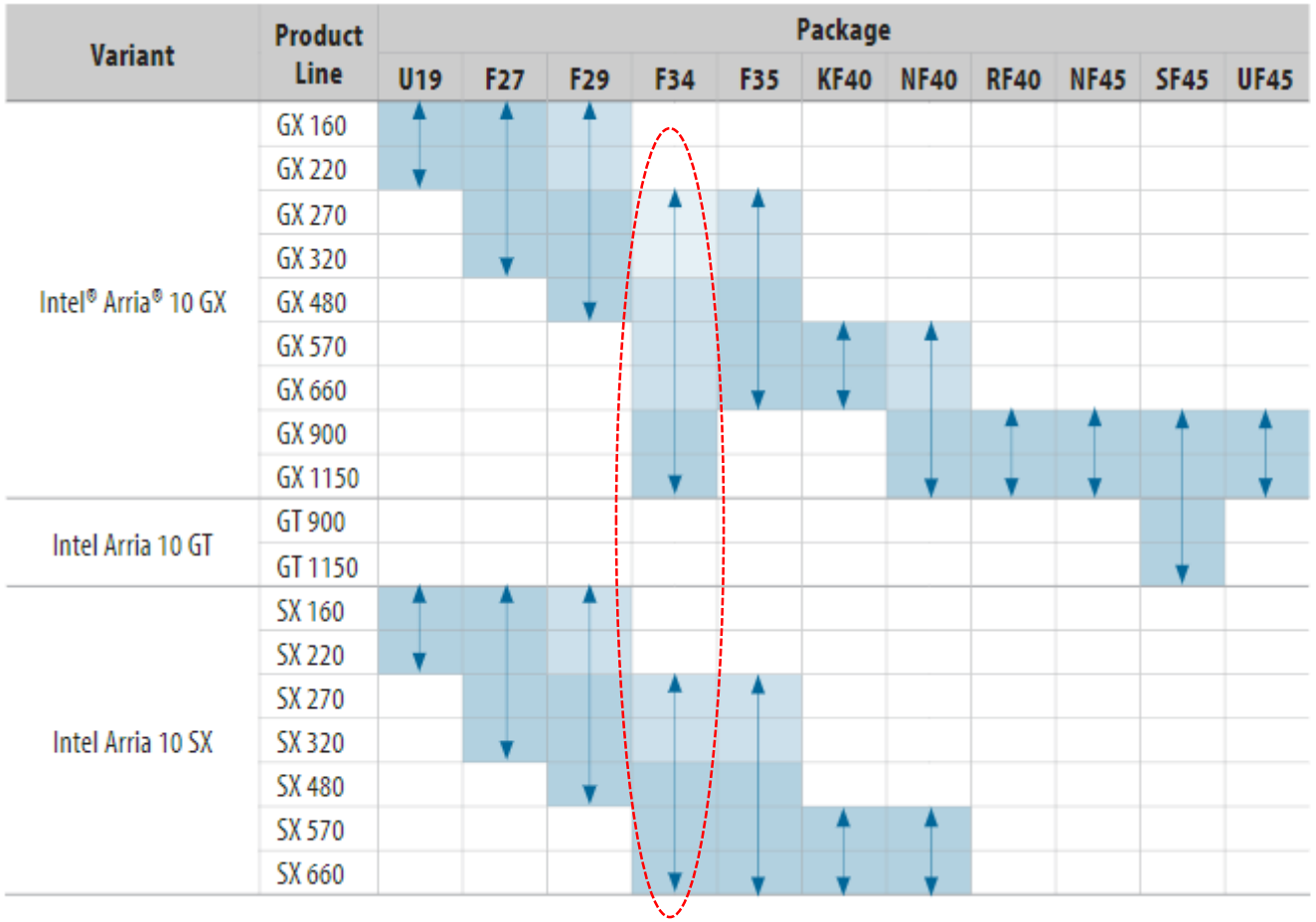
•**Headers:**
- HPS/FPGA JTAG, FPGA AS headers

•**240 Pin Board to Board Connector:**

•**Arria10 SoC HPS IO interfaces:**
- Gigabit Ethernet x 1 Port
- USB 2.0 OTG x 1 Port
- SD (4bit) x 1 Port
- SPI x 1 Port, I2C x 1 Port
- Full Function UART x 1 Port
- Console UART, GPIOs – 4 Nos

System on Module based on Arria 10 SoC

Example of Pin Compatibility for Upgradeability



Variant	Product Line	Package										
		U19	F27	F29	F34	F35	KF40	NF40	RF40	NF45	SF45	UF45
Intel® Arria® 10 GX	GX 160											
	GX 220											
	GX 270											
	GX 320											
	GX 480											
	GX 570											
	GX 660											
	GX 900											
	GX 1150											
Intel Arria 10 GT	GT 900											
	GT 1150											
Intel Arria 10 SX	SX 160											
	SX 220											
	SX 270											
	SX 320											
	SX 480											
	SX 570											
	SX 660											

Note: To verify the pin migration compatibility, use the **Pin Migration View** window in the Intel® Quartus® Prime software Pin Planner.

Arria 10 SOC FPGA System On Module (SOM) Highlights:

•Arria10 SX SOC & GX FPGA compatibility
- SX270, SX320, SX480, SX570, SX660
- GX270, GX320, GX480, GX570, GX660

~ Price Range 1 to 8 KEuro

Preliminary estimations for a new possible design

	Design time & complexity	Debugging	Prototyping cost	Small volume production cost	Mass production cost	Software Support	Expandability and Versatility	Obsolescence and Maintenance	Total score
Complete Single Board	1	2	2	1	5	2	2	1	**16**
Commercial SOM & Custom Carrier	5	5	4	4	3	5	3	4	**33**
Custom SOM & Custom Carrier	1	3	1	3	4	2	5	5	**24**

Scores: 1 very negative, 2 negative, 3 neutral, 4 positive, and 5 very positive. Assign 3 if dubious.

The FMC+ Connector Pinout (an interesting standard connector)

14 x 40	M	L	K	J	H	G	F	E	D	C	B	A	Z	Y
1	GND	RES1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND	HSPC_PRSNT_M2C_L	GND
2	DP23_M2C_P	GND	GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P	GND	DP23_C2M_P
3	DP23_M2C_N	GND	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N	GND	DP23_C2M_N
4	GND	GBTCLK4_M2C_P	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND	DP22_C2M_P	GND
5	GND	GBTCLK4_M2C_N	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND	DP22_C2M_N	GND
6	DP22_M2C_P	GND	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P	GND	DP21_C2M_P
7	DP22_M2C_N	GND	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N	GND	DP21_C2M_N
8	GND	GBTCLK3_M2C_P	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND	DP20_C2M_P	GND
9	GND	GBTCLK3_M2C_N	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND	DP20_C2M_N	GND
10	DP21_M2C_P	GND	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P	GND	DP10_M2C_P
11	DP21_M2C_N	GND	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N	GND	DP10_M2C_N
12	GND	GBTCLK2_M2C_P	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND	DP11_M2C_P	GND
13	GND	GBTCLK2_M2C_N	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND	DP11_M2C_N	GND
14	DP20_M2C_P	GND	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P	GND	DP12_M2C_P
15	DP20_M2C_N	GND	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N	GND	DP12_M2C_N
16	GND	SYNC_C2M_P	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND	DP13_M2C_P	GND
17	GND	SYNC_C2M_N	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND	DP13_M2C_N	GND
18	DP14_C2M_P	GND	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P	GND	DP14_M2C_P
19	DP14_C2M_N	GND	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N	GND	DP14_M2C_N
20	GND	REFCLK_C2M_P	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND	GBTCLK5_M2C_P	GND
21	GND	REFCLK_C2M_N	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND	GBTCLK5_M2C_N	GND
22	DP15_C2M_P	GND	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P	GND	DP15_M2C_P
23	DP15_C2M_N	GND	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N	GND	DP15_M2C_N
24	GND	REFCLK_M2C_P	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND	DP10_C2M_P	GND
25	GND	REFCLK_M2C_N	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND	DP10_C2M_N	GND
26	DP16_C2M_P	GND	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P	GND	DP11_C2M_P
27	DP16_C2M_N	GND	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N	GND	DP11_C2M_N
28	GND	SYNC_M2C_P	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND	DP12_C2M_P	GND
29	GND	SYNC_M2C_N	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND	DP12_C2M_N	GND
30	DP17_C2M_P	GND	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P	GND	DP13_C2M_P
31	DP17_C2M_N	GND	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N	GND	DP13_C2M_N
32	GND	RES2	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND	DP16_M2C_P	GND
33	GND	RES3	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND	DP16_M2C_N	GND
34	DP18_C2M_P	GND	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P	GND	DP17_M2C_P
35	DP18_C2M_N	GND	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N	GND	DP17_M2C_N
36	GND	12P0V	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND	DP18_M2C_P	GND
37	GND	12P0V	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND	DP18_M2C_N	GND
38	DP19_C2M_P	GND	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P	GND	DP19_M2C_P
39	DP19_C2M_N	GND	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N	GND	DP19_M2C_N
40	GND	12P0V	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND	3P3V	GND