First tests and characterization of the RD50-MPW2 active pixel matrix, bandgap voltage reference and SEU tolerant memory

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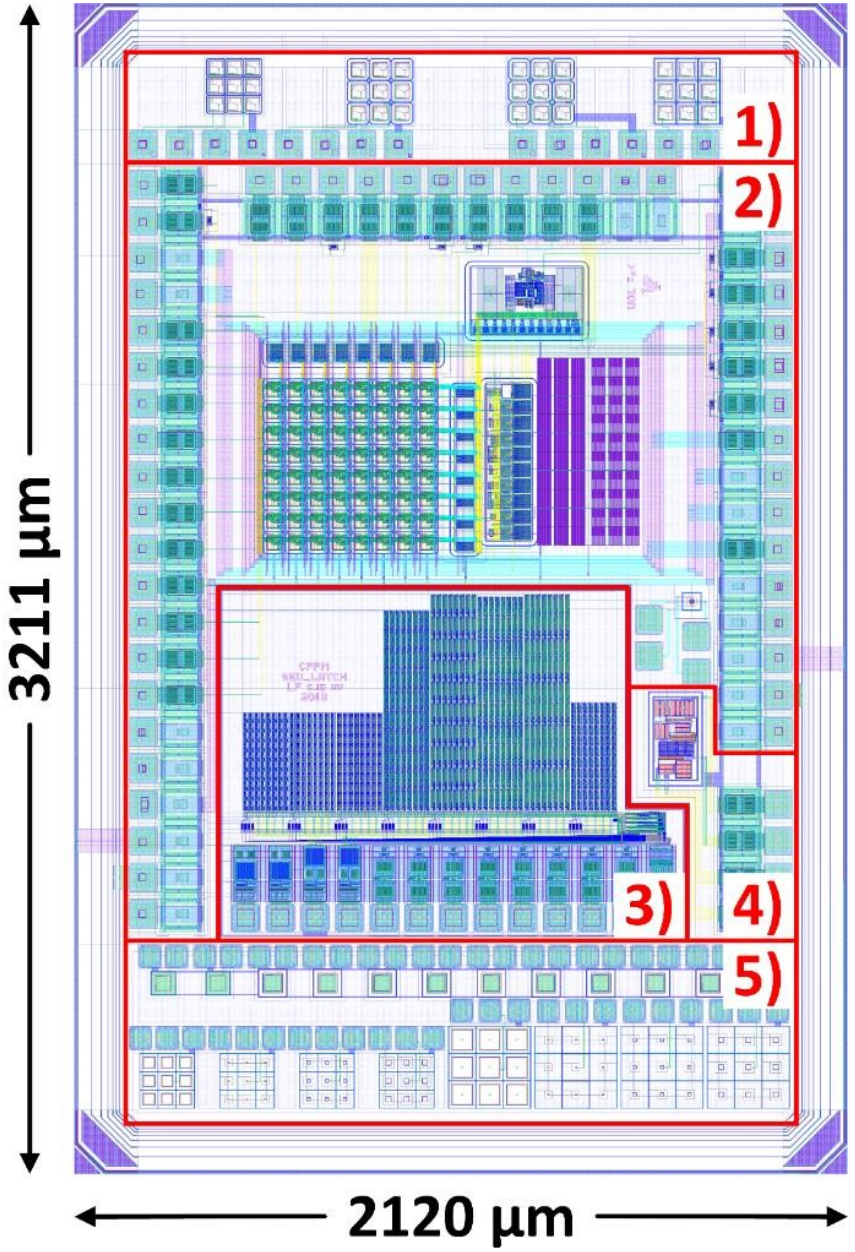
Outline

- RD50-MPW2 overview.
- Bandgap voltage reference tests.
- SEU tolerant memory.
  - Objective and blocks implemented.
  - Tests performed.
- Matrix of DMAPS CMOS.
  - Design overview.
  - Device operation tests.
  - Tests with in-pixel injection circuit.
  - Tests with radioactive source.
- Conclusions and outlook.

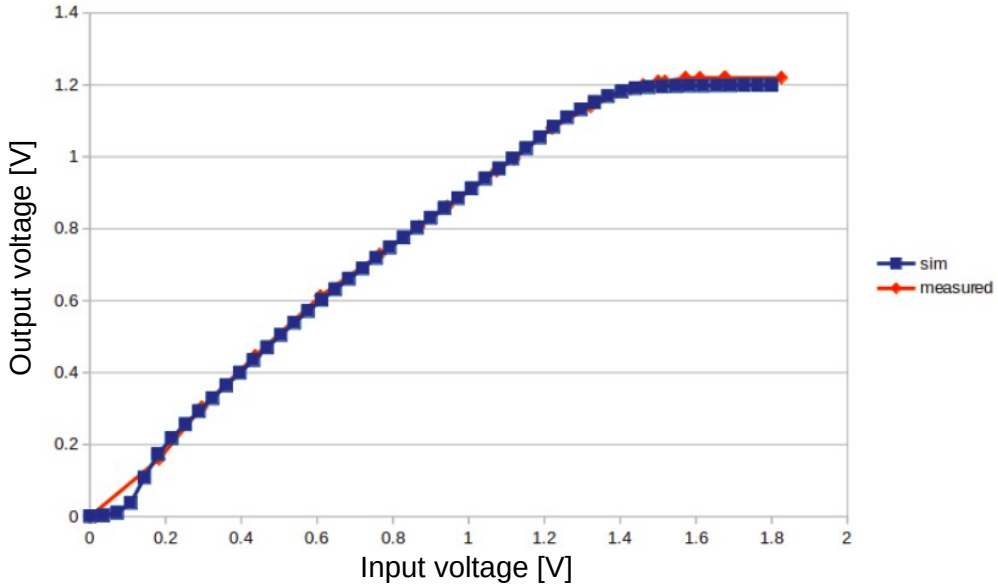
RD50-MPW2 overview

- RD50 collaboration common project.
- LFoundry 150 nm CMOS process.
- Substrate available with four different resistivities (10 Ω·cm, 0.5-1.1 kΩ·cm, 1.9 kΩ·cm and > 2 kΩ·cm).
- Minimize leakage current and test different technology aspects.
- Tests structures with depleted CMOS pixels (1).
- Matrix of depleted CMOS pixels with analog readout (2).
  - 8 x 8 pixels.
  - 60 µm x 60 µm pixel area.
  - Analog readout embedded in the sensing area.
- SEU tolerant memory array (3).
- Bandgap reference voltage (4).
- Test structures with SPADs and depleted CMOS pixels (5).

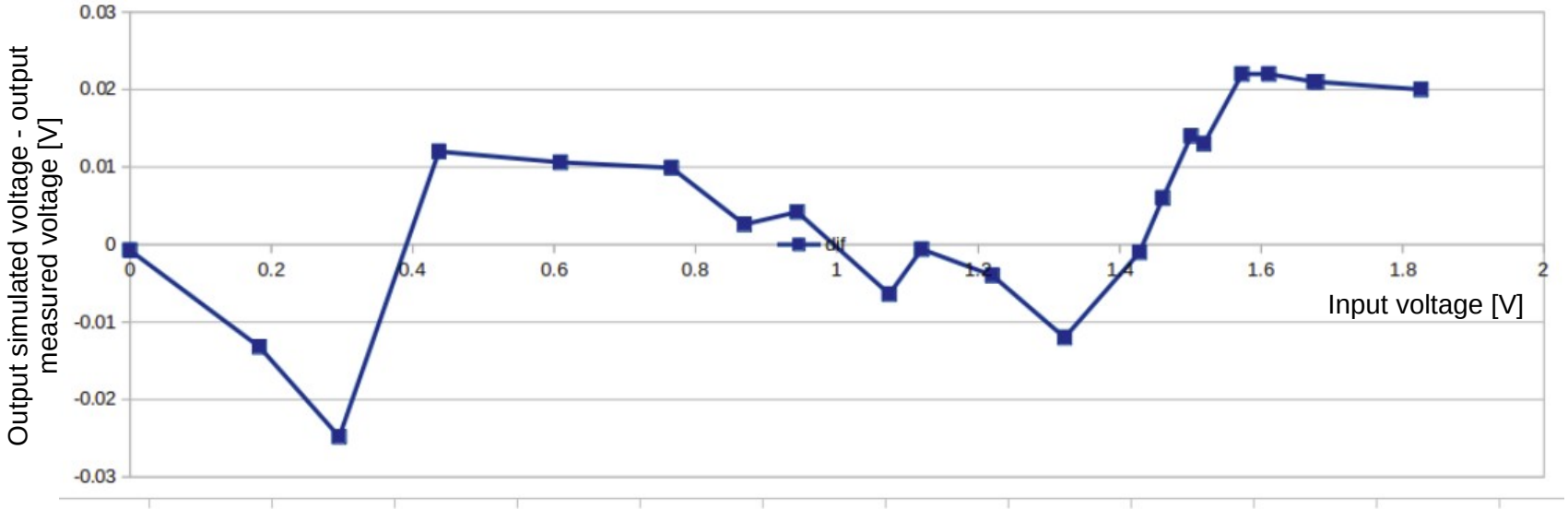


Bandgap voltage reference

- Provides a constant output voltage regardless of voltage input, temperature and output load variations.
- Measured the output voltage versus the input voltage: very good agreement with simulations.
  - Max. variation of 20 mV from simulation over operating range (1.4-1.8 V).



Bandgap reference output voltage (V) versus input voltage (V).

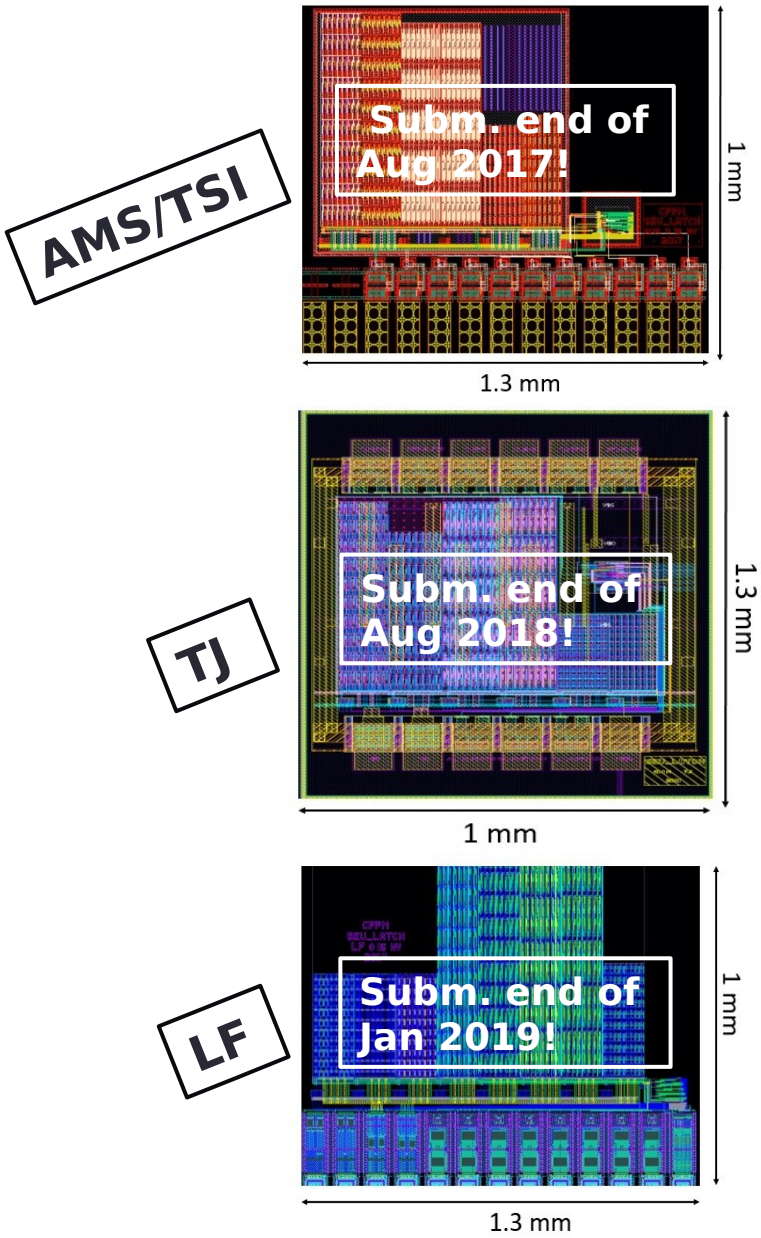


Bandgap reference output simulated voltage minus output measured voltage (V) versus input voltage (V).

SEU tolerant memory array

- Particles deposit sufficient charge in small region of silicon.
- The charge might flip the state of a memory bit (SEU Single Event Upset).
  - Expected 0.2-0.5 GHz/cm² particle flux for inner layer in ATLAS (HL-LHC).
- Main objective: to design a SEU tolerant memory in several technologies and nodes.
  - AMS and TSI 180 nm HV.
  - TowerJazz 180 nm CIS.
  - LFoundry 150 nm.
- Several architectures also designed and tested.
- Technologies and architectures will be compared each others: latch standard cell as a reference.
- Measuring the SEU cross section of 1-bit memory, allows to estimate the effect of the tolerance to SEU.

$$\sigma(cm^2) = \frac{BER}{\phi} = \frac{N_{err}}{\phi \cdot N_{latches}}$$

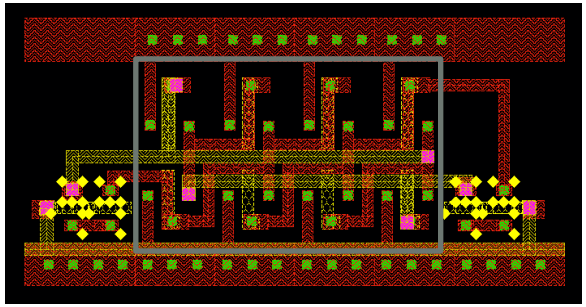


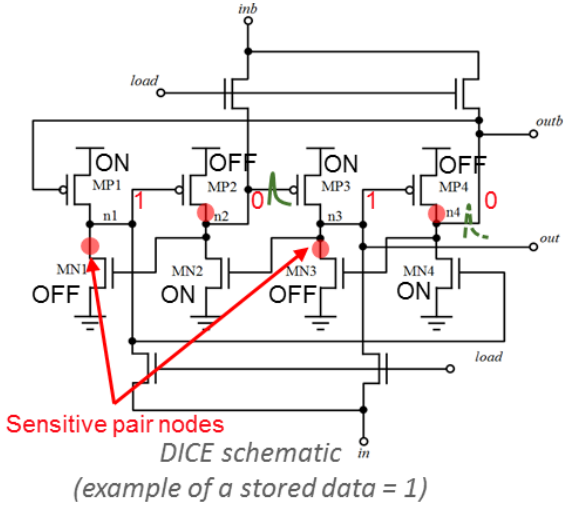
SEU tolerant memory in RD50-MPW2

- To study the SEU tolerance of several memory cells by comparing them to the standard cell.
- Eight different flavours arranged in columns.

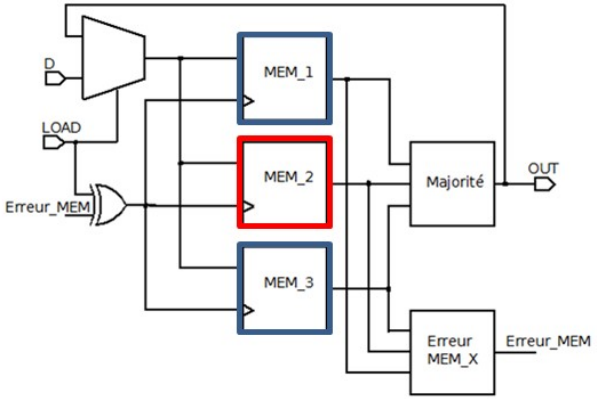
1. SRAM (6 transistors).
2. Standard cell from LFoundry library (latch cell). 8 transistors.
3. DICE (Dual Interlocked Storage Cell) latch (full custom). 12 transistors. x5 BER (Bit Error Rate).
   - Based on two cross-coupled inverters.
   - Inmunity against SEUs (non-simultaneus).
4. Enhanced DICE latch.
   - Larger spacing between sensitive nodes.
   - Immunity against simultaneous SEUs.
5. Standard cell with TRL (Triple Redundancy Logic). x200 BER.
   - With feedback correction commanded by a latch error detection.
6. DICE cell with TRL.
7. Standard cell with TRL and split latch. x4000 BER.
   - TRL split between 2 bits to separate sensitive nodes further.
8. DICE cell with TRL and split latch.

- Additional functions implemented (column selector, digital buffer, DNW isolation).





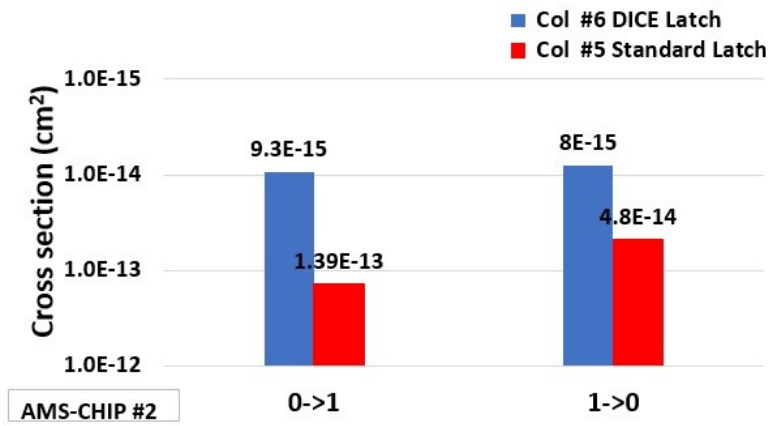
DICE latch.

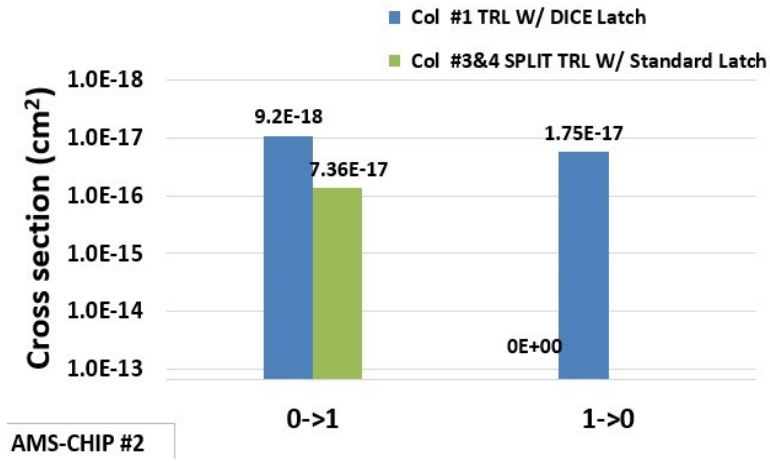


Triple redundancy logic.

SEU tolerant memory tests

- AMS device already tested.
  - CERN PS 24 GeV proton beam line. No LET calculation.
  - Specific DAQ developed (Beaglebone nanoPC + FPGA).
  - Enough data measured for acceptable SEU statistic (80 cells/latch type and spill number > 10000).
- Preliminary results show:
  - DICE latch is x15 more robust than the standard cell.
  - TRL DICE latch is x15000 more robust than the standard cell.
  - The Mean Time between Upset (MTBU) is few hours for TRL DICE latch.

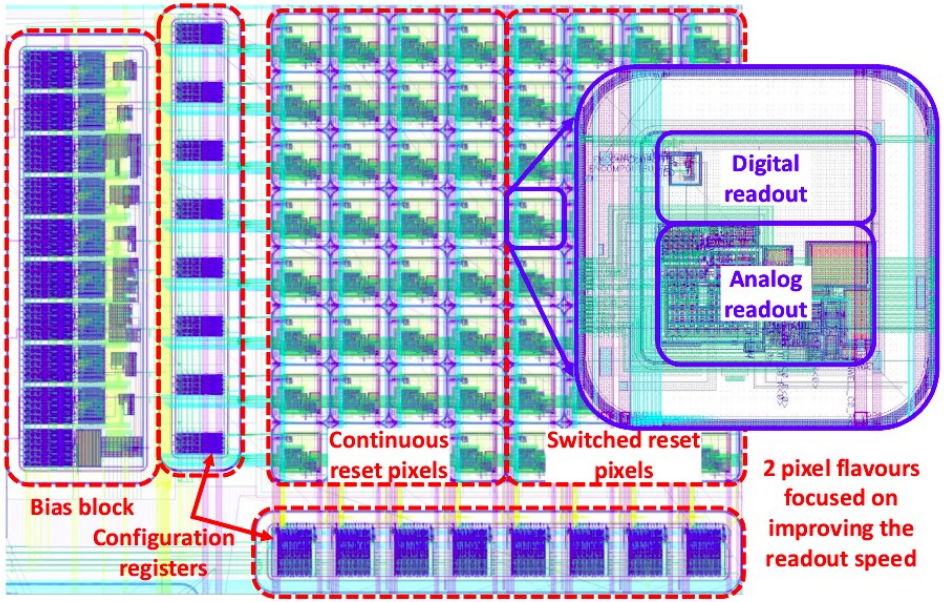




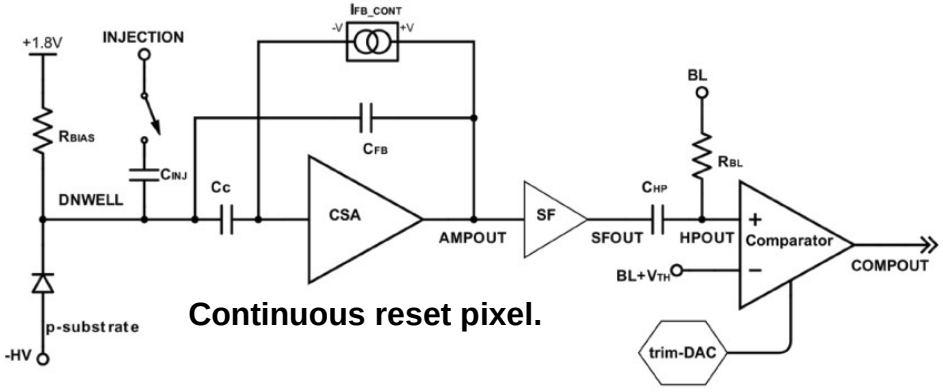
Latch Flavor	SEU Cross Section (err/cm²)	Estimated MTBU (1-bit/cm²)	Estimated MTBU (AMS-CMOS chip) 2cm x 2cm
Standard Latch 0->1	138,6E-15	2 days	2,9 sec
Standard Latch 1->0	48,0E-15	7 days	8,3 sec
DICE Latch 0->1	9,3E-15	36 days	43,1 sec
DICE Latch 1->0	8,0E-15	41 days	49,7 sec
TRL DICE 0->1	9,2E-18	99 years	12,1 hours
TRL DICE 1->0	17,5E-18	52 years	6,3 hours
SPLIT TRL Standard Latch 0->1	73,6E-18	12 years	1,5 hours
SPLIT TRL Standard Latch 1->0			

Active pixel matrix overview

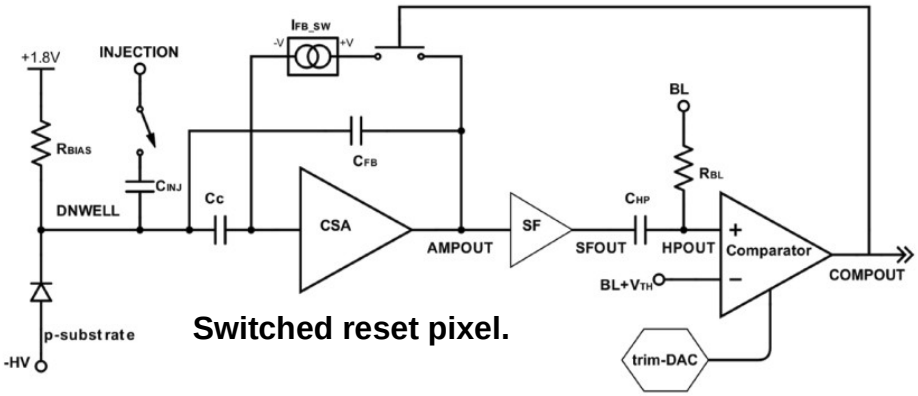
- Matrix of depleted CMOS pixels (60 µm x 60 µm) with analog embedded readout.
- Two flavours of analog readout.
  - Columns 0-3: continuous reset pixels.
  - Columns 4-7: switched reset pixels.
- Bias block: generates the bias voltages to set transistors DC operating points.
  - 9 channels.
  - 6-bit current DAC and current mirror.
- Configuration registers: bias block DACs, pixel trim-DACs and pixel output enable.
- Analog buffer/multiplexer (12 channels): monitoring bias voltages and pixel analog output increasing driving capability.



Active pixel matrix floorplan.



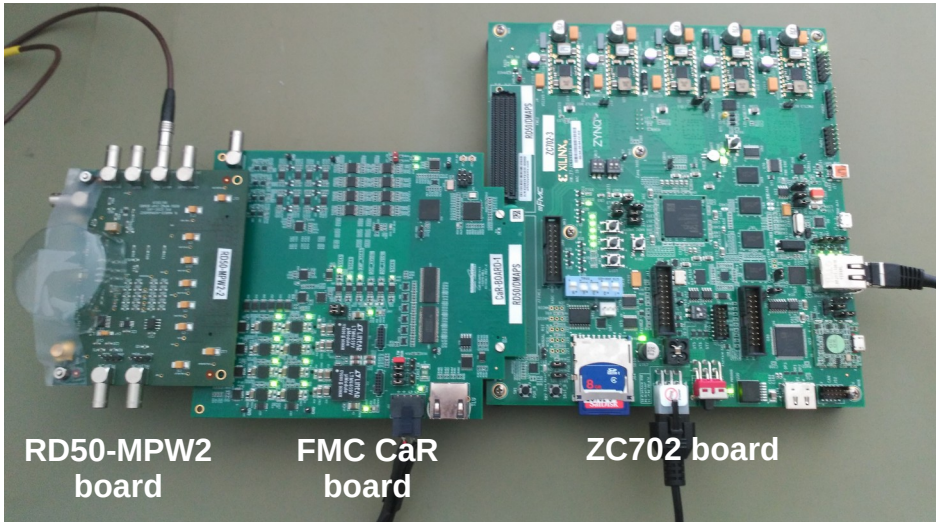
Continuous reset pixel.



Switched reset pixel.

Active matrix operation tests

- Specific DAQs developed: see C. Irmler talk.
  - SoC development cards used (ZC702/ZC706).
  - FMC CaR board and custom chip board.
  - Custom VHDL blocks, Linux and C/Python scripts.
  - SSH from host PC.
- Power consumption measurements.
  - MPW2 voltage and current power supply levels monitored.
  - ABUFF power on/off verified.



Active matrix DAQ with ZC702 board.

```
CaR temperature (C): 37.187500
P1V8A_NW_RING (PWR_OUT_1) voltage (V): 1.838750
P1V8A_NW_RING (PWR_OUT_1) current (mA): 0.300000
P1V8D_VDD_IO (PWR_OUT_2) voltage (V): 1.842500
P1V8D_VDD_IO (PWR_OUT_2) current (mA): 0.000000
P1V8A_VSENSBIAS (PWR_OUT_3) voltage (V): 1.840000
P1V8A_VSENSBIAS (PWR_OUT_3) current (mA): 0.500000
P1V8A_VDDA (PWR_OUT_4) voltage (V): 1.822500
P1V8A_VDDA (PWR_OUT_4) current (mA): 6.500000
P1V8D_VDDC (PWR_OUT_5) voltage (V): 1.820000
P1V8D_VDDC (PWR_OUT_5) current (mA): 4.800000
P1V3A_VSSA (PWR_OUT_6) voltage (V): 1.347500
P1V3A_VSSA (PWR_OUT_6) current (mA): 0.500000
P1V8D_VDDD (PWR_OUT_7) voltage (V): 1.846250
P1V8D_VDDD (PWR_OUT_7) current (mA): 0.300000
P1V8A_BG_VDD (PWR_OUT_8) voltage (V): 1.843750
P1V8A_BG_VDD (PWR_OUT_8) current (mA): 0.800000
```

RD50-MPW2 current consumption. Registers configured. ABUFF powered.

```
CaR temperature (C): 37.187500
P1V8A_NW_RING (PWR_OUT_1) voltage (V): 1.837500
P1V8A_NW_RING (PWR_OUT_1) current (mA): 0.300000
P1V8D_VDD_IO (PWR_OUT_2) voltage (V): 1.843750
P1V8D_VDD_IO (PWR_OUT_2) current (mA): 0.000000
P1V8A_VSENSBIAS (PWR_OUT_3) voltage (V): 1.840000
P1V8A_VSENSBIAS (PWR_OUT_3) current (mA): 0.000000
P1V8A_VDDA (PWR_OUT_4) voltage (V): 1.838750
P1V8A_VDDA (PWR_OUT_4) current (mA): 1.000000
P1V8D_VDDC (PWR_OUT_5) voltage (V): 1.821250
P1V8D_VDDC (PWR_OUT_5) current (mA): 5.000000
P1V3A_VSSA (PWR_OUT_6) voltage (V): 1.346250
P1V3A_VSSA (PWR_OUT_6) current (mA): 0.800000
P1V8D_VDDD (PWR_OUT_7) voltage (V): 1.846250
P1V8D_VDDD (PWR_OUT_7) current (mA): 0.300000
P1V8A_BG_VDD (PWR_OUT_8) voltage (V): 1.842500
P1V8A_BG_VDD (PWR_OUT_8) current (mA): 0.800000
```

RD50-MPW2 current consumption. Registers configured. ABUFF powered down.

Active matrix operation tests

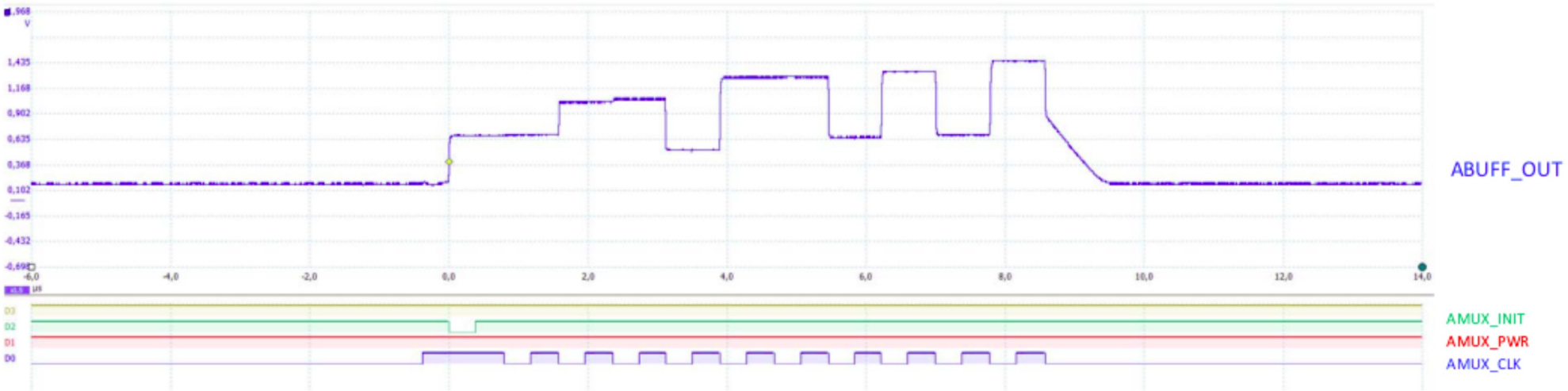
- Configuration registers programmed.
  - Serial data stream in/out compared.
- Analog buffer/multiplexer verified.
  - Channel configuration and output.

```
Retrieved line of length 148:
00100001110000001000000100000010000001000000010000000000000000000000000000011110000101010101000101100101001010110101100101001100100111001000000000


Retrieved line of length 148:
00100001110000001000000100000010000001000000010000000000000000000000000000011110000101010101000101100101001010110101100101001100100111001000000000


readback value = 00100001110000001000000100000010000001000000010000000000000000000000000000011110000101010101000101100101001010110101100101001100100111001000000000
sent     value = 00100001110000001000000100000010000001000000010000000000000000000000000000011110000101010101000101100101001010110101100101001100100111001000000000
FILES MATCH :)
```

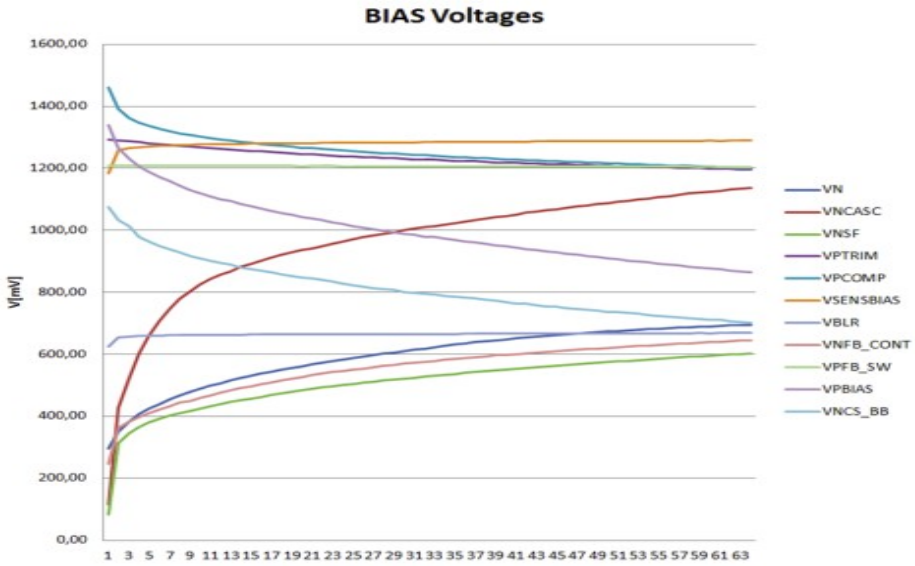
Serial data stream configuration check function output.



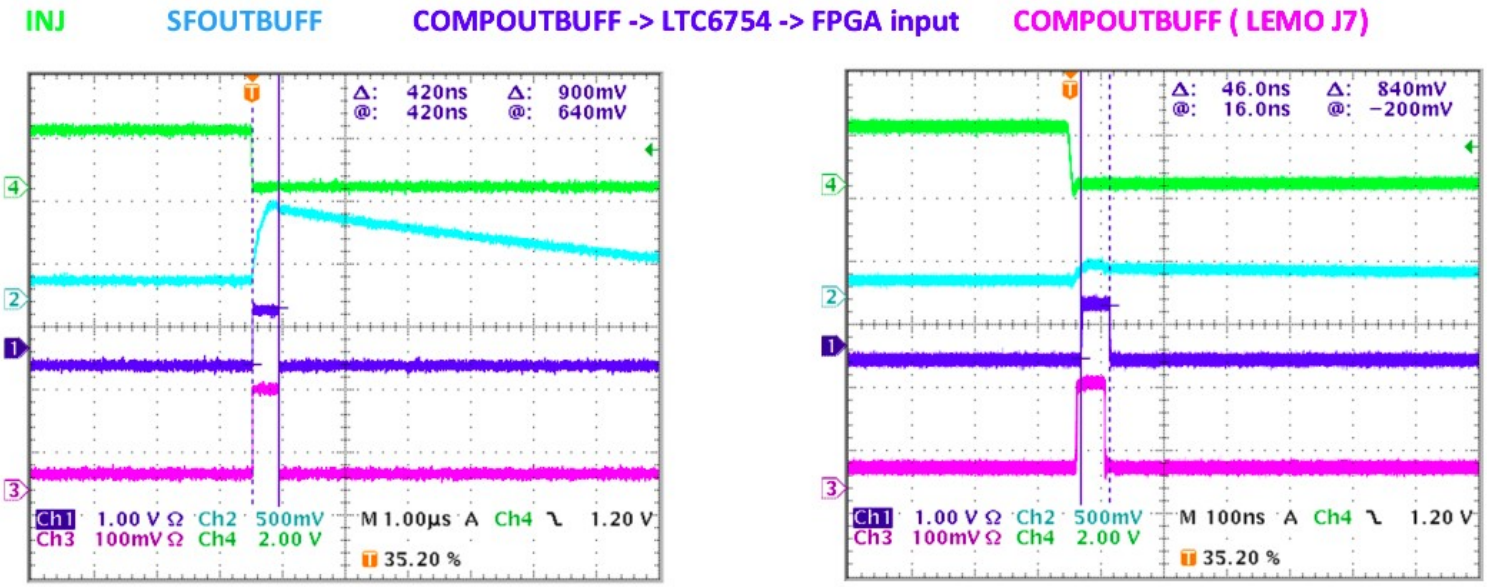
Analog buffer output (ABUFF_OUT) and control signals (AMUX_INIT, AMUX_PWR and AMUX_CLK) when configuring the 12 different channels.

Active matrix operation tests

- Bias voltages measured.
  - With on-board ADC, using ABUFF and with electrometer.
- Analog and comparator pixel output checked.
  - Dedicated pads and ABUFF.
  - Injection of pulses through pixel calibration circuit.



Measured bias voltages (mV) with on-board ADC versus bias DAC value programmed.



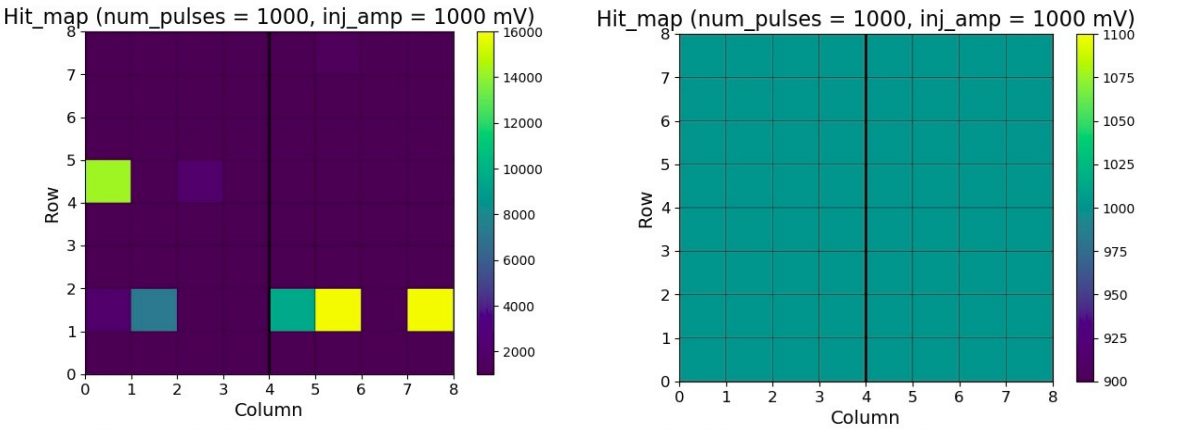
COL 2 / ROW 1

COL 6 / ROW 1

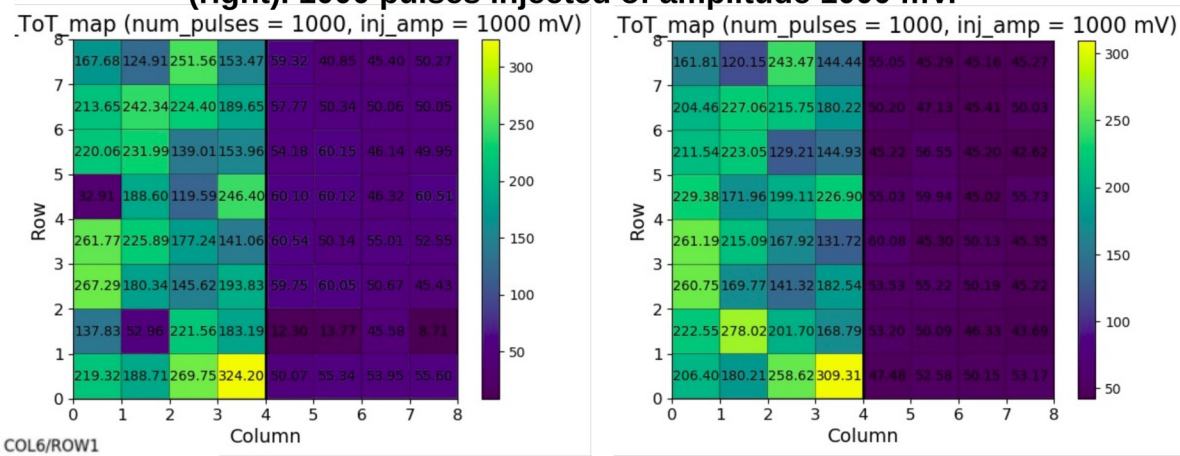
Test input pulse (green), pixel amplifier output (blue) and pixel comparator output (purple tones) for a CR pixel (left) and SR pixel (right).

Tests with pixel calibration circuit

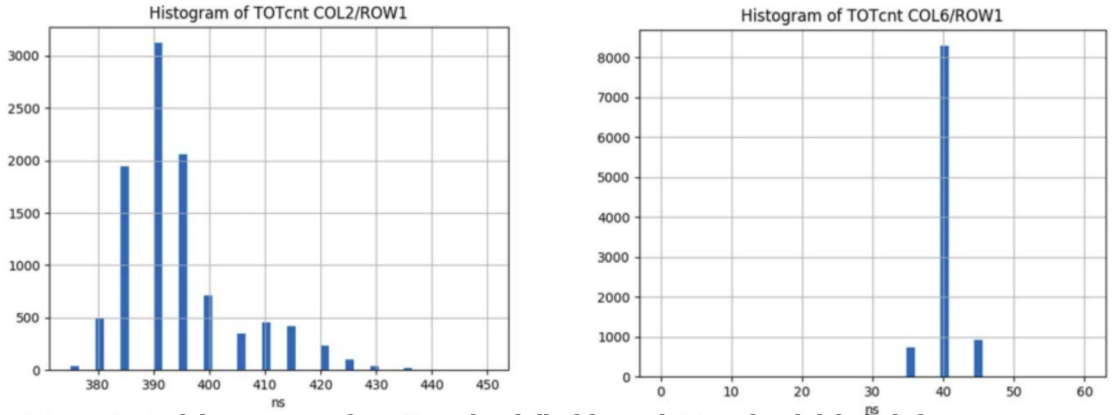
- Pixel comparator output pulse acquire with DAQ.
  - Bias registers configured with nominal values.
- Hitmaps
  - Number of pulses detected.
- Mean ToT maps.
  - Mean pulse width measurement per pixel.
- ToT histogram for a pixel.
  - Distribution of pulse width measurement.



Full matrix hit map for comparator threshold 950 mV (left) and 990 mV (right). 1000 pulses injected of amplitude 1000 mV.



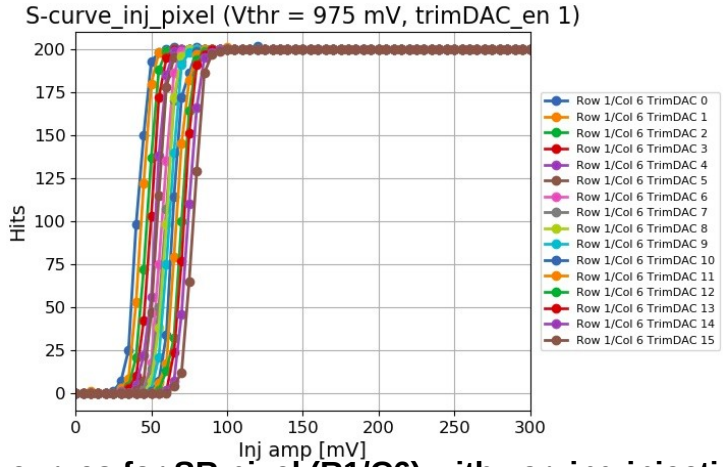
Full matrix mean ToT map for comparator threshold 950 mV (left) and 990 mV (right). 1000 pulses injected of amplitude 1000 mV.



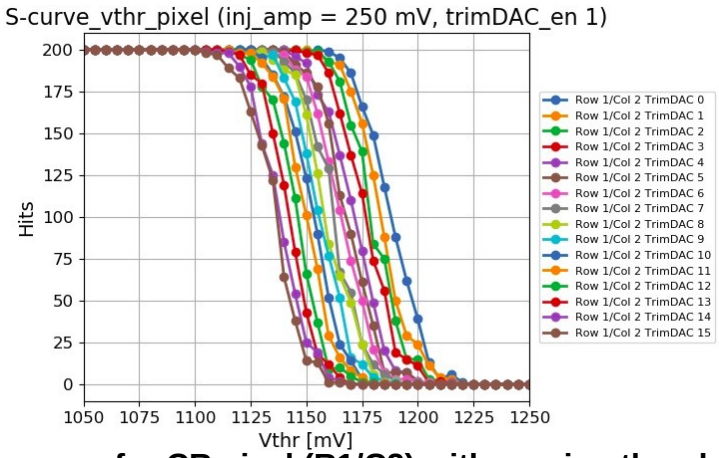
Mean ToT histogram for CR pixel (left) and SR pixel (right) for comparator threshold 950 mV. 10000 pulses injected of amplitude 1800 mV.

Tests with pixel calibration circuit

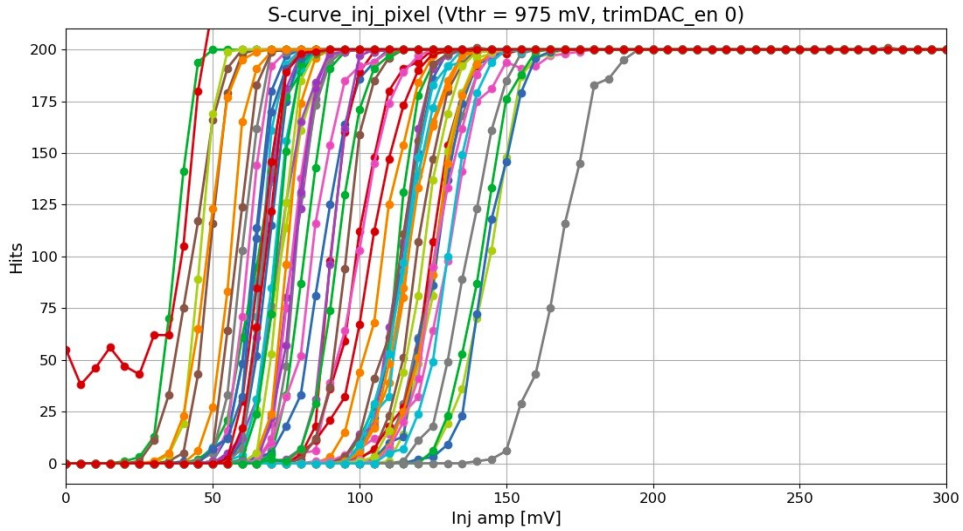
- S-curves: number of hits as a function of...
  - Injection amplitude variation.
  - Comparator threshold variation.
  - Also Trim DAC value variation.



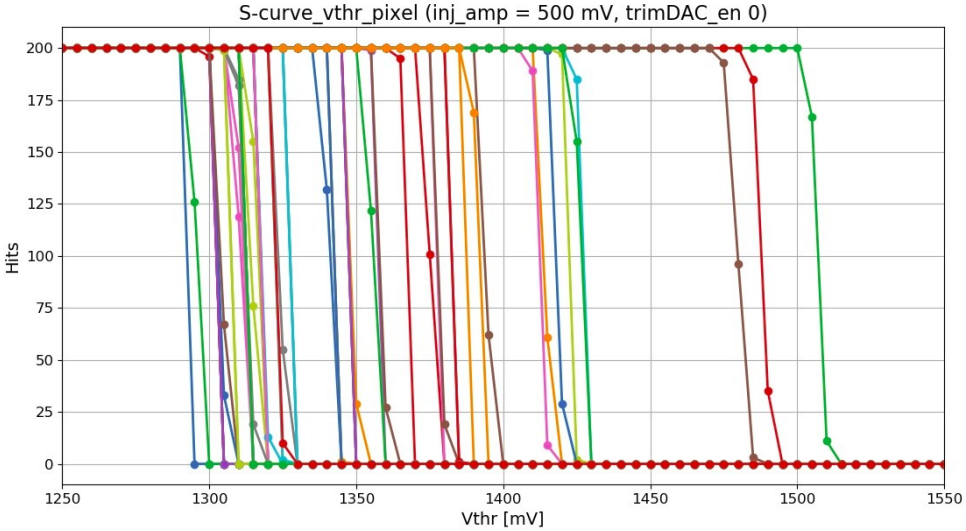
S-curves for SR pixel (R1/C6) with varying injection amplitude (0-300 mV). Threshold voltage 975 mV and trim DAC enable (trim DAC value 0-15).



S-curves for CR pixel (R1/C2) with varying threshold voltage (1050-1250 mV). Injection amplitude 250 mV and trim DAC enable (trim DAC value 0-15).



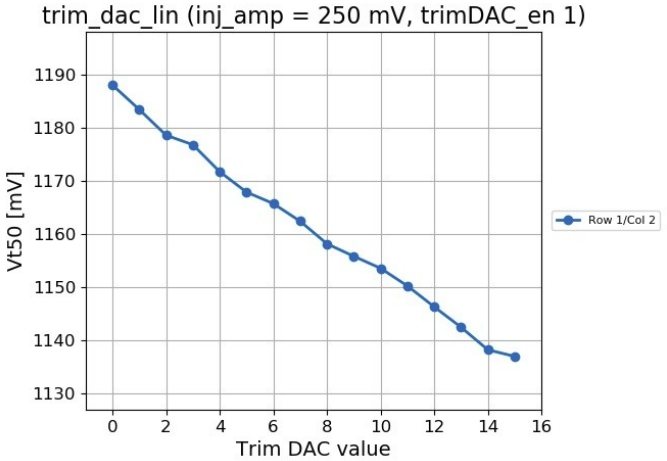
S-curves for all pixels with varying injection amplitude (0-300 mV). Threshold voltage 975 mV and trim DAC disabled.



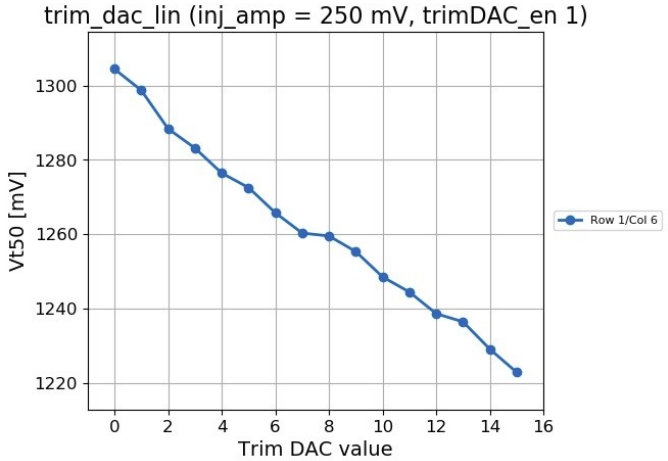
S-curves for all pixels with varying threshold voltage (1250-1550 mV). Injection amplitude 500 mV and trim DAC disabled.

Tests with pixel calibration circuit

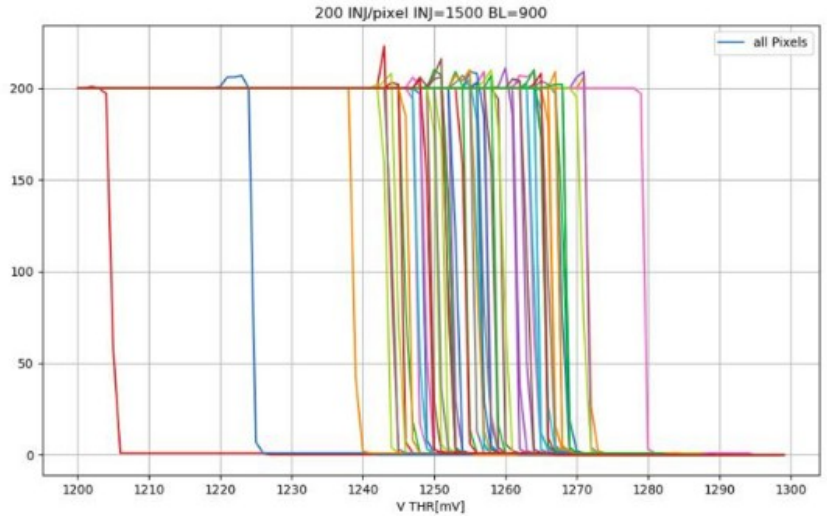
- S-curves.
  - Trim DAC value variation linearity verification: Vt50 vs trim DAC value.
  - Trim DAC value optimization to reduce s-curve width.



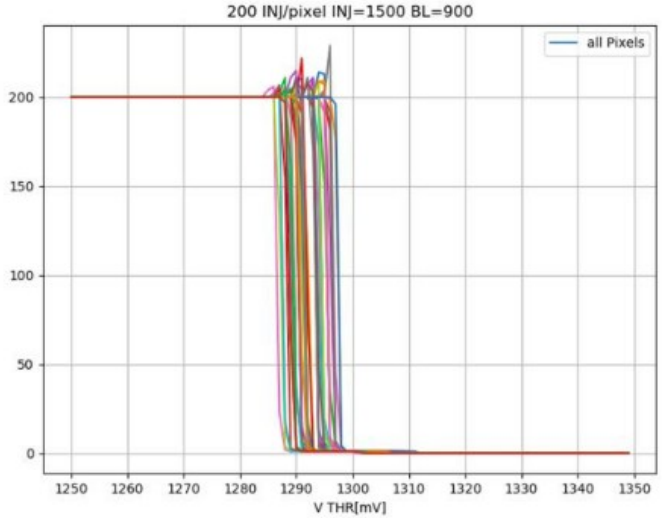
Vt50 (mV) versus trim DAC value for a CR pixel (R1/C2). Injection amplitude 250 mV.



Vt50 (mV) versus trim DAC value for a SR pixel (R1/C6). Injection amplitude 250 mV.



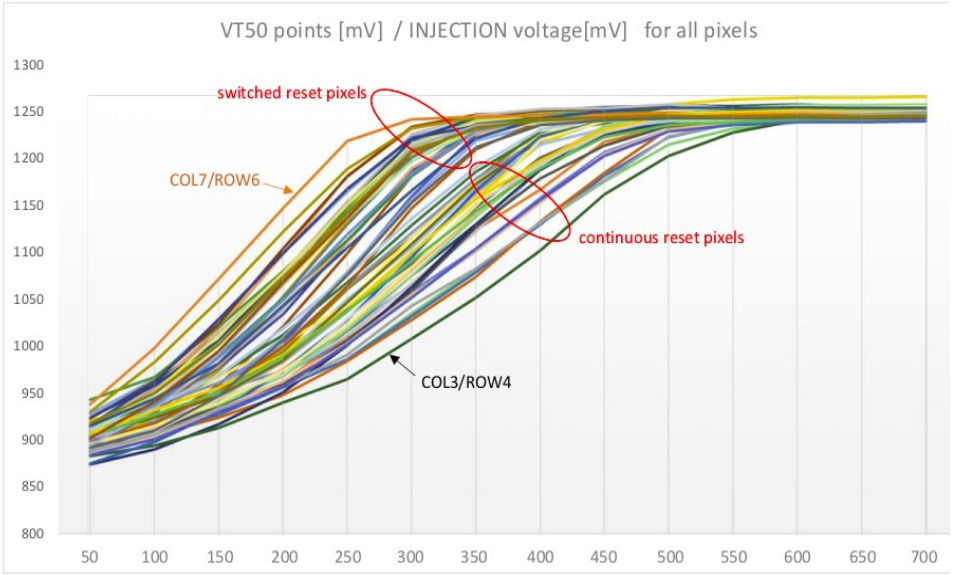
S-curves for all pixels with threshold variation. Trim DAC value 15. Injection amplitude 1500 mV.



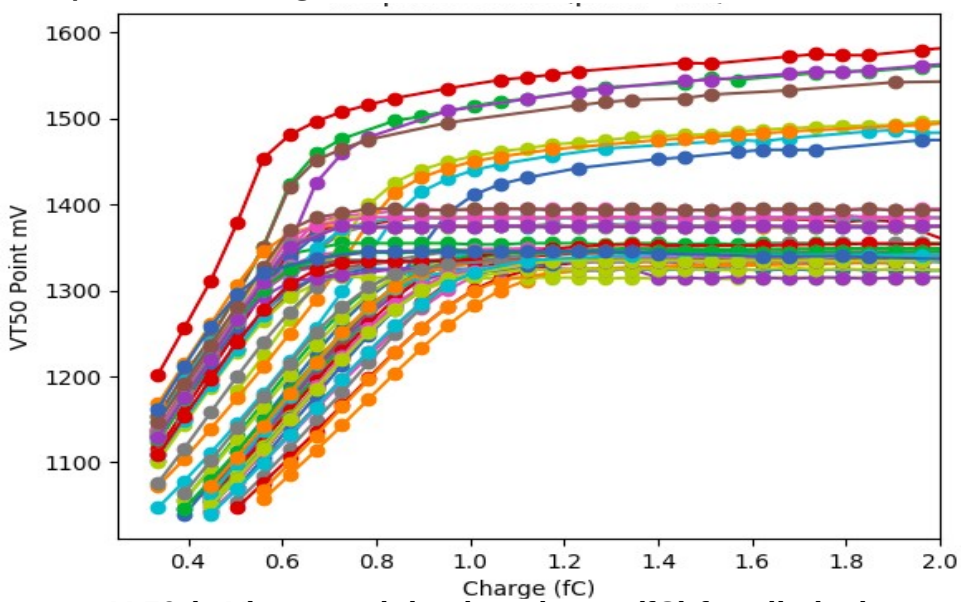
S-curves for all pixels with threshold variation. Trim DAC values adjusted. Injection amplitude 1500 mV.

Tests with pixel calibration circuit

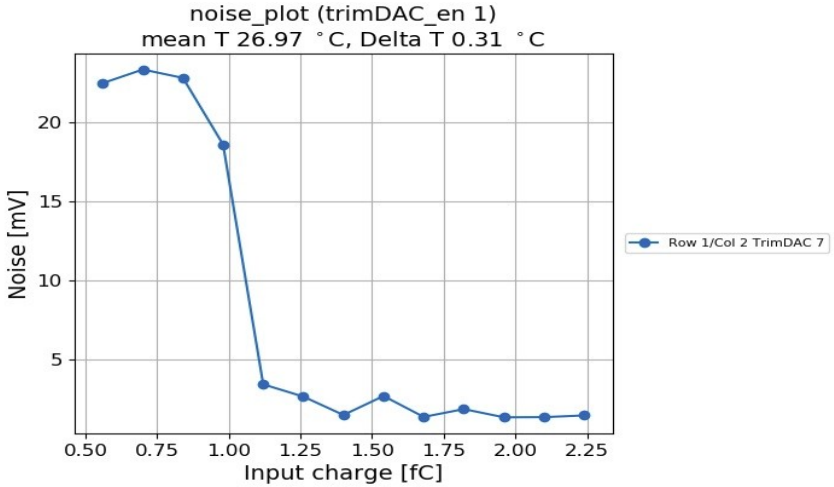
- Gain and noise measurements.
  - Vt50 value from s-curves versus injection amplitude/charge (1 fC = 357 mV).
  - Vt84 -Vt16 value from s-curves versus injection amplitude/charge.



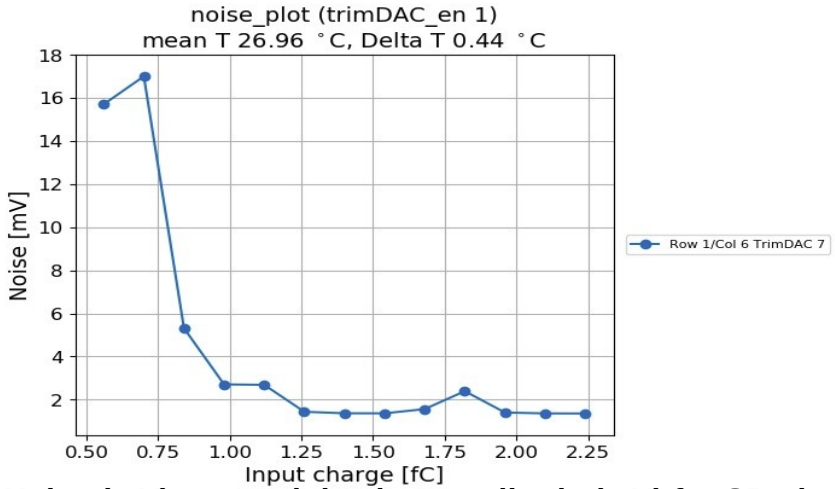
Vt50 (mV) versus injection amplitude (mV) for all pixels.



Vt50 (mV) versus injection charge (fC) for all pixels.



Noise (mV) versus injection amplitude (mV) for CR pixel (R1/C2).



Noise (mV) versus injection amplitude (mV) for SR pixel (R1/C6).

Tests with pixel calibration circuit

- Gain measurements summary.
  - Values measured at different places with different setups tend to agree.
  - Baseline value (comparator input DC value) influences the gain measured.

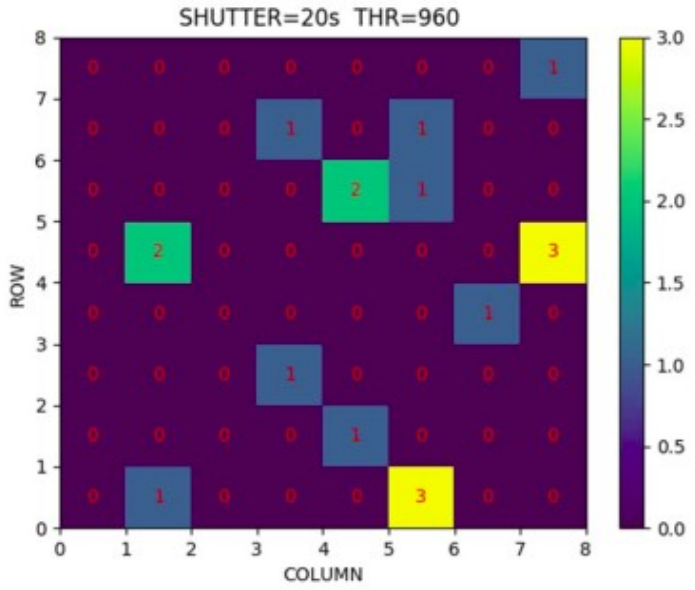
	Vienna		Liverpool		Valencia	
	CR	**SR**	**CR**	**SR**	**CR**	**SR**
Bias registers	Nominal values		Nominal values		Nominal values	
BL (mV)	800		900		900	
Linear range (mV)	150-450	150-450	150-400	150-350	150-450	150-450
Linear range[1] (fC)	0.42-1.26	0.42-1.26	0.42-1.12	0.42-1.12	0.42-1.26	0.42-1.26
Gain (mV/mV)	0.9-1.1	1.2-1.4	1.4-1.68	1.96-2.1	1.26-1.4	1.54-1.68
Gain[1] (mV/fC)	321-392	428-500	500-600	700-750	450-500	550-600
[1]Considering C_{inj} 2.8 fF						

Tests with radioactive source

- ^{90}Sr source (10 mCi/370 MBq) used.
- Two RD50-MPW2 samples measured (W14, > 2kΩ·cm).
- Shutter time per pixel 20 s.
- Noise trimming process (HV = -50 V): find trim DAC value per pixel to minimize noise.

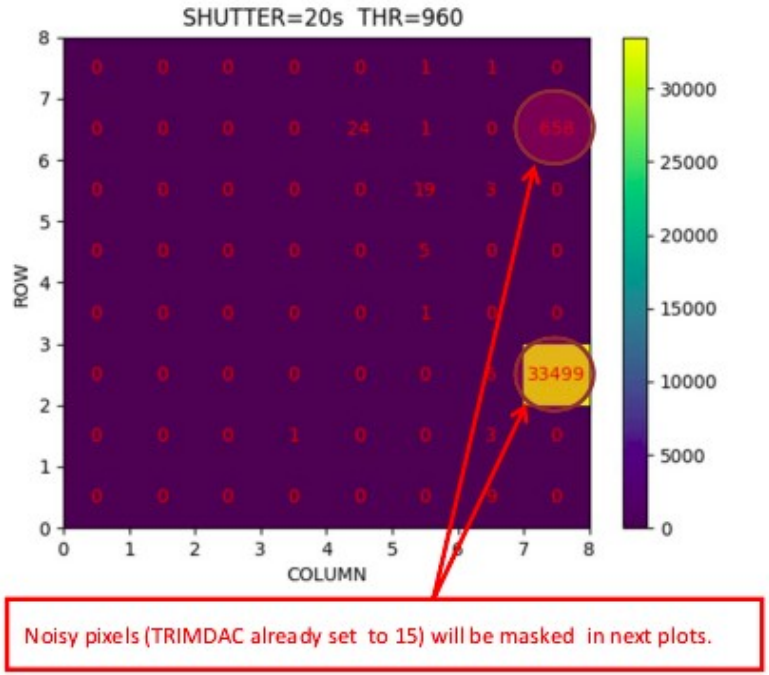
W14_1 >2 kΩ·cm

Noise trimming: HV=-50V BL=900



W14_2 >2 kΩ·cm

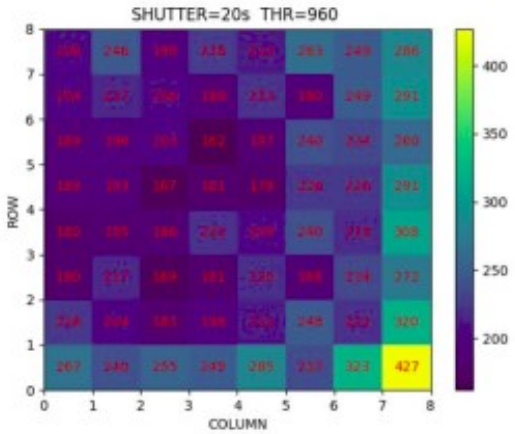
Noise trimming: HV=-50V BL=900



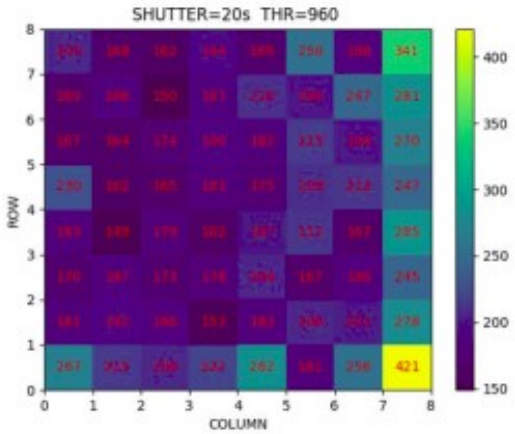
Tests with radioactive source

- Hitmap (W14_1) for different HV.

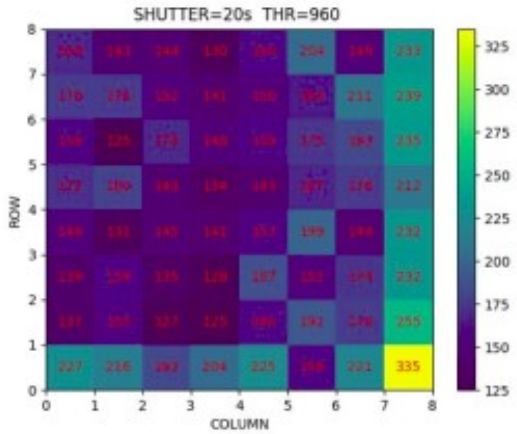
HV = -90V



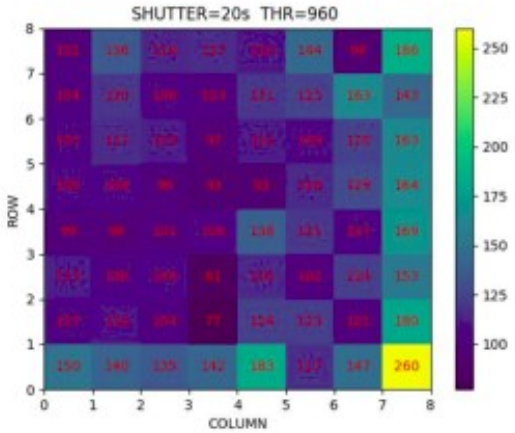
HV = -70V



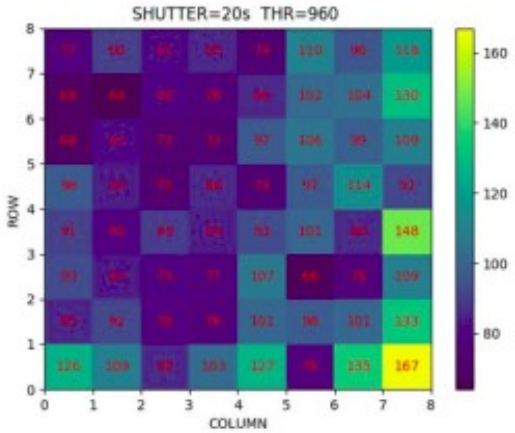
HV = -50V



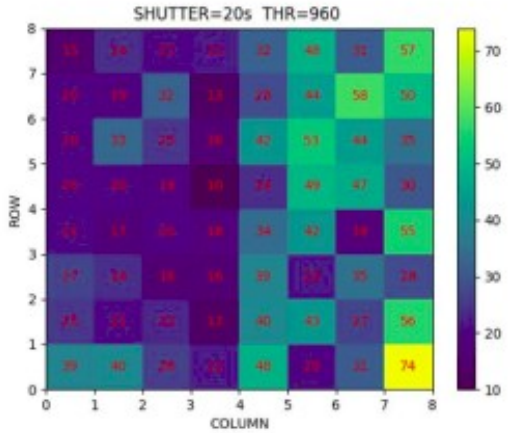
HV = -20V



HV = -10V



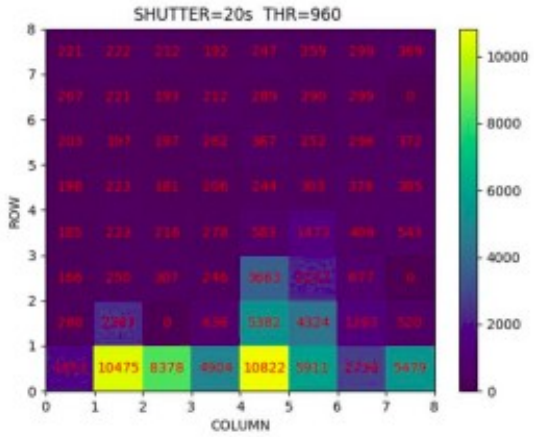
HV = 0 V



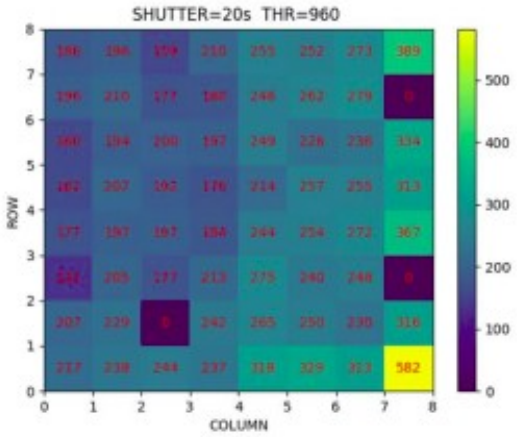
Tests with radioactive source

- Hitmap (W14_2) for different HV.

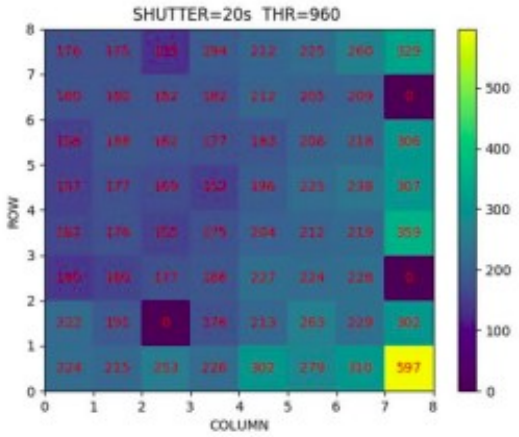
HV = -110V



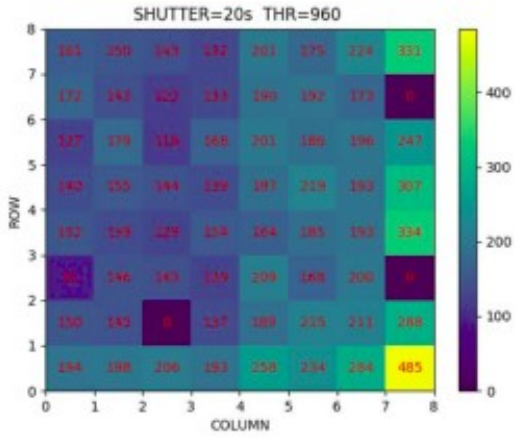
HV = -90V



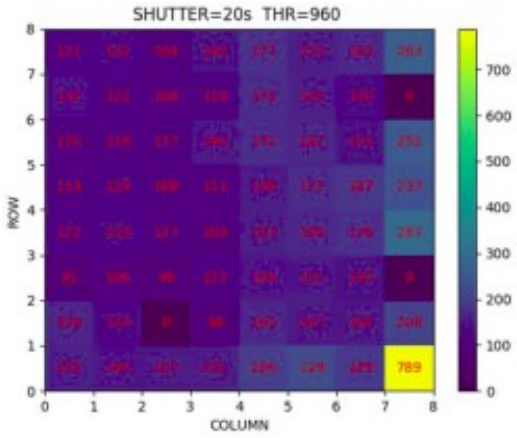
HV = -70V



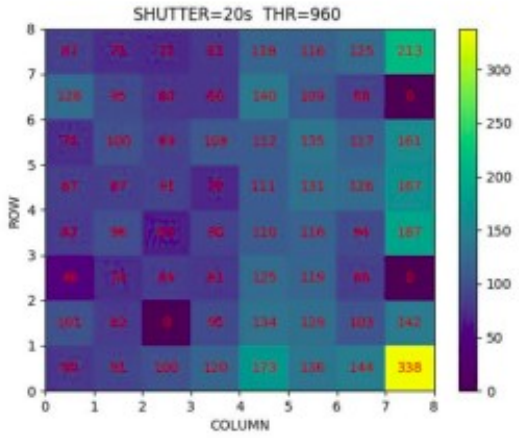
HV = -50V



HV = -30V

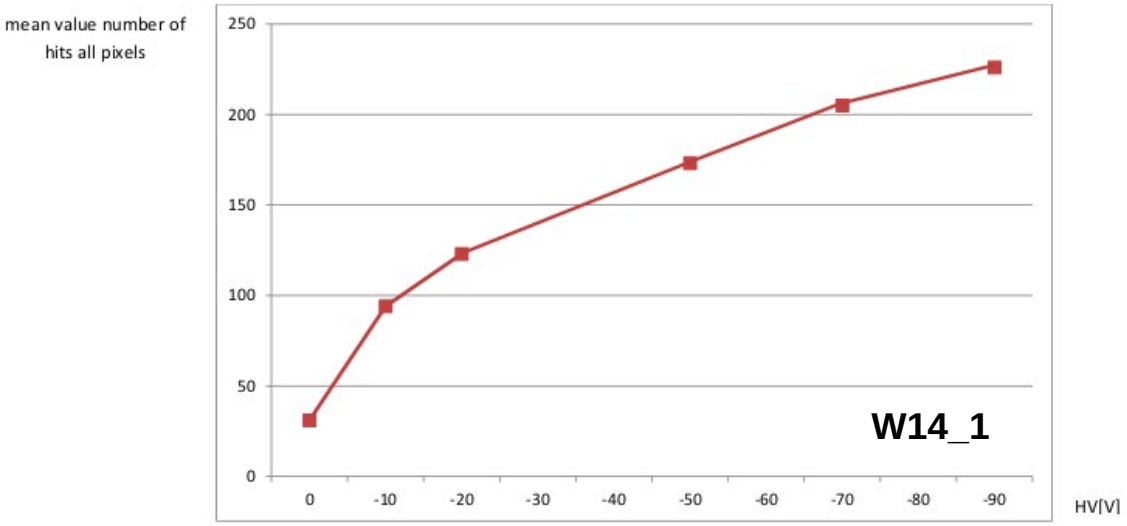


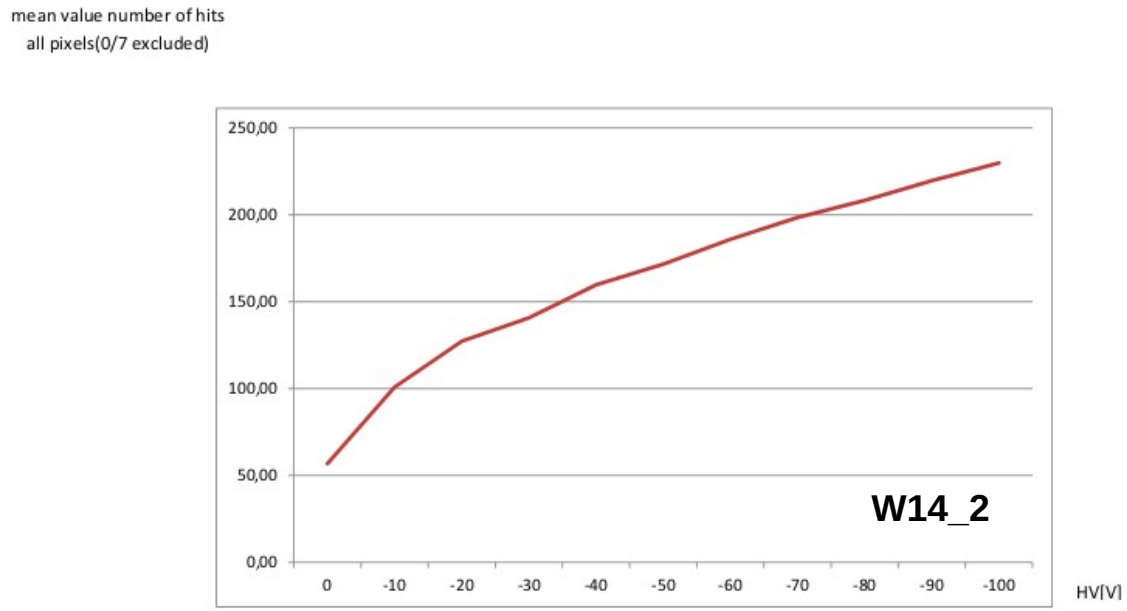
HV = -10 V



Tests with radioactive source

- Number of hits mean value (all pixels) versus HV.





Conclusion and outlook

- First lab tests and characterization of RD50-MPW2 active pixel matrix, bandgap voltage reference and SEU tolerant memory array presented.
- Bandgap voltage reference output voltage versus input voltage measurement agrees with simulated behaviour.
  - Next steps: output voltage variation with T and measurement with irradiated samples.
- SEU tolerant memory array implemented in AMS 180 nm CMOS process measurements show SEU robustness of DICE latch (x 15) and TRL DICE latch (x15000). MTBU of few hours for TRL DICE latch.
  - Next steps: LFoundry SEU memory and other chips tests at Groningen (KVI-CART).
- Extensive active pixel matrix lab measurements performed.
  - Verification of proper operation of different active pixel matrix blocks.
  - Tests with in-pixel injection circuit to characterize analog readout electronics.
  - Tests with radioactive source with pixels biased.
  - Next steps: analog readout electronics characterization with pixels biased, measurements with irradiated devices (neutrons) and TID measurements after X-rays (surface damage).

First tests and characterization of the RD50-MPW2 active pixel matrix, bandgap voltage reference and SEU tolerant memory

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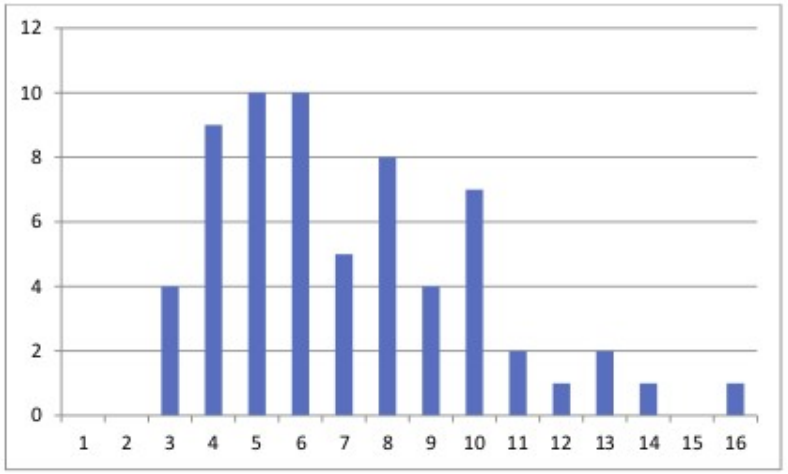
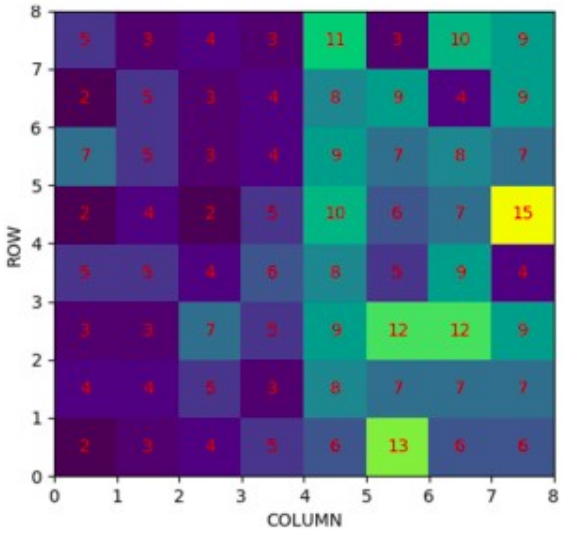
Tests with radioactive source

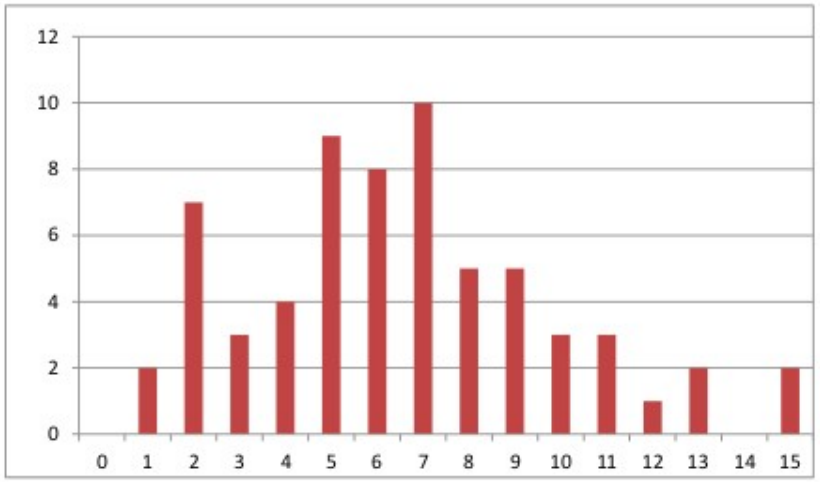
- Trim DAC values used to minimize noise.

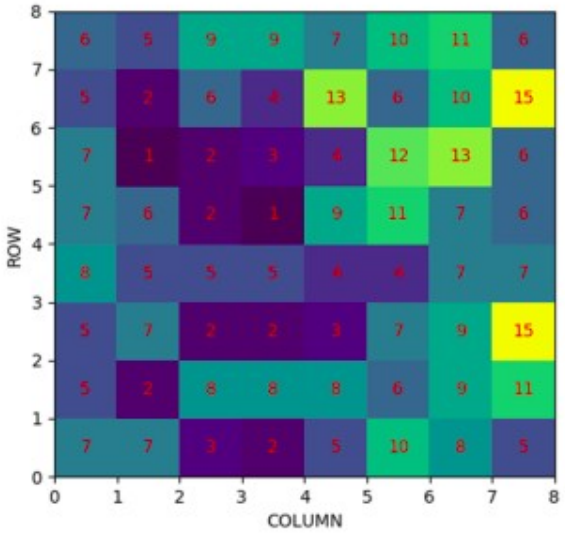
TRIMDAC values used for **W14_1**





W14_2





Tests with radioactive source

- Matrix row and column distribution.