Update on Radiation damage investigation of epitaxial P- type Silicon using Schottky/PN junctions

LGAD – GaN activities

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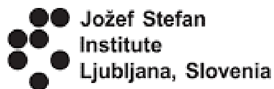

Overview

- Schottky project description and goals
  - update and fabrication details
- LGAD project description
  - design and simulations
- GaN devices
  - irradiation plan
- Summary

Schottky Project description and goals

1. RAL PPD, UK
2. IHEP, China
3. JSI, Slovenia
4. University of Birmingham, UK
5. University of Carleton, Canada

What: To fabricate a number of Schottky and n^+p diodes on p-type epitaxial (50µm thick) silicon wafers, of doping concentrations as they are normally found in CMOS MAPS devices

Why: The purpose is to investigate and gain a deeper understanding of radiation bulk damage in CMOS sensors. Also with a view to developing reliable damage models that can be implemented in TCAD device simulators (Synopsys or Silvaco)

How: We purchased 6 inch wafers, 25 x 5 B-doped epitaxial levels (10^{13}, 10^{14}, 10^{15}, 10^{16} and 10^{17} cm^{-3}), total **125 wafers**. The fabrication process has started both at ITAC (RAL) and Carleton University Microfabrication Facility (CUMFF). Tests will be carried out at RAL, Birmingham, JSI, CUMFF, IHEP.
The remaining wafers, upon agreement, could be distributed among other groups and/or RD50 institutes interested in participating in this project, whether at device design and/or at device test level

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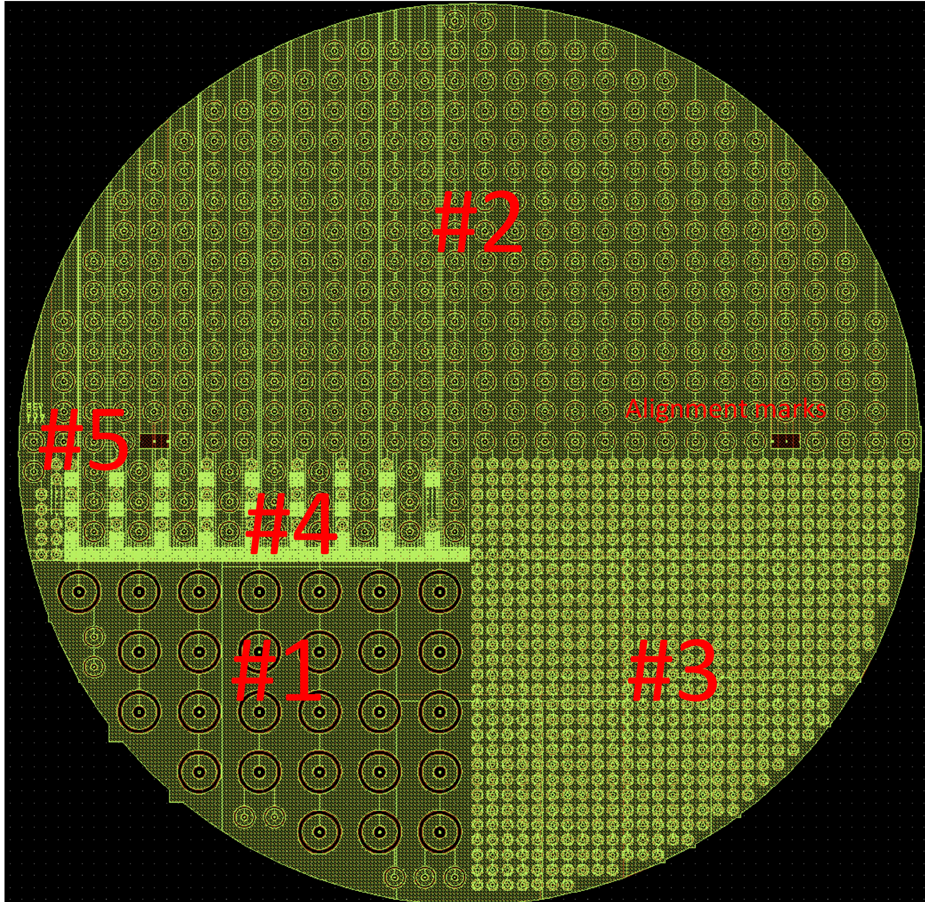
Design and layouts of devices

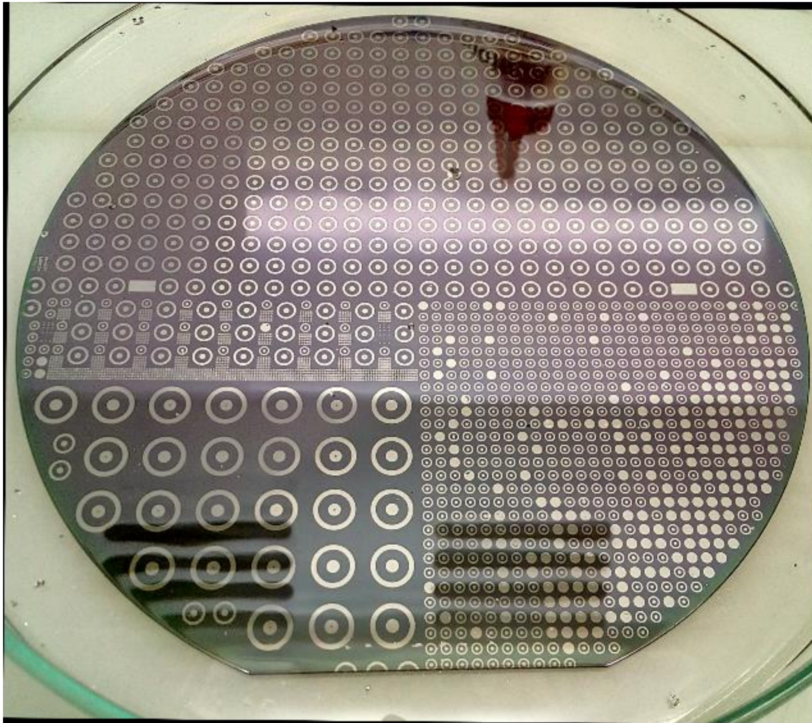
6 '' wafer:



5 type of devices proposed:

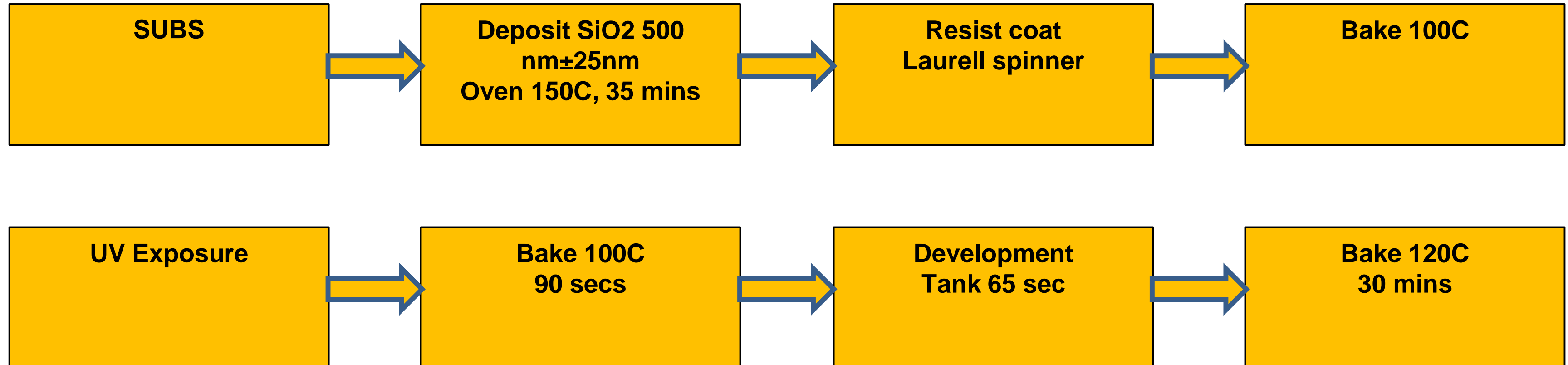
- **#1**: 2 mm Ø cathode with 0.4 mm Ø central hole, device inside a 10 x 10 mm2 area
  IV,BV, CV, Laser injection test
- **#2**: 1 mm Ø cathode, 0.2 mm Ø central hole device inside a 5 x 5 mm2 area
  IV,BV, CV, MIP Laser injection test
- **#3**: 0.5 mm Ø cathode, no central hole device inside a 2.5 x 2.5 mm2 area
  IV,BV, CV, MIP injection & TCAD comparison
- **#4**: 0.1 mm Ø cathode, no central hole device inside a 0.5 x 0.5 mm2 area
  IV,BV, CV, MIP injection & TCAD comparison
- 'cell' with the previous 3 flavors (2,3,4) grouped together, to exploit wafer uniformity on small area
- #5: 6 TLM points for contact and epi resistance
- 2 masks only (metal and oxide)
- For detailed description see previous 35th RD50 workshop

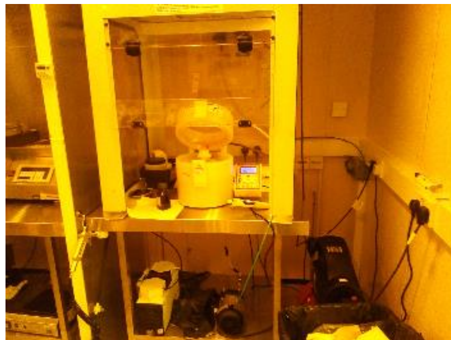
Project Update

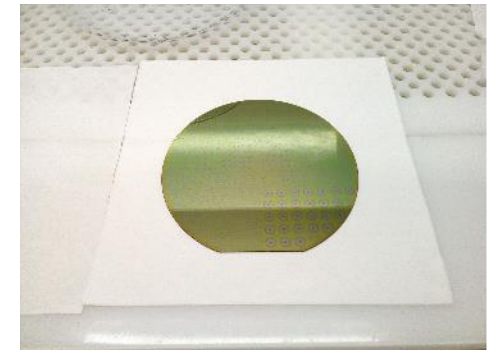


- All wafers arrived to RAL back in January (HR arrived earlier)
- All related activities stopped beginning of March
- Currently completed the first HR 6’’ wafer that includes Schottky diodes at RAL/ITAC
- Also completed the first HR 4’’ in wafer at CUMFF that includes PN junctions. Very preliminary results
- Description of fabrication process in the next slides

Schottky fabrication details RAL-ITAC

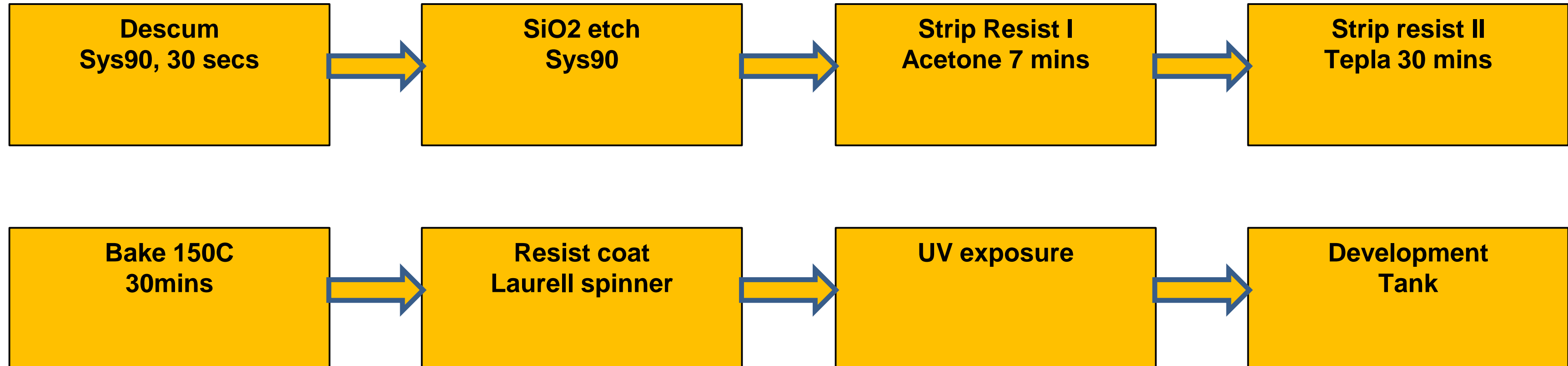


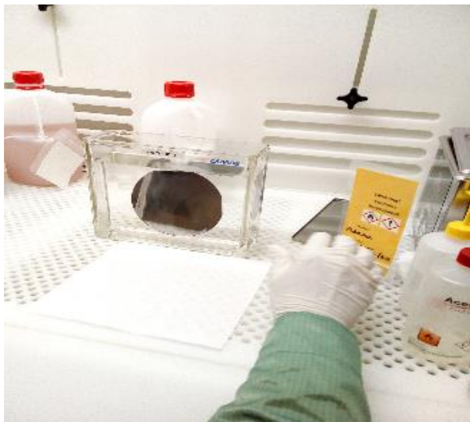

Resist spinner


6'' wafer with developed resist for Oxide etching

- Fabrication process I for Schottky diodes at ITAC, RAL
- Process steps were optimized first by processing test wafers

Schottky fabrication details RAL-ITAC

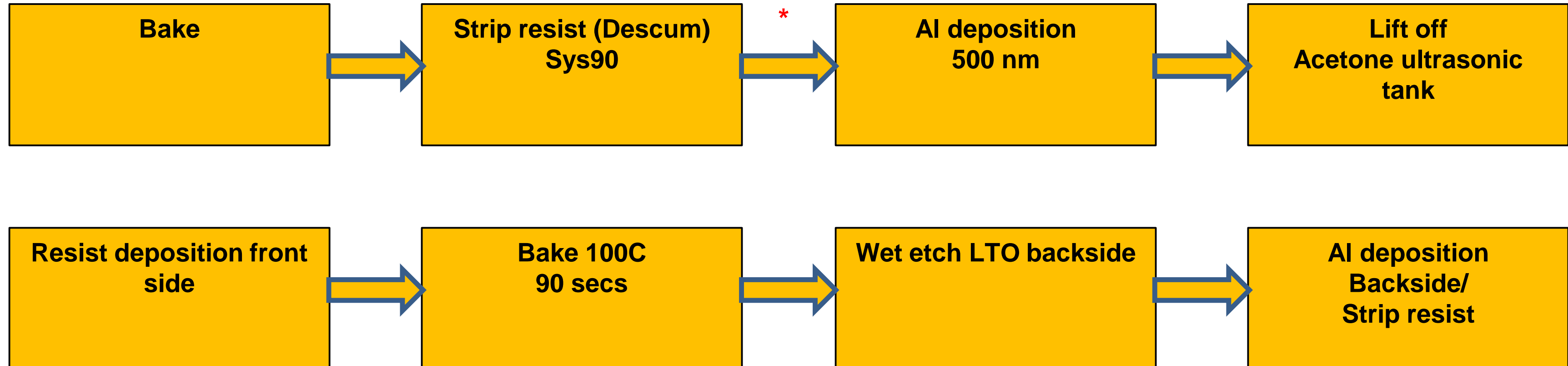




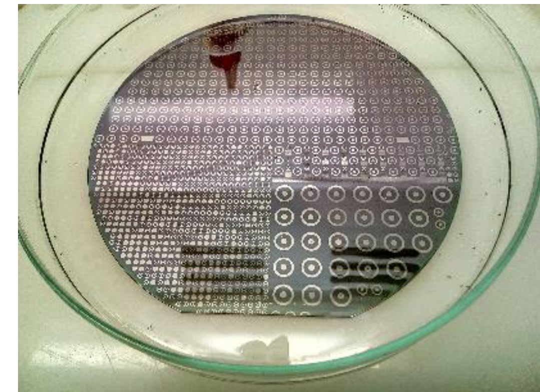
6'' wafer in ultrasonic bath

- Fabrication process II for Schottky diodes at ITAC, RAL

Schottky fabrication details RAL-ITAC



CVC601 Sputtering machine

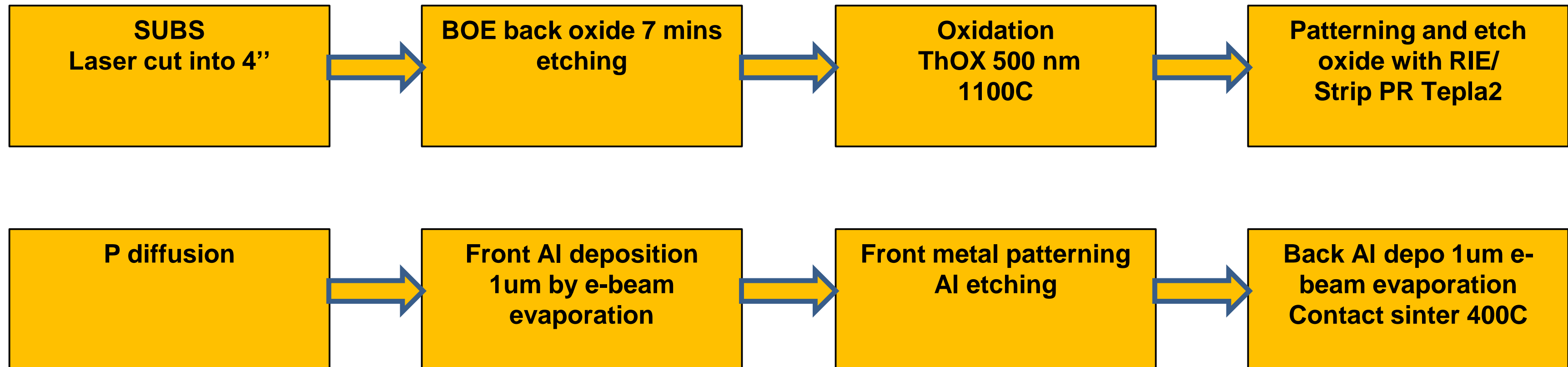


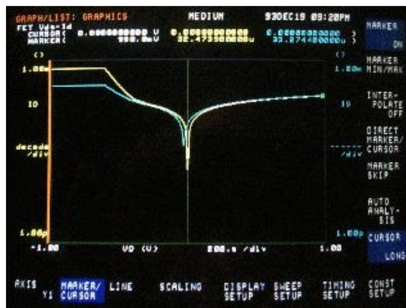
Final Al lift off of the first 6'' HR wafer

- Fabrication process III for Schottky diodes at ITAC, RAL
- First HR wafer complete, will start testing when possible

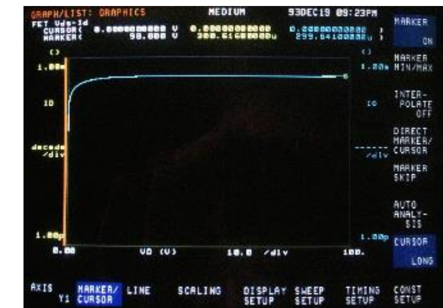
* No extra SiO2 thin layer added in this iteration

PN junctions fabrication details CUMFF



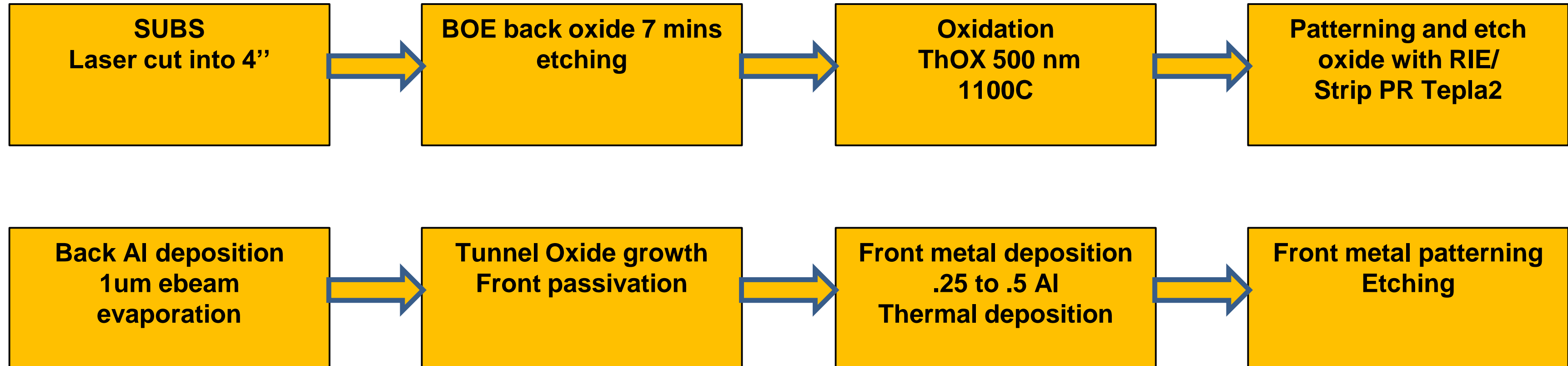


IV HR 2mm PN junctions
Cathode
GR (gnd)



- Fabrication process for PN junction diodes at CUMFF, Carleton University
- Two 4'' HR runs completed - one 4'' wafer arrived to RAL late February, will test it when possible
- Very preliminary results done at CUMFF show BV > 100V and high surface current

Schottky fabrication details CUMFF



- Fabrication process for Schottky diodes at CUMFF, Carleton University
- First steps completed on HR 4'' wafer up to Oxidation step

<u>* When again possible, the test of theses devices will follow the same plan as described in previous RD50 workshop</u>

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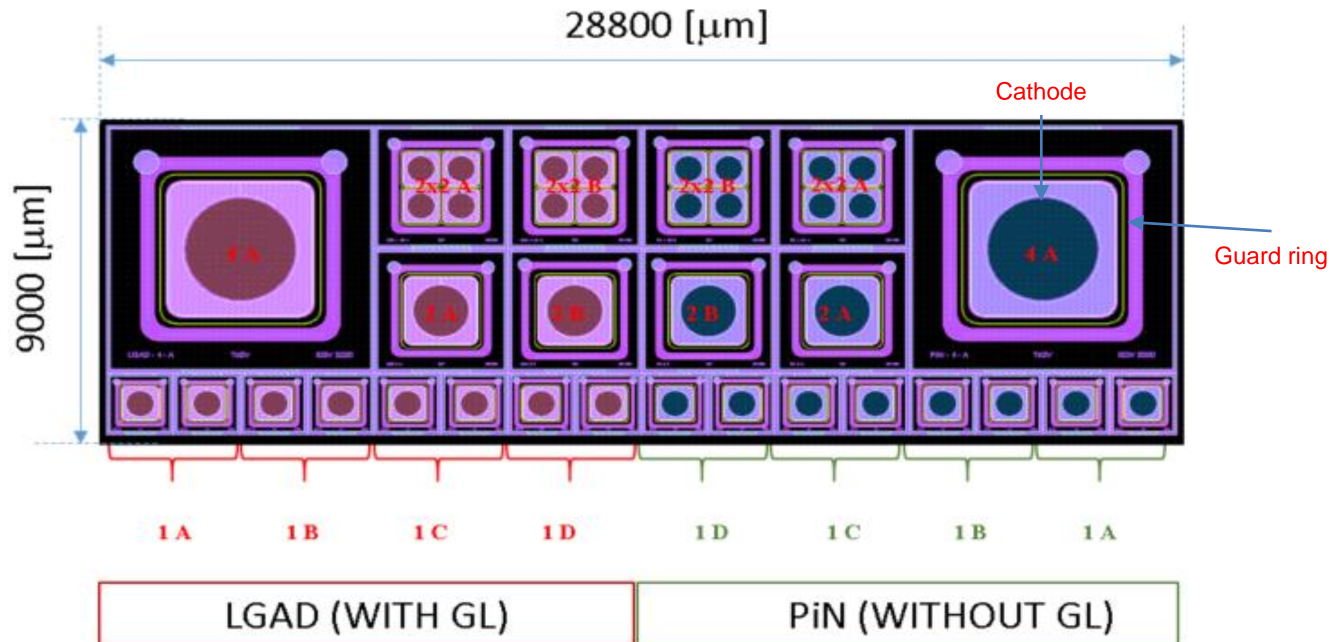
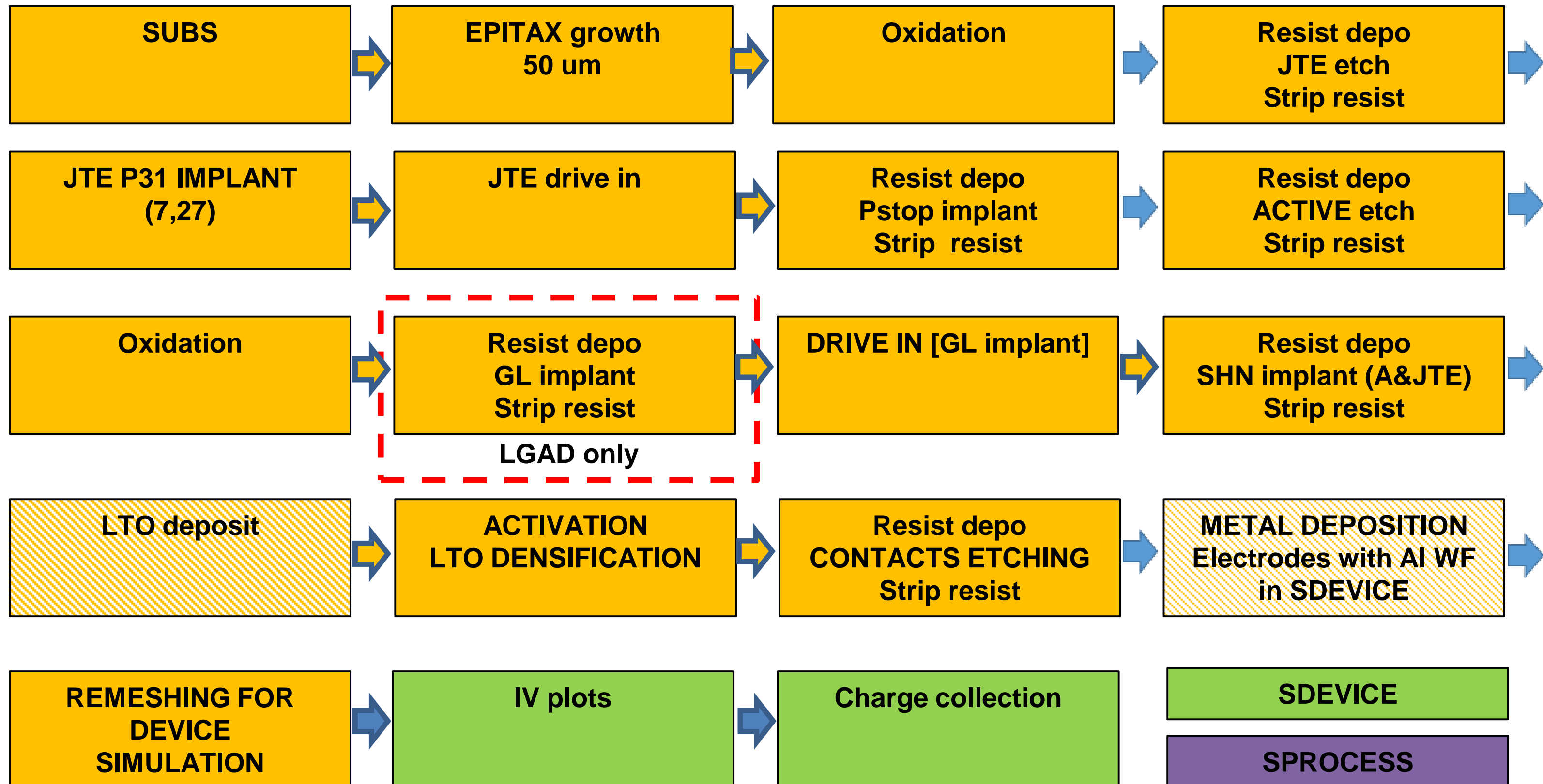
LGAD Project description and goals



A RAL, University of Oxford, University of Birmingham and Open University project in collaboration with Teledyne e2v foundry for LGAD production

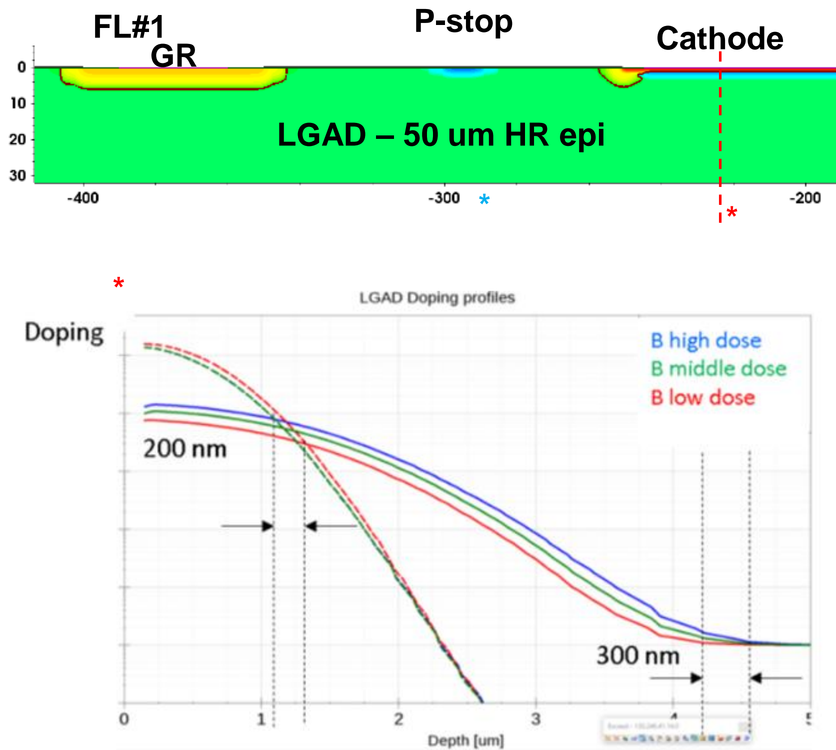
- Three types of cathode size of single cells and one of 2 x 2 array of cells. Up to four different cell layout flavors are implemented with different distances of guard ring to the cathode
- LGAD and PiN diodes share the same layouts on each split, only difference being the presence or not of the gain layer
- Three different gain layer doses and energy
- Fabrication expected July 2020

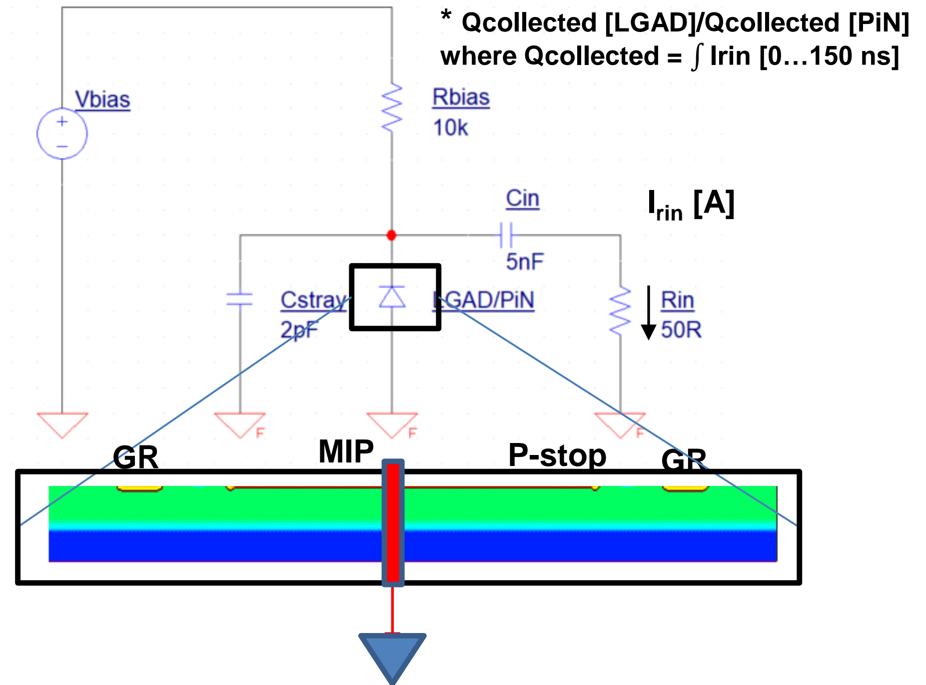
LGAD simulations



- Full process simulation implemented for LGAD and PiN

LGAD simulations





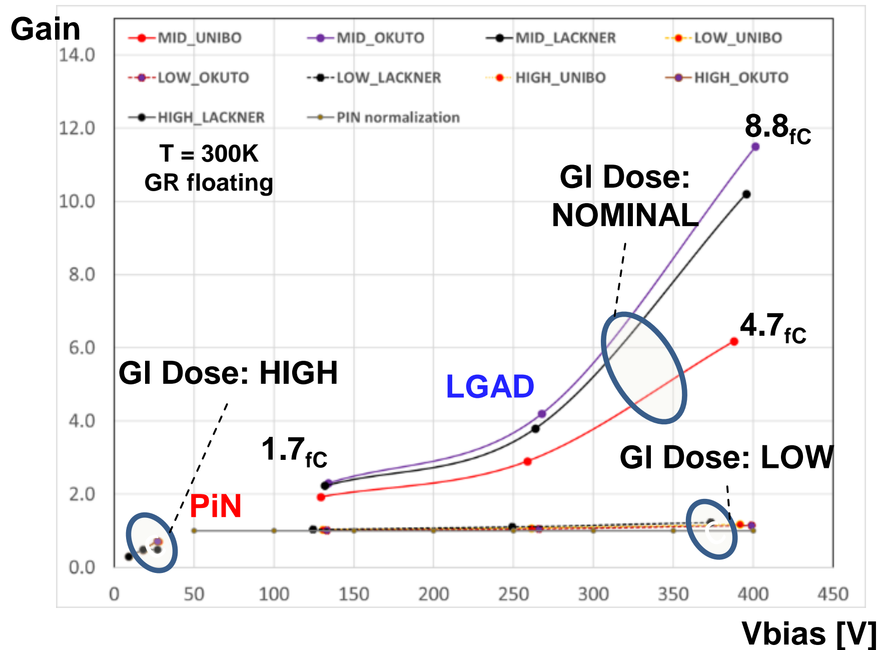
- Extension of GL changes by around 0.5 um in going from LOW DOSE to MAX DOSE

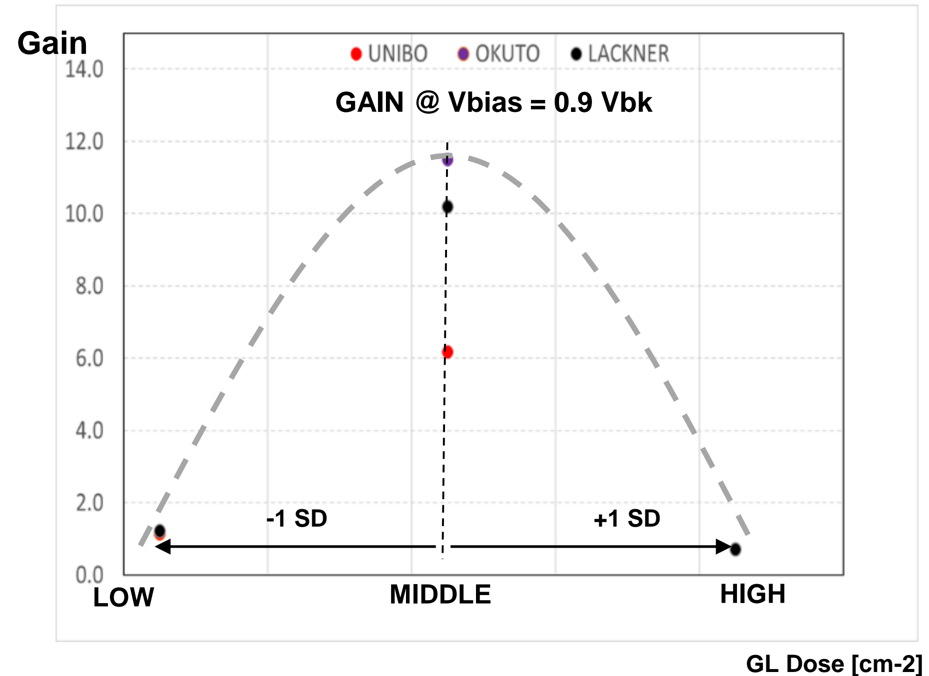
Electrical simulation setup, common to PiN and LGAD, with RC network

- IV plots
- Bulk radiation damage not included in this iteration, but SiO_2-Si interface traps implemented
- CCE for vertical MIP hit (80 e/h /um) through centre

* with no SRH Qcoll ~ Qinj ± 0.1%

LGAD simulations

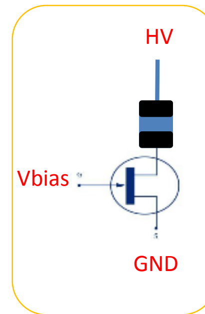


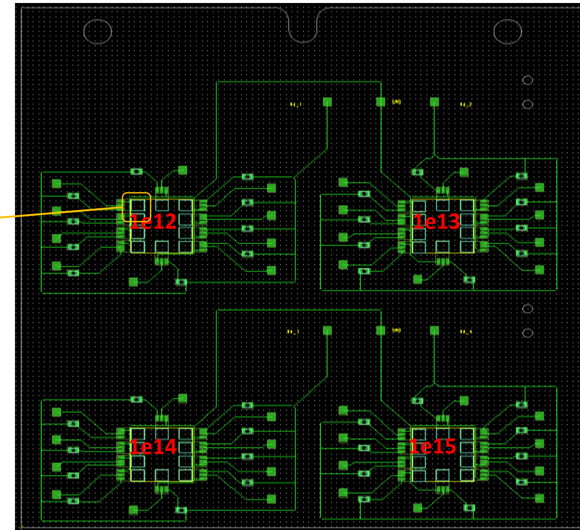


- **Gain is defined as ratio of LGAD/PIN collected charge for a 50 ns transient and normalized to 0.3,0.6,0.9 BV**
- **Each LGAD gain curve is normalized w.r.t. PIN that uses the same Impact Ionization model (3 models used: Unibo, Okuto, Lackner)**
- **A gain of > 10 is predicted for 2/3 I2 models used for the MIDDLE dose**
- **At GL dose that differ by 1 SD the gain reduces to 1 or less (i.e. little difference w.r.t. to PIN or early BV prevents epitaxial depletion, hence little charge collected)**

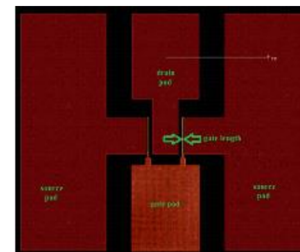
GaN devices irradiation plan

- **In collaboration with NRC, we plan to investigate the possible use of GaN-based devices for next generation of rad-hard detectors/electronics, in line with RD50 mandate for next years' R&D work**
- **Depletion HEMT GaN devices characterization already performed at NRC**
- **We are planning to irradiate some GaN HEMTs fabricated by NRC with 26MeV p up to fluences of 1e15 [cm-2] (i.e. TID around 230Mrad [GaN]) to compare them with previously irradiated Panasonic GanFETs used in Strips ITK**
- **Irradiation campaign was scheduled for March 2020, postponed to maybe late summer**
- **If test is successful our intention would be to submit an RD50 related proposal**





PCB holding up to 40 NRC 1x2 mm2 GaN devices, divided into 4 blocks. Each block of 10 devices receives a different p fluence, up to 1e15 [cm-2]



NRC 1x2 mm2 GaN HEMT layout.
Each 1x2 mm2 chip contains 4 HEMTs, differing in gate length

Summary and Conclusion

- First HR wafer processed for Schottky devices is ready. Tests will resume as soon as lab facilities reopen
- First HR wafers processed for PN junctions fabricated at CUMFF are ready and additional Schottky will be soon. Very preliminary results on a PN device show BV higher than 100V and high surface current. Tests will resume as soon as lab facilities reopen
- LGAD project ongoing. First batch of fabricated LGAD devices available by August
- Planned irradiation of NRC GaN devices will commence when facilities will become available again.

THANK YOU