Effects of neutron irradiation on HV-JFETs

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36th RD50 Workshop – June 5th 2020

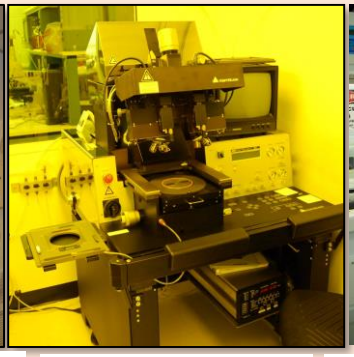
Outline

- HV silicon JFET
  → for multiplexing in ATLAS ITk
  - concept
  - Measurements after irradiation (TRIGA, JSI, Ljubljana, Slovenia)
  - TCAD simulation to get insight of the physics

Review other known irradiation effects:
- Double peak in electric field
- Stability of scribeline

All silicon process done in BNL Instrumentation Division Class-100 Clean Room

Furnaces for dry oxidations and annealings



Double-sided mask aligner

Wet bench (HF, RCA I & II, piranha, polyetch, …)

Sputtering (Al, Al1%Si, Ti)

RTA for sintering

Laser dicing

+ dry etching and thin films deposition, but we need to outsource:
- Ion implantation
- Polysilicon depostion

A novel HV silicon JFET for ATLAS, and other silicon R&D activities at BNL

32nd RD50 workshop – 4-6 June 2018 Hamburg

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U.S. DEPARTMENT OF ENERGY

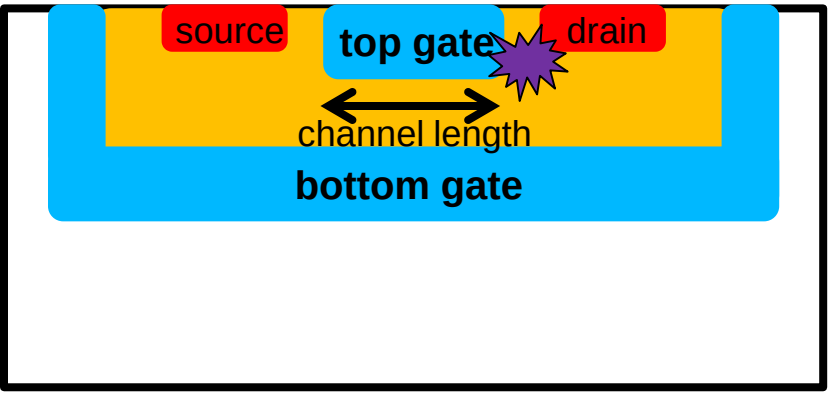
Irradiated at the TRIGA reactor at JSI (Ljubljana, Slovenia) with 4e14, 8e14, 1.5 e15 n_{eq}/cm^2

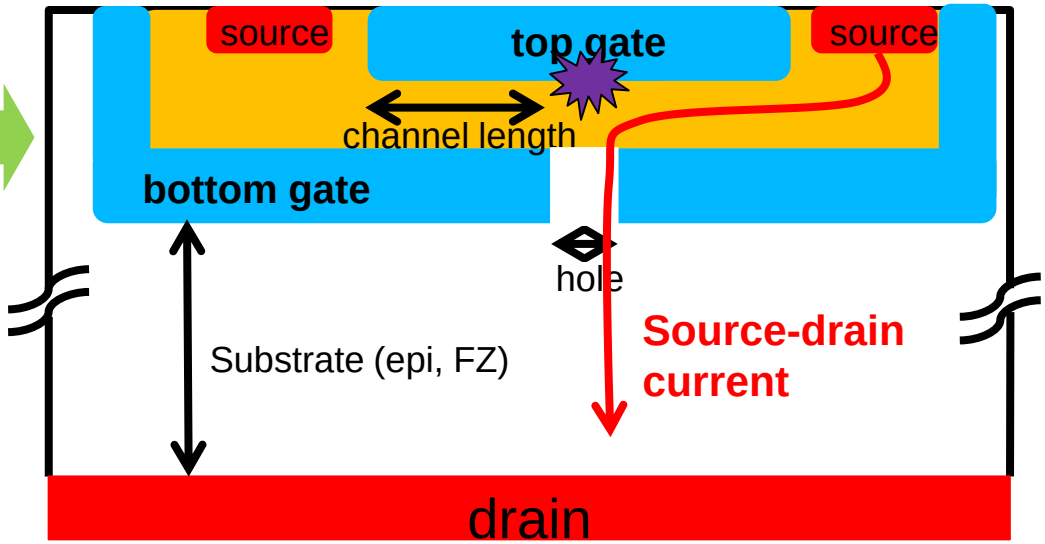
G. Giacomini, et al., “Fabrication and Electrical Characterization of High-Voltage Silicon JFETs”, 2019 JINST 14 P05007.
G. Giacomini, et al., “High-Voltage Silicon JFET for HV Multiplexing for the ATLAS MicroStrip Staves” POS(TWEPP2018)030.
G. Giacomini, et al., “A HV Silicon vertical JFET: TCAD simulations,” Nucl. Instrum. Methods A, vol. 919, 2019 , pp. 119-124.

The vertical HV Silicon JFET

Originally, conceived as a rad-hard switch to be used in the ATLAS ITk HV-Mux. GaN JFETs are very rad-hard, so HV-Mux will go with GaN.

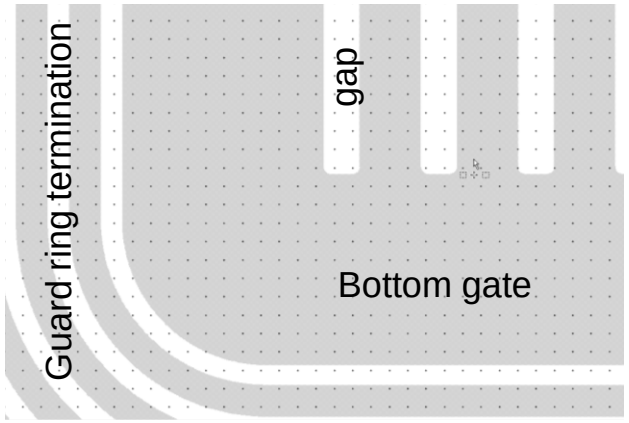
We can modify the structure of the standard JFET by making a gap in the bottom-gate.
Over the gap, the top-gate. The channel and the source as in the standard JFET. The drain is the back contact.
The current flows (= drifts) from source to drain through the gap in the bottom-gate.
The high voltage applied to the drain falls in the thick substrate, being the bottom-gate almost a planar implant.

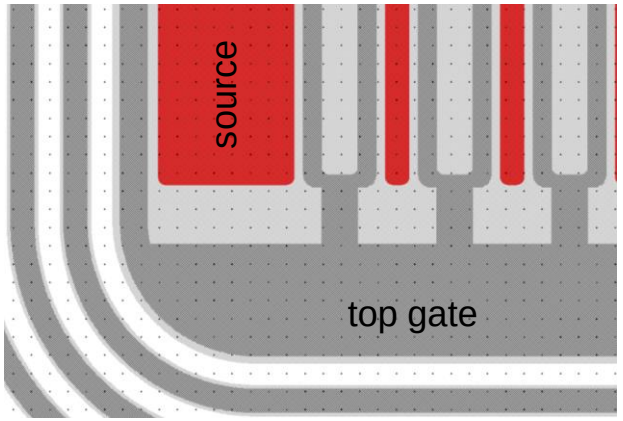


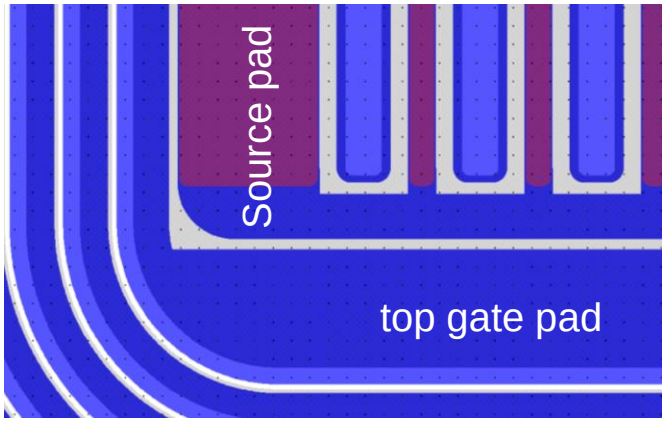


The highest electric field develops at the junction top-gate/channel, so special care in the choice of the parameters (hole width, channel doping concentration).
GR termination also needed at the border of the bottom-gate.

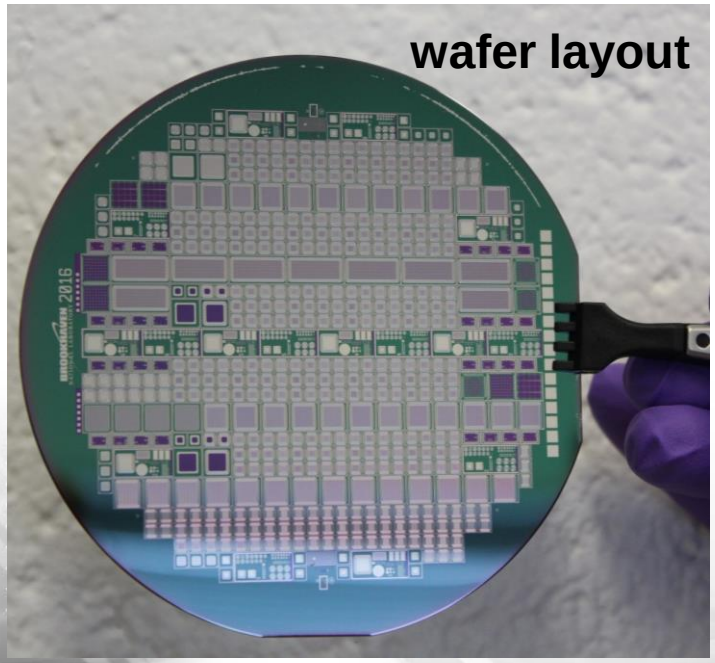
The layout

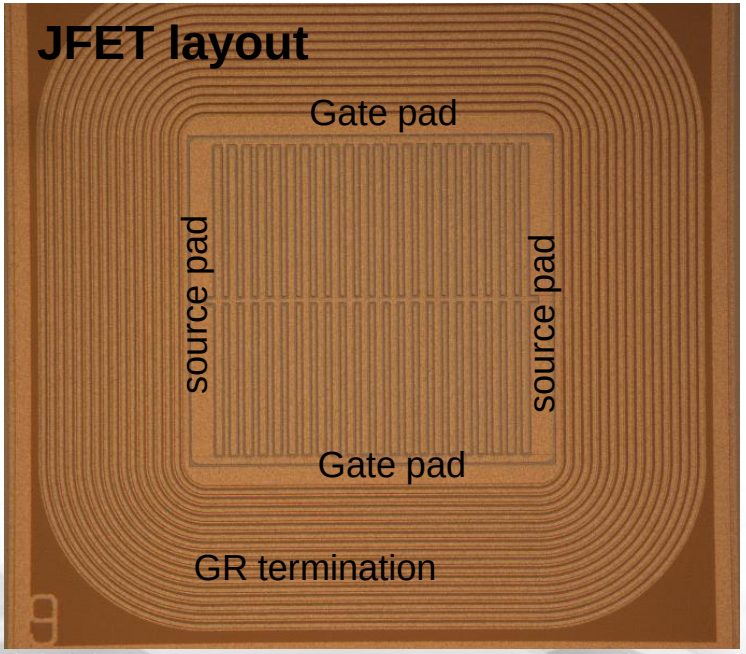






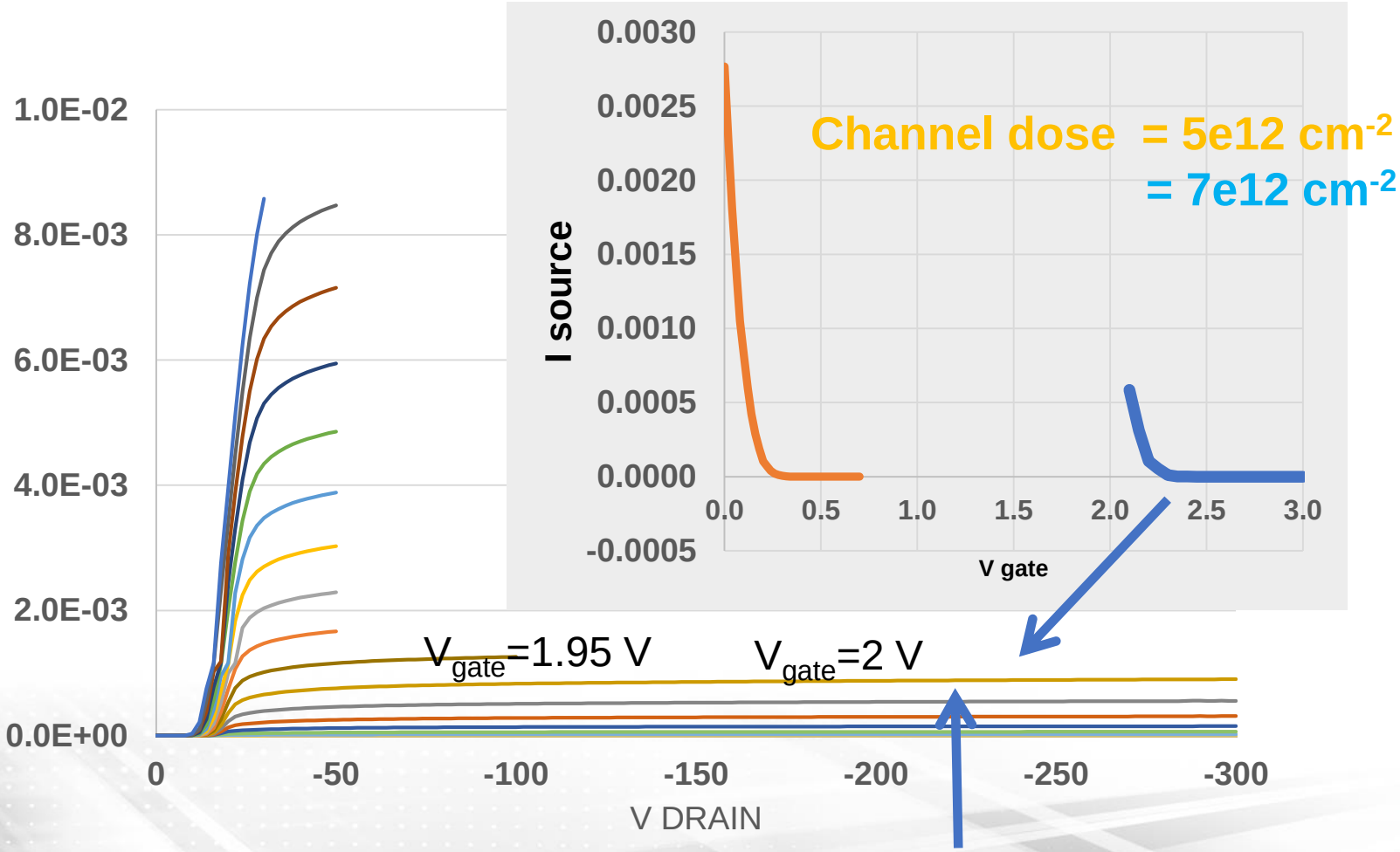
Interdigitated design to increase the gate width and thus the ON current (especially after irradiation).
The active area is 1x1 mm^2, which sets the gate width to 20 cm.
Triode configuration, top-gate connected to the bottom-gate.
6 photolithographic masks, 4 implants.
Both *n*-type and *p*-type JFET, on 4" epitaxial wafers (TOPSIL): 50μm thick, N_C~ 1e14cm^{-3}.





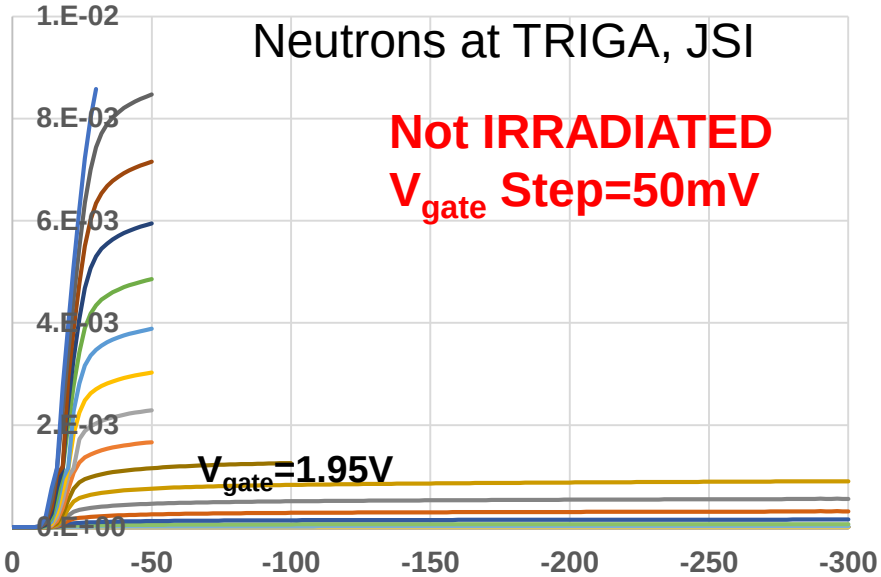
I-V characteristics before irradiation

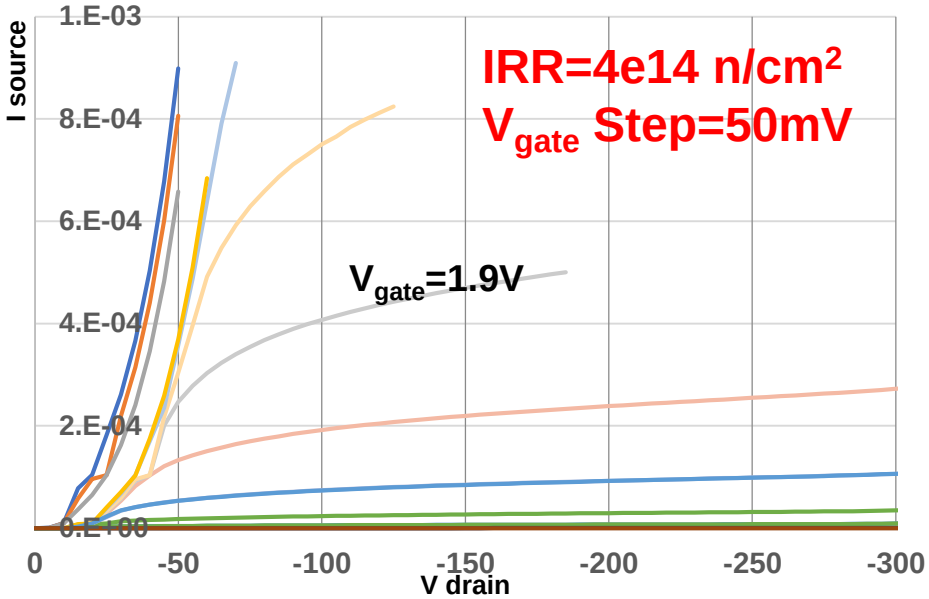
Splittings on the channel dose.
At the lower doses, the channel was pinched-off already at V_{gate}=0V
The higher the dose, the lower V_{BD}.



We irradiated the devices with higher current capability (but lower V_{bd})

Irradiation results

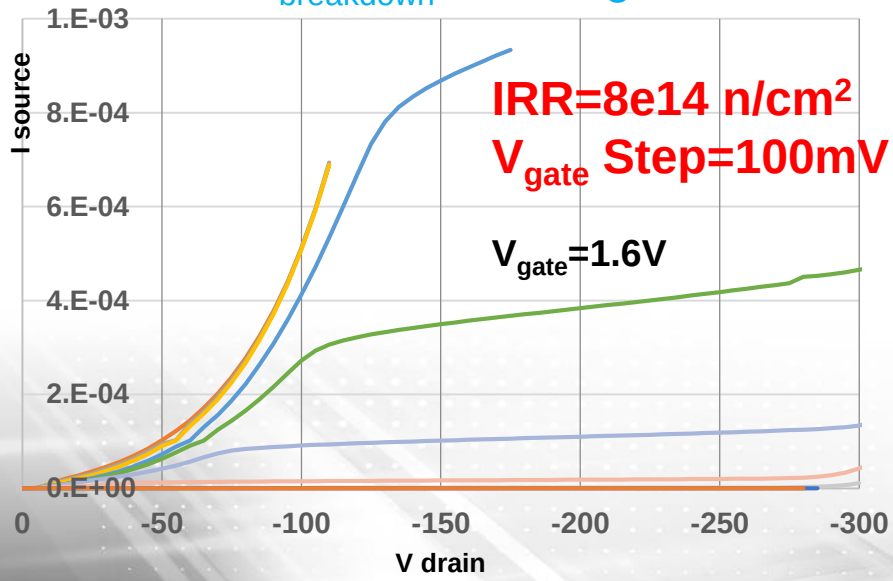


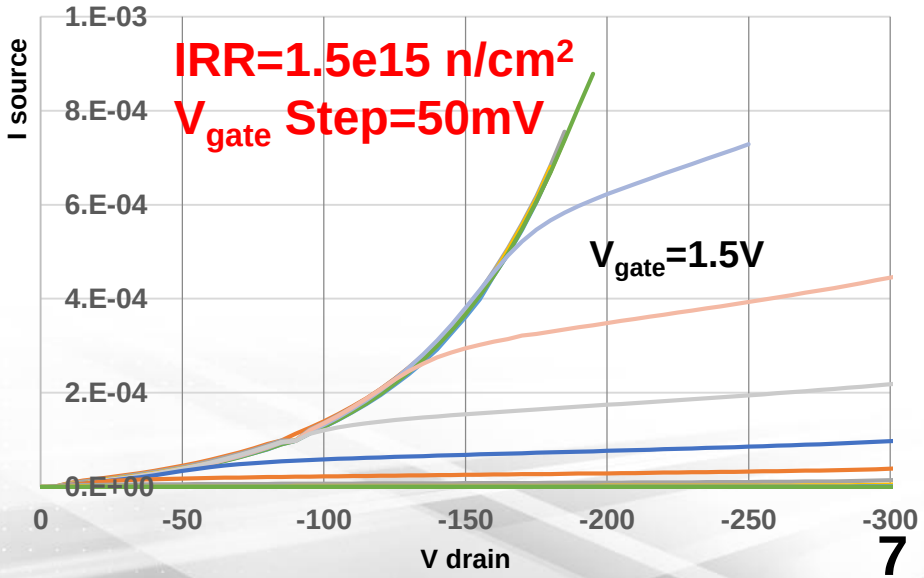


1- effect of acceptor removal: lower V_{gate} needed to pinch-off the channel

2- dramatic change of $V_{drain,\ \mathbf{Saturation}}$ with fluence

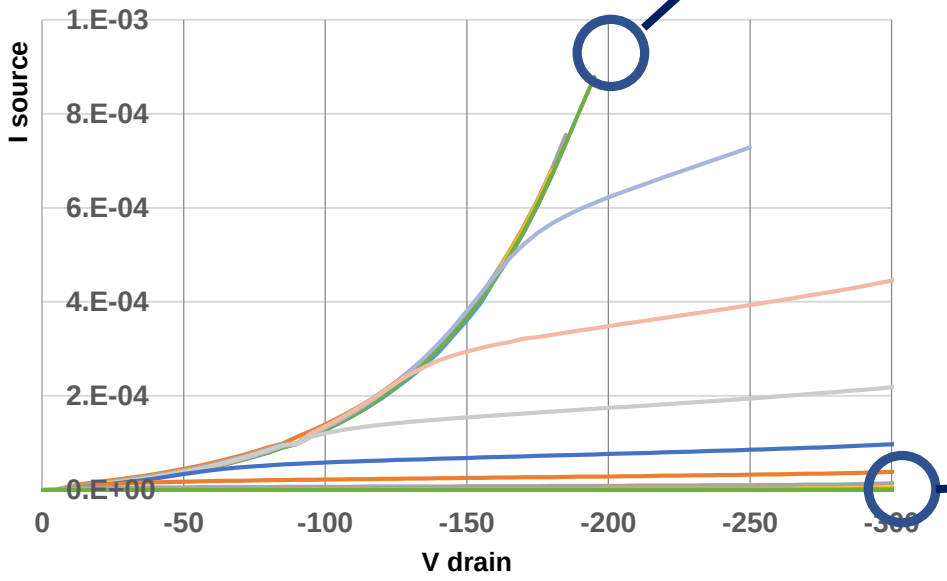
3- $V_{breakdown}$ unchanged





Suitability as a switch for HV-Mux

IRR=1.5e15 n/cm²



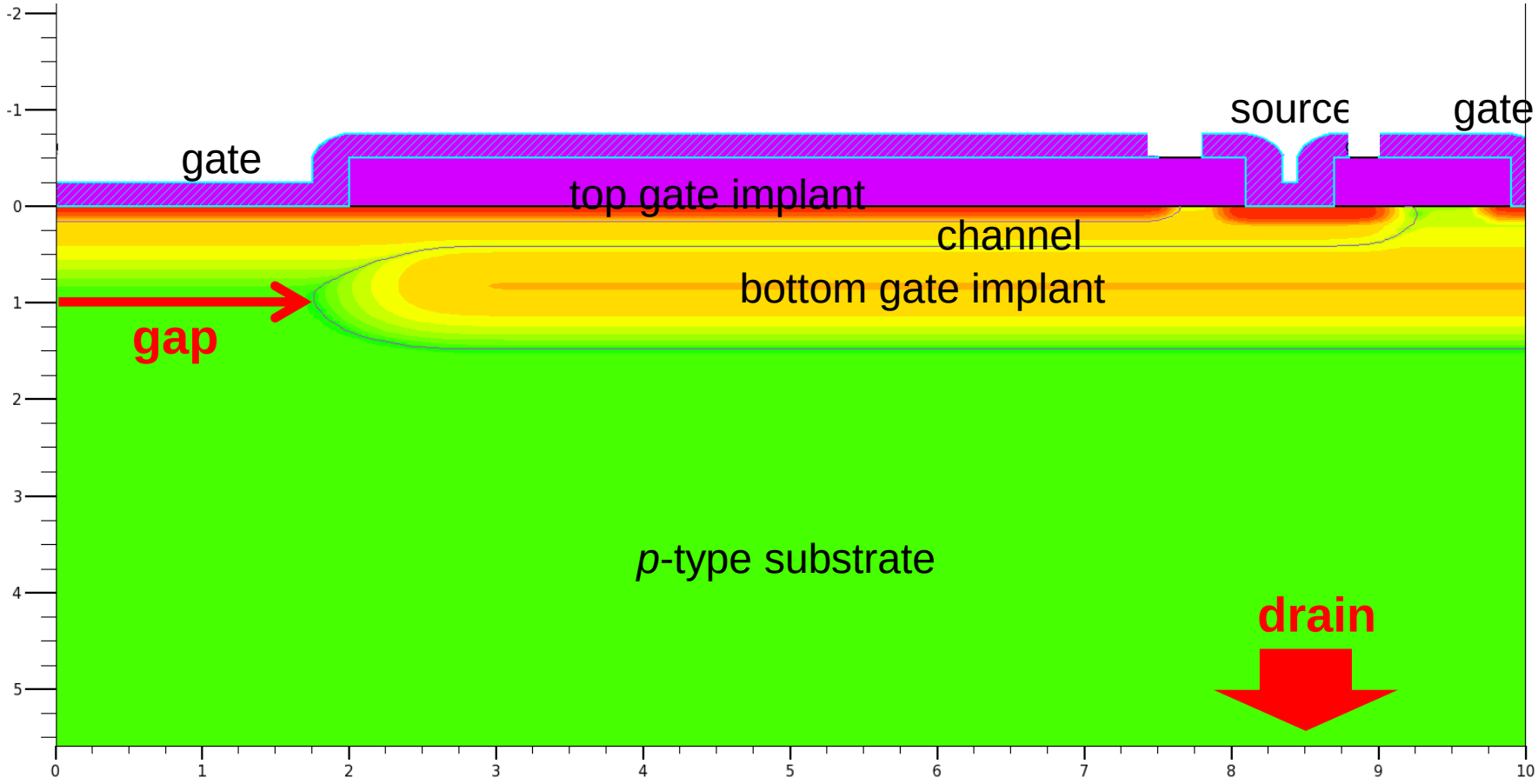
ON state:

- ideally, V_{drain} ~0, I_{drain}~ infinity
- $I_{drain,\ saturation}$ limited by the channel dose (which needs to be small to have high VBD)
- $V_{Drain,\ saturation}$ very high: high power dissipation within the JFET

OFF state:

- $V_{breakdown}$ low (600V needed)
- Gate leakage current ~ OK

TCAD simulations



Perugia model:

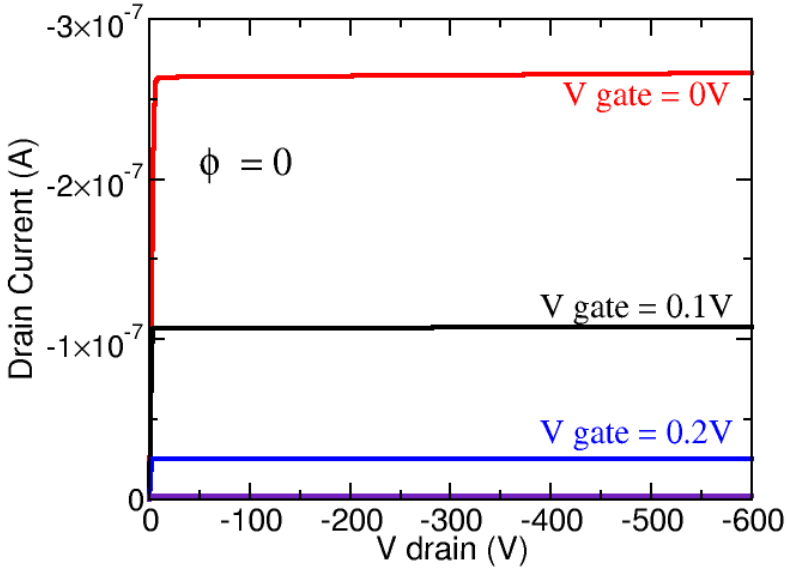
#fluence = Φ n_{eq}/cm2

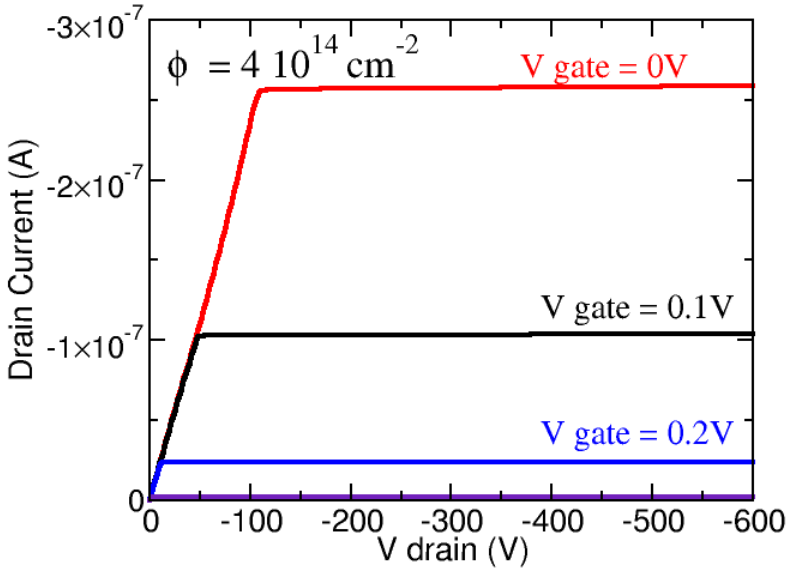
trap acceptor e.level=0.42 density=1.6* Φ degen=1 sign=2e-15 sigp=2e-14

trap acceptor e.level=0.46 density=0.9 * Φ degen=1 sign=5e-15 sigp=5e-14

trap donor e.level=0.36 density=0.9 * Φ degen=1 sign=2.5e-14 sigp=2.5e-15

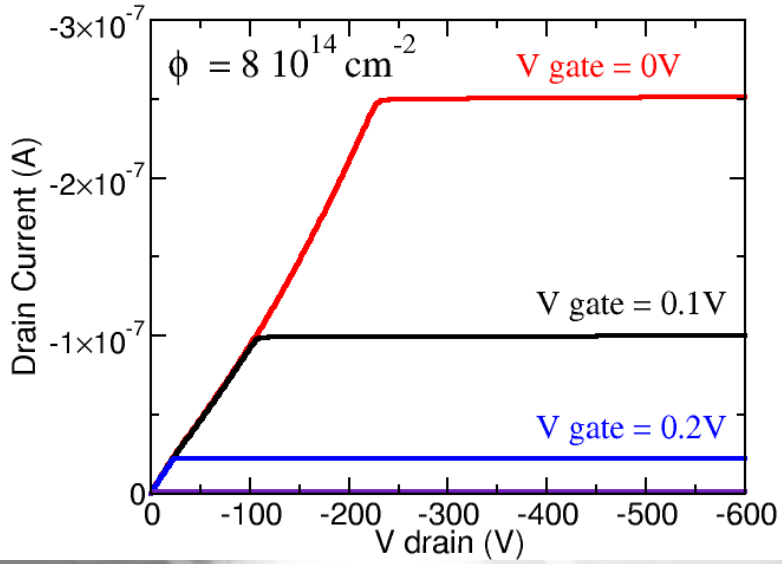
TCAD simulation of ideal irradiated HV-JFETs

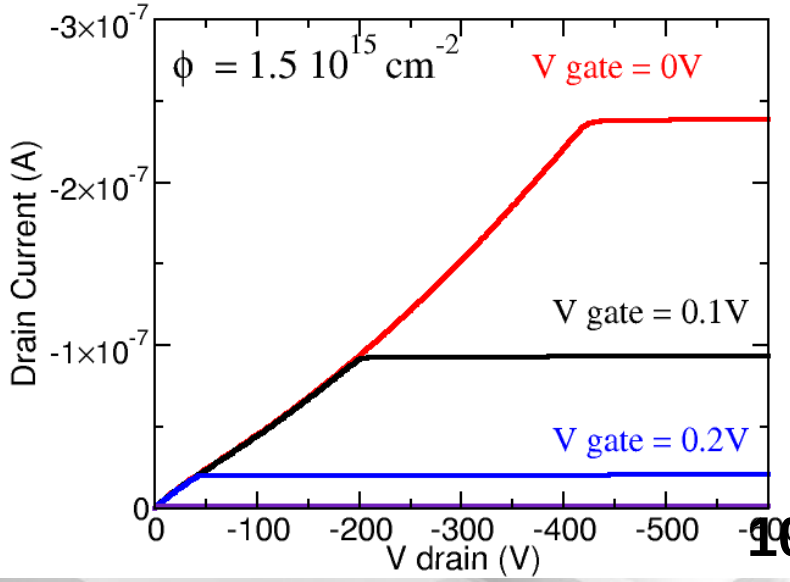




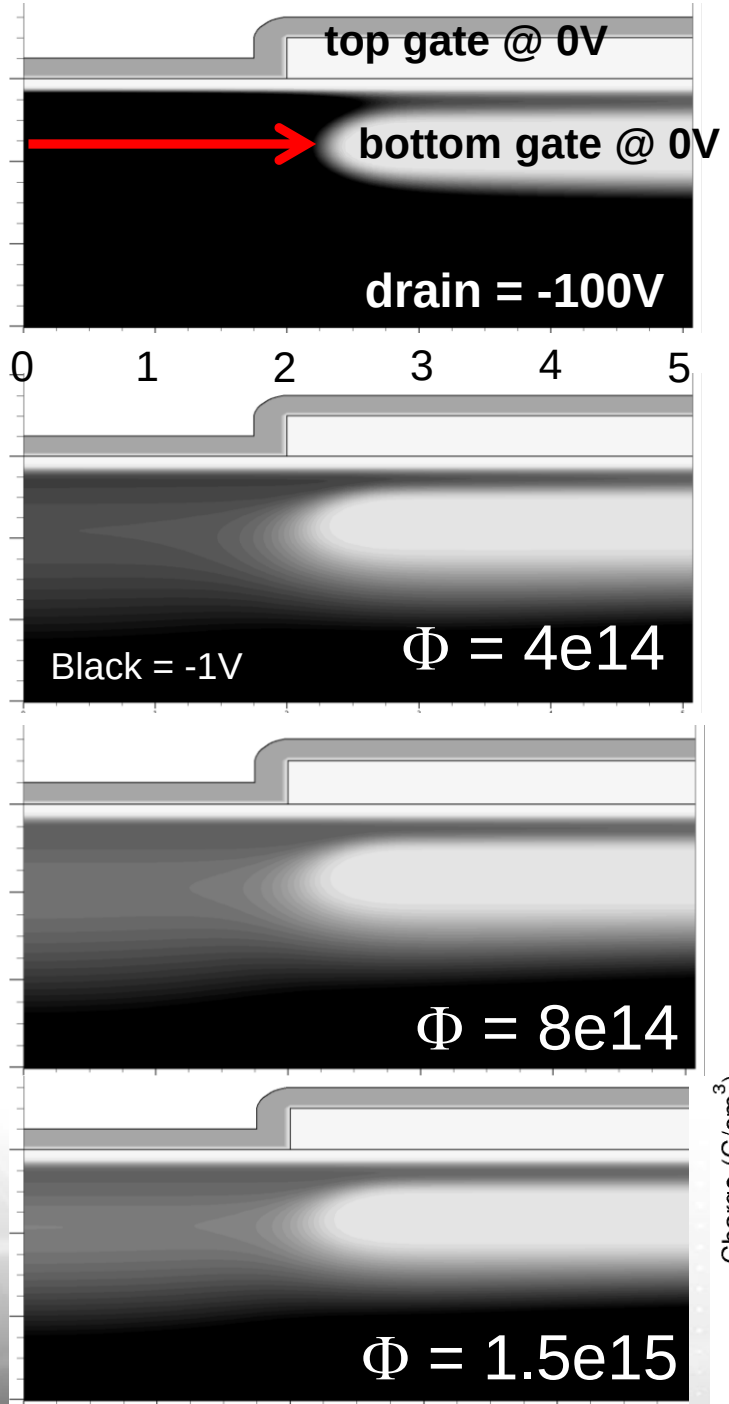
1- Perugia model does not simulate acceptor removal:
saturation currents are the same for every fluence

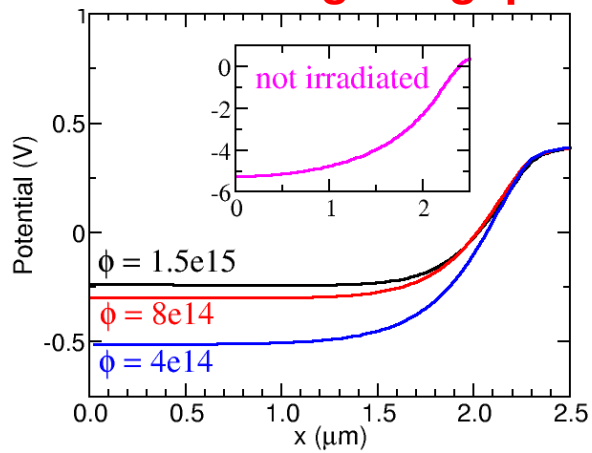
2- still dramatic change of V_{drain} vs fluence

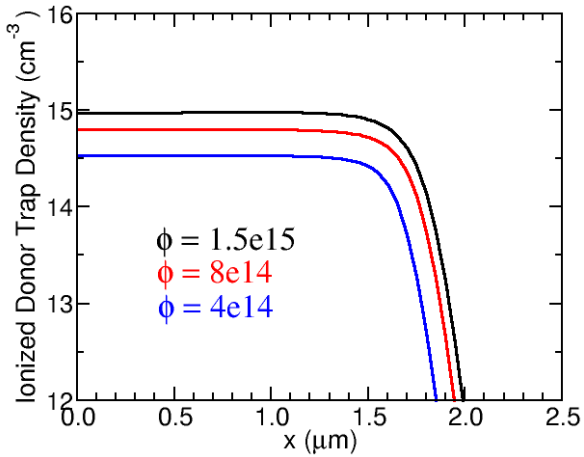


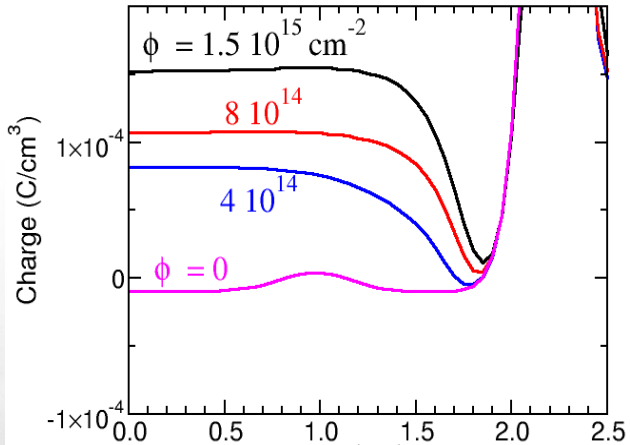


Cutlines along the gap







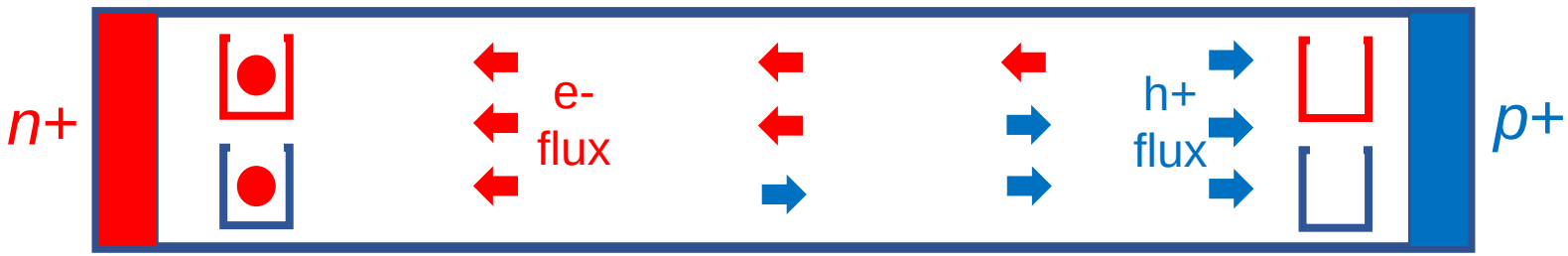


The height of the potential barrier that the holes need to cross before injection to the substrate (drain) increases with fluence.

- The potential barrier is lowered by V_{drain}, so larger V_{drain} must be applied at higher Φ.
- The potential barrier is due to the build-up of positive charge, from the ionized donor traps (no electrons to fill-up the traps!!!)

Other effects in irradiated Silicon that can be explained with trap charging – 1

Double peak of the electric field

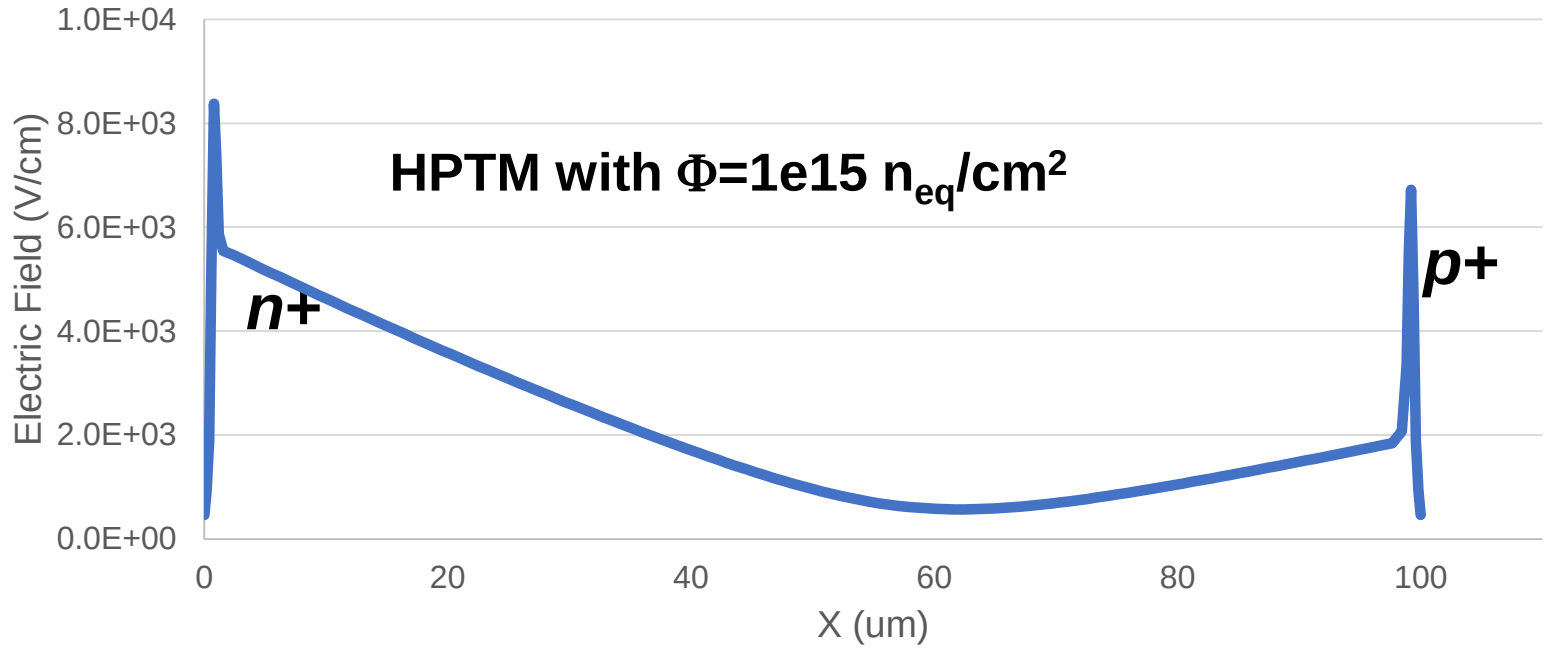


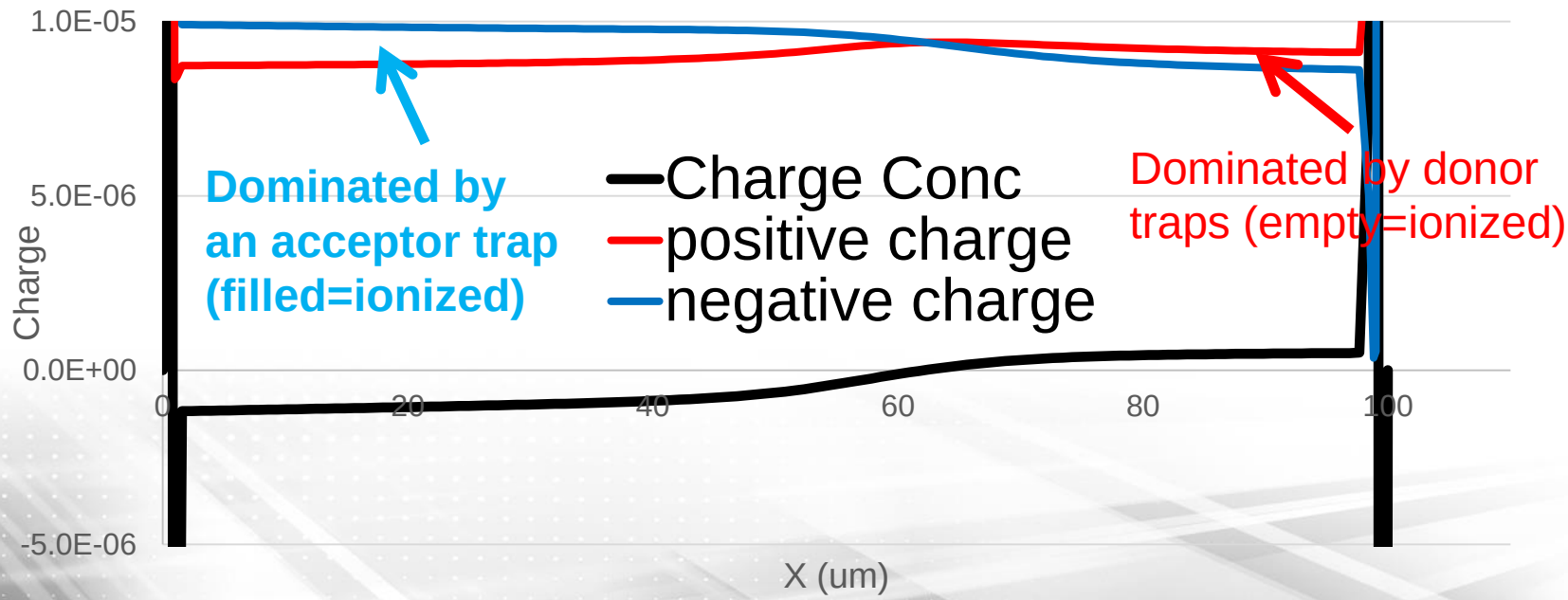
- Plenty of electrons towards the n+
- So “all” traps are filled with electrons:
  - donor traps are neutral,
  - acceptor traps are negative
- net negative charge close to the n+
  → regular junction n+/p-

- Plenty of holes towards the p+
- So “all” traps are empty
  - donor traps are positive
  - acceptor traps are neutral
- net positive charge close to the p+
  → regular junction p+/n-

- Can be simulated using the Hamburg Penta Trap model (HPTM)
- In the explored parameter range (substrate thickness, fluence, bias voltage), Perugia model doesn’t show the double peak.

Simulation of the double peak of the electric field



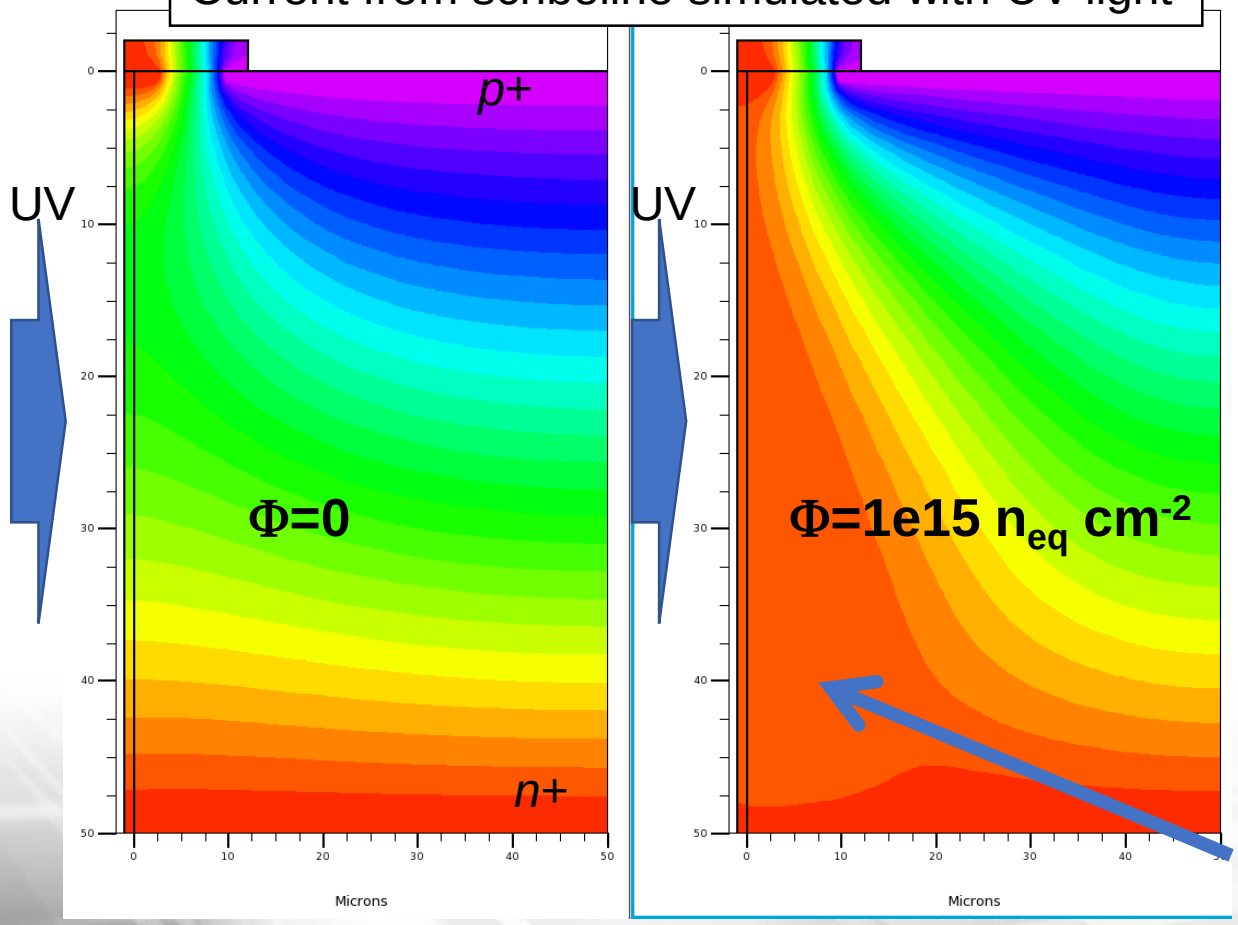


Other effects in irradiated Silicon that can be explained with trap charging – 2

Stability of scribeline

Known effect that, in pin diodes, after type inversion, the scribeline doesn't inject much current

Map of the electrostatic potential
Current from scribeline simulated with UV light



- From the damaged region, plenty of electrons and holes
- From the simulations: close to the scribeline,
  - 10% of any trap is ionized
  - 90% of Donor traps are filled (with electrons), and neutral
  - 90% of Acceptor traps are empty ($s_p = 10 s_n$), and neutral
- Low potential!

Conclusions

<u>A new silicon structure:</u>

vertical HV-JFET successfully fabricated at BNL

- Irradiated up to the fluence level of ITk ATLAS, and characterized
- Not really the best switch for the HV-Mux …

- Curves explained with TCAD simulations

  → high $V_{drain,\ saturation}$ due to positive charges, introduced by ionized donor traps

- Charged (ionized) traps explain other effects, for example:
  - stability of scribeline
  - double peak effect
  - ….

BACK-UP