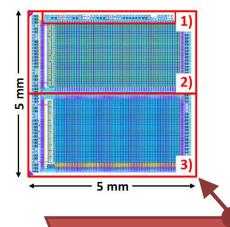


#### **RD50-MPW1**



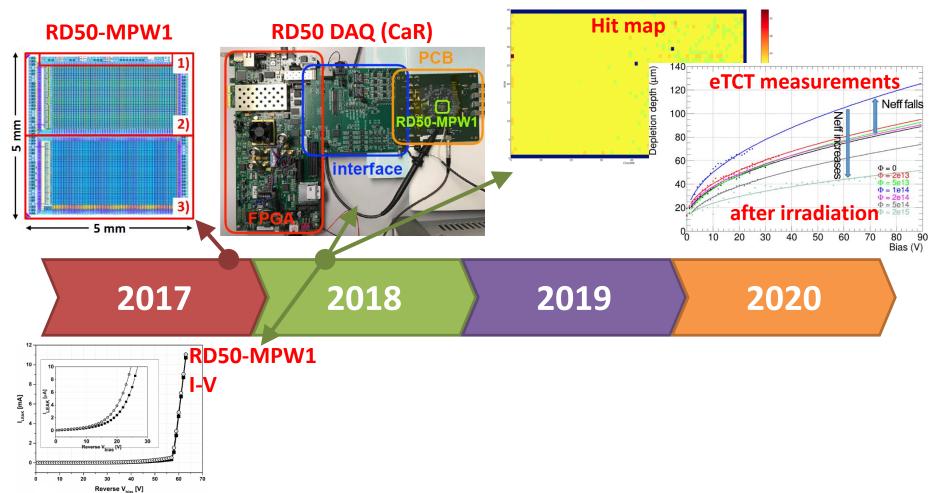
2017

2018

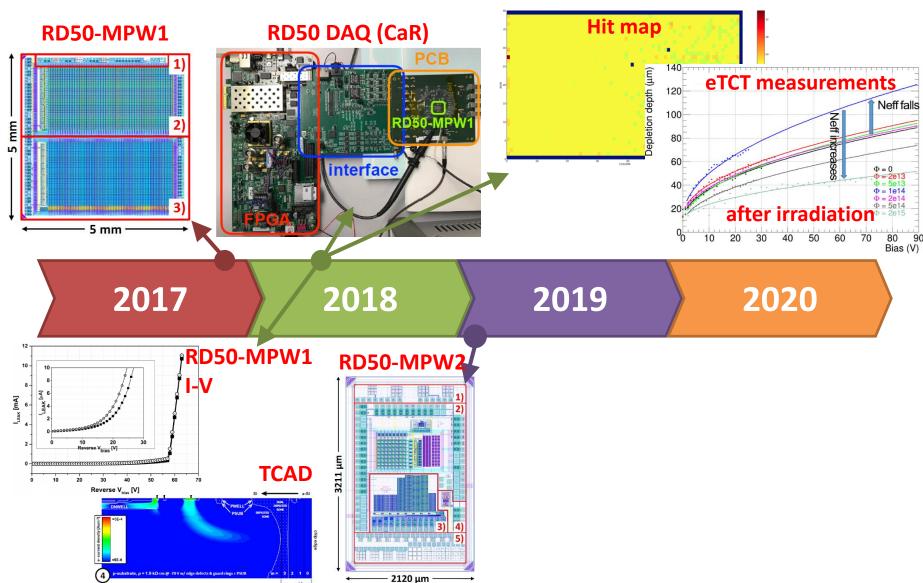
2019

2020



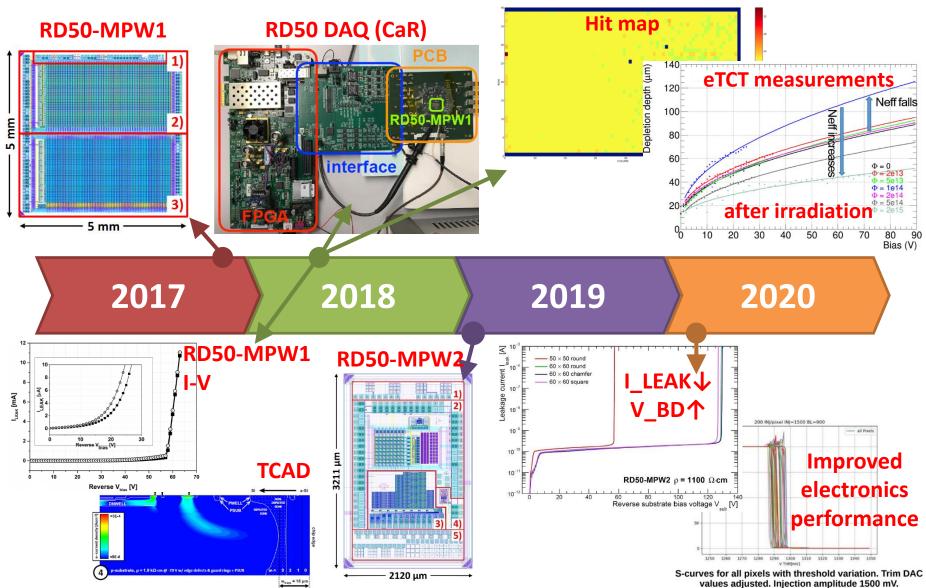




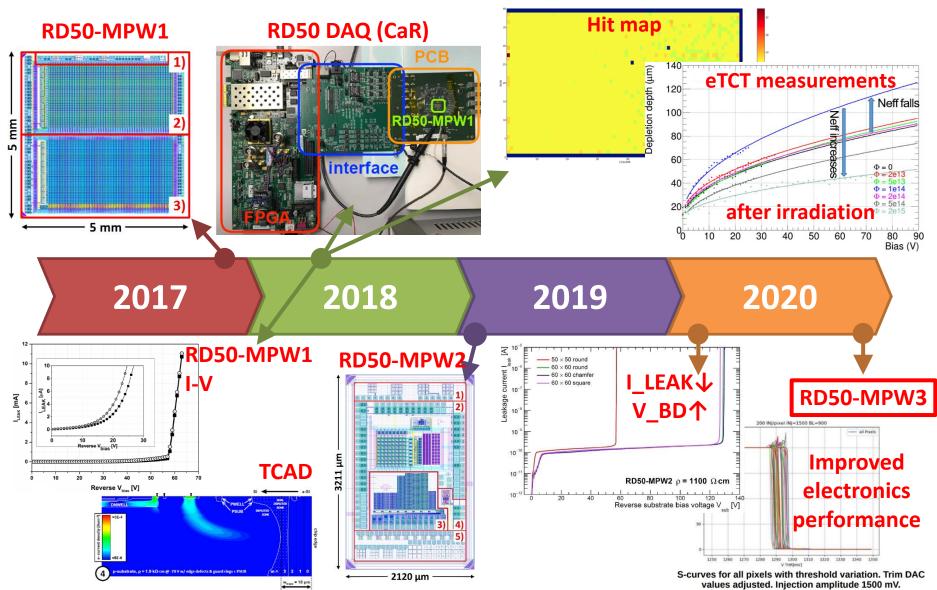


w<sub>traps</sub> = 18 μm











#### RD50 CMOS – Where are we?

- After a difficult start, we are now in the right direction
- RD50-MPW2 performs very nicely
  - Despite the lockdown situation, we have lots of interesting results already
  - Collaborators are very much enthusiastic and motivated
  - Many of the RD50-MPW2 results shown today have been taken at collaborators' home offices
  - We plan having many more results soon (full e-TCT evaluation, after irradiation...)



#### We have started design work towards our next chip submission (RD50-MPW3)

- 2 matrices of fully monolithic pixels
  - Improved FE-I3 matrix
  - Sampling matrix (results from MPWTiming expected soon)
- Small pixels with analogue and digital readout electronics
- Methods to optimise I LEAK and V BD developed for RD50-MPW2
- Improved peripheral readout electronics to optimise chip data output



#### **RD50 CMOS – Milestones**

#### RD50 prolongation request – May 2018

- M1: Characterization of the diodes and readout electronics of unirradiated and irradiated RD50-MPW1 samples (Q4/2018) → <u>Achieved</u>
  - M1.2 (new): Design and submission of RD50-MPW2 (Q1/2019) →
    Achieved
  - M1.3 (new): Characterization of unirradiated and irradiated RD50-MPW2 samples (Q1+Q2/2020) → Ongoing
  - M1.4 (new): Design and submission of RD50-MPW3 (Q2/2020, Q1/2021)
    → Ongoing
- M2: Design and submission for fabrication of RD50-ENGRUN1 (Q4/2018)
- M3: Characterization of unirradiated and irradiated RD50-ENGRUN1 samples (Q3/2019, Q3/2020)
- M4: Characterization of irradiated backside biased RD50-ENGRUN1 samples for operation beyond  $10^{16}$  n<sub>eq</sub>/cm (Q4/2020)
- M5: Studies of stitching process options (Q4/2021)
- M6: Characterization of unirradiated and irradiated stitched samples (Q4/2022)

