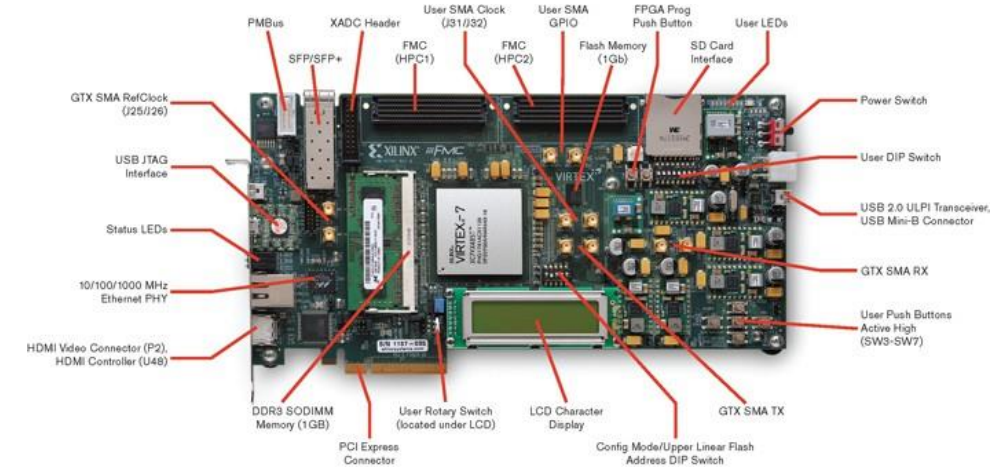


EMCI non-exhaustive testbench proposal

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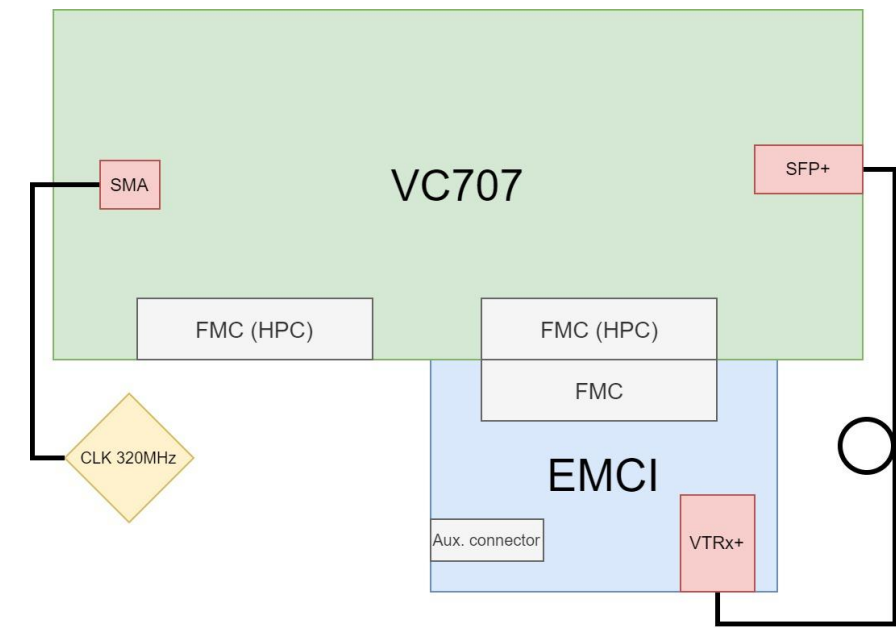
VC707: Virtex 7 Evaluation Board

- FMC HPC connector
 - Banks configurable @1.2V (VADJ)
- SFP+ connector
- SMA clock input
- Used in VLDB+ testbench



Testbench implementation

- Plugging EMCI FMC male connector directly into FMC connector of a VC707
 - VC707 may be configured to work @1.2V
 - 12V power coming from VC707 (FMC)
- High speed link is tested using VTRx+/SPF+
 - External 320MHz clock needed (SMA connectors)
 - eLinks need the CDR from the downlink stream to work
- Auxiliary connector tested by means of Raspberry Pi separately (provided with VLDB+)

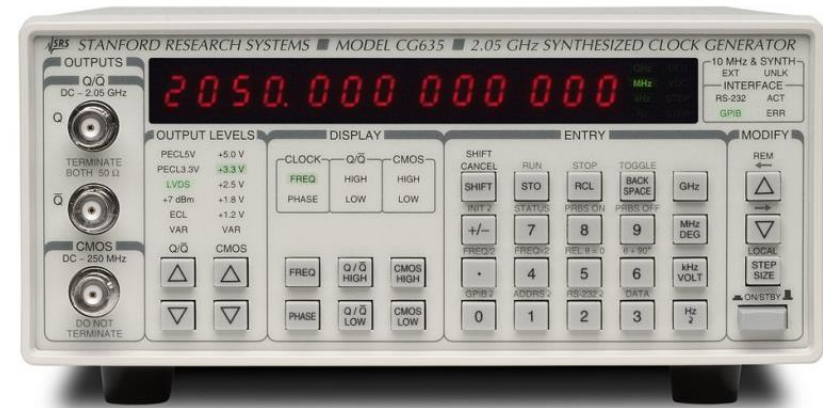


Tested features

- eLinks testing
 - Downlink: from 80 to 320 Mbps
 - Uplink: from 160 to 1280 Mbps
- With normal IO pin (using SERDES)
 - VLDB+ has been tested up to 640 MHz
- VC707 FMC transceivers cannot be used
 - Need external clock coming from FMC
- High speed testing
 - SPF+ transceiver
 - External clock generator needed [Proposal: CG635 (available in e-pool)]
- I2C master/slave, GPIO, PSClock, *ADC/DAC

Input eLinks (up-link)												
Up-link bandwidth [Gb/s]	5.12						10.24					
FEC coding	FEC5			FEC12			FEC5			FEC12		
Bandwidth [Mb/s]	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6

Output eLinks (down-link)			
Bandwidth [Mb/s]	80	160	320
Maximum number	16	8	4



Problems

- Not all eLinks/features can be tested (even with optimal routing)
 - Max 58 pairs for testing (including eLinks TX/RX/CLK, GPIO, I2C...)
- ADC and DAC (1V range) cannot be properly tested
 - IpGBT ADC max input 1V, but 1.2V should be OK
 - IpGBT DAC can deliver 1V to VC707 (1.2 V high level)
- For better testing, a different testbench with an FMC breakout board would be needed to plug to a function generator/oscilloscope
 - Cannot be tested at the same time as the rest of the features
- Final pinout depends on routing

	K	J	H	G	F	E	D	C	B	A
Standard	EMC1	EMC1	EMC1	EMC1	EMC1	EMC1	EMC1	EMC1	EMC1	EMC1
	Standard	EMC1	Standard	EMC1	Standard	EMC1	Standard	EMC1	Standard	EMC1
1	C	H25Y Par	GND	GND	YREF_A_MDC	H25V25Y Par	GND	GND	PSL_MDC	GND
2	GND	GND	P	GND	GND	GND	GND	GND	GND	GND
3	GND	GND	N	GND	GND	GND	GND	GND	GND	GND
4	P	GND	GND	GLR0_MDC_P	GND	GND	GND	GND	GND	GND
5	N	GND	GND	GLR0_MDC_N	GND	GND	GND	GND	GND	GND
6	GND	GND	ELNK_OUT_P3	GND	GND	LASS_P CC	ELNK_IN_P4	GND	GND	GND
7	HAR0_P	ADCC	HAR0_N	ELNK_OUT_M0	HAR0_P	GLR0_N CC	ELNK_IN_M4	HAR0_P	ELNK_IN_P10	HAR0_N
8	HAR0_N	ADCC	GND	LAG0_N	GND	GND	HAR0_N	ELNK_IN_N10	GND	GND
9	GND	GND	HAR0_P	ELNK_OUT_P3	GND	GND	LASS_P	ELNK_IN_P10	GND	GND
10	HAR0_P	ELNK_CLK_P	HAR0_N	ELNK_OUT_M0	HAR0_P	GLR0_N	HAR0_N	ELNK_IN_N10	GND	GND
11	HAR0_N	ELNK_CLK_N	HAR0_P	ELNK_OUT_M0	HAR0_P	GLR0_N	HAR0_N	ELNK_IN_N10	GND	GND
12	HAR0_P	HAR0_P	HAR0_P	ELNK_OUT_P3	GND	GND	LASS_P	ELNK_IN_P10	LASS_P	ELNK_OUT_M0
13	HAR0_N	HAR0_P	HAR0_P	ELNK_OUT_P3	GND	GND	LASS_P	ELNK_IN_P10	LASS_P	ELNK_OUT_M0
14	HAR0_N	PSCLK_M0	HAR0_P	ELNK_OUT_P3	GND	GND	LASS_P	ELNK_IN_P10	LASS_P	ELNK_OUT_M0
15	HAR0_P	PSCLK_N0	HAR0_P	ELNK_OUT_P3	GND	GND	LASS_P	ELNK_IN_P10	LASS_P	ELNK_OUT_M0
16	HAR0_P	PSCLK_P1	HAR0_N	ELNK_OUT_P1	LAR0_P	GLR0_P	LAR0_N	ELNK_IN_P1	HAR0_P	ELNK_IN_P10
17	HAR0_P	PSCLK_N1	HAR0_N	ELNK_OUT_P1	LAR0_P	GLR0_P	LAR0_N	ELNK_IN_P1	HAR0_P	ELNK_IN_P10
18	GND	GND	HAR0_P	ELNK_IN_P8	GND	GND	LAR0_P	ELNK_IN_P1	HAR0_P	ELNK_IN_P10
19	HAR0_P	PSCLK_P2	HAR0_N	ELNK_IN_N8	LAR0_P	GLR0_P	LAR0_N	ELNK_IN_P1	HAR0_P	ELNK_IN_P10
20	HAR0_N	PSCLK_N2	HAR0_N	ELNK_IN_N8	LAR0_P	GLR0_P	LAR0_N	ELNK_IN_P1	HAR0_P	ELNK_IN_P10
21	GND	GND	HAR0_P	ELNK_IN_P8	GND	GND	LAR0_P	ELNK_IN_P1	HAR0_P	ELNK_IN_P10
22	HAR0_P	PSCLK_P3	HAR0_N	ELNK_IN_N8	LAR0_P	GLR0_P	LAR0_N	ELNK_IN_P1	HAR0_P	ELNK_IN_P10
23	HAR0_N	PSCLK_N3	HAR0_N	ELNK_IN_N8	LAR0_P	GLR0_P	LAR0_N	ELNK_IN_P1	HAR0_P	ELNK_IN_P10
24	GND	GND	HAR0_P	ELNK_IN_P8	GND	GND	LAR0_P	ELNK_IN_P1	HAR0_P	ELNK_IN_P10
25	HAR0_P	CC GPIO0	HAR0_N	ELNK_IN_N8	LAR0_P	GLR0_P	LAR0_N	ELNK_IN_P1	HAR0_P	ELNK_IN_P10
26	HAR0_N	CC GPIO0	HAR0_N	ELNK_IN_N8	LAR0_P	GLR0_P	LAR0_N	ELNK_IN_P1	HAR0_P	ELNK_IN_P10
27	GND	GND	HAR0_P	ELNK_IN_P8	GND	GND	LAR0_P	ELNK_IN_P1	HAR0_P	ELNK_IN_P10
28	HAR0_P	CC GPIO0	HAR0_N	ELNK_IN_N8	LAR0_P	GLR0_P	LAR0_N	ELNK_IN_P1	HAR0_P	ELNK_IN_P10
29	HAR0_N	CC GPIO0	HAR0_N	ELNK_IN_N8	LAR0_P	GLR0_P	LAR0_N	ELNK_IN_P1	HAR0_P	ELNK_IN_P10
30	GND	GND	HAR0_P	ELNK_IN_P8	GND	GND	LAR0_P	ELNK_IN_P1	HAR0_P	ELNK_IN_P10
31	HAR0_P	CC GPIO0	HAR0_N	ELNK_IN_N8	LAR0_P	GLR0_P	LAR0_N	ELNK_IN_P1	HAR0_P	ELNK_IN_P10
32	HAR0_N	CC GPIO0	HAR0_N	ELNK_IN_N8	LAR0_P	GLR0_P	LAR0_N	ELNK_IN_P1	HAR0_P	ELNK_IN_P10
33	GND	GND	HAR0_P	ELNK_IN_P8	GND	GND	LAR0_P	ELNK_IN_P1	HAR0_P	ELNK_IN_P10
34	HAR0_P	ELNK_IN_P2	HAR0_N	ELNK_IN_N2	LAR0_P	GLR0_P	LAR0_N	ELNK_IN_P1	HAR0_P	ELNK_IN_P10
35	HAR0_N	ELNK_IN_P2	HAR0_N	ELNK_IN_N2	LAR0_P	GLR0_P	LAR0_N	ELNK_IN_P1	HAR0_P	ELNK_IN_P10
36	GND	GND	HAR0_P	ELNK_IN_P2	LASS_P	GLR0_P	LASS_P	ELNK_IN_P1	HAR0_P	ELNK_IN_P10
37	HAR0_P	CC PRTOUT0	HAR0_N	ELNK_IN_N2	LAR0_P	GLR0_P	LAR0_N	ELNK_IN_P1	HAR0_P	ELNK_IN_P10
38	HAR0_N	CC PRTOUT0	HAR0_N	ELNK_IN_N2	LAR0_P	GLR0_P	LAR0_N	ELNK_IN_P1	HAR0_P	ELNK_IN_P10
39	GND	GND	VIO_B_MDC	GND	GND	GND	VADU	GND	GND	GND
40	VIO_B_MDC	GND	GND	VADU	GND	GND	VADU	GND	GND	GND