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PicoTDCv2:
Pico-second TDC for HEP

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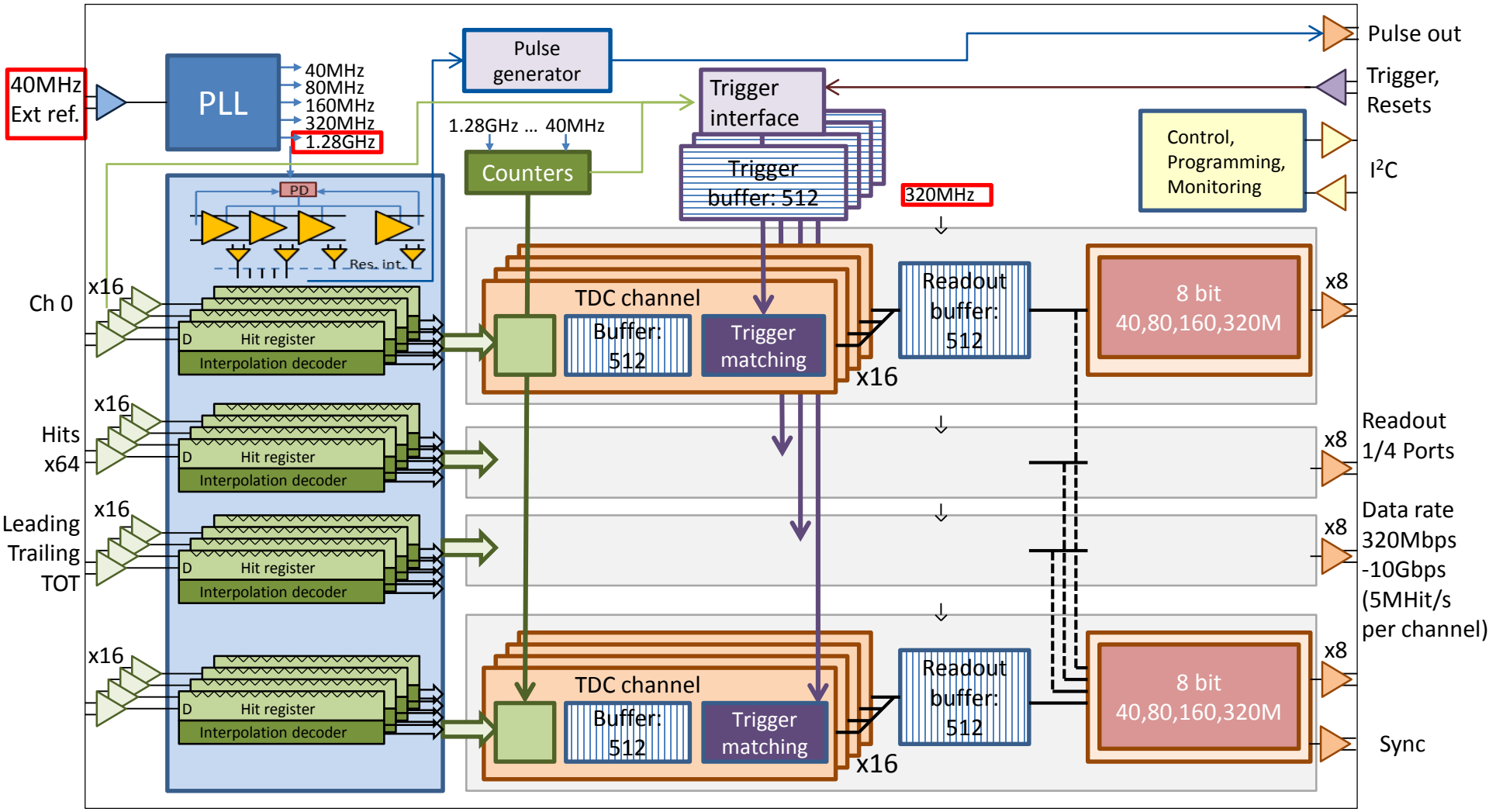
CERN/EP-ESE

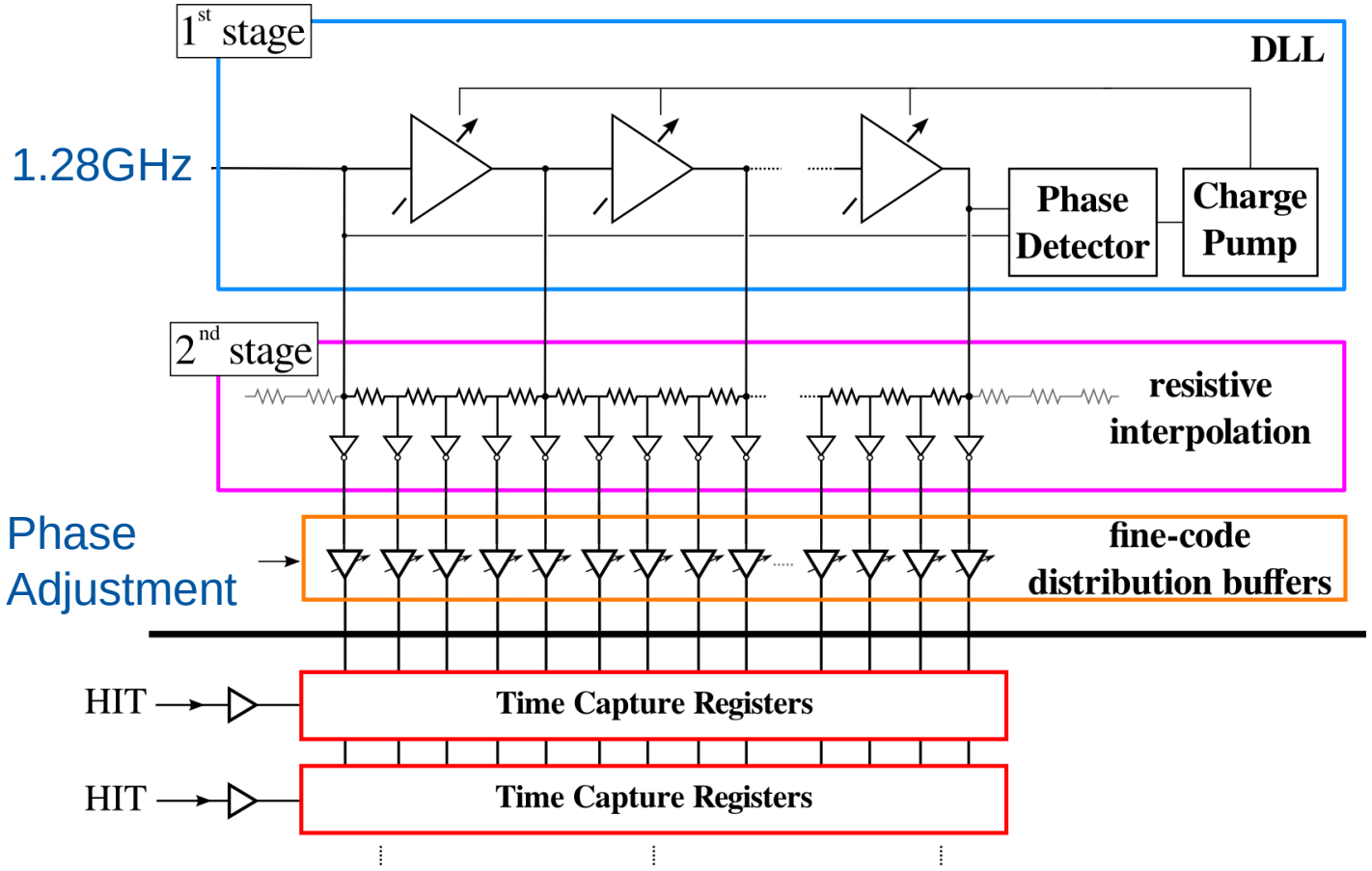
PicoTDC architecture

PicoTDC Architecture



64 channels, 3ps or 12ps time binning, 200us dynamic range

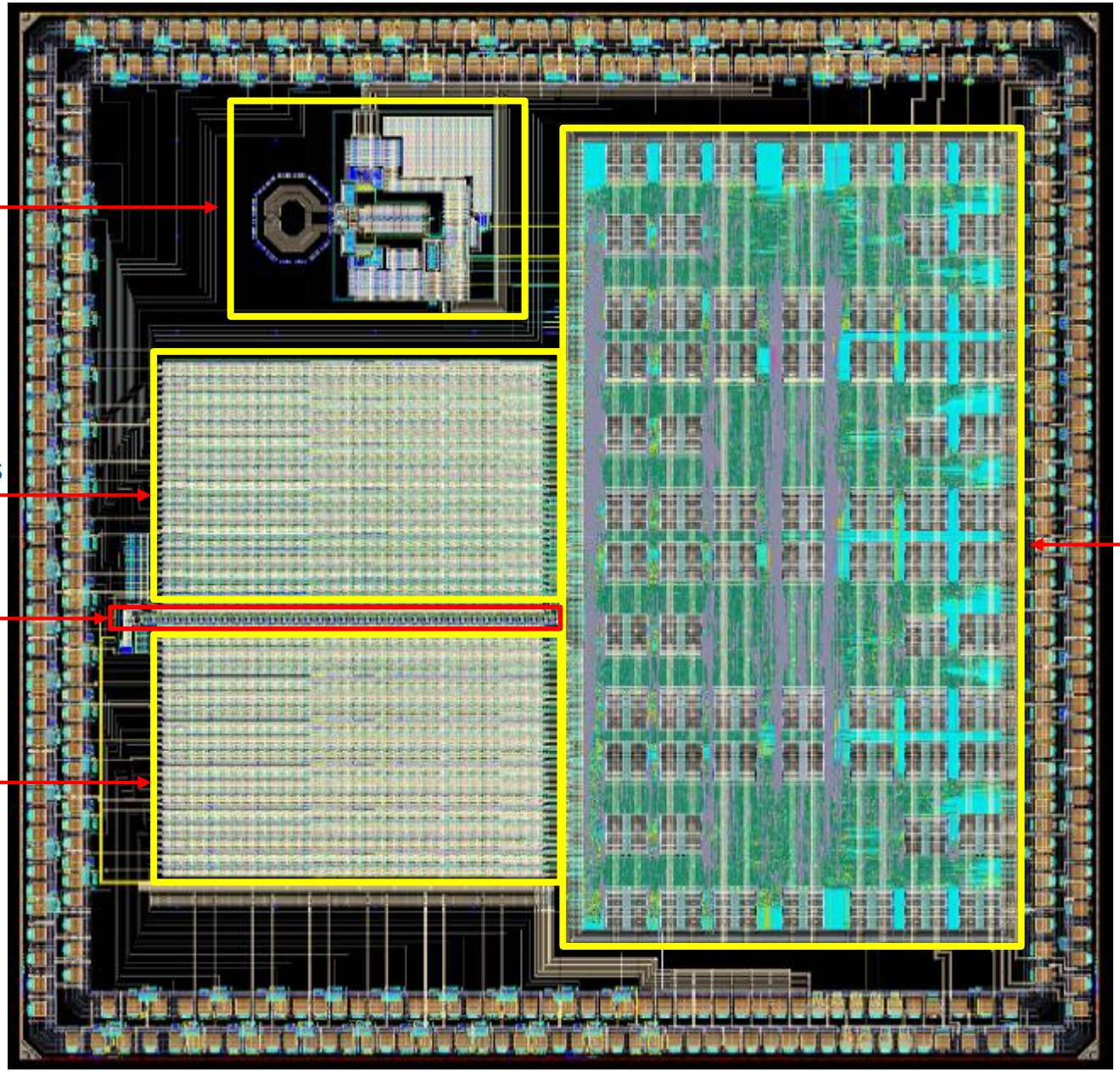
Two Stage Time Interpolation



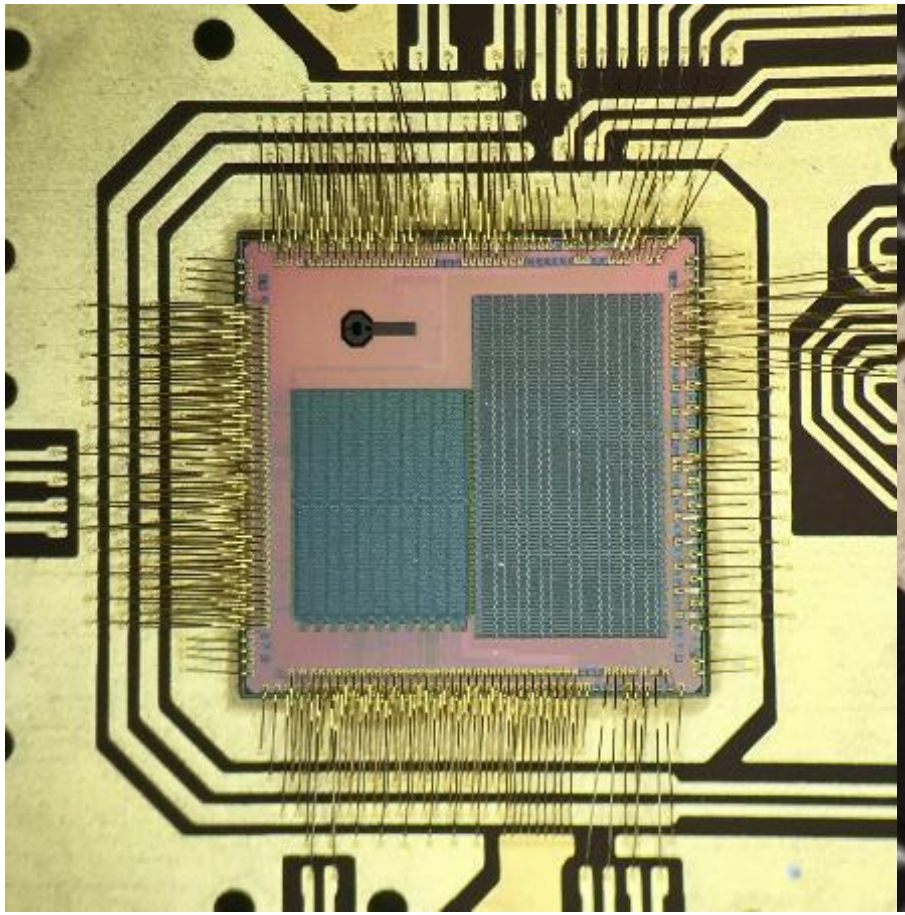
12.2ps delay
(Coarse time)

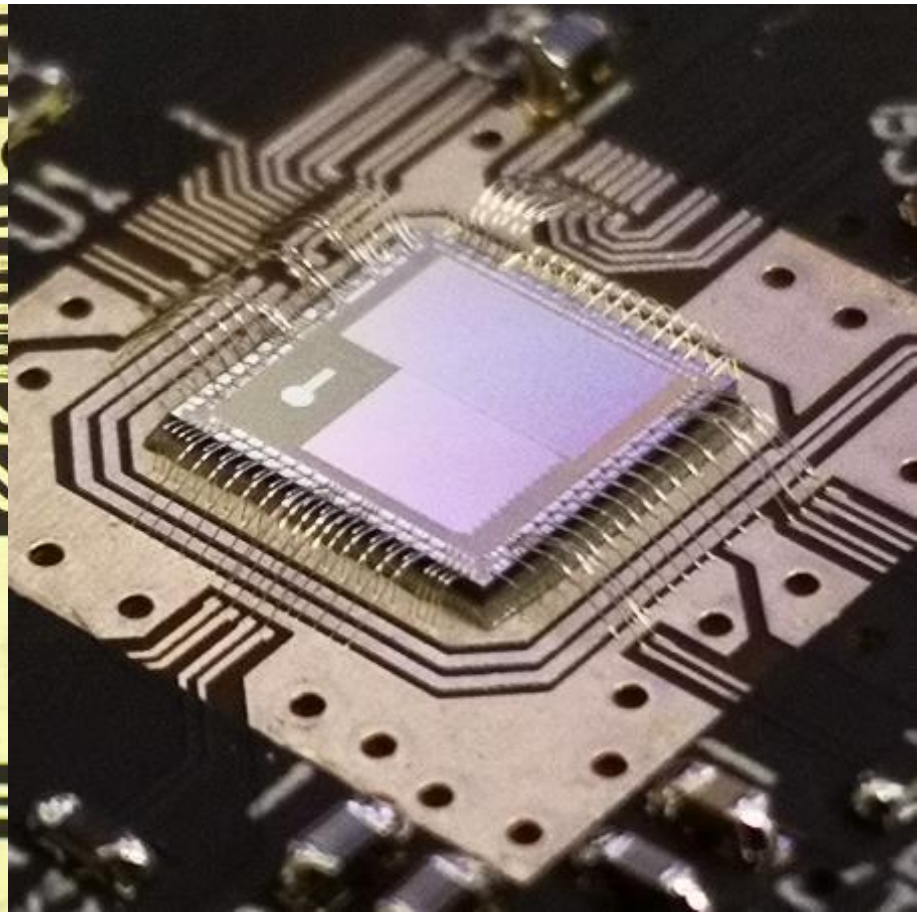
3.05ps delay
(Fine time)

32 steps each with
0.6ps resolution

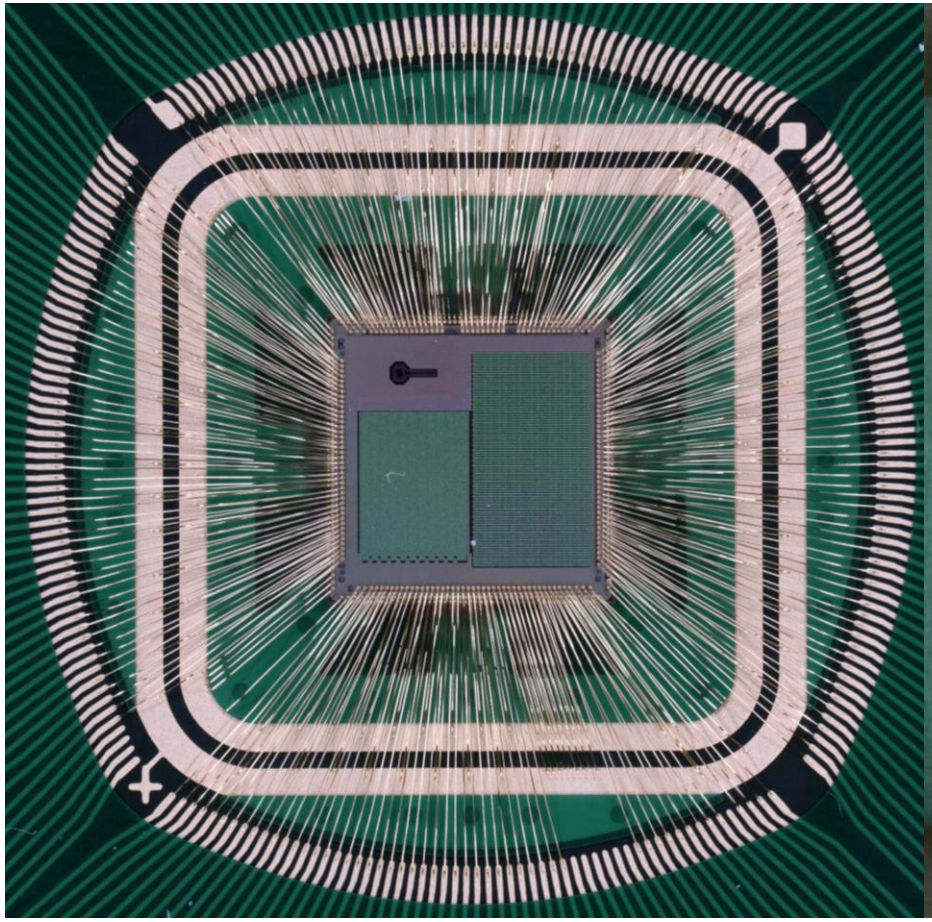

PLL
Top hit receivers
DLL
Bottom hit receivers
Logic

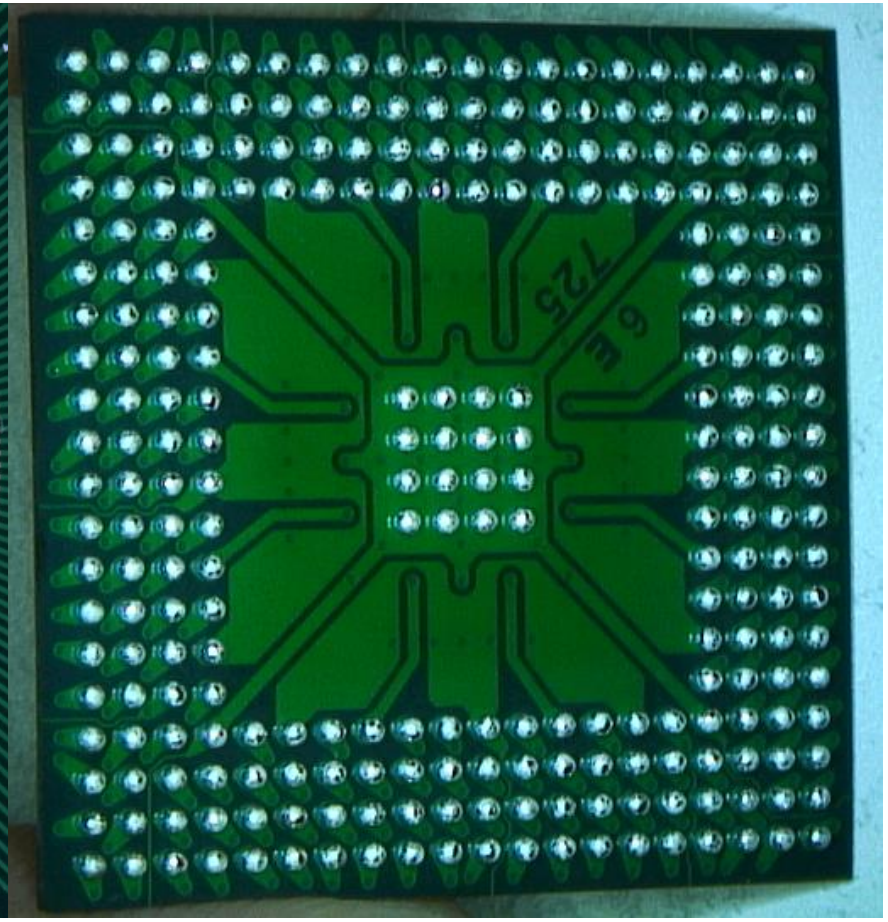
PicoTDC on Test Card first version





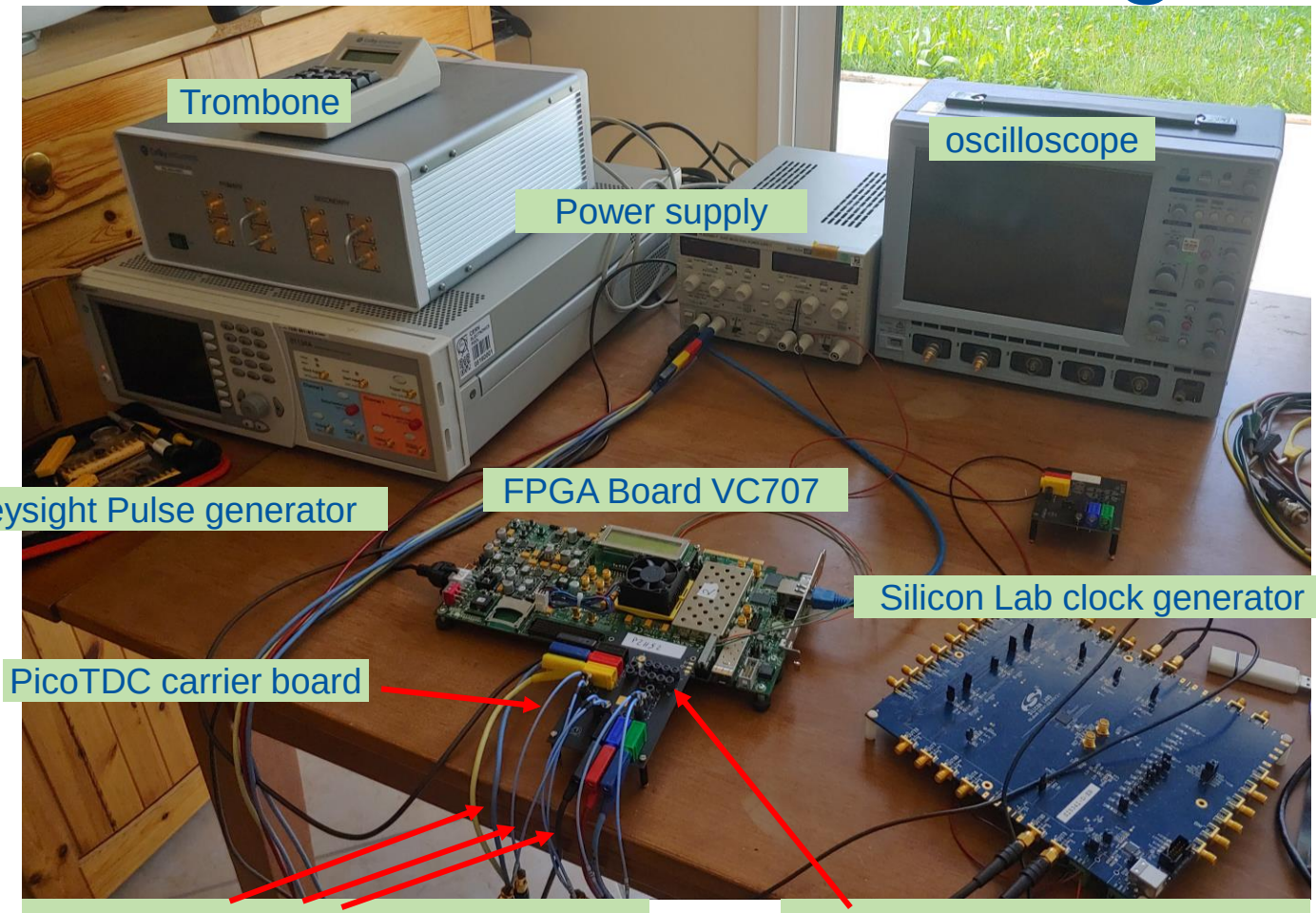
PicoTDC on Generic Package



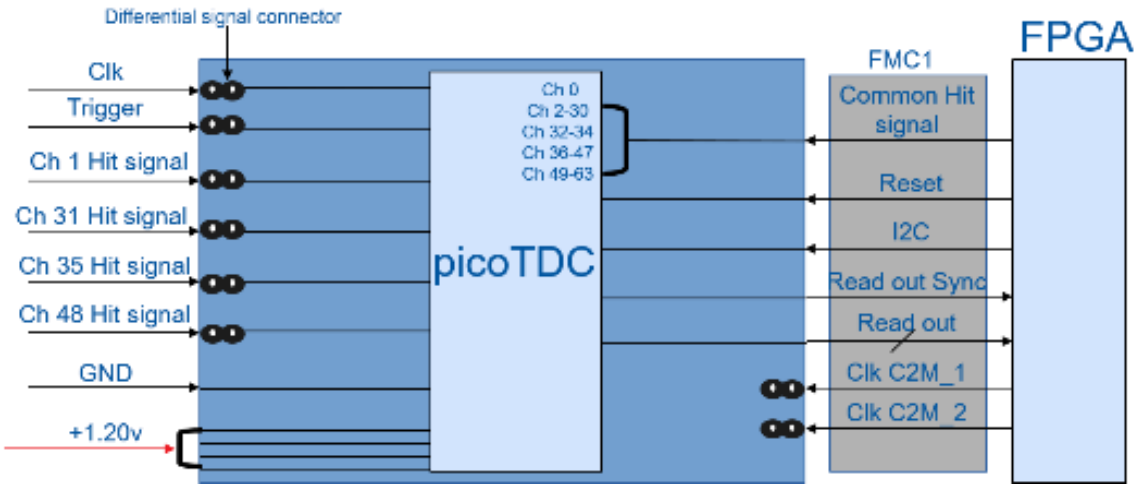


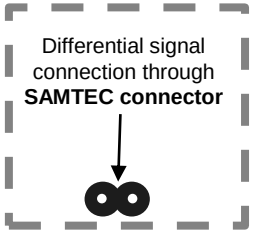
PicoTDC testing system

Instrumentation for testing

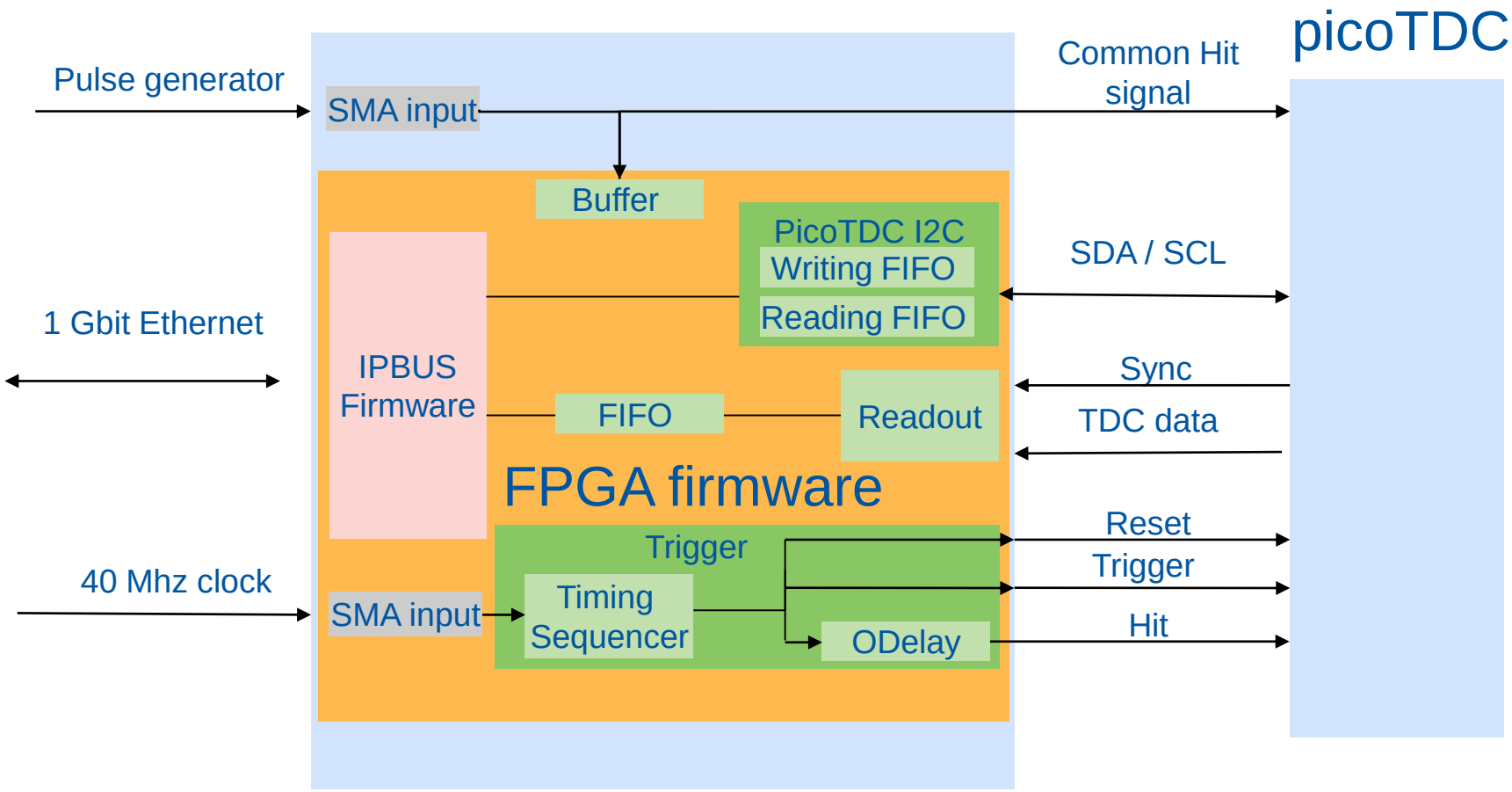


PCB mezzanine test board

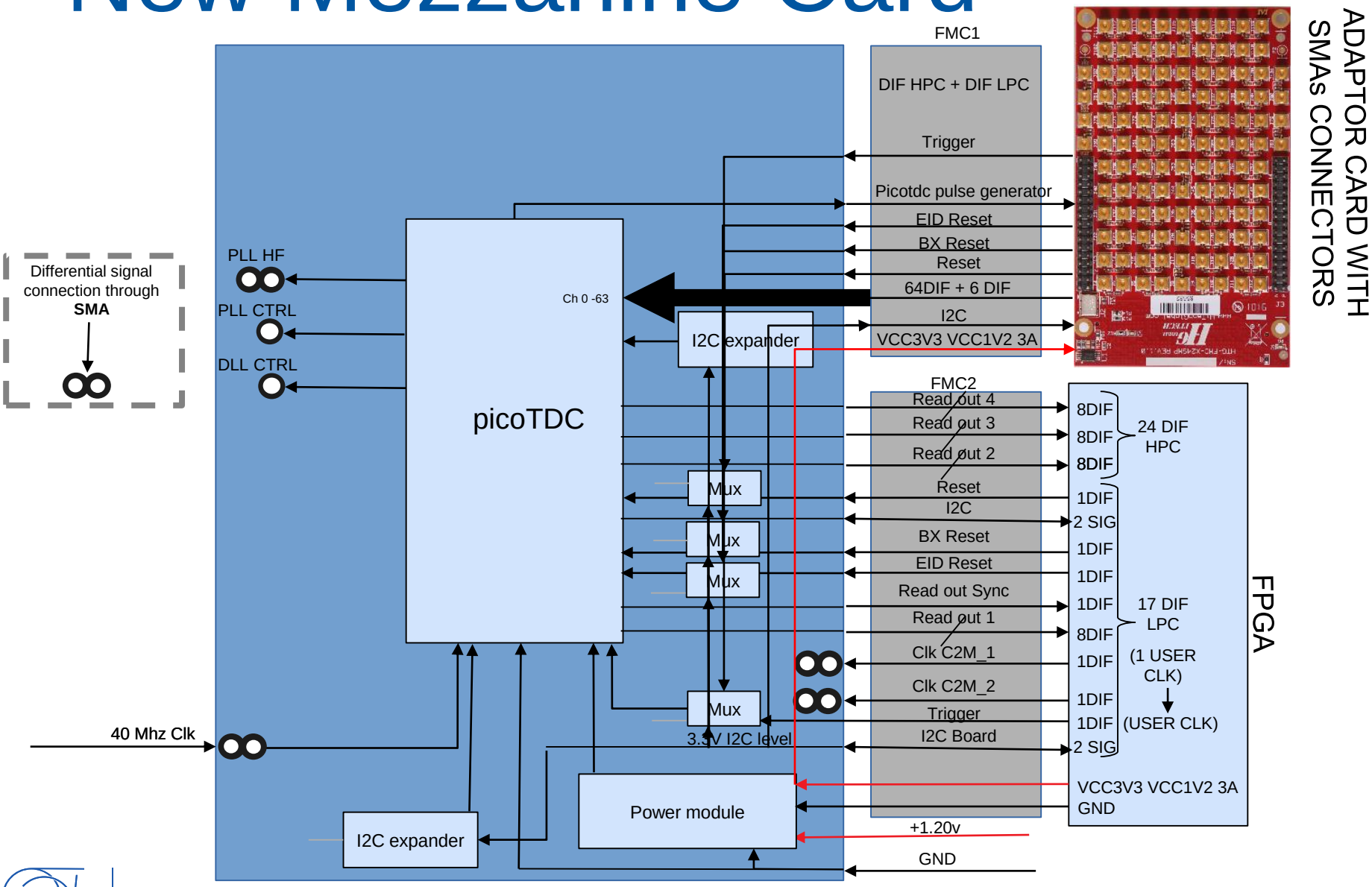




FPGA Board (VC707 Xilinx commercial board)



New Mezzanine Card



New Mezzanine Card

- All SMA connectors (NO Samtec CCH-J-02 , or Samtec CCH-J-04)
- Power lines available on FMC1 directly from FMC2
- Future version with final package will include some connections between FMC1 and FMC2, a bridge between the FPGA and the Adaptor card. Currently users can have some generic output pin availability from XADC Header or FMC2 from the VC707 evaluation board.
- Availability:
  - With chip in generic package: ~June
  - With chip in final package: ~ autumn (depending on when final package available)

Share point link for the new mezzanine card and adaptor card PCB and schematic:
http://cern.ch/PicoTDC

PicoTDC test routines

PicoTDC: Delay sweep test

- Sweep test is performed to measure effective single shot RMS resolution covering linearities and jitter
- The silicon lab board (Si5341-D-EVB with sub-100 fs rms phase jitter) is used to perform sweep test providing the clock signal and the hit signal which is then delayed by the trombone, or by the board itself.
- The limitation of the silicon lab board is the fact that it is able only to generate clock, which are then shifted in phase of 0.3ps to obtain a hit signal delayed in time.
- The trombone is a very precise and repeatable programmable delay line, but with maximum 600ps delay.
- The Keysight generator can overcome the limitations of the trombone and the silicon lab board. The Keysight generator is more flexible in generating delay and pulses, but with higher internal non-linearity and jitter.

PicoTDC: Delay sweep test

- The pulse is generated in sync with the clock and is going to the hit input of the picoTDC. There is a delay between the 2 signals, which goes with steps of 0.3 ps.

- PicoTDC main DLL clock cycle is 1.28 Ghz, 780ps, the course time counter clock cycle is 40 Mhz, 25ns, so usually delay sweep measurements are provided in this 2 forms to check any non-linearity in both elements.

- 500 hits per delay step are acquired, calculating from them: Standard deviation (std in red), minimum (min in green), maximum (max in green)

- INL or RMS_resolution or also called single shot RMS resolution, comprise:
  - Jitter
  - Quantization
  - INL (standard INL calculated in code density test, not including jitter and quantization).

- This value is calculated as RMS value through all the measurements taken without any averaging.

PicoTDC: Code density test

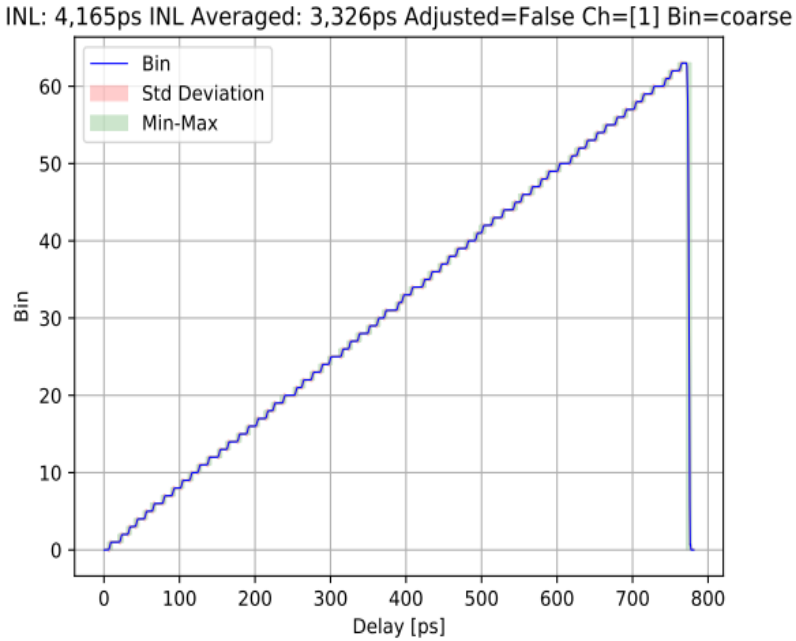
- Code density test is performed to measure the effective bin size. The code density test is in principle made with uncorrelated random hit generator (or systematic sweep with silicon labs card)
- The system can provide the same amount of expected pulses in each bin.
- The resulting histogram is the result of the measured amount of hits collected per each bin. This test could be done with bin size of 3 ps (fine time), 12 ps (coarse time).
- The measurements don’t include jitter and quantization, INL and DNL don’t include jitter and quantization too.

PicoTDC delay sweep test

PicoTDC: Delay sweep test

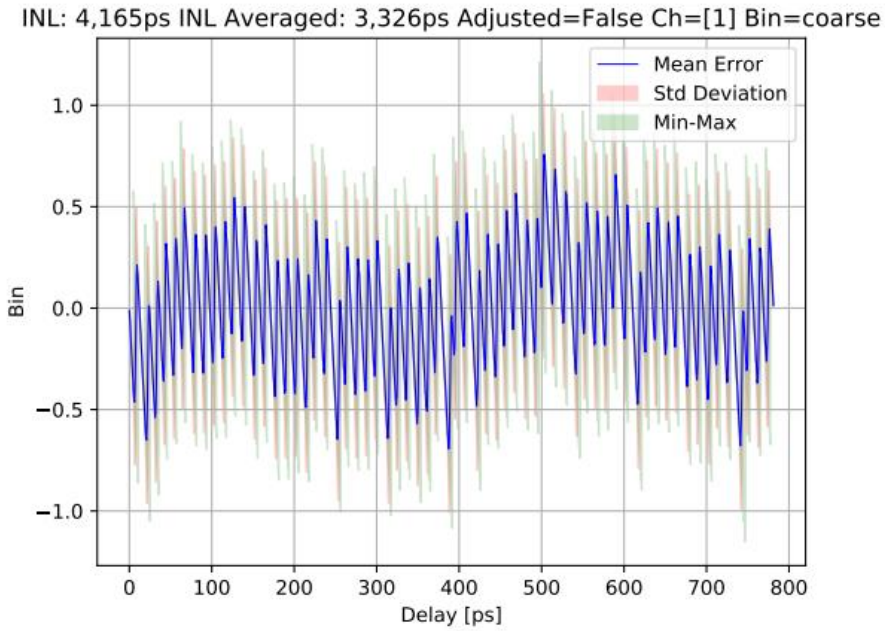
Ch 1, not adjusted, **coarse mode**, bin 12ps, RMS_resolution = 4,165ps

*RMS_resolution includes jitter, quantization and INL



https://cernbox.cern.ch/index.php/s/4Jc4wv68w8V4Ofi

* Link for interactive web plot



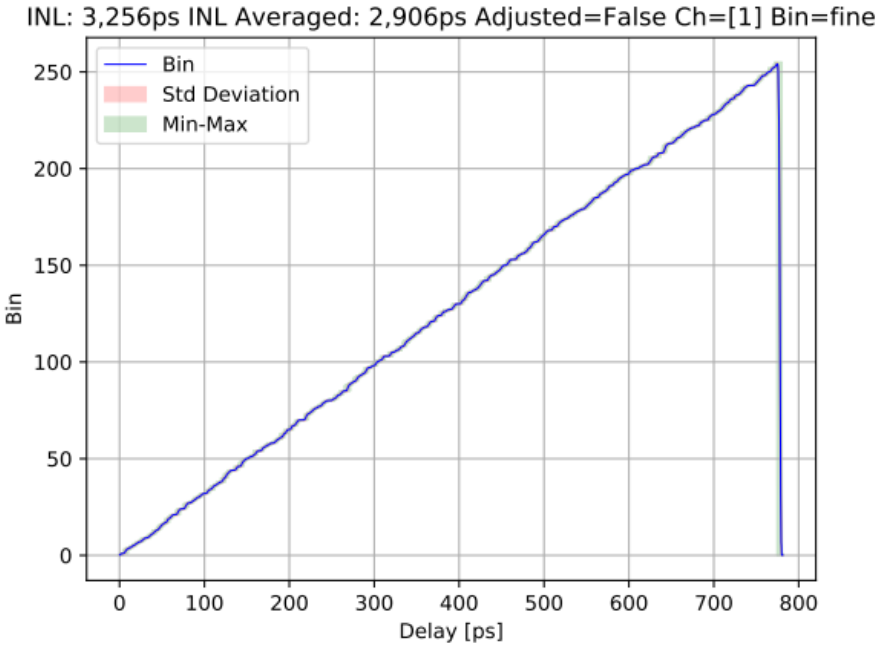
https://cernbox.cern.ch/index.php/s/GvY7rTUIu6CgGBx

* Link for interactive web plot

PicoTDC: Delay sweep test

Ch 1, not adjusted, **fine mode**, bin 3ps, RMS_resolution = 3,256ps

*RMS_resolution includes jitter, quantization and INL



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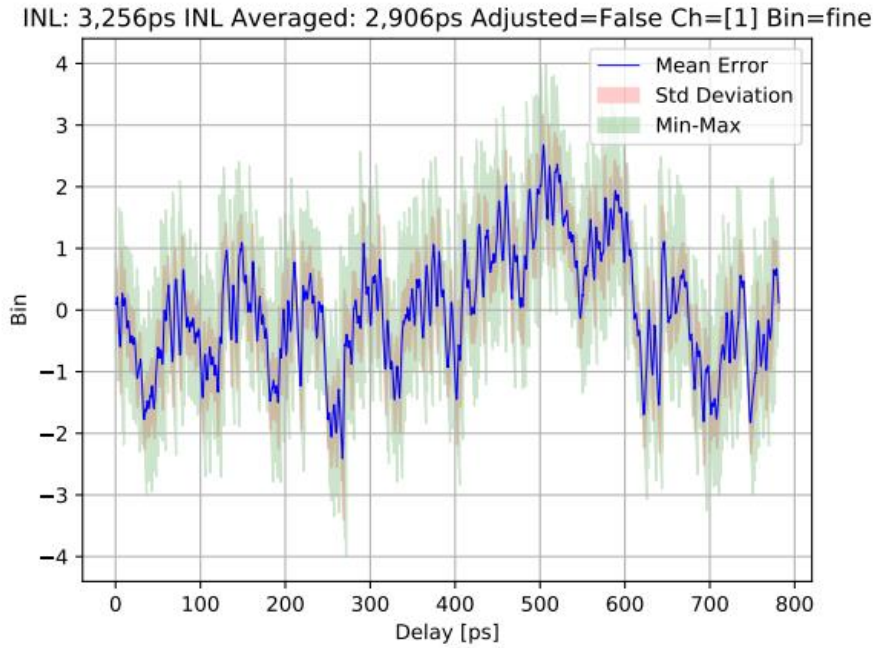
* Link for interactive web plot



https://cernbox.cern.ch/index.php/s/fpqJKaSbkbPG0vX

* Link for interactive web plot

PicoTDC: performances summary

			Sweep Test (PicoTDCV2)	Sweep Test (PicoTDCV1)
	Ch	adjusted	RMS_resolution	RMS_resolution
Coarse time	1	NO	4,165ps	X
	31	NO	4,066ps	4,129ps
	35	NO	4,085ps	X
	48	NO	4,015ps	X
Fine time	1	NO	3,256ps	X
	31	NO	2,904ps	3,416ps
	35	NO	2,822ps	X
	48	NO	2,707ps	X

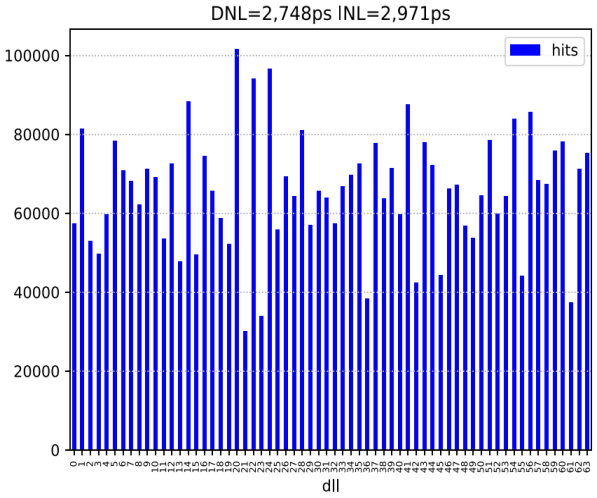
*RMS_resolution includes jitter, quantization and INL

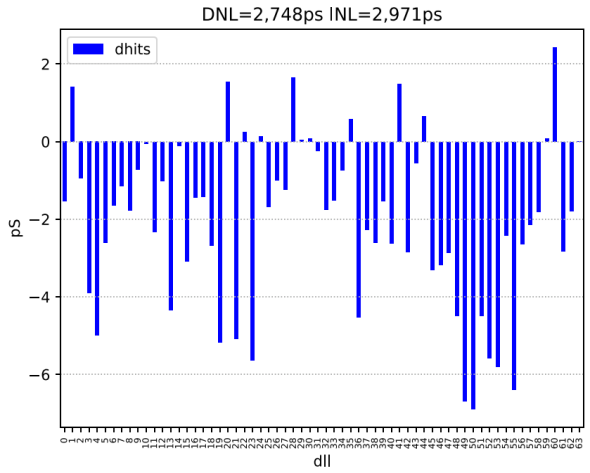
PicoTDC code density test comparison old/new PicoTDC

PicoTDC: Code density test comparison

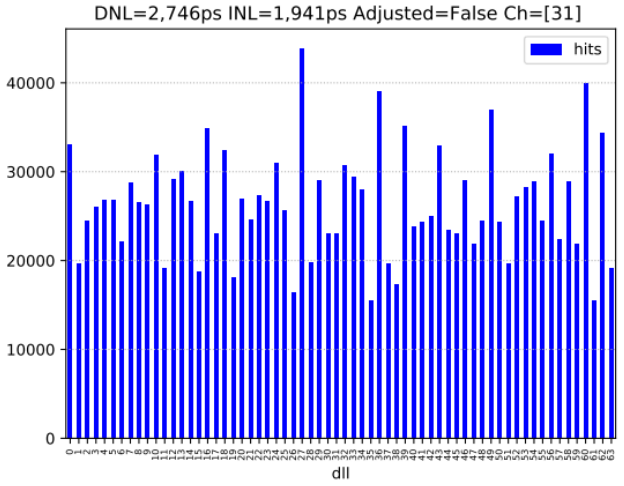
Ch 31, not adjusted, **coarse mode**, bin 12ps

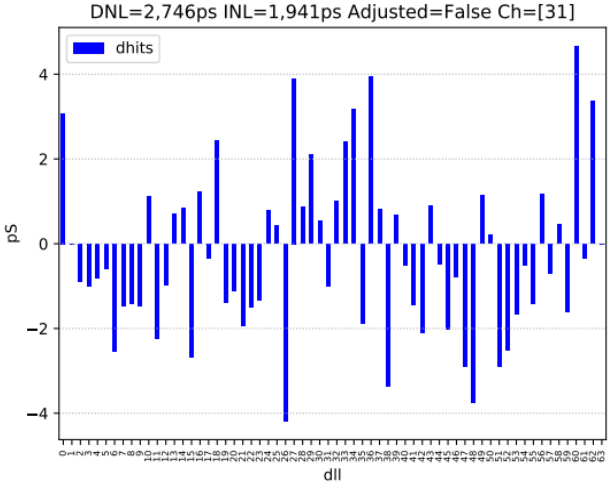
PicoTDC v1





PicoTDC v2

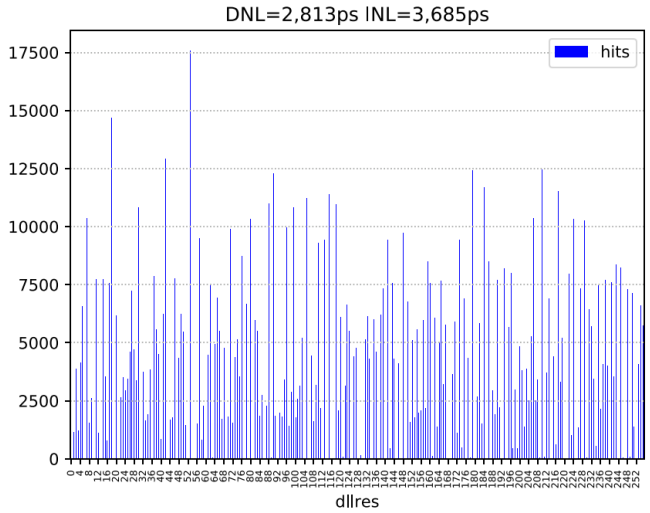


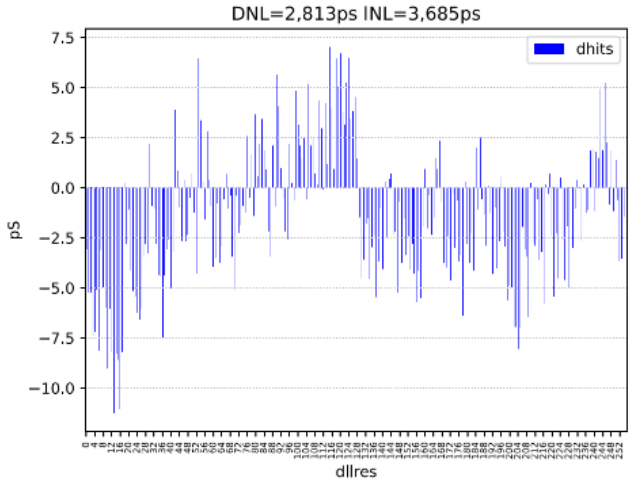


PicoTDC: Code density test comparison

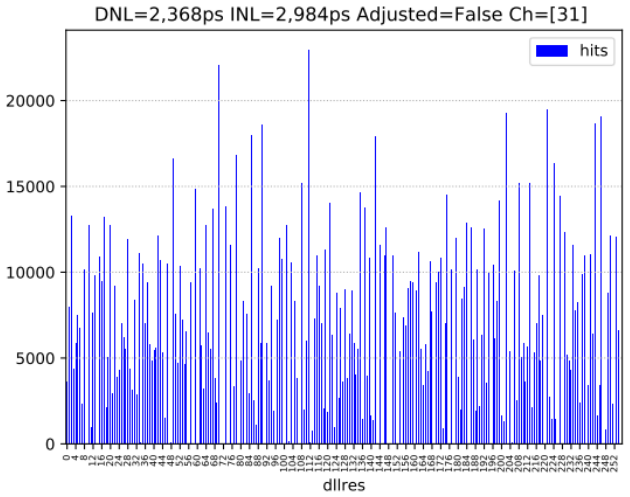
Ch 31, not adjusted, **fine mode**, bin 3ps

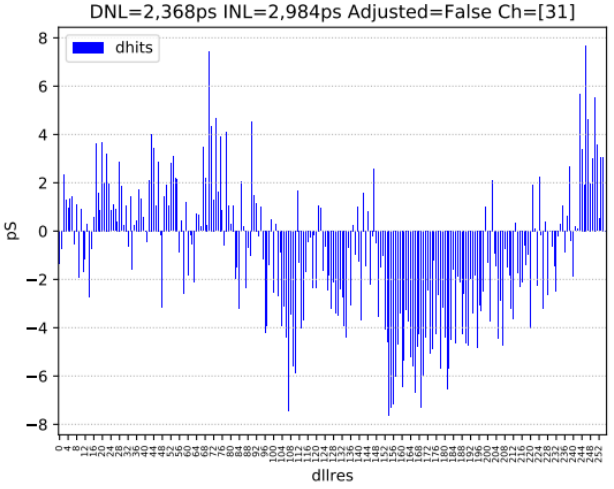
PicoTDC v1





PicoTDC v2

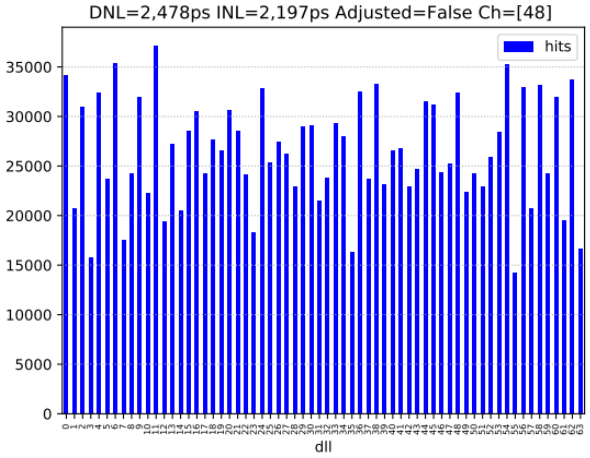


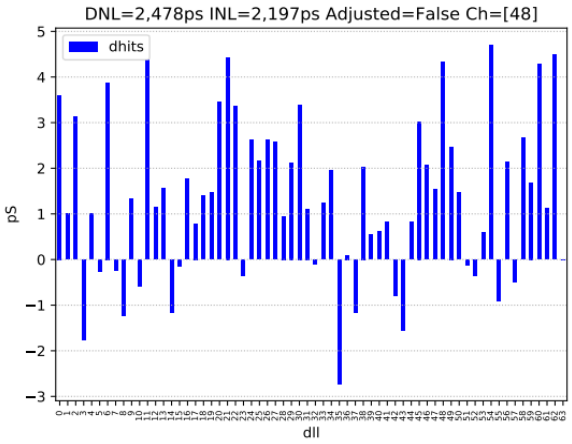


PicoTDC Focus on channel 48

PicoTDC: Code density test

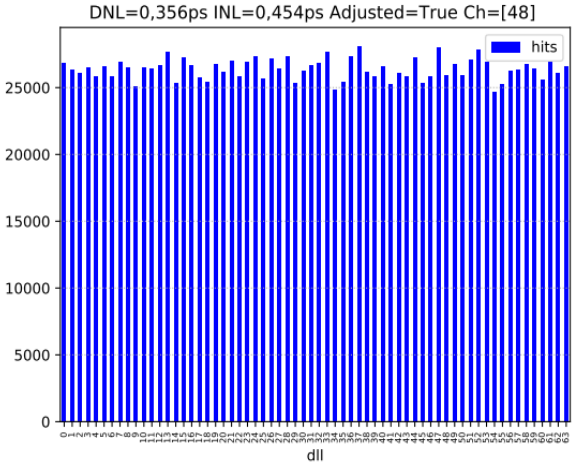
Ch 48, not adjusted, **coarse mode**, bin 12ps, RMS_dnl= 2,478ps, RMS_inl= 2,192ps

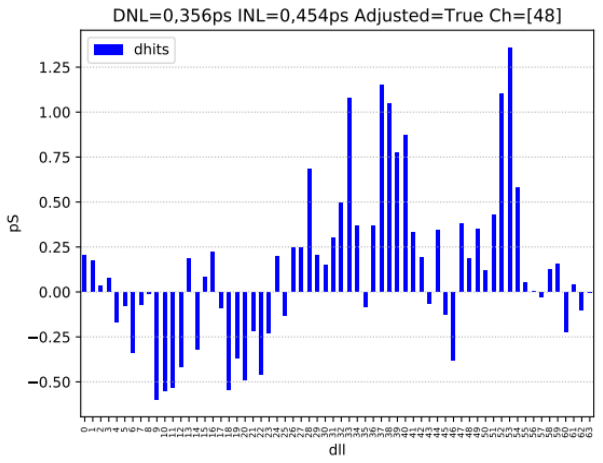




Ch 48, adjusted, **coarse mode**, bin 12ps, RMS_dnl= 0,356ps, RMS_inl= 0,454ps

Adjustment for Ch 48 is performed for this channel alone

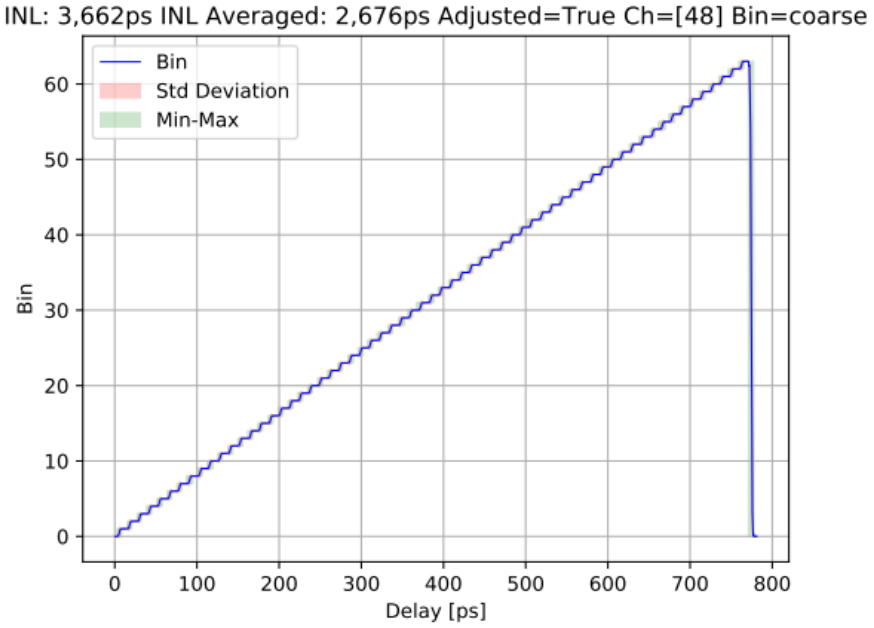




PicoTDC: Delay sweep test

Ch 48, adjusted, **coarse mode**, bin 12ps, RMS_resolution = 3,662ps

*RMS_resolution includes jitter, quantization and INL



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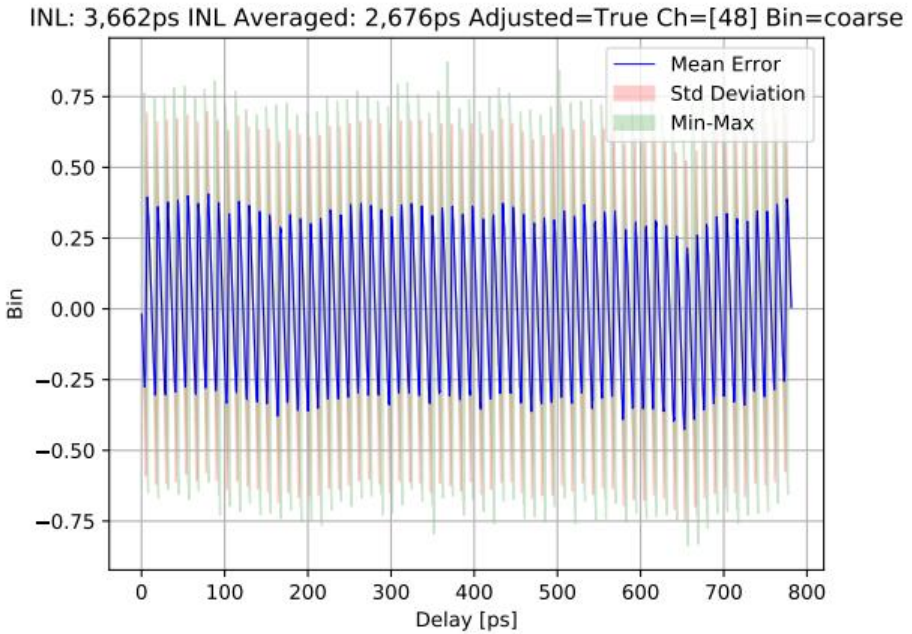
* Link for interactive web plot



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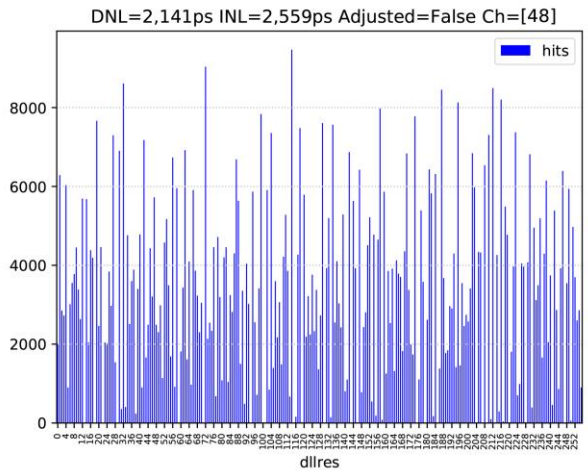
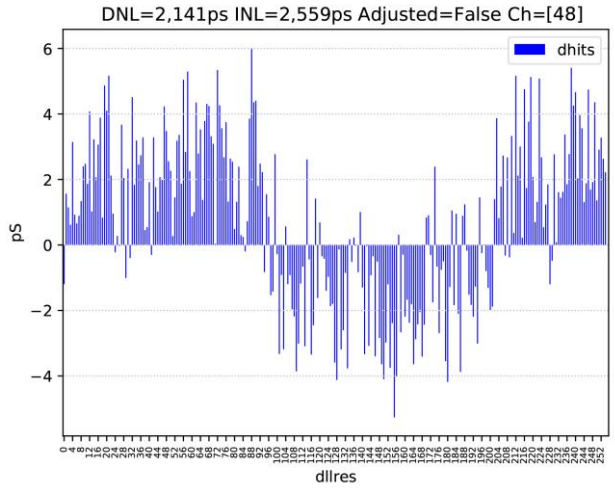
* Link for interactive web plot

PicoTDC: Code density test

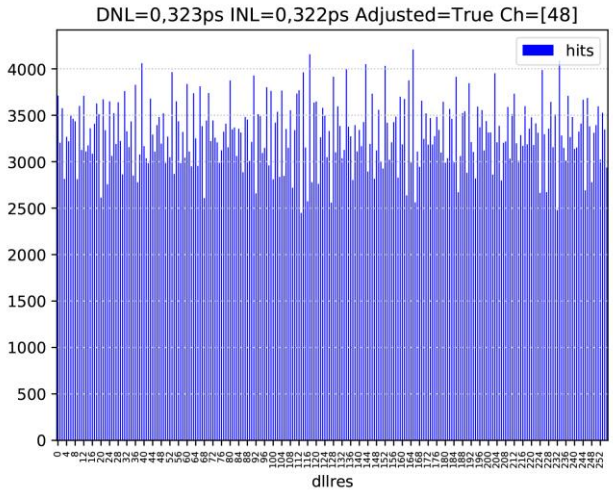
Ch 48, not adjusted, **fine mode**, bin 3ps, RMS dnl= 2,141ps, RMS inl= 2,559ps

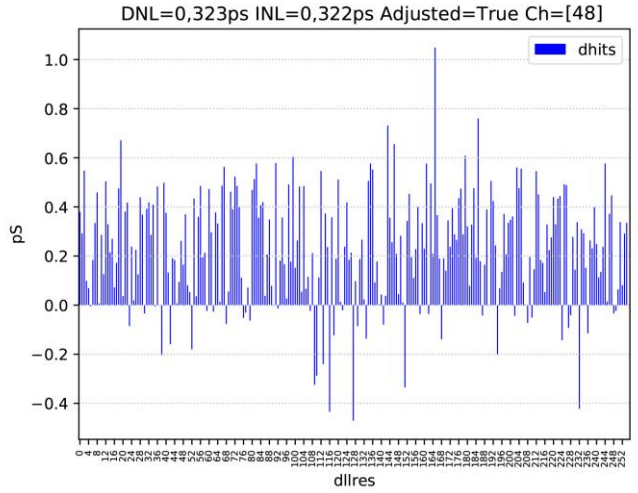




Ch 48, adjusted, **fine mode**, bin 3ps, RMS_dnl= 0,323ps, RMS_inl= 0,322ps

Adjustment for Ch 35 is performed for this channel alone

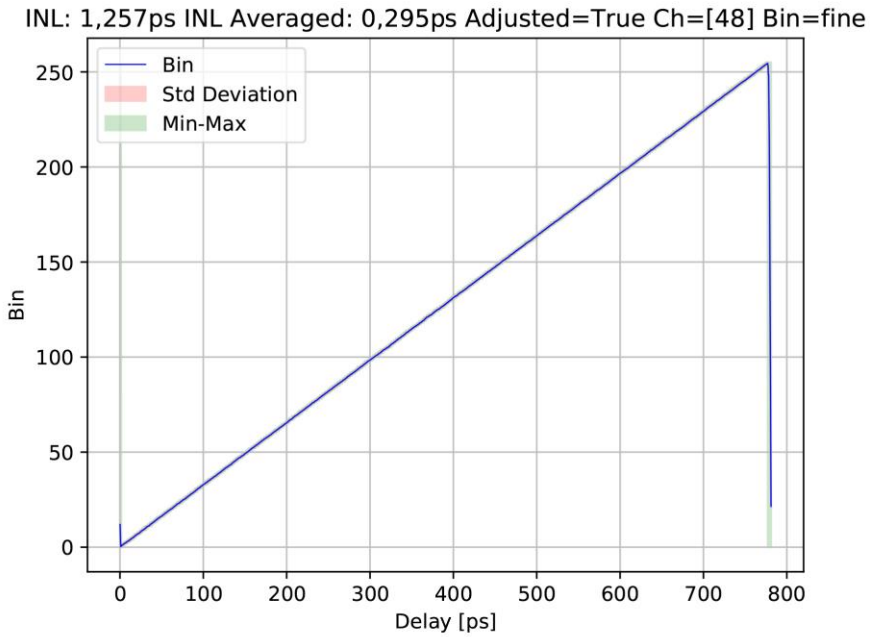


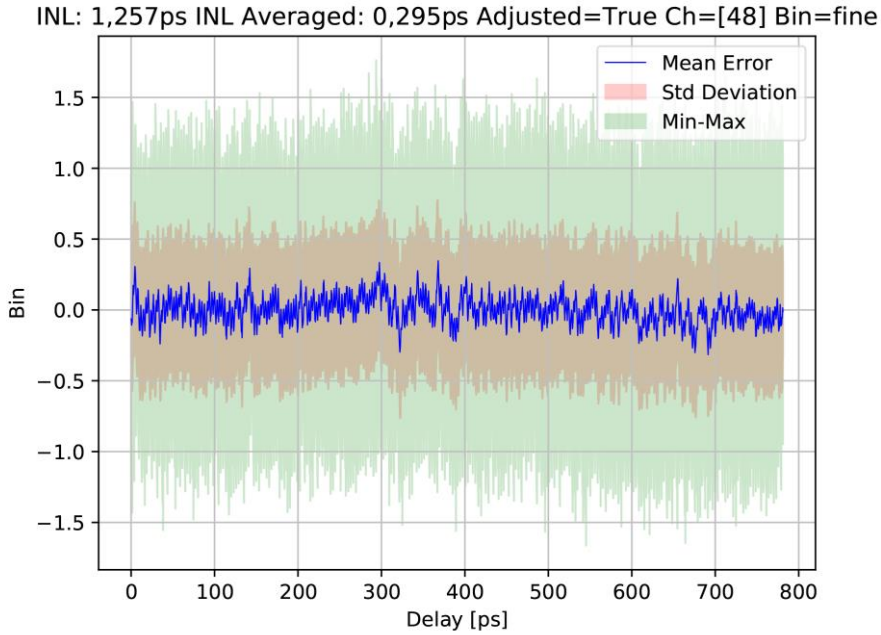


PicoTDC: Delay sweep test

Ch 48, adjusted, **fine mode**, bin 3ps, RMS_resolution = 1,257ps

*RMS_resolution includes jitter, quantization and INL





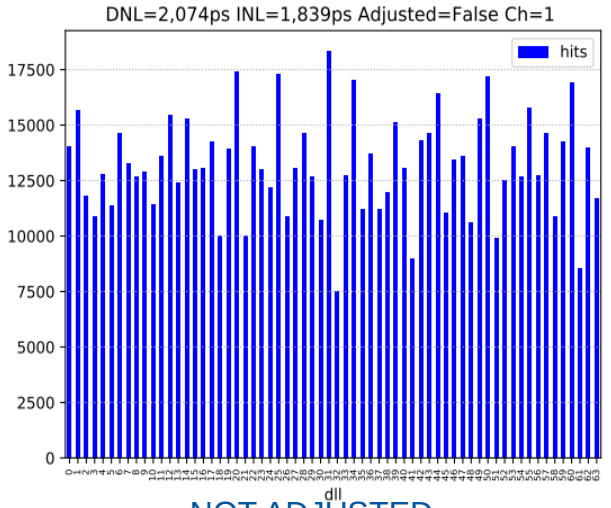
https://cernbox.cern.ch/index.php/s/3OFMDr2Mz4brwMA * Link for interactive web plot

https://cernbox.cern.ch/index.php/s/bL1LSva2binJkb7 * Link for interactive web plot

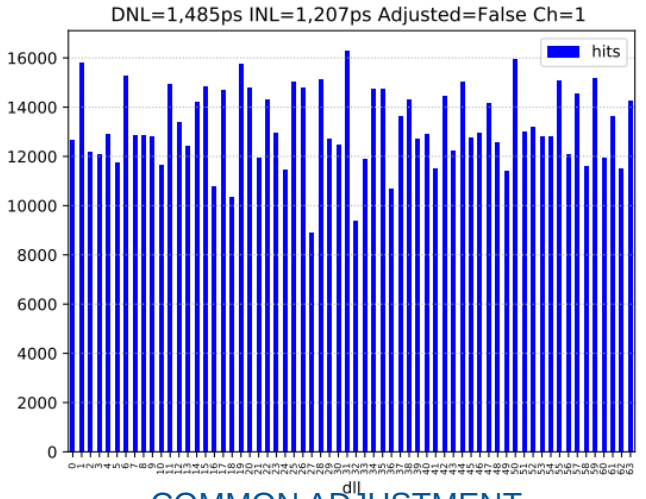
PicoTDC Common adjustment

PicoTDC: Common adjustments

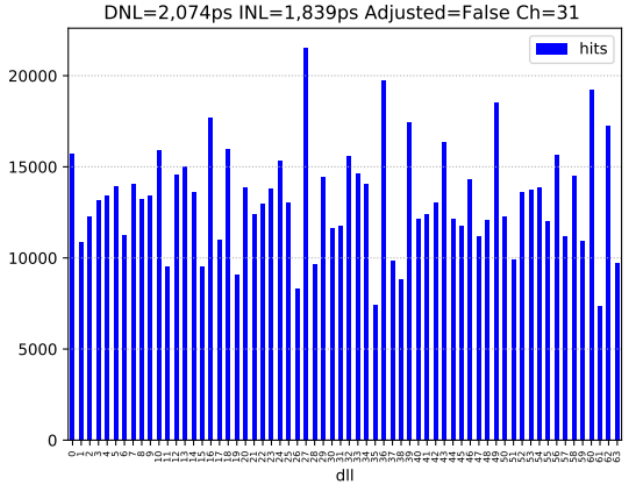
Ch 1-31, **coarse mode**, bin 12ps, RMS_dnl_notadj= 2,074ps, RMS_dnl_adj= 1,485ps

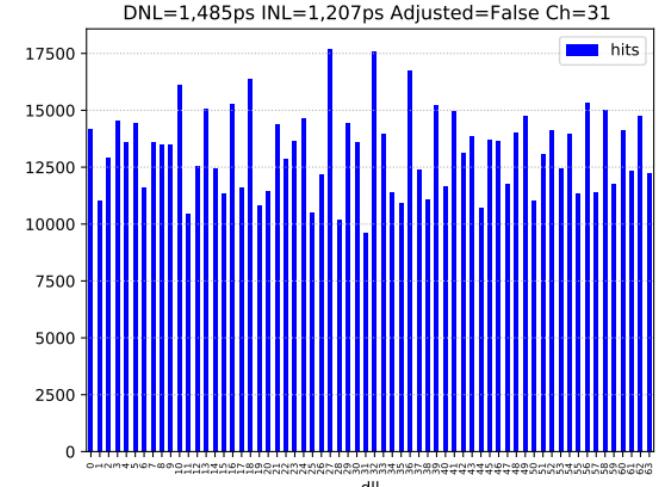


NOT ADJUSTED



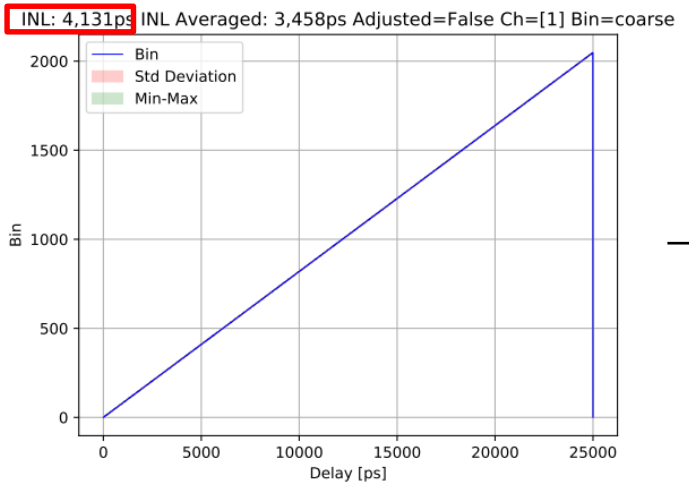
COMMON ADJUSTMENT



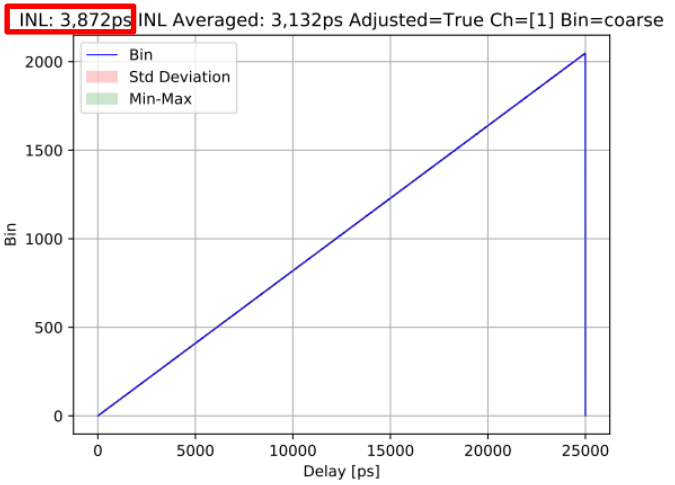


PicoTDC: Common adjustments

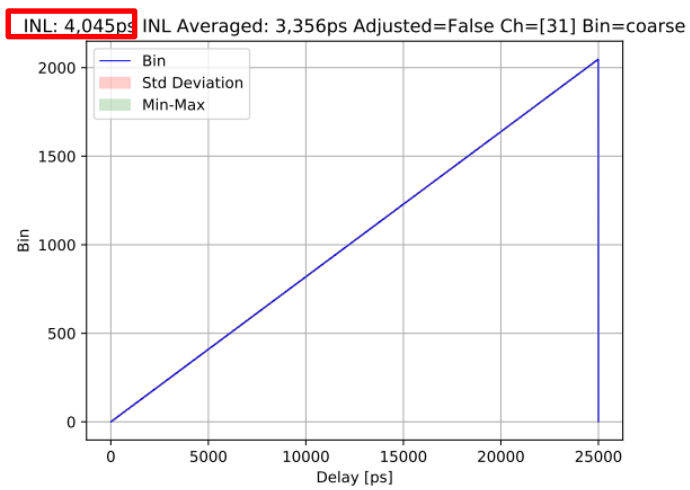
Ch 1-31, **coarse mode**, bin 12ps,

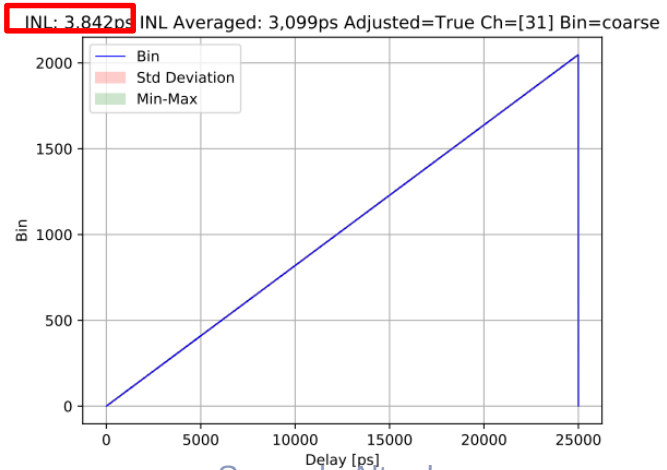


NOT ADJUSTED



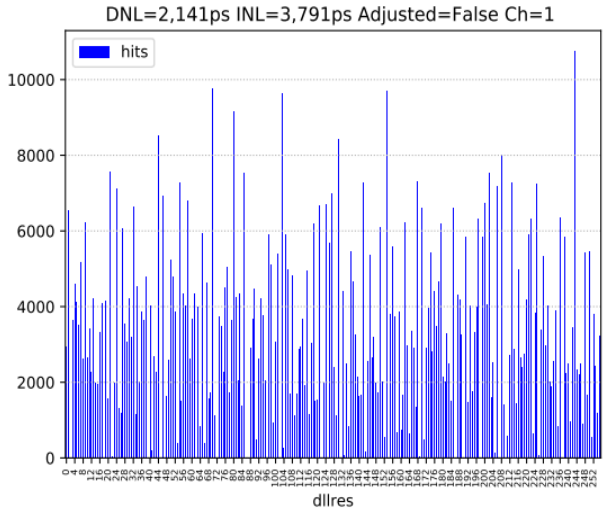
COMMON ADJUSTMENT



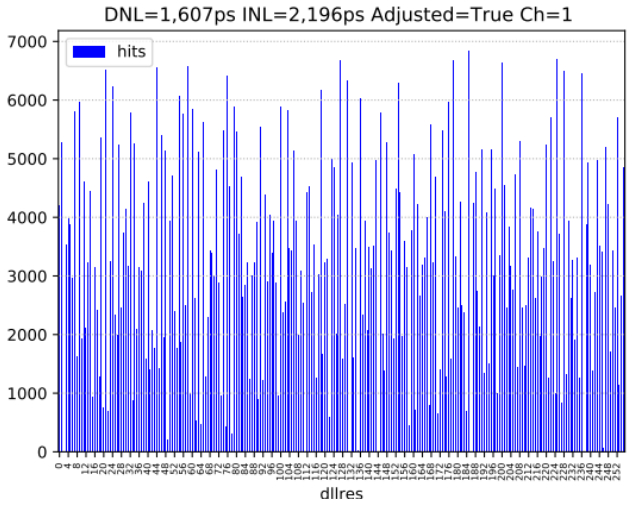


PicoTDC: Common adjustments

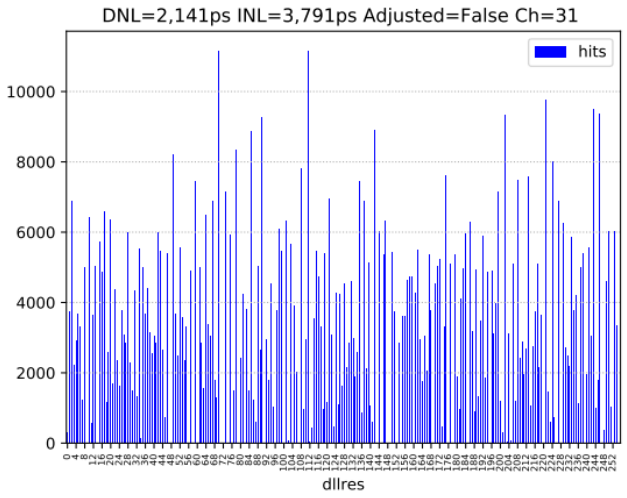
Ch 1-31, **fine mode**, bin 3ps, RMS_dnl_notadj= 2,141ps, RMS_dnl_adj= 1,607ps

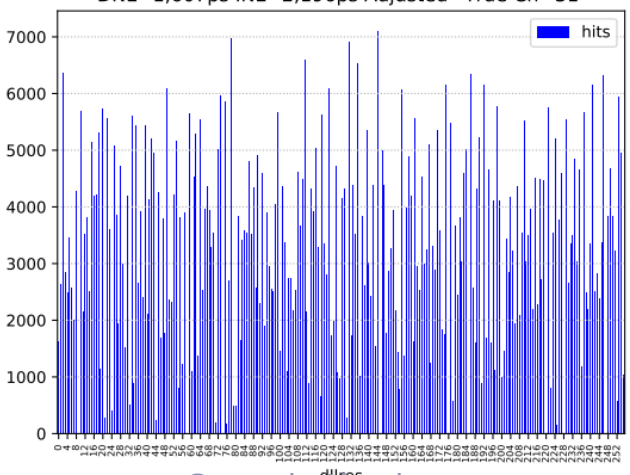


NOT ADJUSTED



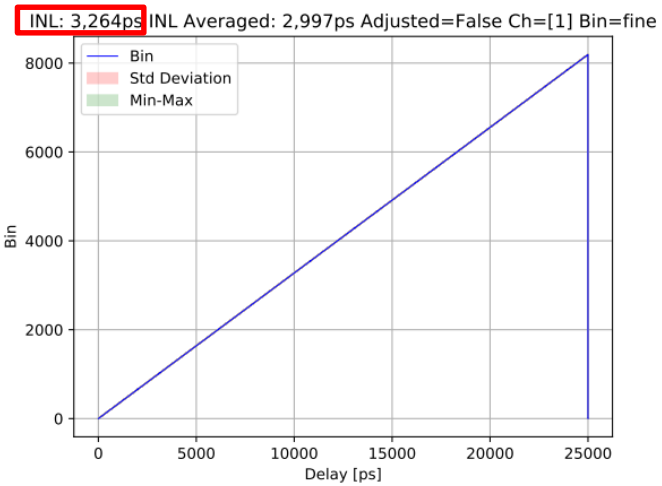
COMMON ADJUSTMENT



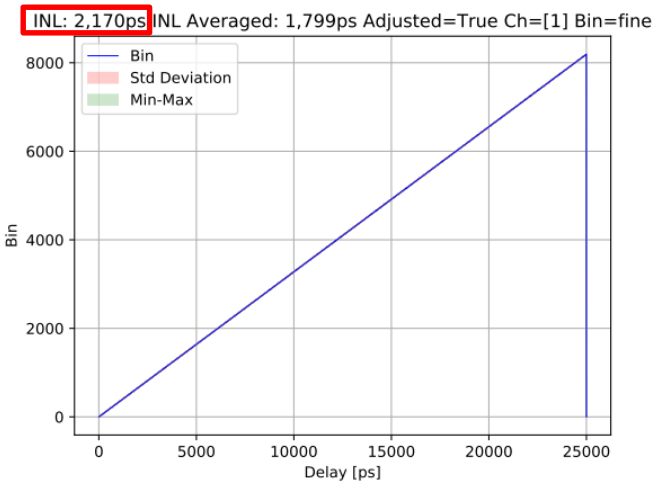


PicoTDC: Common adjustments

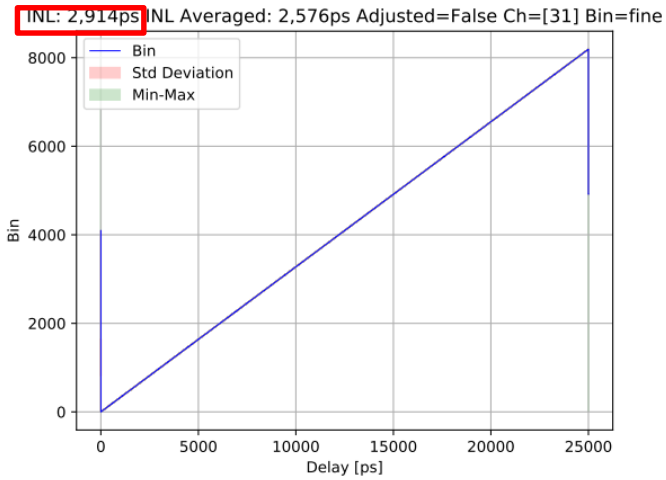
Ch 1-31, **fine mode**, bin 3ps,

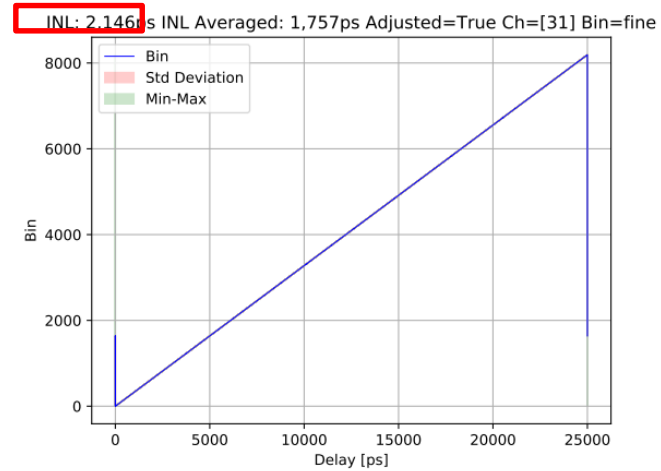


NOT ADJUSTED



COMMON ADJUSTMENT



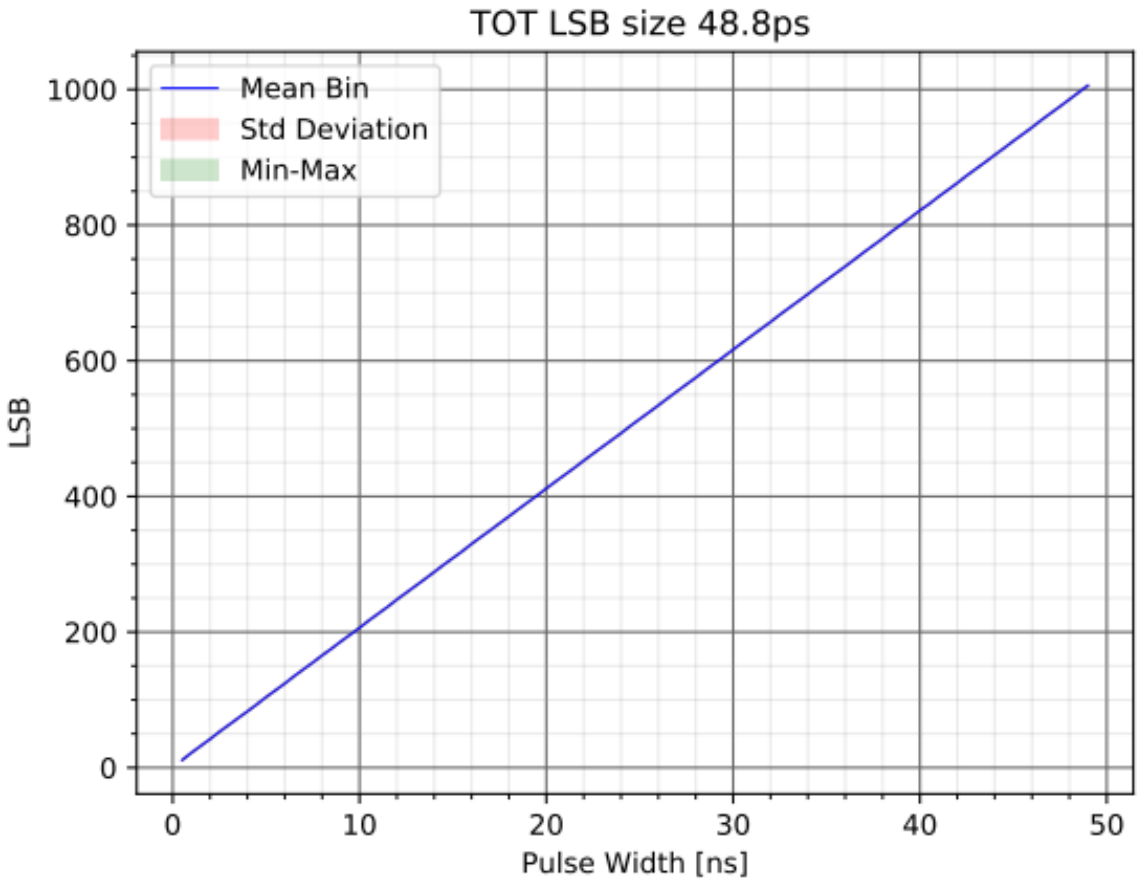


PicoTDC TOT measurements

PicoTDC: TOT test

Ch 1, **fine mode**, bin 3ps, LSB TOT 24.4 ps Clock period 20Mhz

In TOT mode, both leading edge and TOT have programmable resolution.

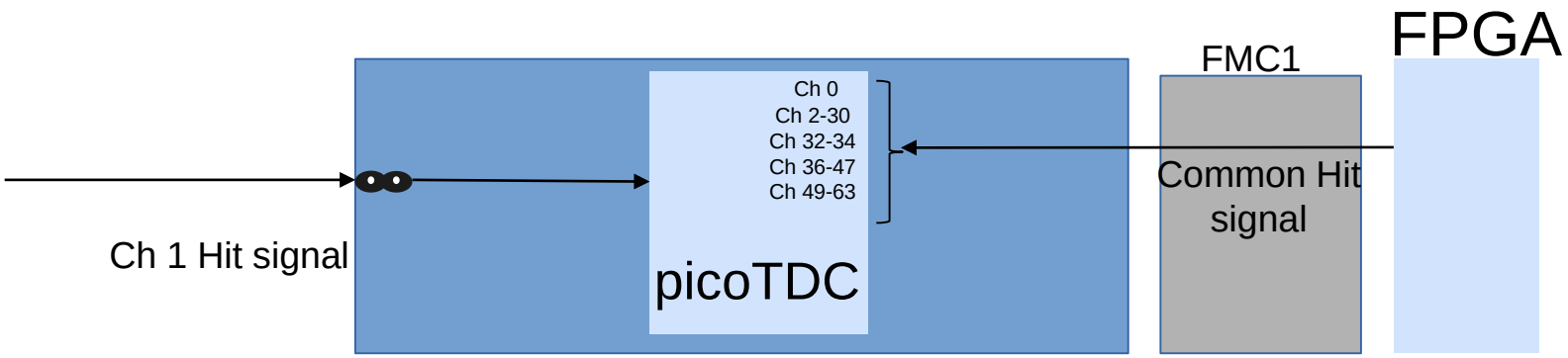


PicoTDC Crosstalk test

PicoTDC: Crosstalk test

Cross talk test is performed to quantify the noise introduced by the others channels against one. Worst case in exam: one against all.

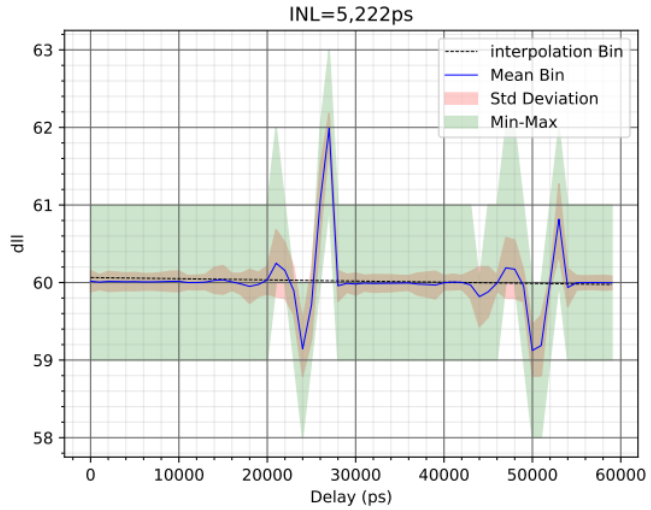
Test scheme simplified



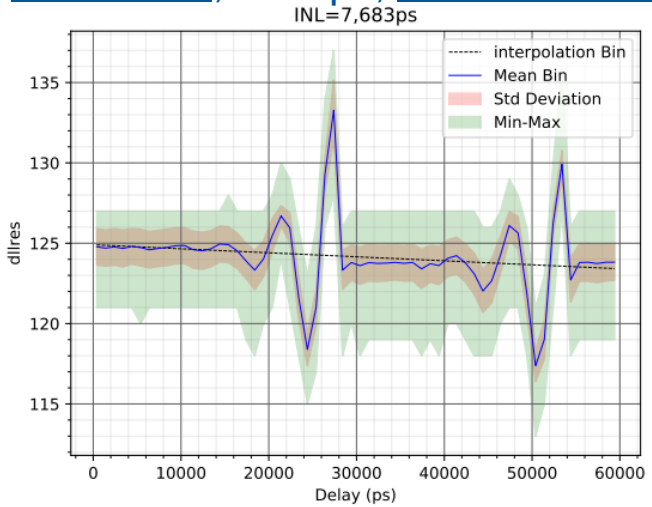
Common Hit signal delay sweep from 0ps to 60000ps
Ch 1 Hit signal at fixed delay

PicoTDC: Crosstalk test

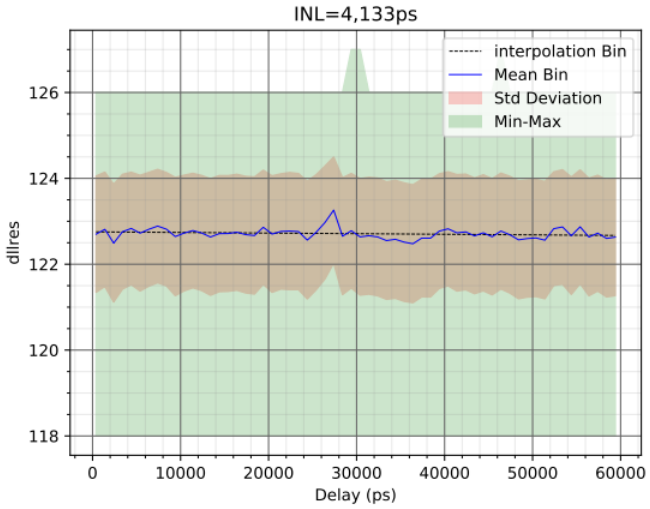
Ch 1, **coarse mode**, bin 12ps, 1 channel vs all



Ch 1, **fine mode**, bin 3ps, 1 channel vs all



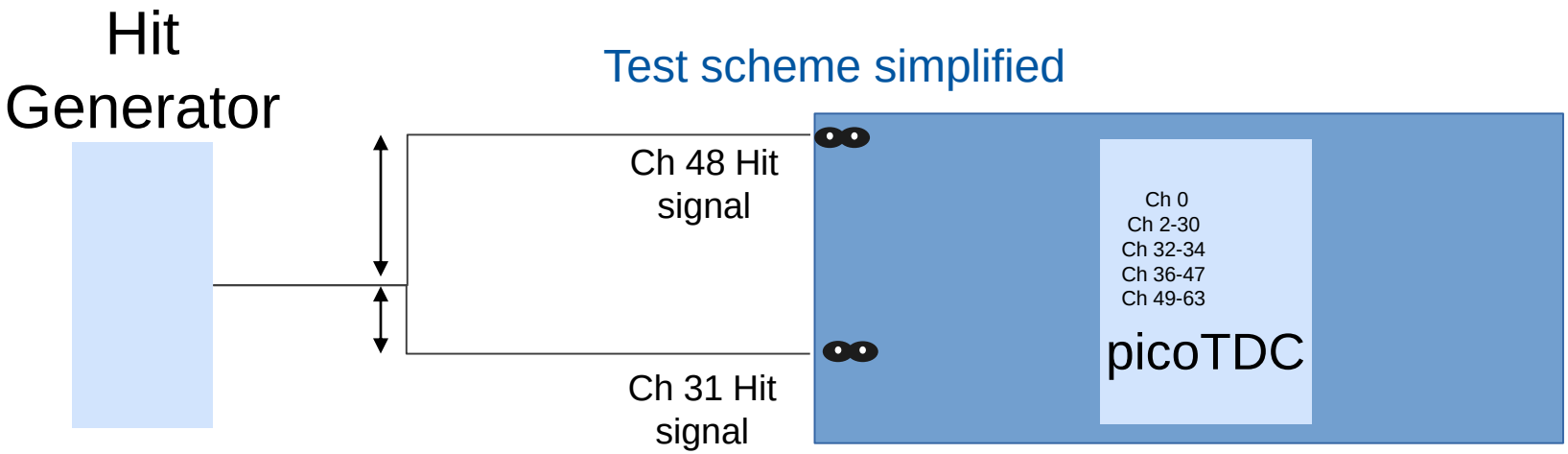
Ch 1, **fine mode**, bin 3ps, 1 channel vs 1 channel adjacent (ch 2)



PicoTDC Cable delay test

PicoTDC: Cable delay test

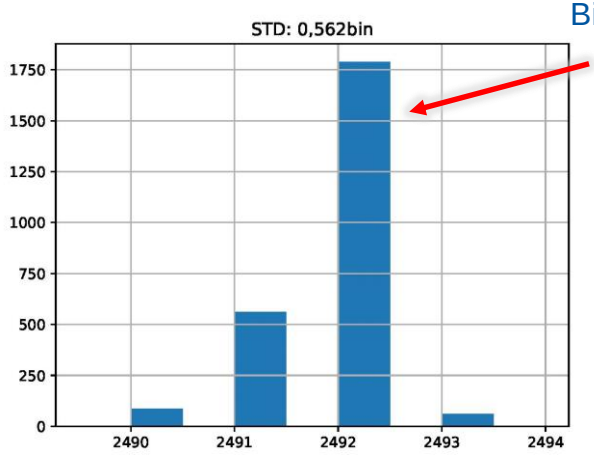
Cable delay test is performed to quantify the linearity of the system over multiple clock cycle, around 200ms



Hit generator outputs a delay sweep hits.
Hits go through different cables with different lengths to channel 31 and 48. Our TDC will measure the time of arrival of the two hits.

PicoTDC: Cable delay test

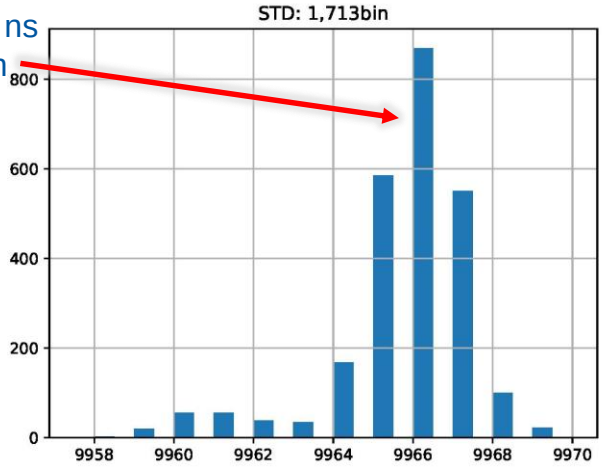
Ch 31, Ch 48, not adjusted , **coarse mode**



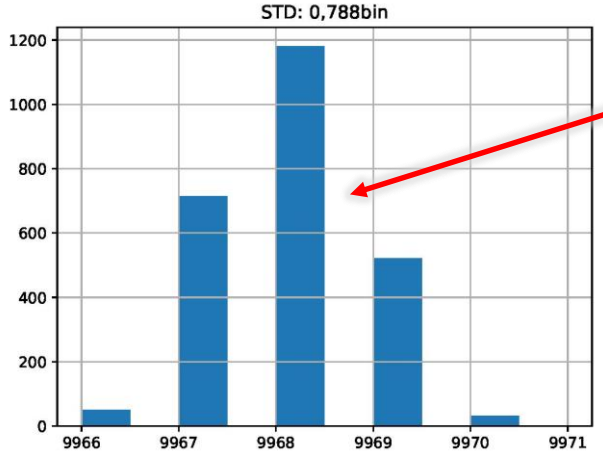
Bin 2492 ~30 ns
Cable length difference

Ch 31, Ch 48, not adjusted , **fine mode**

Bin 9966 ~30 ns
Cable length difference



Ch 31, Ch 48, adjusted each half , **fine mode**

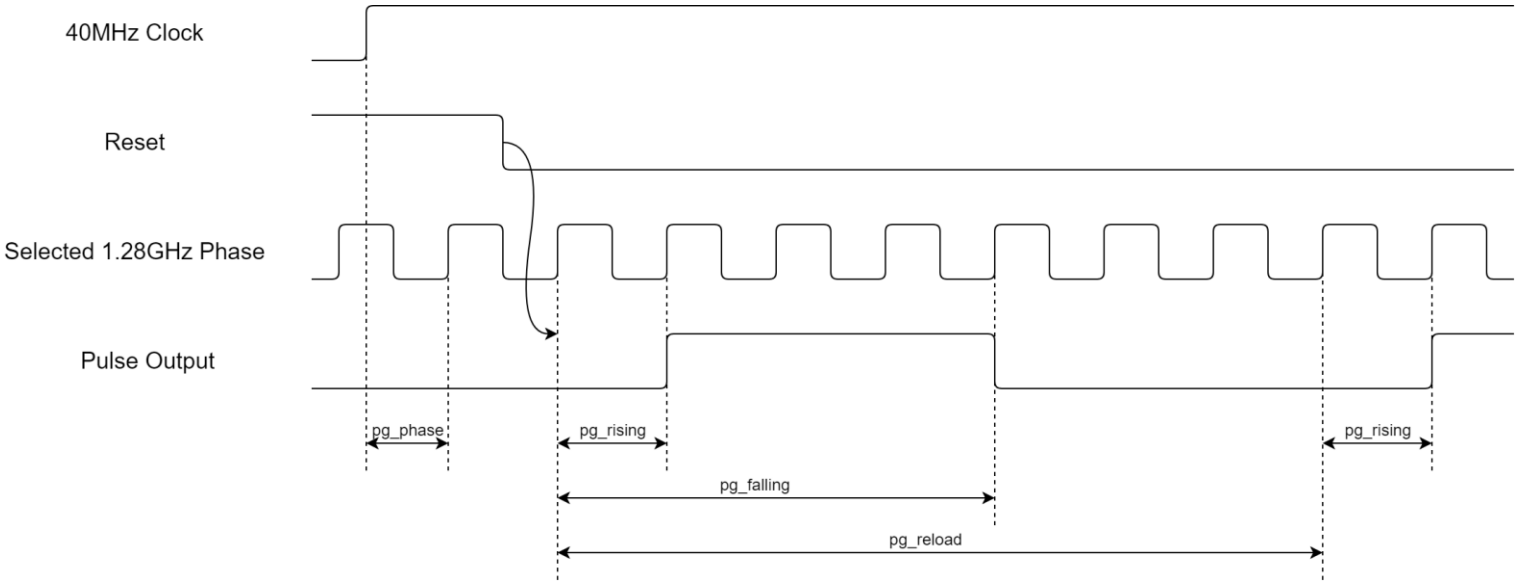


Bin 9968 ~30 ns
Cable length difference

PicoTDC Integrated Pulse Generator

PicoTDC: Integrate Pulse Generator test

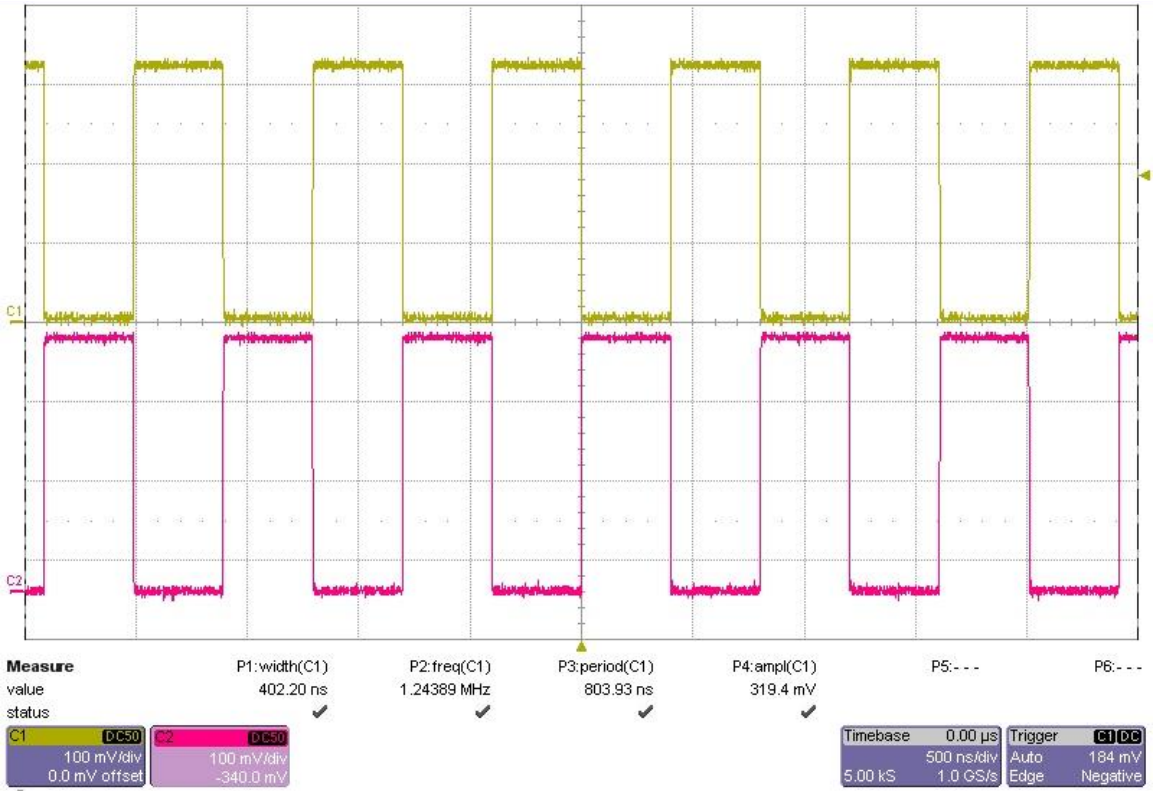
- The PicoTDC contains a pulse generator for system testing purposes, able to generate a differential output signal.
- The output can either be a 1.28GHz clock with selectable phase shift or a configurable pulse.This works internally with a selection of one of the 256 clock phases of the upper half of the timing macro.
- In this example, the pulse generator was configured to use clock phase 192 (relation to the 40MHz clock), the time of the rising edge is set to 1, the falling edge to 4 and the repetition time to 7.



PicoTDC: Integrate Pulse Generator test

Ch 1, phase 3, rising 513(LSB), falling 1027(LSB), reload 1028(LSB)

Period= reload(LSB)*0.78125ns=803 ns



Measurement done with limited bandwidth and sampling frequency scope.
More measurements to be done with high speed scope back to CERN.

PicoTDC new version

PicoTDC v2

New features available on version 2:

- Configurable pulse generator on chip
- Trigger from channel 1

Production schedule:

- PicoTDCv2 at CERN bonded on old test board available and tested
- Functional and timing performance test of PicoTDCv2 bonded on old PCB ongoing
- Functional and timing performance test of PicoTDCv2 on generic package in April - May 2020
- Functional and timing performance test of PicoTDCv2 in final package in July - September 2020

Share point link for info and material: http://cern.ch/PicoTDC

For more info and request access to the material write to:

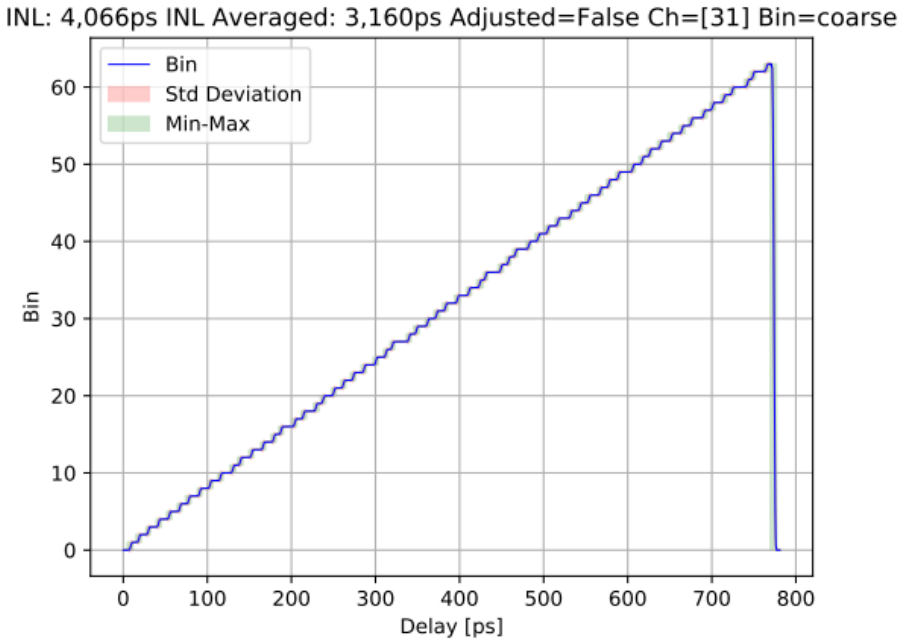
Jorgen Christiansen <Jorgen.Christiansen@cern.ch>
Samuele Altruda <samuele.altruda@cern.ch>


CERN

PicoTDC: Delay sweep test

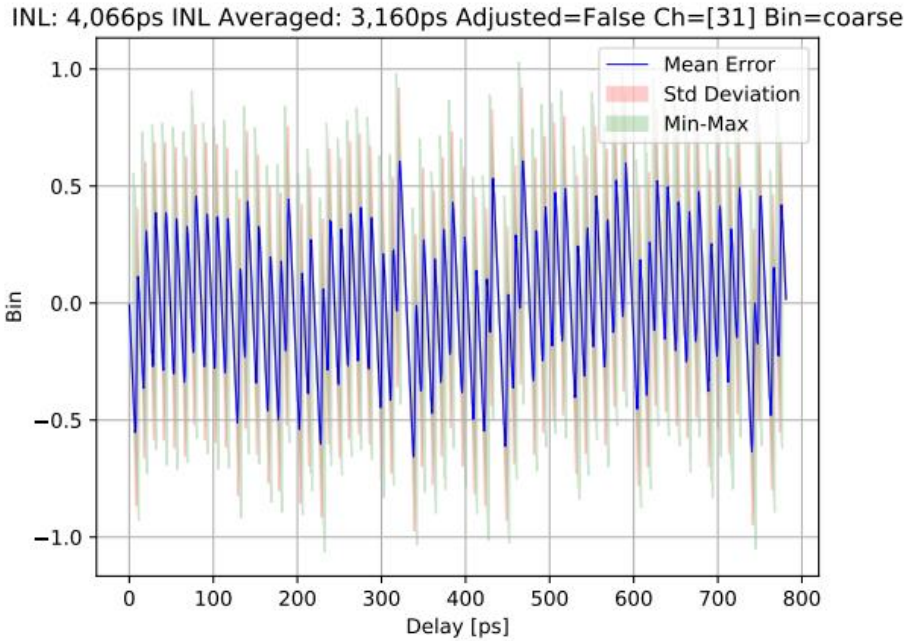
Ch 31, not adjusted, **coarse mode**, bin 12ps, RMS_resolution = 4,066ps

*RMS_resolution includes jitter, quantization and INL



https://cernbox.cern.ch/index.php/s/b2bdVf2JDZU1wPc

* Link for interactive web plot



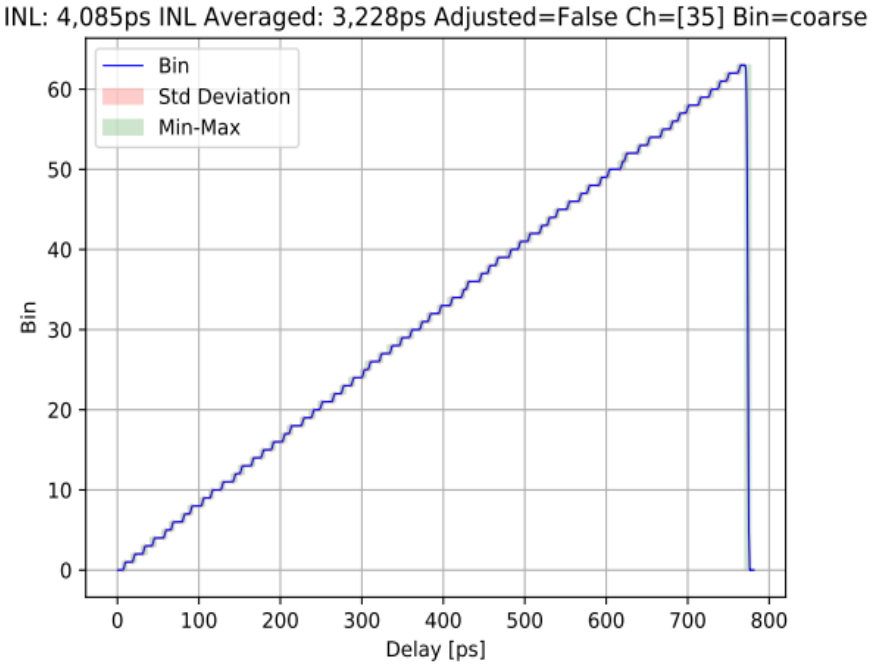
https://cernbox.cern.ch/index.php/s/MVsmlaZT0ztRpNQ

* Link for interactive web plot

PicoTDC: Delay sweep test

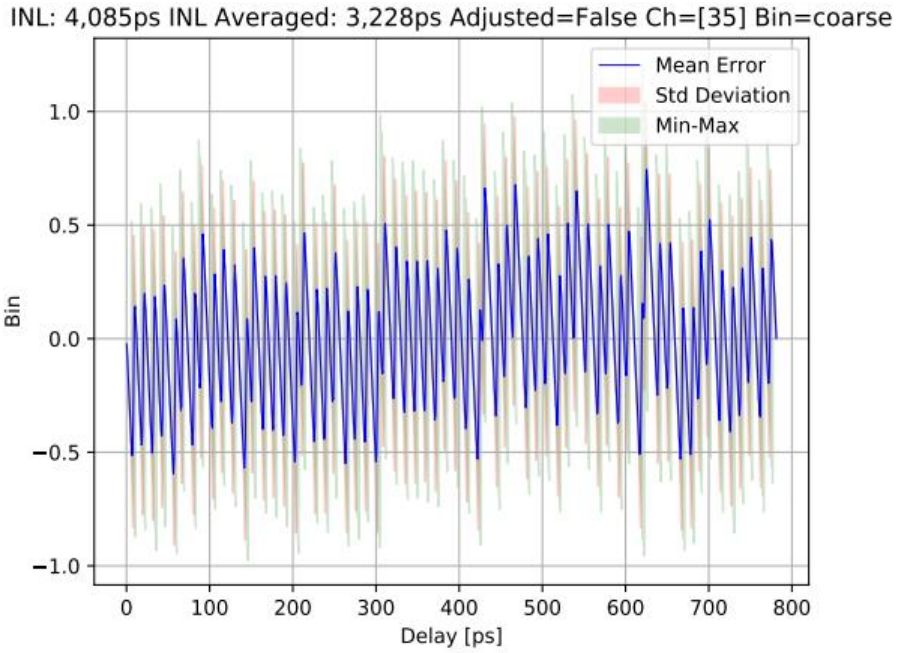
Ch 35, not adjusted, **coarse mode**, bin 12ps, RMS_resolution = 4,085ps

*RMS_resolution includes jitter, quantization and INL



https://cernbox.cern.ch/index.php/s/Od3gfXKGbDd4gGA

* Link for interactive web plot



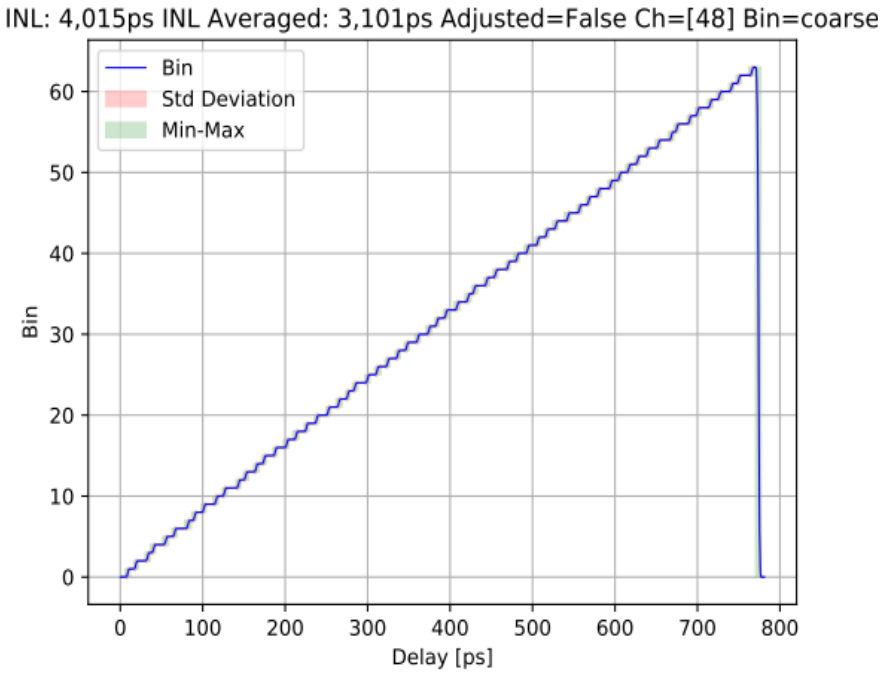
https://cernbox.cern.ch/index.php/s/9bvaWodjuWe0puq

* Link for interactive web plot

PicoTDC: Delay sweep test

Ch 48, not adjusted, **coarse mode**, bin 12ps, RMS_resolution = 4,015ps

*RMS_resolution includes jitter, quantization and INL



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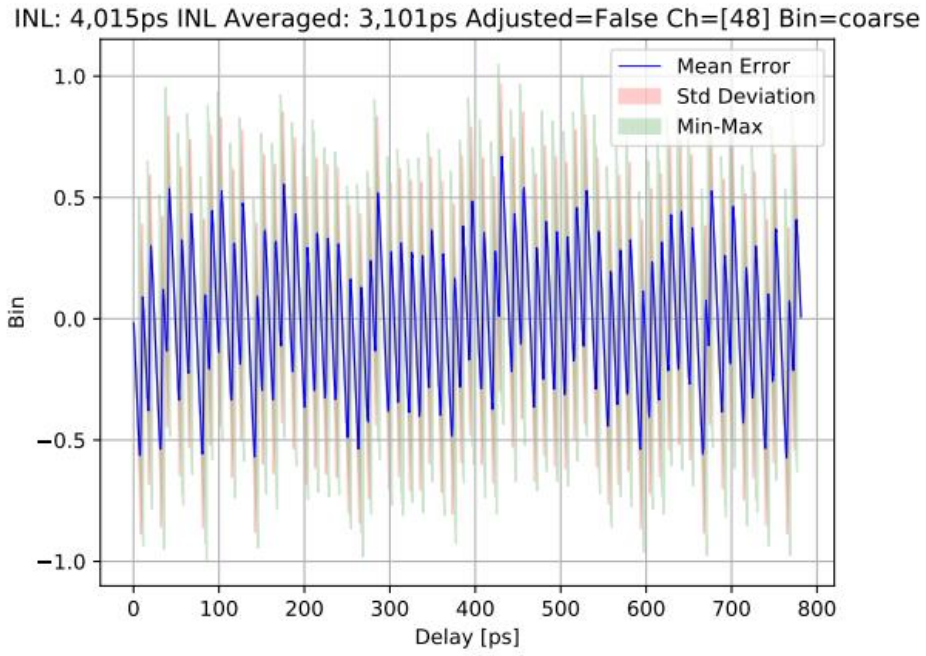
* Link for interactive web plot



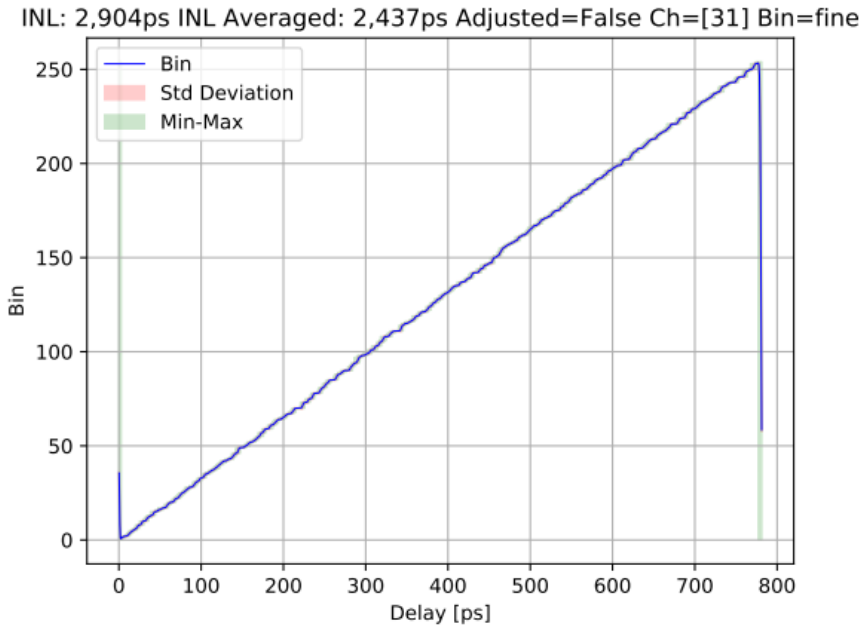
https://cernbox.cern.ch/index.php/s/ft5glBUL7PSWP4k

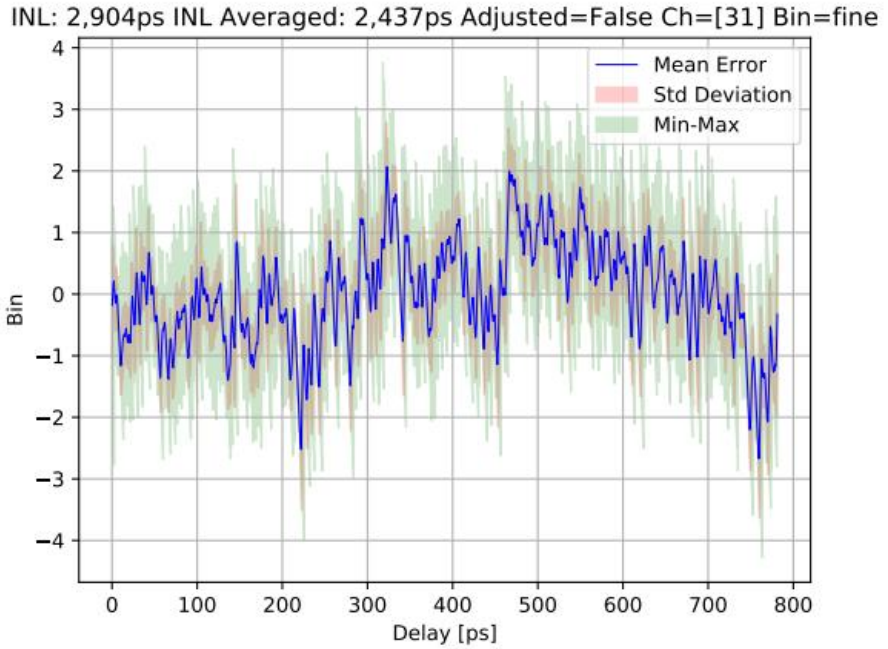
* Link for interactive web plot

PicoTDC: Delay sweep test

Ch 31, not adjusted, **fine mode**, bin 3ps, RMS_resolution = 2,904ps

*RMS_resolution includes jitter, quantization and INL





https://cernbox.cern.ch/index.php/s/fskC5r9l2V7ZMVq

* Link for interactive web plot

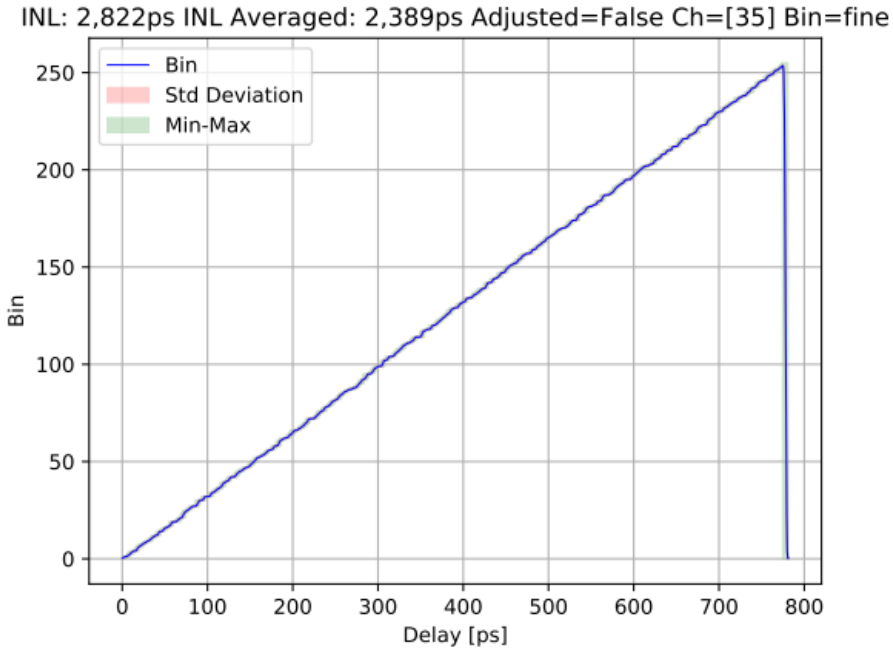
https://cernbox.cern.ch/index.php/s/QtcVm2R0UYcXNNa

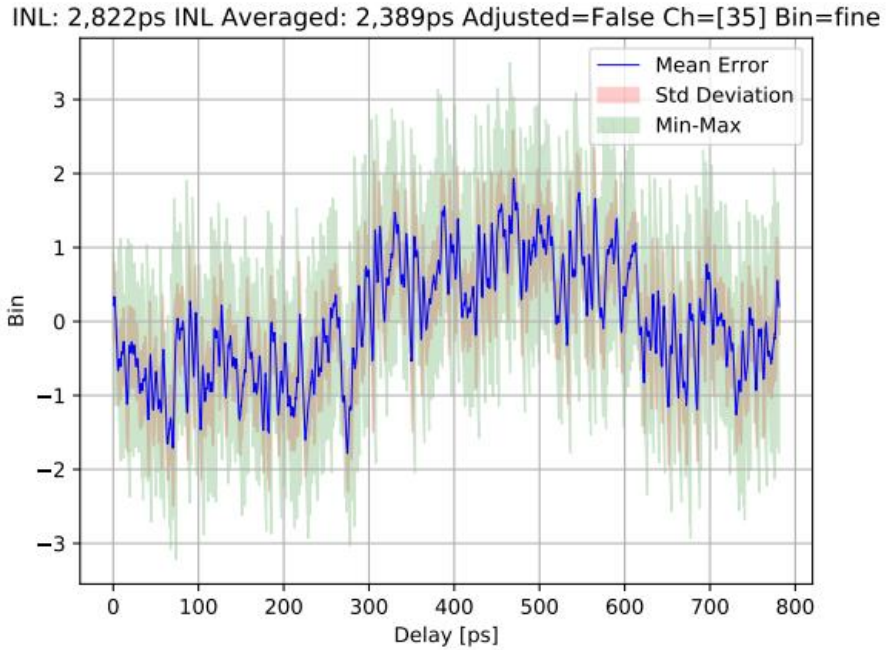
* Link for interactive web plot

PicoTDC: Delay sweep test

Ch 35, not adjusted, **fine mode**, bin 3ps, RMS_resolution = 2,822ps

*RMS_resolution includes jitter, quantization and INL





https://cernbox.cern.ch/index.php/s/kFmKMVg7X0JlZzC

* Link for interactive web plot

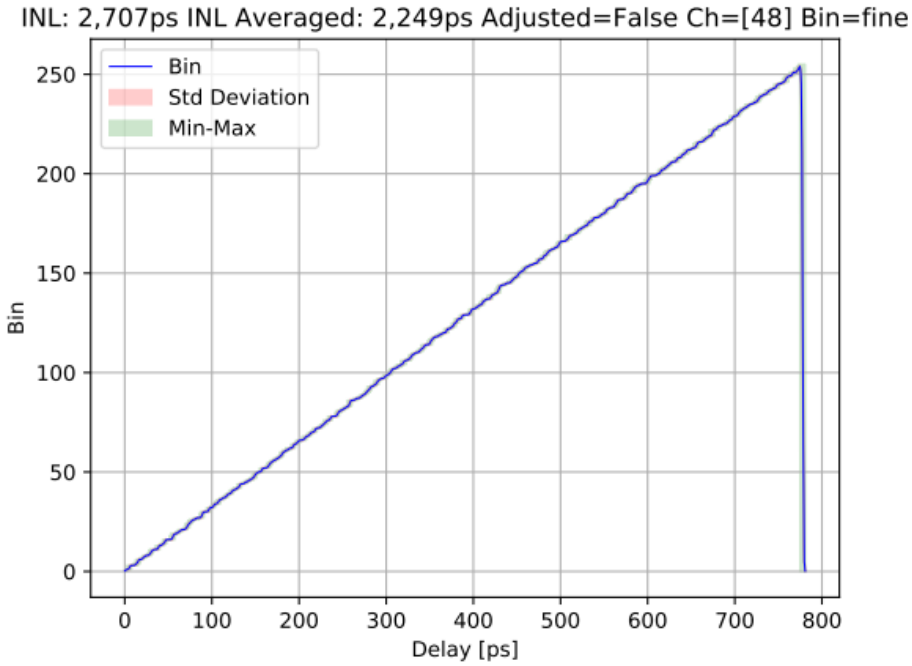
https://cernbox.cern.ch/index.php/s/ZdxoMEgEyYxAXc4

* Link for interactive web plot

PicoTDC: Delay sweep test

Ch 48, not adjusted, **fine mode**, bin 3ps, RMS_resolution = 2,707ps

*RMS_resolution includes jitter, quantization and INL



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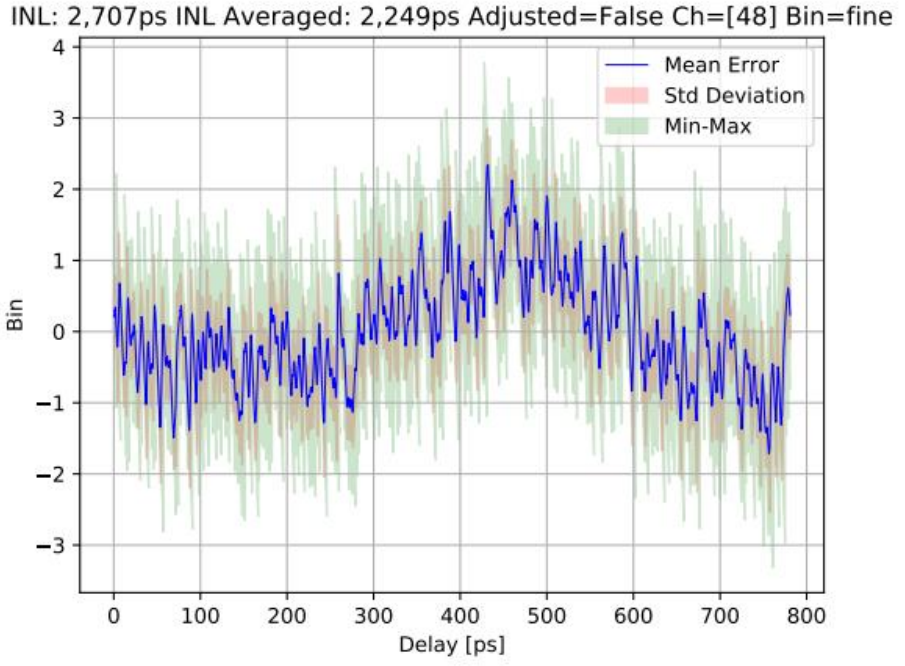
* Link for interactive web plot

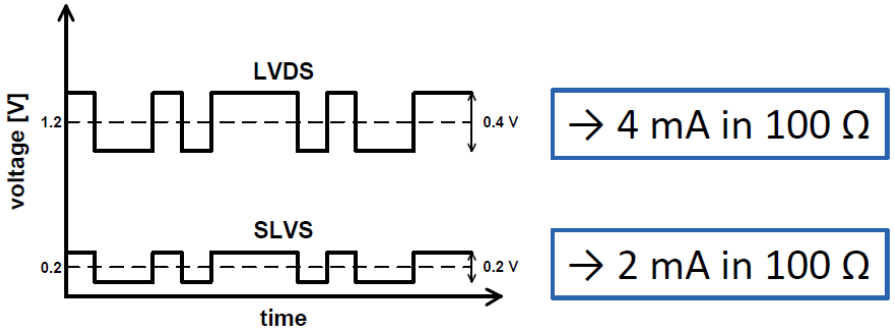


https://cernbox.cern.ch/index.php/s/g3sH0f4zMbw4KOf

* Link for interactive web plot

Electrical Interfaces

- Hits: Differential (LVDS “compatible”, common mode from 0.2V to 1.2V)
  - Highest speed (resolution) @ ~800mV common mode
- Time reference: 40MHz differential
  - Low jitter reference critical for high time resolution
- Trigger/Event-Rst/BX-Rst/Reset: Sync Yes/No
- Control/monitoring: I^2C at CMOS 1.2V-levels
- Readout: 4 readout ports of 8 differential signals
  - Common mode 0.6V, programmable current 1-5mA
  - Compatible with LpGBT and FPGAs
- Packaging: 400 BGA (1mm pitch)



Config / Control / Status Interface

- I^2C Interface, up to 1MBit/s
- 1.2V CMOS Levels
- 348 Bytes configuration / control
  - Additional 322 bytes delay adjust
- 300 Bytes status

Readout

- 1 or 4 differential readout ports with 8 bits
  - 40 - 320MHz
  - Bandwidth:
    - Min 320Mbits/s (~0.15 Mhits/s per channel)
    - Max 10Gbits/s (~4 Mhits/s per channel)
- Readout data: 32 bit words
  - TDC data, headers, trailers etc.

32 Bit Frames

TDC measurement

Event headers (up to two)

Possible fields: Event ID, Bx ID, Natural ID

Event trailers

Channel group separator (for single readout port)

Idle frame

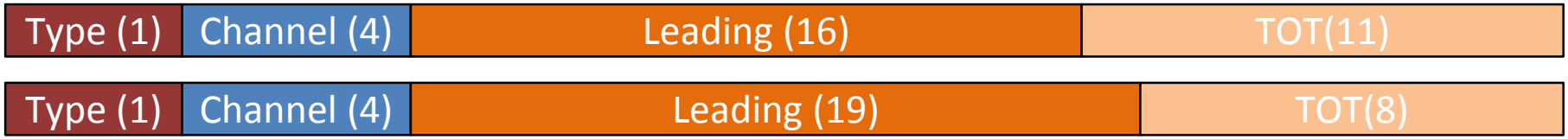
Absolute TDC data

FULL TDC data, **DEFAULT FORMAT**

Relative to Trigger

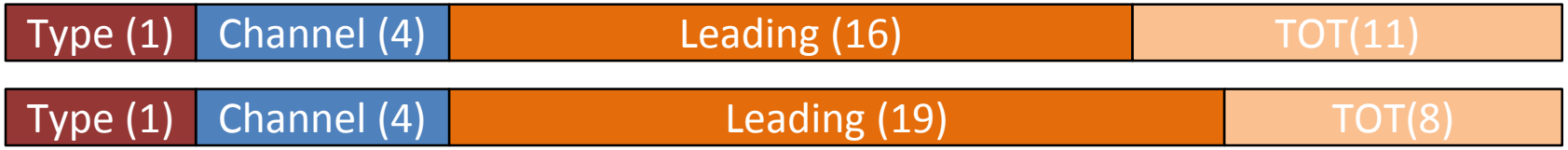
Triggered with relative time: Same as absolute

B: Triggered with relative leading and TOT: Same as absolute Lead. + TOT



Leading + TOT

- Packet Type: 1bit
- Channel ID: 4 bits, for single port readout +2 bit group separator
- Leading: 16/19 bits
  - Large dynamic range
    - 16bit 3ps resolution: 200ns
    - 19bit 3ps resolution: 1600ns
  - **Programmable part of full 25bits leading TDC**
  - (**Relative to trigger to be useable**)
- TOT (Relative to leading): 11/8 bits
  - Short dynamic range:
    - 8bit 3ps resolution: 780ps
    - 11bit 3ps resolution: 6.1ns
  - **Programmable part of full 25bits TOT difference**
    - TOT assumed to be used for offline time-walk correction of leading.
- Alternative: Readout of Individual Leading and Trailing edges with full range/resolution
  - 2x readout bandwidth



Estimated Power Consumption

Highly dependent on hit rate, values based on 1 MHz per channel

- High resolution, 64 channels: 1300mW
- High resolution, 32 channels: 900mW
- Low Resolution, 64 channels: 850mW
- Low Resolution, 32 channels: 550mW