

Introduction

Run4 module concept

Timing measurements

TDC requirements

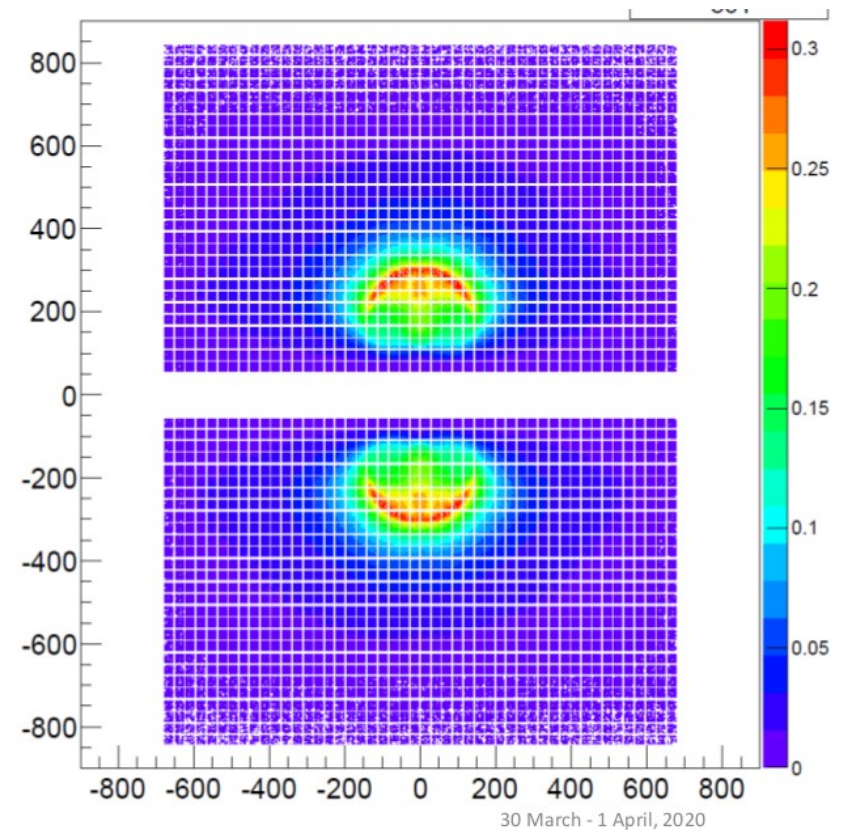
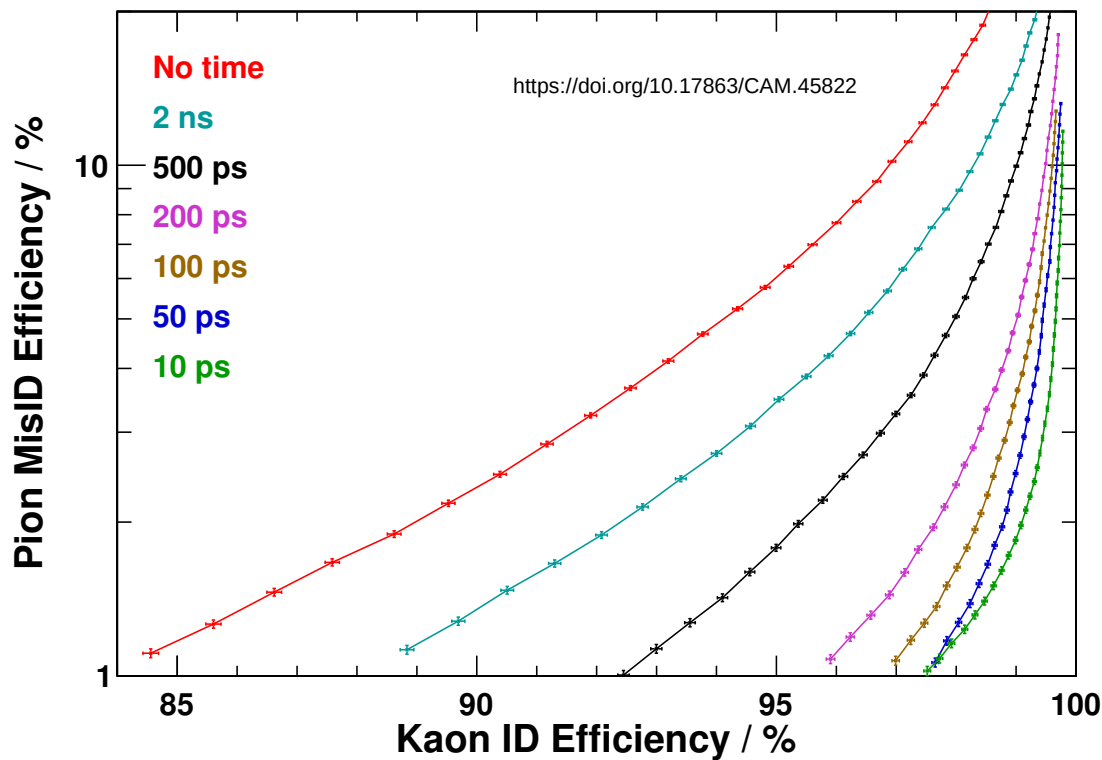
Readout integration

Summary of quantities



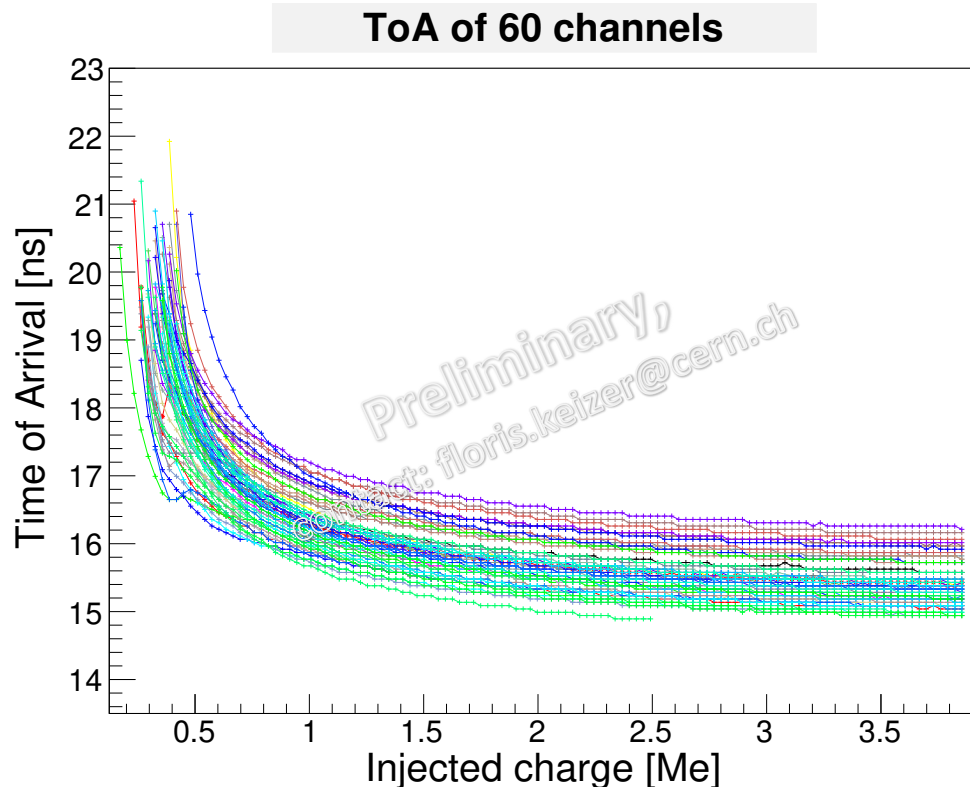
# LHCb RICH from Run3 to Run5

- Detector occupancy will increase significantly in future
- PID performance will degrade unless...
- Use photon arrival time
- RICH has excellent intrinsic timing characteristics and will be further optimised in future
- We want to exploit this in future upgrades



# Run3 to Run5 (cont.)

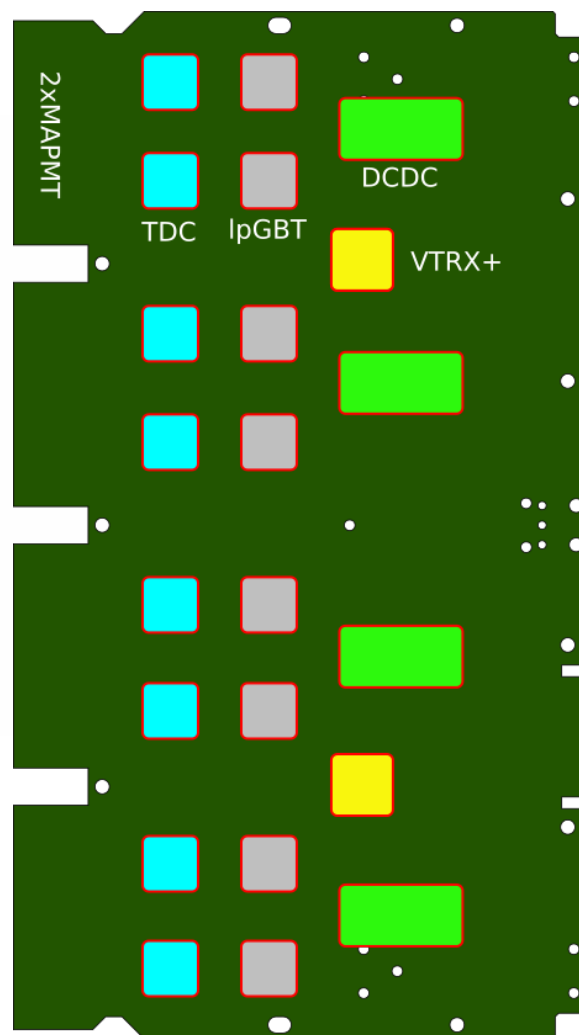
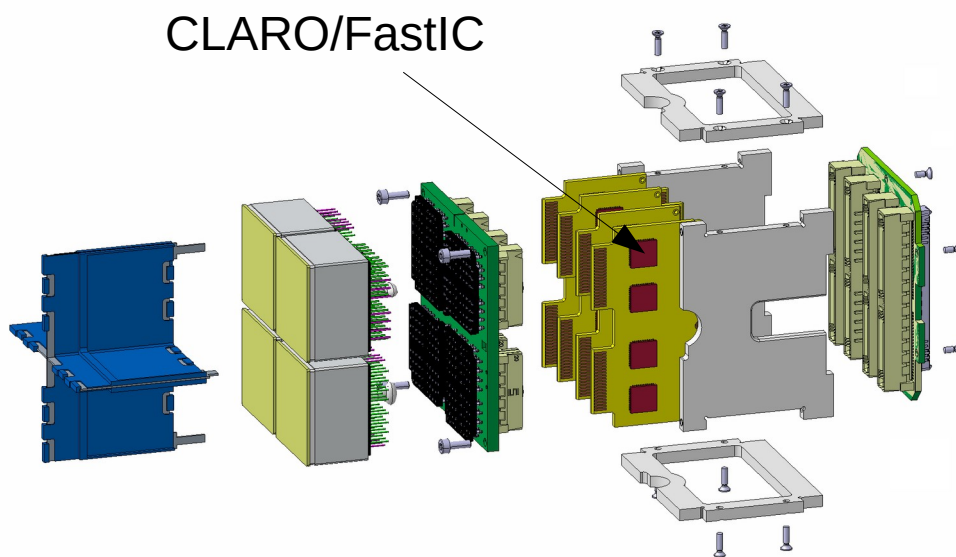
- Timing measurements with Run3 electronics are encouraging
- Example - ToA vs charge: Current FE ASIC (CLARO) + Kintex7, injected test pulse
- Expect to see benefits already in Run3 (3ns gating)
- We want to take the next step for Run4 (300ps photon ToA measurement)
- Further improvement with new sensors from Run5 (SiPM, MCP, other...)



## Notes:

- Channel-to-channel time variation is likely due to FPGA propagation delay and not a property of the CLARO.
- Can be compensated in the FPGA for Run3.
- Coarse timewalk correction can be applied in FPGA.

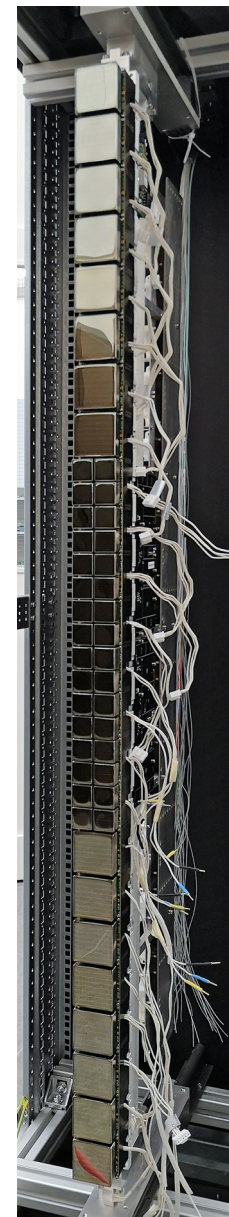
# Photon sensor module



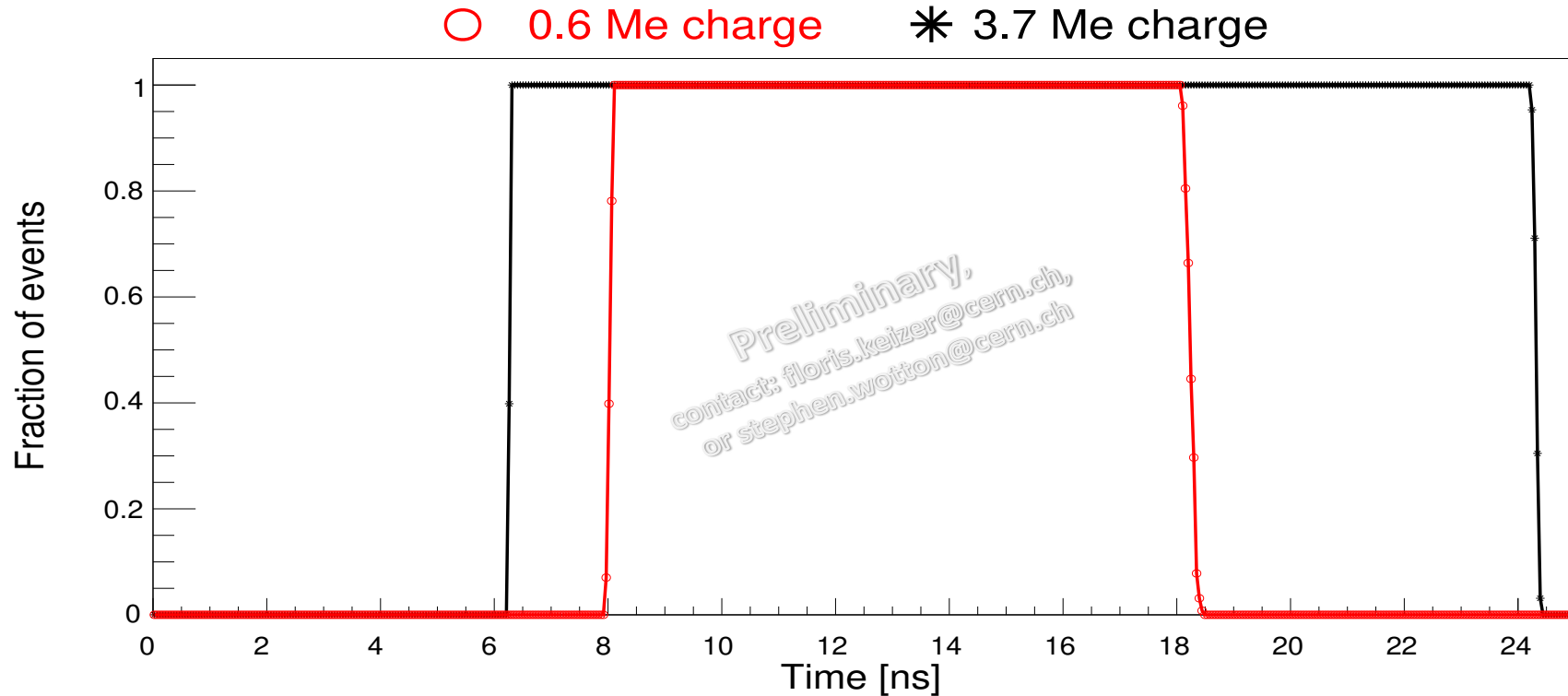
Possible Run4 concept

Minimise mechanical changes  
Re-engineer the FE electronics

- New FEB with FastIC
- New DB with picoTDC, IpGBT & VTRX+



# Timing measurements - Run3 module



- Measure ToA and ToT by using test pulse & scanning clock phase
- Measurement conditions similar to having TDC located on DB but use FPGA to capture data
- Single-ended signalling, 3 connectors, ~8cm PCB traces
- 48ps scan step size (using GBTX phase-programmable clock)
- ~70 channels firing at almost but not precisely the same time
- Leading edge 0-100% in two steps for 3.7 Me- input charge

# TDC considerations

- Run4 timing limited by MAPMT transit time spread (300ps FWHM)
- ToA and ToT required
- Precision requirements relatively modest (for Run4)
- Bandwidth requirement will be a strong driver of the system cost
- Need cost efficiency over wide range of occupancies
  - Low: cost optimisations possible by using 8-bit output mode to reduce the number of data links)
  - High: active channels limited by output bandwidth
- Radiation hardness
  - Validate by irradiations
- Compatibility of data format with LHCb readout to be addressed

# Readout considerations

- Data transport will use IpGBT with VTRX+
- Maximum picoTDC output bandwidth roughly the same as IpGBT 10Gbs FEC5 mode
- IO compatibility between picoTDC and IpGBT looks OK
  - Compatible electrical differential standards
  - Compatible IO rate
- Mismatch in bus width
  - picoTDC 32 differential outputs
  - IpGBT 28 differential inputs
- In high occupancy region, 64 channels will generate twice bandwidth limit of picoTDC
- In low occupancy region the bandwidth capability will be heavily underused in 32bit output mode
- Use different readout modularity in different occupancy regions

# Estimates of quantities for Run4

- Define occupancy regions
  - High: where limited by picoTDC bandwidth
  - Intermediate: if necessary
  - Low: where 8-bit picoTDC output mode sufficient

Readout “unit cell”				
	MAPMT (64ch)	CLARO/FastIC	TDC	lpGBT
High	1	8/2	2	2
Intermediate	1	8/2	1	1
Low	3	24/6	3	1

Quantities (excl. spares/prototypes)			
High/Low	3%/97%	5%/95%	10%/90%
FastIC	6176	6176	6176
picoTDC	3141	3242	3397
lpGBT	1171	1286	1544



# Summary

- Uses existing or nearly existing elements
- Looks possible to meet Run4 timing requirements
- Total number of links less than current system because of zero-suppression
- Component count mostly similar to existing system but may be more challenging in high occupancy region
- Radiation tolerance to be addressed (we may avoid use of FPGAs but need to evaluate FastIC & TDC)
- Power domains no more complex than now
- Heat management will need review
- Downstream data transport compatibility with LHCb needs to be addressed

# Quantities

Approximate production quantities			
High/Low	3%/97%	5%/95%	10%/90%
FastIC	6176	6176	6176
picoTDC	3141	3242	3397
lpGBT	1171	1286	1544

## Notes:

- Production requirements are intended only for forward planning estimates and should not be taken as a request at this stage.
- FastIC and picoTDC quantities not a strong function of assumptions about occupancy
- lpGBT caveat: the 32/28 IO mismatch not accounted for in the table. Might require significantly more lpGBT

Prototyping quantities	
FastIC (8 channel)	20 + 150 (See Note 1)
picoTDC (64 channel)	25

1) 20 early samples (packaged). We also have an interest in a small number of bare die. Additional 150 after validation of first samples.