BLM hardware changes in SPS during LS2

BE-BI-BL

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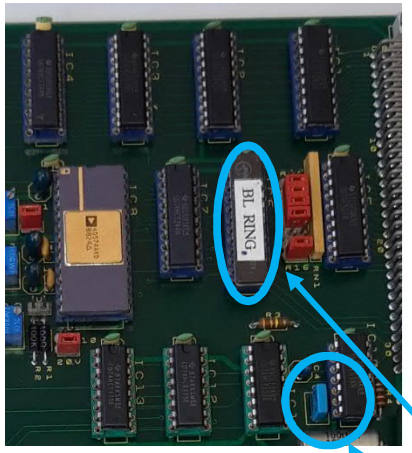
Motivation for the changes

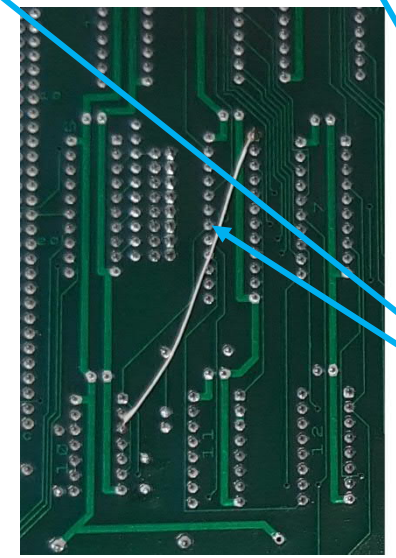
- Standard maintenance work during the long shutdown.
- New detectors or detector replacement requests by users.
- Harmonizing of the installation (SPS and LHC ICs type on single integrator card).
- Electronic was installed in the end of 90's (degradation of capacitors).
- VME timing problems during last run (latest CPU upgrade).
- Faster readout time (5 ms) of the system and introduction of the running sums.
- Not sufficient number of spare integrator cards.
- A lot of different versions of the integrator cards (capacitor gain, hardware dump, inhibit), that creates additional spare shortage.
- Large error between the low & high gain ratio and software factor (error in read value).

General maintenance works in the SPS BLM hardware to prepare for run 3

- All integrator cards have been collected and brought back to the workshop.
- All the BLM chassis have been checked for (not used) interface cards and removed.
- All cards have been cleaned in ultrasonic bath.
- Soldering of all cards verified and when needed re-soldered.
- Front-panels exchanged with new version due to problems with the plastic card handles (aging).
- For better ventilation all empty slots closed with blind front panel.
- Exchange of the filter of the Ventilator (still to be done).
- Production of 5 spare integrator cards.

Changes on the Integrator card (VME-bus)

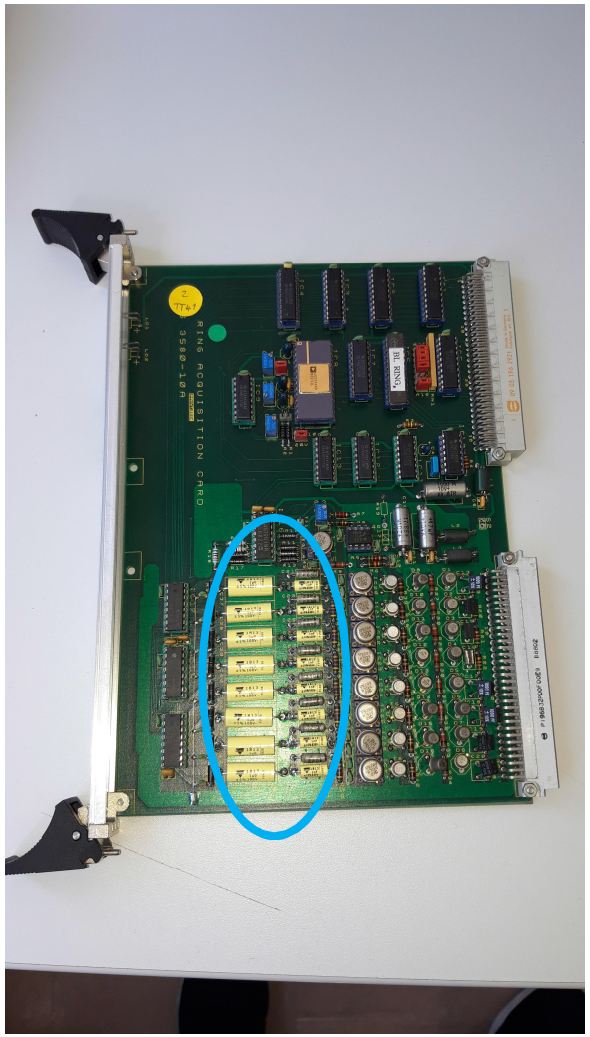




Due to timing problems (last run) of the VME bus and to decrease the read-out time, the following changes where carried out:

- All ICs have been exchanged and harmonized (several different families found, e.g. 74, 74LS, 74HCT, 74F, etc.)
- Version of the GAL verified, wrong behavior found while testing.
- Capacitor value (VME timing) harmonized on all cards.
- Jumper settings on all cards verified and harmonized.
- Verification if the PCB modification were performed on all cards. Was modified due to CPU exchange in 1999.

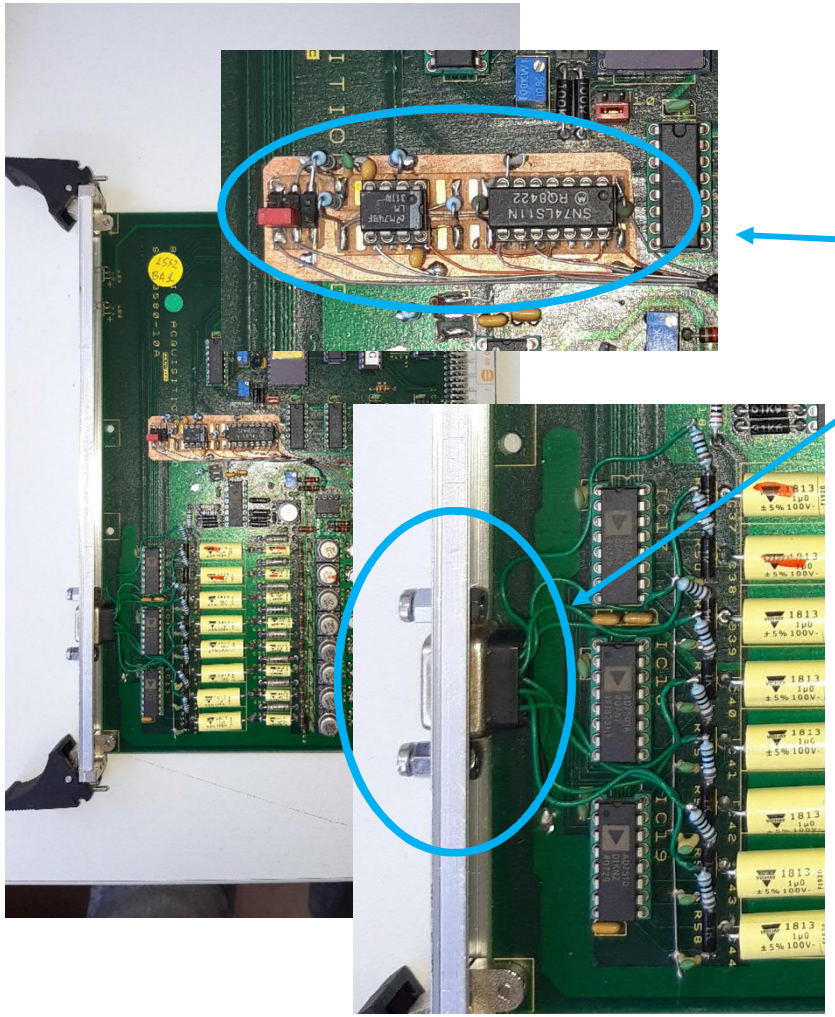
Changes on the Integrator card (Integrator)



Exchange of the all capacitors of the integrator, due to aging capacitors and combinations variety.

- Existing combinations, gain ratio and resulting error in respect to software ratio 200
  - 5.1nF/1uF -> Gain ratio = 196 (-2%)
  - 4.7nF/1uF -> Gain ratio = 213 (+6.5%)
  - 33nF/4.7uF -> Gain ratio = 142 (-29%)
  - 5.1nF/9.4uF -> Gain ratio = 1843 (+817%)
  - 33nF/9.4uF -> Gain ratio = 285 (+42.5%)
  - 38nF/9.4uF -> Gain ratio = 247 (+23.4%)
- Future: two combinations and software ratio:
  - 1nF / 1uF -> Gain ratio = 1000 (0%)
  - 10nF /10uF -> Gain ratio = 1000 (0%)
- Combination reduced from 6 to 2 types
  - improvement of spare situation

Modification of integrator cards (Functions)



- 3 different version of integrator cards are used with different gain combinations.
  - Standard integrator -> ring and low loss areas like transfer lines.
  - Inhibit integrator (INH) -> dump region (LSS5).
  - Hardware dump (HWD) -> high radiation areas where faster dump response is needed.
- 12 different integrator cards versions existing
  - with 14 spare cards available.
- Reduced to 4 Integrator versions
  - V1: 1nF/1uF: 57 inst. -> 11 spares
  - V2: 1nF/1uF HWD: 3 inst. -> 2 spares
  - V3: 1nF/1uF HWD, INH: 1 inst. -> 2 spares
  - V4: 10nF/10uF HWD: 9 inst. -> 5 spares

Changes in hardware related variables and function in the software layer

- Calibration factor Gy/bit (SPS type BLM detector)
  - 3.6 E-05 C/Gy (Latest adaption in 2011 by Gianluigi)
  - Resulting a conversion factor 1.36E-04 Gy/bit for 1uF/1nF
    - Wrong factors (1.1E-4, 1.104E-4, 1.14E-4, 1.3E-4) changes to 1.36E-4
  - Resulting a conversion factor 1.36E-03 Gy/bit for 10uF/10nF
    - Wrong factors (1.072E-3, 1.27E-4, 1.3E-3, 1.3E-4) changes to 1.36E-3
- Calibration factor Gy/bit (LHC type BLM detector)
  - 5.9 E-05 C/Gy (SPS IC + 64%)
  - Resulting a conversion factor 2.230E-04 Gy/bit for 1uF/1nF
    - Wrong factors (1.3E-4) changes to 2.2302E-4
- Re-use of current pulse injection on the integrator input
  - Test function to verify integrator functionality and eventually threshold
  - For the moment not implemented and test
- Software option in the BLMI FECs (Transfer lines) to increase integration time
  - Allows to verify detector connectivity in the transfer lines

Improvement due to modification of integrator cards

- More spare cards available.
- Version can also be exchanged.
- V2 and V3 can also be used as V1.
- V3 can also be used as V2.
- All cards were tested and validated in the test bench.
- Verification of all integrator gains and linear gains form 8 to 48 hours with automatic script.
- Verification of the most used gain settings with current source.
- Additional test functions for better system commissioning and testing.

Tunnel installation changes during LS2

- LSS1: Removal and displacement of BLM due to dump replacement.
- LSS1: Installation of additional BLM on the TPID.
- LSS2: Displacement of BLM due to ZS exchange.
- LSS5: Installation and displacement of BLMs due to dump installation.
- LSS6: Installation of additional BLM on the TPSG.
- TI2: Installation of additional BLM at the PMI2.
- TI2: Displacement of BLM due to collimator displacement.
- TI8: Displacement of BLM due to collimator displacement.
- TDC2: Installation of additional BLM due to cable exchange.
- Others: Removal and re-installation due to maintenance work on the machine.

Thanks a lot!

Any question?