HCCStar Schedule Update
July 9 2020

Milestones

- Complete essential design revisions by end of August
- Complete SEE simulations by end of September
- FDR possible in mid-October

Task	Estimate	Uncertainty	End Date
Replace LCB decoder with Verilog version	5	3	8-Aug-20
-- Adjust register implementation	5	3	13-Aug-20
-- Rewrite LCB passthru in Verilog	0	0	13-Aug-20
-- Rewrite LCB 40 MHz clock recovery in Verilog	0	0	13-Aug-20
Switch to synchronous resets	14	7	27-Aug-20
Update HPR module (triplicated)?	0	0	27-Aug-20
Verification stripped down verilog for 640 MHz simulation	3	1	30-Aug-20
SEE simulations	30	14	29-Sep-20
Final checks	14	7	13-Oct-20
PNR	14	5	27-Oct-20
Sign-off	7	2	3-Nov-20
Contingency (add uncertainties in quadrature)			21-Nov-20
Contingency (add uncertainties linearly)			15-Dec-20

Design changes for preproduction

- Three major issues with prototype design
  - ✓640 Mbps output
  - ✓Logic reset for HCCStar event counters
  - SEE issues with control structures prevented us from seeing potential issues
- Challenges with estimates from December 2019
  - Multiple iterations take time
    - Parts of design have to grow to implement triplication as SEE mitigation
    - Limited space available in fixed area allowed, design adjustments have to be made
  - Slow down from COVID-19 crisis
  - AMAC design in parallel, FDR on 24 July

Extra pre-production submission?

- Strongly prefer NOT to do this option of ordering AMAC + HCCStar in September, then again after SEE completed.
- Background: the second batch of pre-production powerboards for the barrel needs at least 750 AMAC chips. LBNL needs a date when AMAC preproduction chips will be available to plan contracts with companies for loading the powerboards.
    1. There have already been a lot of changes since the prototype, there is too high a risk of having a HCCStar chip that doesn't work. Less haste, more speed.
    2. The final checks and PNR to be done will take a month starting September (I assume Nandor is working on AMAC in August, yes? No?), so earliest submission is October.
    3. There is only money in the budget for one pre-production submission, US pays entire cost of $412,460. An extra pre-production submission would require an extra $412,460 on top of delays to rest of schedule.
    4. There are 2 months in August and September for Paul Keener to work on the essential design+SEE simulations. Even without the SEE simulations, some of this work needs to happen for a functional chip.
- The discussions last week led to our plan to have a FDR in mid-October with submission for HCCStar in November.
    - P6 needs to be updated, where currently the AMAC chips are available October 16th, assuming vendor fabrication started July 10.

SEE Issues

- Issues were seen at irradiations in TRIUMF and Louvain
  - Registers
  - FIFO control structures
- The SEE issues with the control structures prevented us from seeing potential issues in other parts of the chip
- It is clear that some parts of the design will have to grow to implement triplication as SEE mitigation
  - There is limited space available in the fixed area allowed for HCC, so design adjustments will have to be made

SEE Issues (2)

- Exercise engineering judgement in what needs to be protected
  - Control structures that don't "naturally" reset
  - Portions of data that effect control (eg, end of data markers)
  - Registers and register control
  - Command protocol decoding
  - Resets
- Back it up with simulations
  - These are non-trivial, particularly at the multi-module level
  - Hard to define what "non-working" conditions are acceptable
    - Implement mini-daq ???

SEE – What needs to be done?

- Verify triplication of dual-clock and synchronous FIFO control structures
- Replace LCB protocol decoder with Pedro's Verilog version
  - Knock-on effects on registers
- Evaluate existing triplication through the design
- Replace asynchronous resets with synchronous resets throughout

Things to consider (skipped in schedule)

- Rewrite 40 MHz clock recovery in Verilog to triplicate it
  - Outside effort may be available
- Rewrite LCB passthrough in Verilog to triplicate it
  - Only affects ABCs
  - Probably not worth it – rather use the area elsewhere
- Use triplicated HPR module
  - Module exists
  - Area and integration effort are concerns
- How close to bandwidth edge are we?
  - There are some interesting options here that would require some study but could simply the design and improve performance