Readout electronics update 21-July-2020

HV-Mux: production order in progress with STFC and Cambridge in the UK, vendor says order now will have delivery in Nov-Dec 2020. Have 1500 from prototype batch on hand.

Powerboard: pre-production design (v3.1) complete and approved by ATLAS

- Started producing last batch of 45 v3.0c prototype boards June 1, progress will be slow due to low occupancy at lab
- Preparing order of 250 flexes for v3.1 with EPEC

ABCStar: pre-production wafers back from vendor May 2020, wafer probing in progress

AMAC: FDR July 24

- Add current measurement of AMAC itself on LinPOL input
- Review SEE simulation code
- Prepare for FDR, revise/update specifications document.

HCCStar:

- On hold until after AMAC FDR - Implement updates to PacketBuilder, work on SEE mitigations,
- In progress (Jeff Dandoy, Bruce Gallop, Matt Warren) - Validate HCCStarV0 hardware with realistic physics mode data
- Proof of principle done - (Paul Keener, Nandor Dressnandt) - Demonstrate 640 MHz clock path analog simulation
- This week (Evelyn Thomson) - Revise submission schedule for HCCStarV1.

Coils: production order placed on Feb 21 2020, first batch of 100 coils arrived May 20, irradiation tests in progress, starting to measure dimensions of production coil samples with a Digital Microscope. Also starting electrical QA & QC measurements.

HCCStar Schedule

Milestones

- Complete essential design revisions by end of August
- Complete SEE simulations by end of September
- FDR possible in mid-October

Task	Estimate	Uncertainty	End Date
Replace LCB decoder with Verilog version	5	3	8-Aug-20
-- Adjust register implementation	5	3	13-Aug-20
-- Rewrite LCB passthru in Verilog	0	0	13-Aug-20
-- Rewrite LCB 40 MHz clock recovery in Verilog	0	0	13-Aug-20
Switch to synchronous resets	14	7	27-Aug-20
Update HPR module (triplicated)?	0	0	27-Aug-20
Verification stripped down verilog for 640 MHz simulation	3	1	30-Aug-20
SEE simulations	30	14	29-Sep-20
Final checks	14	7	13-Oct-20
PNR	14	5	27-Oct-20
Sign-off	7	2	3-Nov-20
Contingency (add uncertainties in quadrature)			21-Nov-20
Contingency (add uncertainties linearly)			15-Dec-20

Design changes for preproduction

- Three major issues with prototype design
  - ✓640 Mbps output
  - ✓Logic reset for HCCStar event counters
  - SEE issues with control structures prevented us from seeing potential issues
- Challenges with estimates from December 2019
  - Multiple iterations take time
    - Parts of design have to grow to implement triplication as SEE mitigation
    - Limited space available in fixed area allowed, design adjustments have to be made
  - Slow down from COVID-19 crisis
  - AMAC design in parallel, FDR on 24 July

HCCStar schedules

P6 as of BCP-038 in June 2020				
RE320670	Vendor Effort for Pre-Production for HCC and AMAC Wafers	40	**10-Jul-20**	**4-Sep-20**
RE320760	RECEIVE: Wafers from Fabrication Vendor	0		4-Sep-20
RE320770	Test Pre-Production HCCstar Wafers with Probe Card	20	4-Sep-20	2-Oct-20
RE320780	Wait for First Wafer to Complete Testing Before Sending to Sawing Vendor	5	4-Sep-20	11-Sep-20
RE320790	Send First Tested Wafer to Sawing Vendor	1	11-Sep-20	14-Sep-20
RE320810	Vendor Effort: Saw Wafer	20	15-Sep-20	13-Oct-20
RE320820	RECEIVE: Chips from Sawed First Wafer	0		13-Oct-20
RE320850	Ship Chips to Hybrid/Module Assembly/Test Sites	3	13-Oct-20	16-Oct-20
RE320870A	AVAIL: HCC Chips at BNL Hybrid Assembly Test Site	0		**16-Oct-20**
RE320880A	AVAIL: HCC Chips at LBNL Hybrid Assembly Test Site	0		16-Oct-20
RE320890A	AVAIL: HCC Chips at UCSC Hybrid Assembly Test Site	0		16-Oct-20

Schedule with FDR in October 2020				
RE320670	Vendor Effort for Pre-Production for HCC and AMAC Wafers	40	**20-Nov-20**	**15-Jan-21**
RE320760	RECEIVE: Wafers from Fabrication Vendor	0		15-Jan-21
RE320770	Test Pre-Production HCCstar Wafers with Probe Card	20	15-Jan-21	12-Feb-21
RE320780	Wait for First Wafer to Complete Testing Before Sending to Sawing Vendor	5	15-Jan-21	22-Jan-21
RE320790	Send First Tested Wafer to Sawing Vendor	1	22-Jan-21	25-Jan-21
RE320810	Vendor Effort: Saw Wafer	20	26-Jan-21	23-Feb-21
RE320820	RECEIVE: Chips from Sawed First Wafer	0		23-Feb-21
RE320850	Ship Chips to Hybrid/Module Assembly/Test Sites	3	23-Feb-21	26-Feb-21
RE320870A	AVAIL: HCC Chips at BNL Hybrid Assembly Test Site	0		**26-Feb-21**
RE320880A	AVAIL: HCC Chips at LBNL Hybrid Assembly Test Site	0		26-Feb-21
RE320890A	AVAIL: HCC Chips at UCSC Hybrid Assembly Test Site	0		26-Feb-21