RD50-MPW2 active pixel matrix measurements

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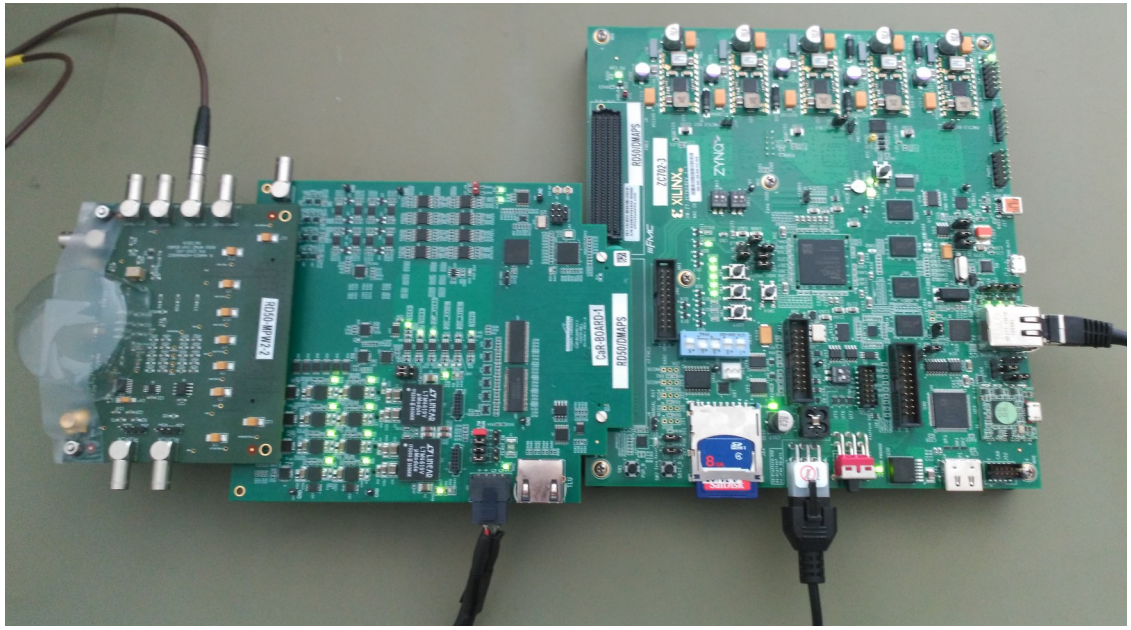
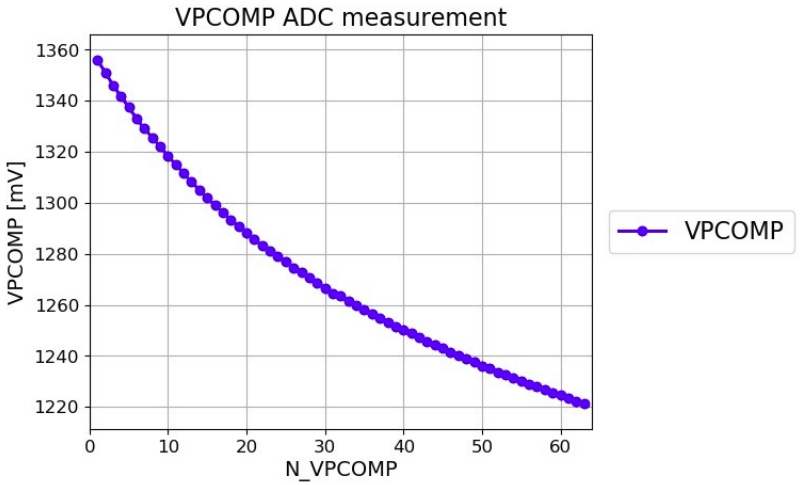
RD50-MPW2 active pixel matrix measurements setup

- Three RD50-MPW2 chip boards used:
  - RD50-MPW2-2: RD50-MPW2 W10 device bonded (1.9 kΩ·cm). Current consumption, ToT measurements and ADC/ABUFF measurements.
  - RD50-MPW2-1: RD50-MPW2 W7 device bonded (0.5-1.1 kΩ·cm). bonded (1.9 kΩ·cm). ADC/ABUFF measurements.
  - RD50-MPW2-3: RD50-MPW2 W14 device bonded (> 2 kΩ·cm). bonded (1.9 kΩ·cm). ADC/ABUFF measurements.
- FMC CaR board, ZC702 board and own firmware/software used.
  - VHDL blocks for RD50-MPW2 stream data generation, analog buffer control, test pulse generation and comparator pulse readout.
  - Linux running in Zynq ARM (from SD card).
  - Python scripts and UIO driver/I2C driver for controlling the system.

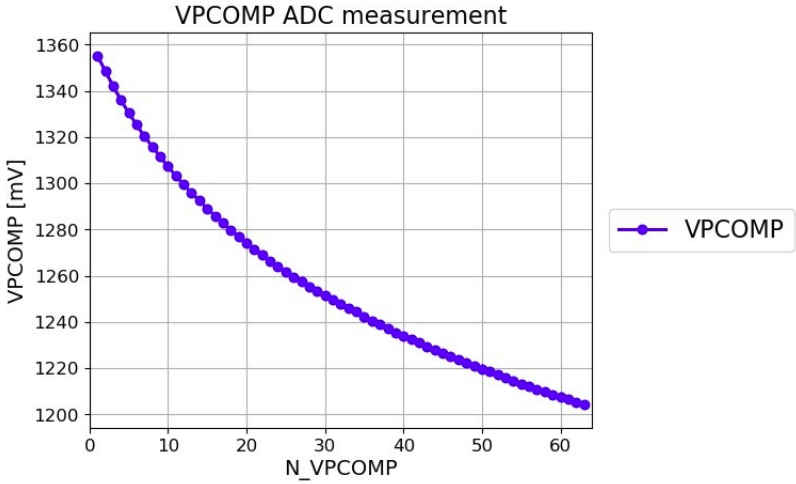


RD50-MPW2 bias voltages measurements

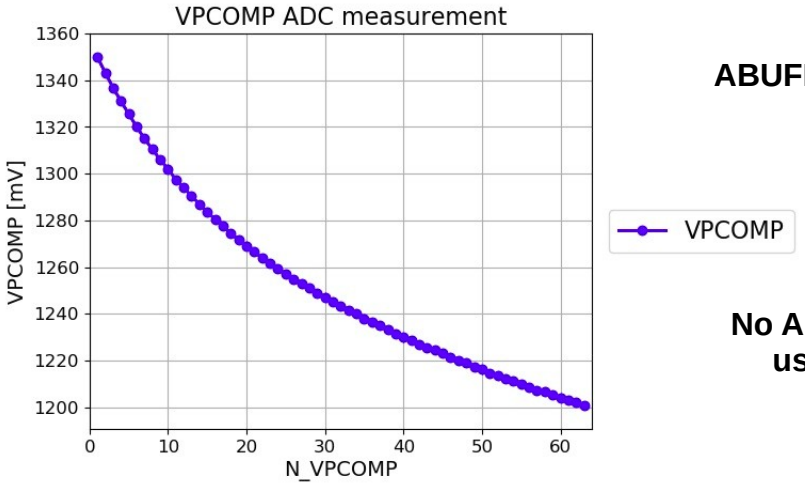
- Measurement details: **VPCOMP (sets current of comparators).**
  - Measurement with on-board **ADC**.
  - Bias register programmed from 0 to 63.



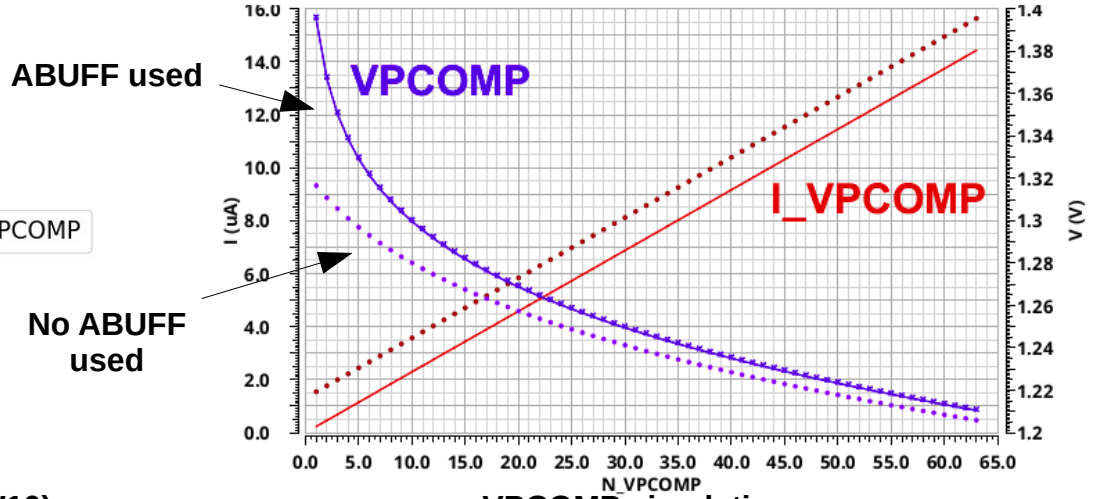
VPCOMP ADC measurement (RD50-MPW2-1 W7).



VPCOMP ADC measurement (RD50-MPW2-3 W14).



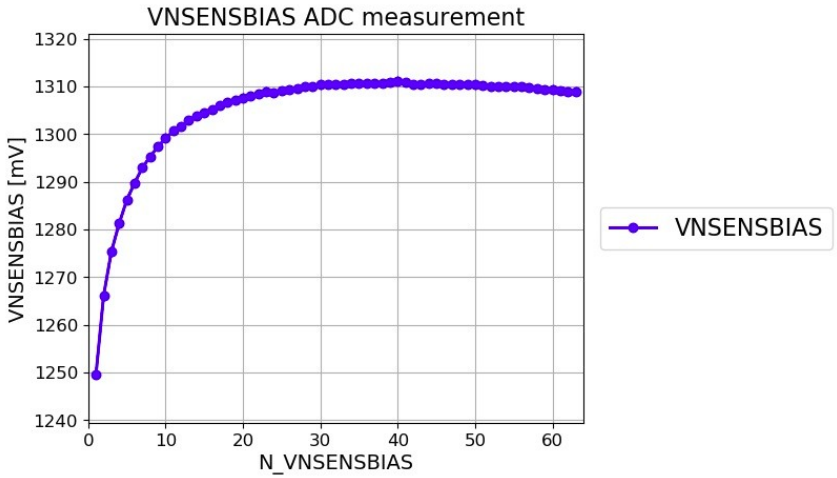
VPCOMP ADC measurement (RD50-MPW2-2 W10).



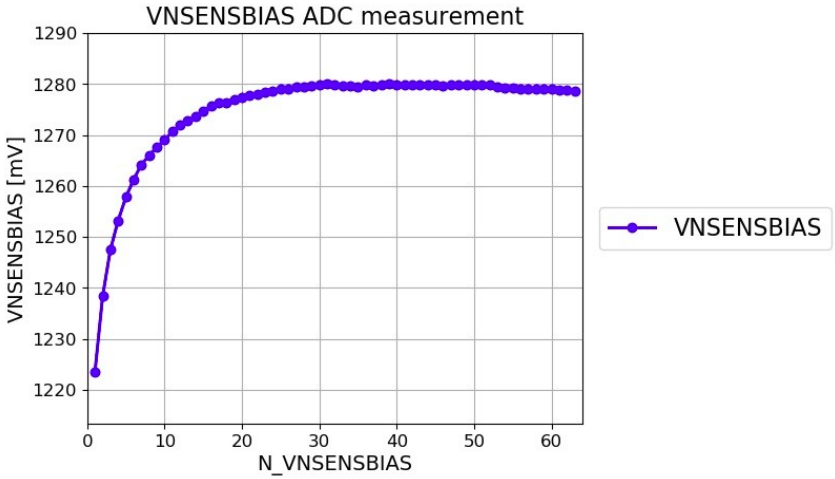
VPCOMP simulation

RD50-MPW2 bias voltages measurements

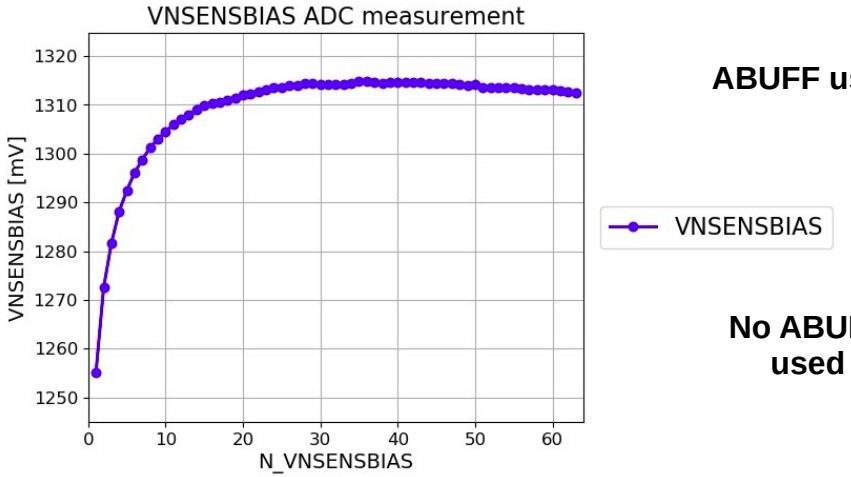
- Measurement details: **VNSENSBIAS (bias transistors as the R for DNWELL).**
  - Measurement with on-board **ADC**.
  - Bias register programmed from 0 to 63.



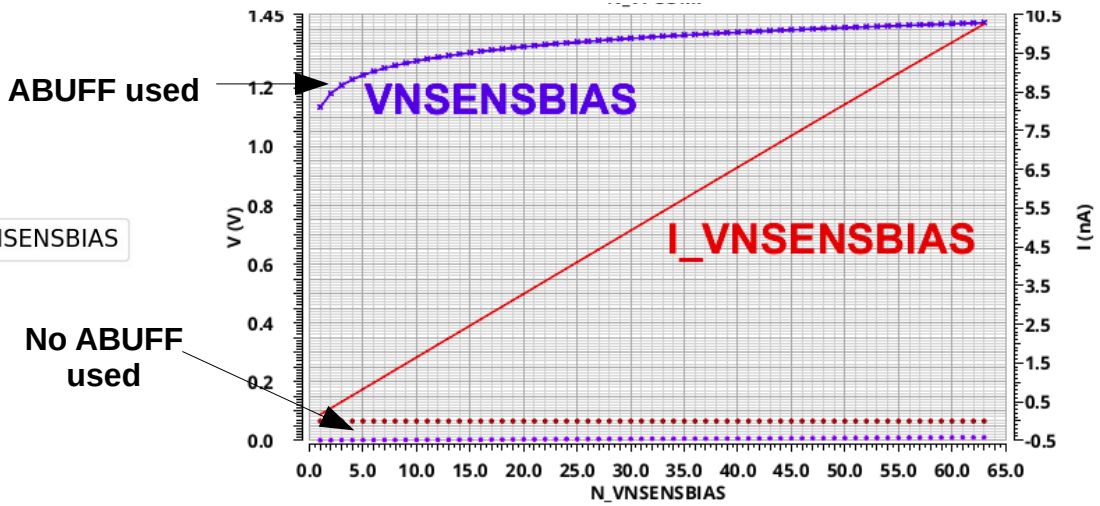
VNSENSBIAS ADC measurement (RD50-MPW2-1 W7).



VNSENSBIAS ADC measurement (RD50-MPW2-3 W14).



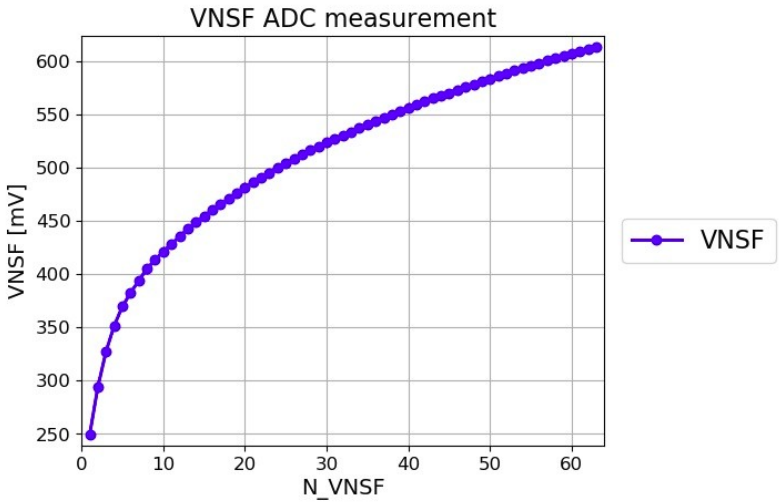
VNSENSBIAS ADC measurement (RD50-MPW2-2 W10).



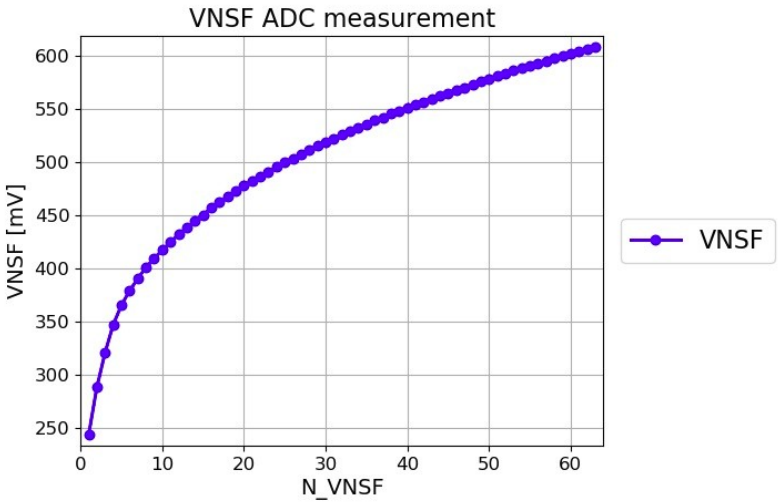
VNSENSBIAS simulation

RD50-MPW2 bias voltages measurements

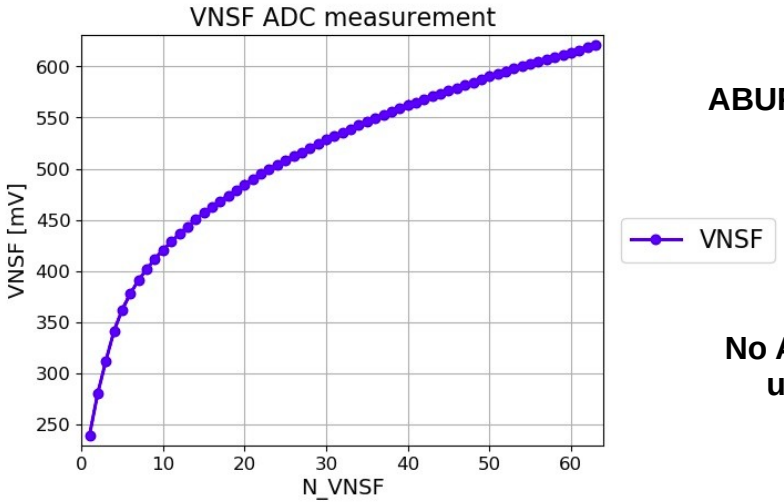
- Measurement details: **VNSF (sets current of source followers).**
  - Measurement with on-board **ADC**.
  - Bias register programmed from 0 to 63.



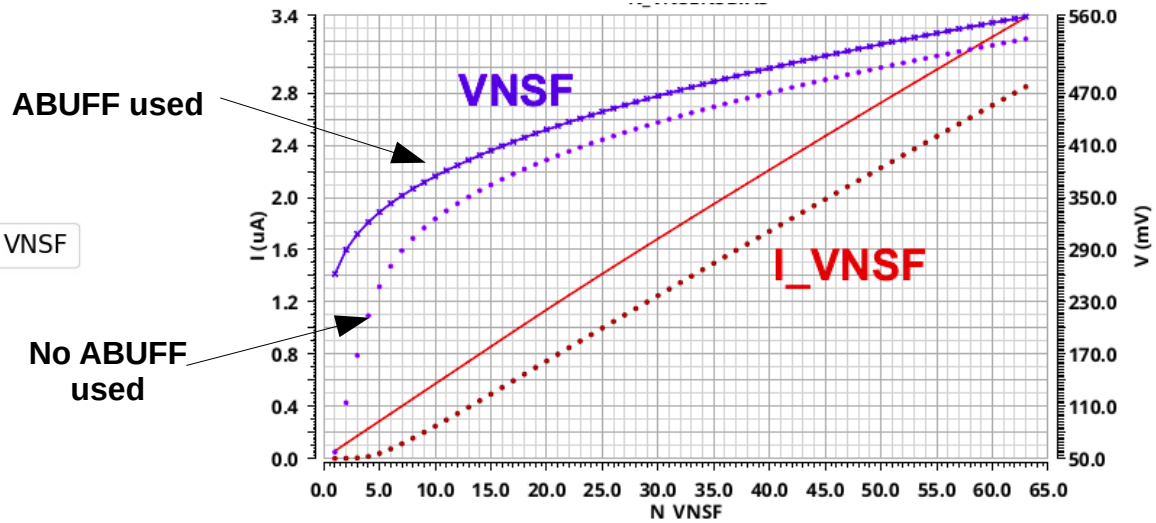
VNSF ADC measurement (RD50-MPW2-1 W7).



VNSF ADC measurement (RD50-MPW2-3 W14).



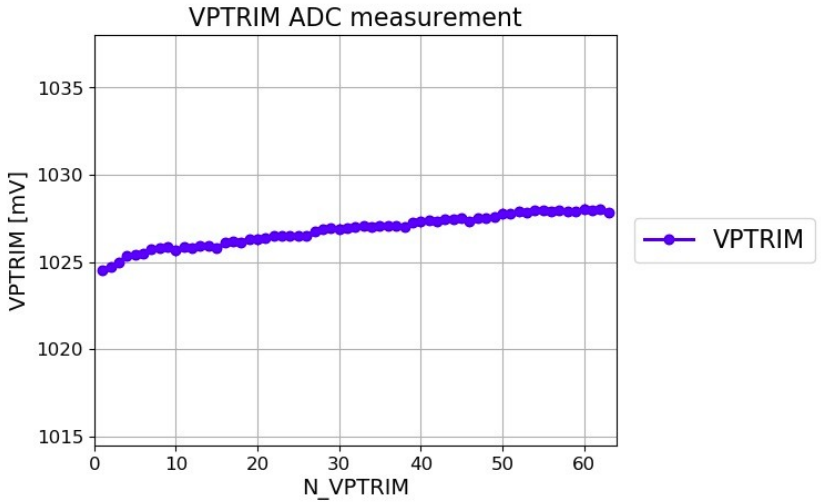
VNSF ADC measurement (RD50-MPW2-2 W10).



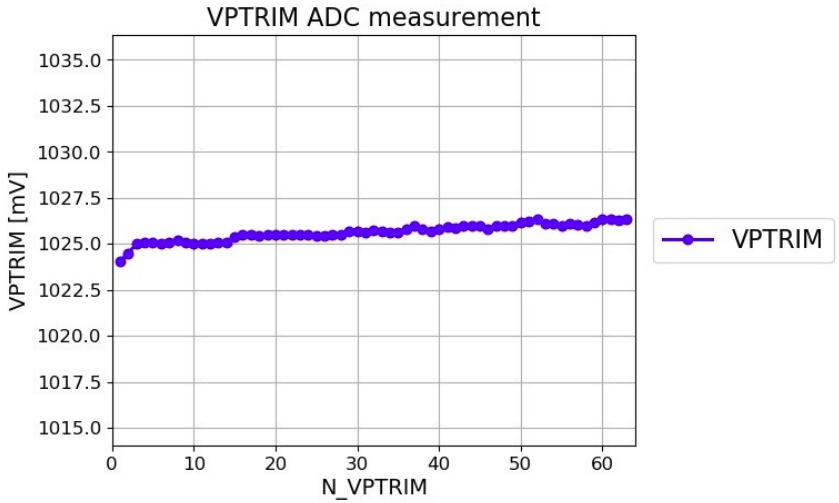
VNSF simulation

RD50-MPW2 bias voltages measurements

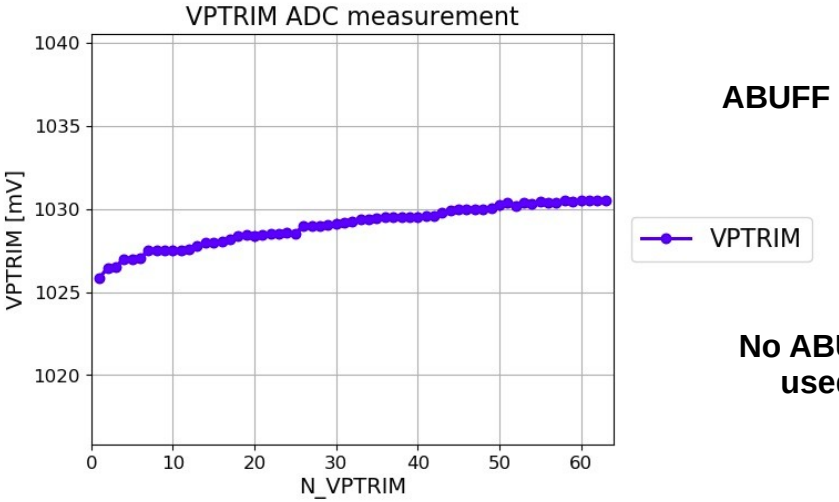
- Measurement details: **VPTRIM (sets current of trimming DACs).**
  - Measurement with on-board **ADC**.
  - Bias register programmed from 0 to 63.



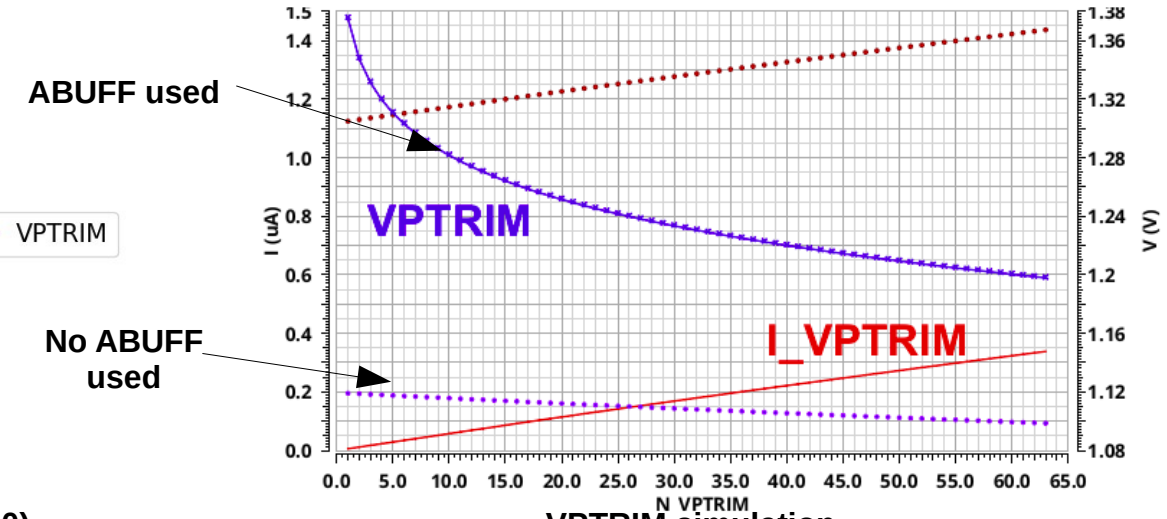
VPTRIM ADC measurement (RD50-MPW2-1 W7).



VPTRIM ADC measurement (RD50-MPW2-3 W14).



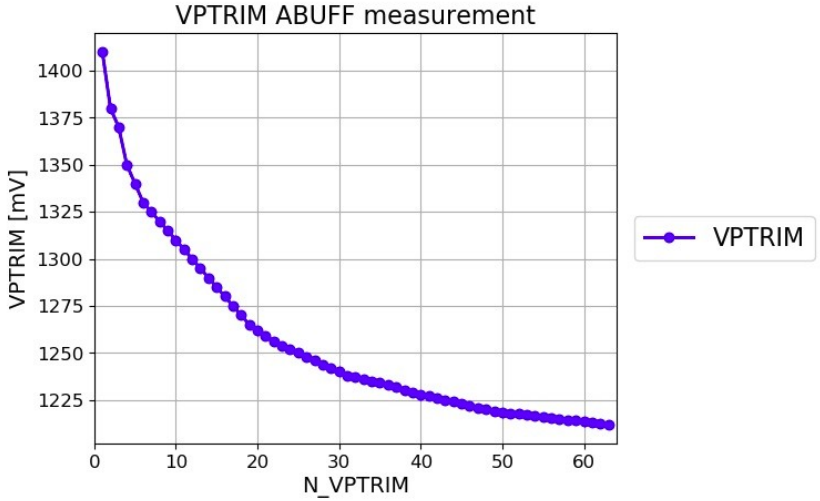
VPTRIM ADC measurement (RD50-MPW2-2 W10).



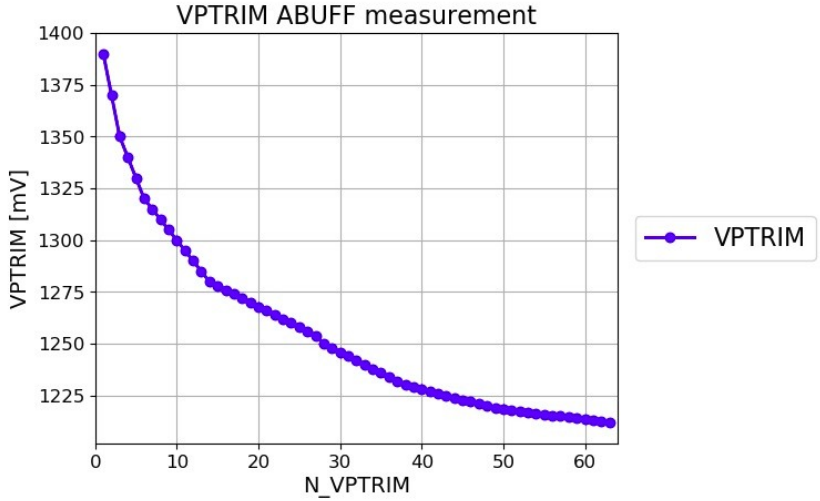
VPTRIM simulation

RD50-MPW2 bias voltages measurements

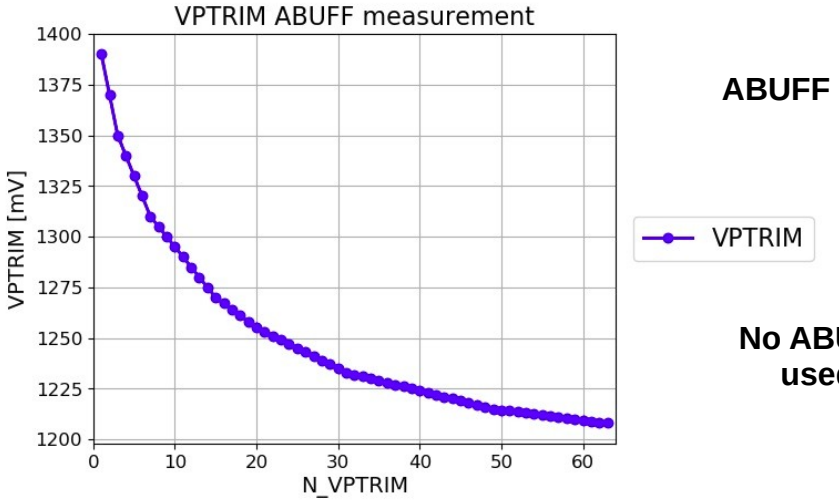
- Measurement details: **VPTRIM (sets current of trimming DACs).**
  - Measurement from **ABUFF output with scope**.
  - Bias register programmed from 0 to 63.



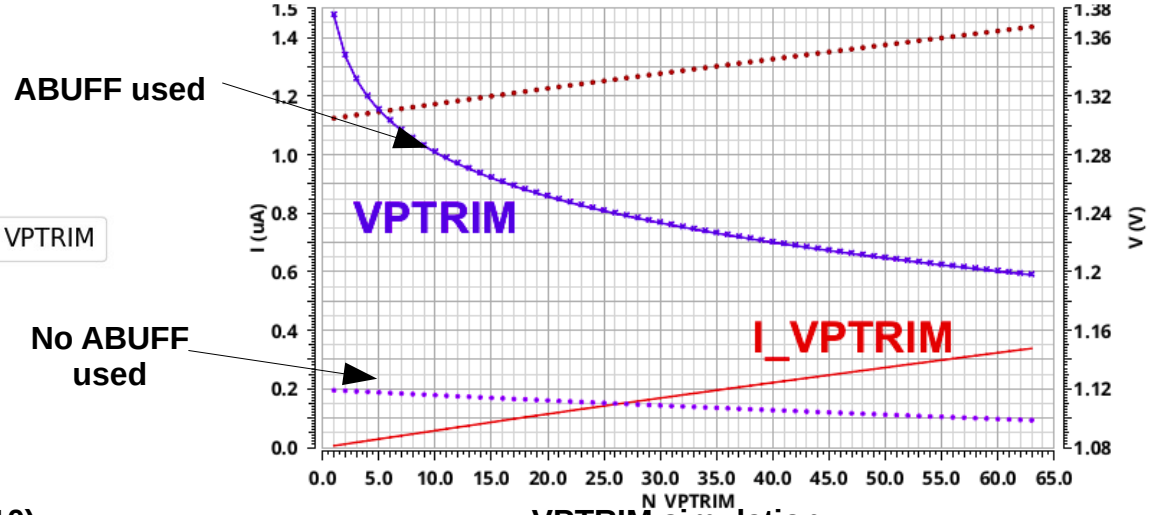
VPTRIM ABUFF measurement (RD50-MPW2-1 W7).



VPTRIM ABUFF measurement (RD50-MPW2-3 W14).



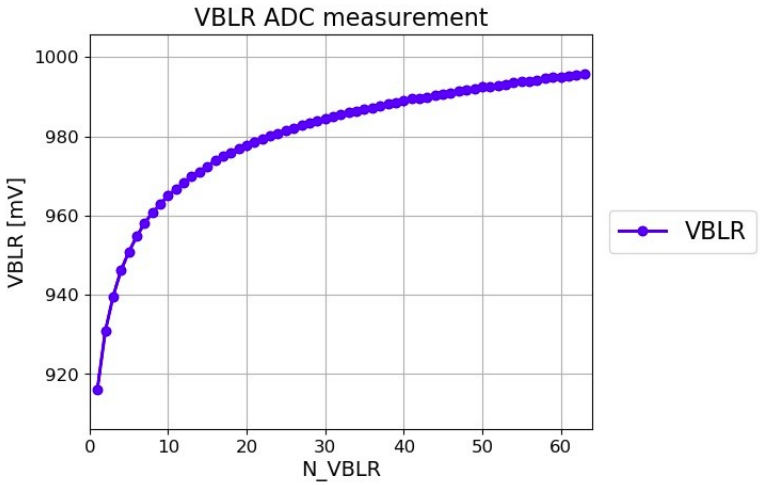
VPTRIM ABUFF measurement (RD50-MPW2-2 W10).



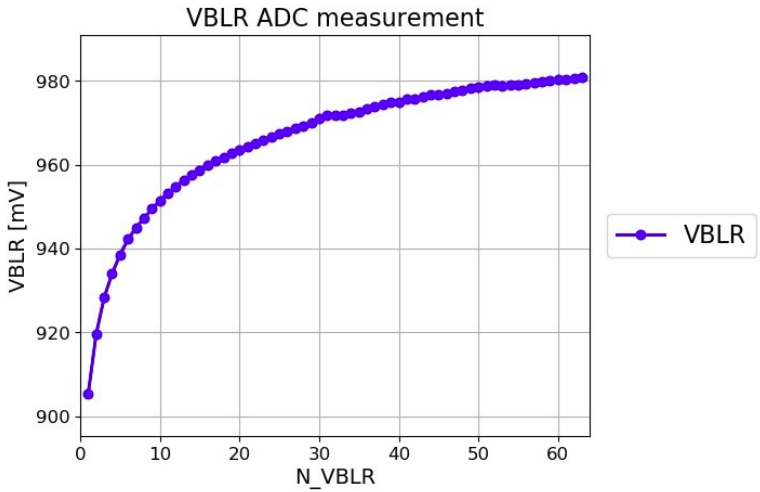
VPTRIM simulation

RD50-MPW2 bias voltages measurements

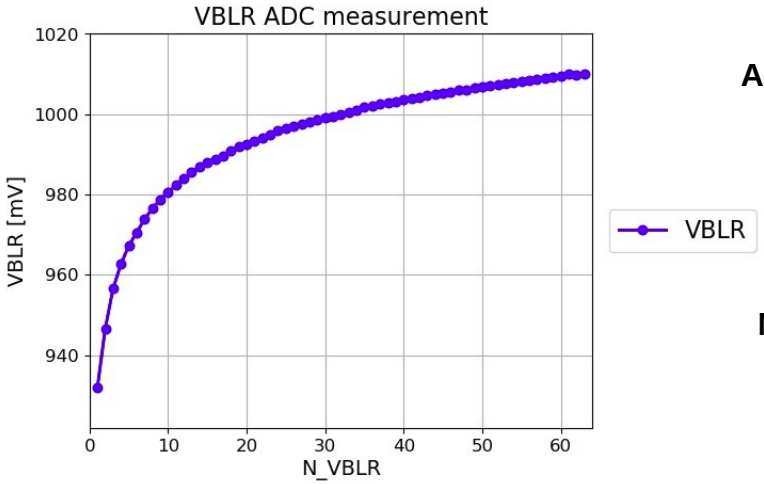
- Measurement details: **VBLR (bias transistors as the R in HP-filters).**
  - Measurement with on-board **ADC**.
  - Bias register programmed from 0 to 63.



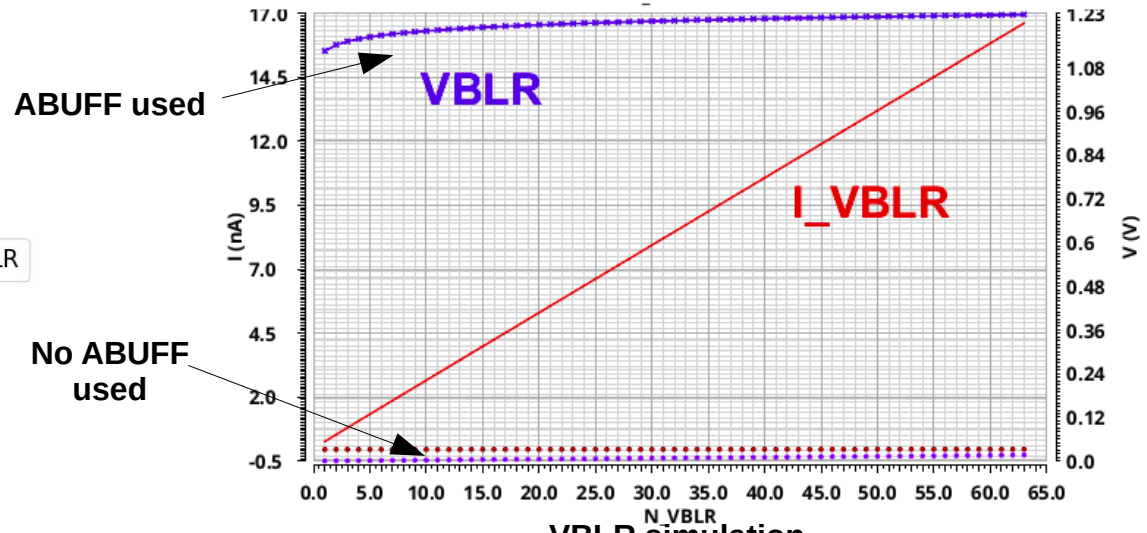
VBLR ADC measurement (RD50-MPW2-1 W7).



VBLR ADC measurement (RD50-MPW2-3 W14).



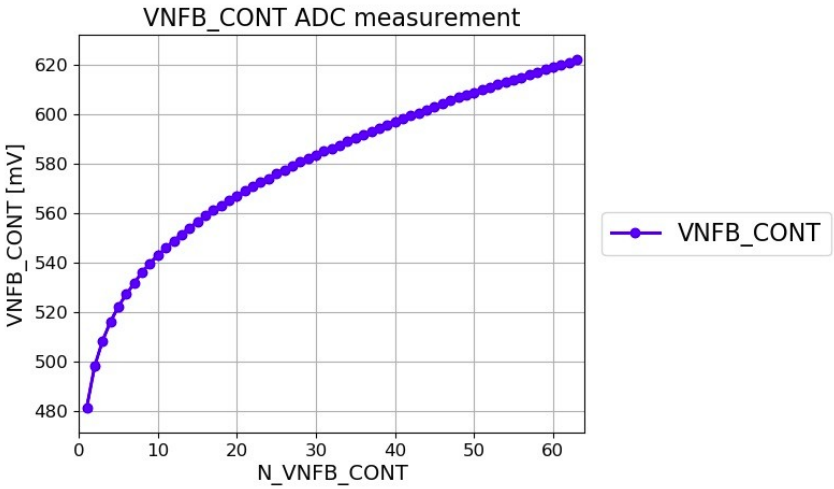
VBLR ADC measurement (RD50-MPW2-2 W10).



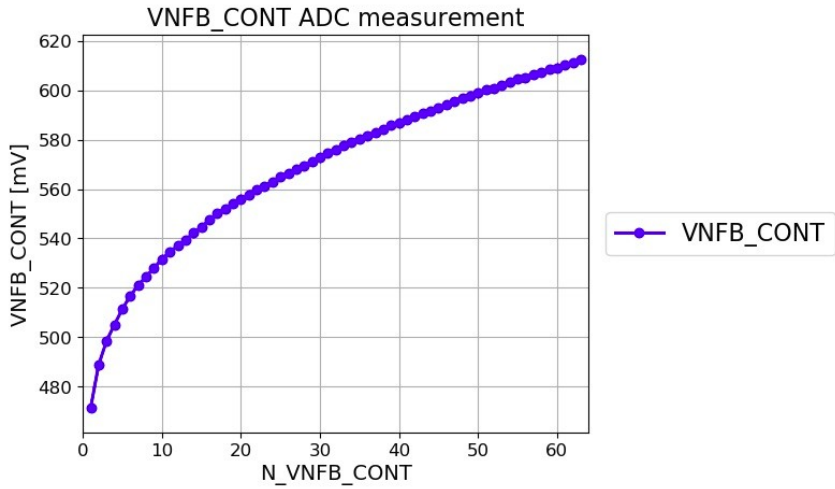
VBLR simulation

RD50-MPW2 bias voltages measurements

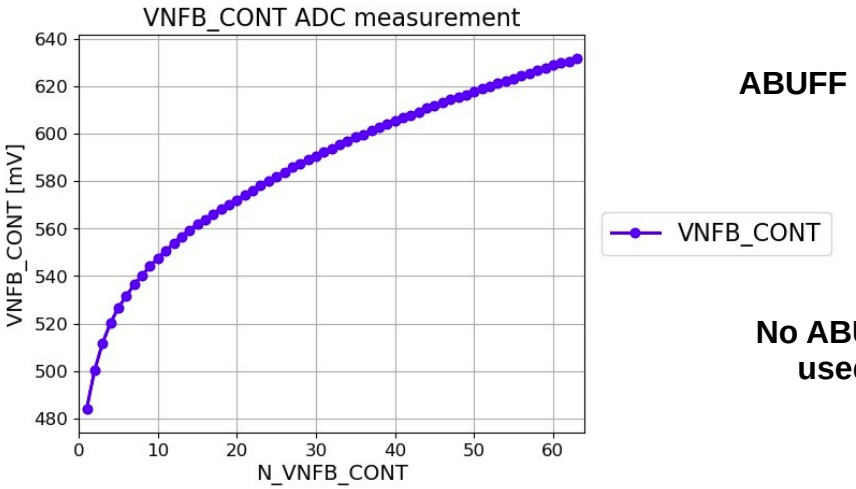
- Measurement details: **VNFB_CONT (sets I_{FB} of continuous-reset pixels).**
  - Measurement with on-board **ADC**.
  - Bias register programmed from 0 to 63.



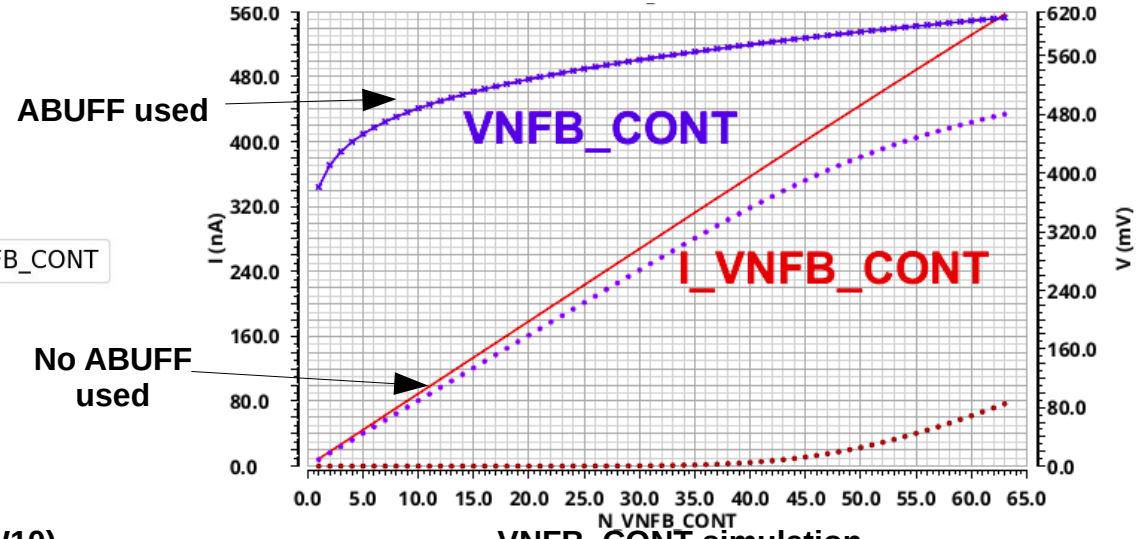
VNFB_CONT ADC measurement (RD50-MPW2-1 W7).



VNFB_CONT ADC measurement (RD50-MPW2-3 W14).



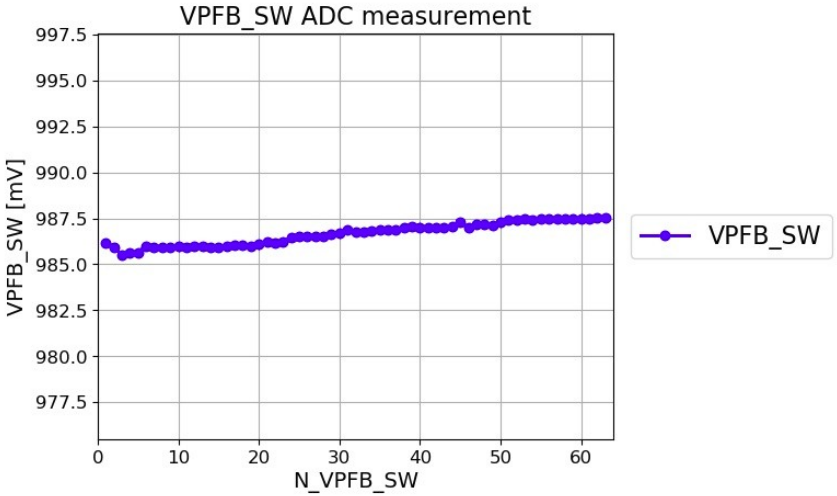
VNFB_CONT ADC measurement (RD50-MPW2-2 W10).



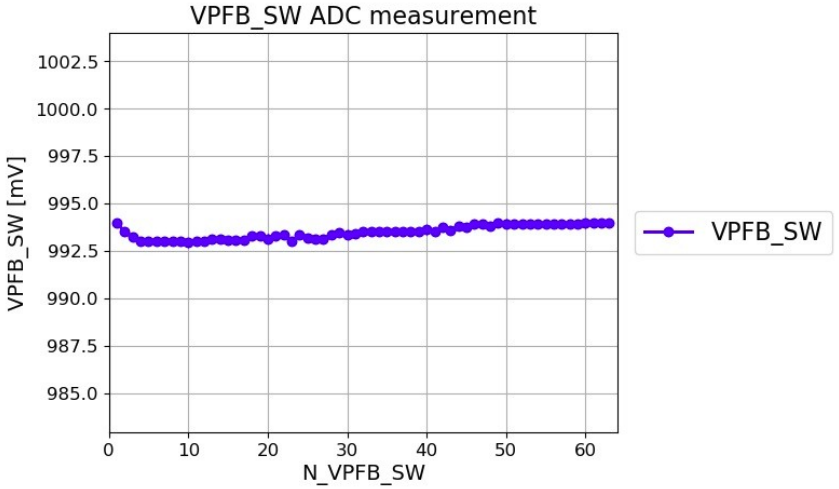
VNFB_CONT simulation

RD50-MPW2 bias voltages measurements

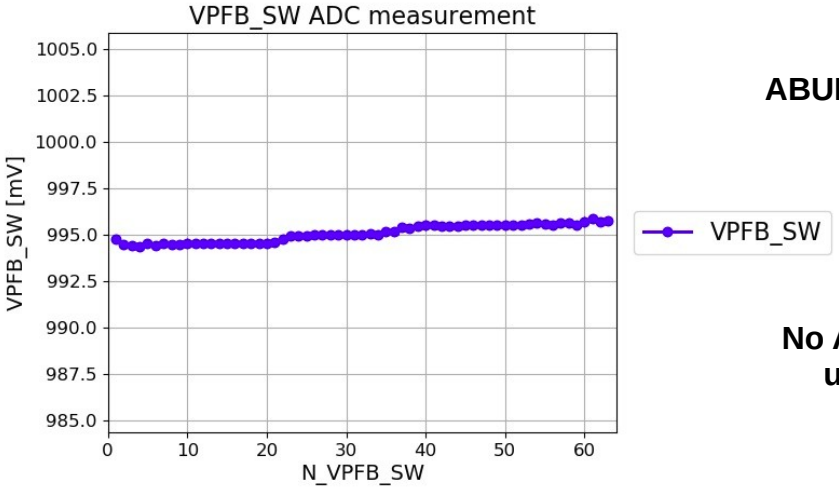
- Measurement details: **VPFB_SW (sets I_{FB} of switched-reset pixels).**
  - Measurement with on-board **ADC**.
  - Bias register programmed from 0 to 63.



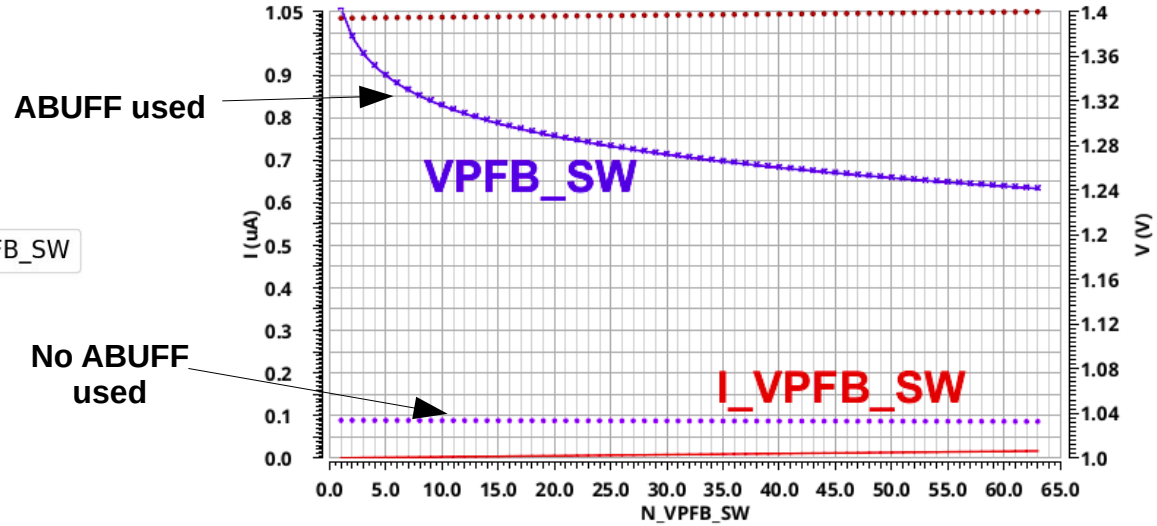
VPFB_SW ADC measurement (RD50-MPW2-1 W7).



VPFB_SW ADC measurement (RD50-MPW2-3 W14).



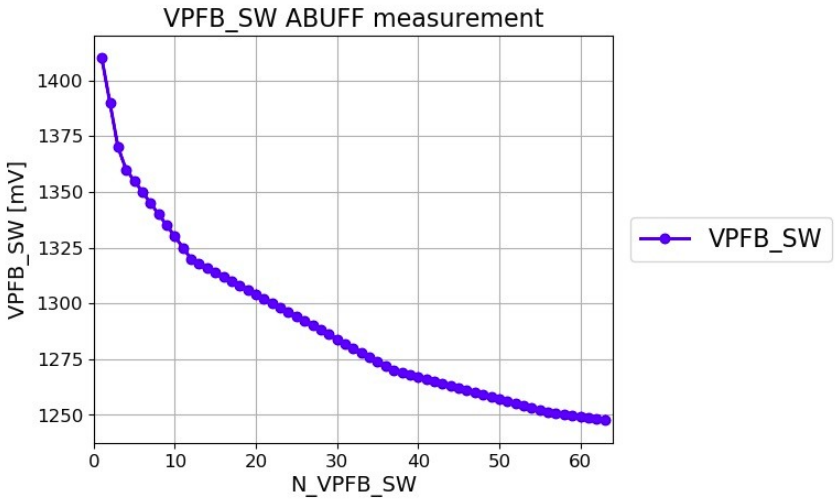
VPFB_SW ADC measurement (RD50-MPW2-2 W10).



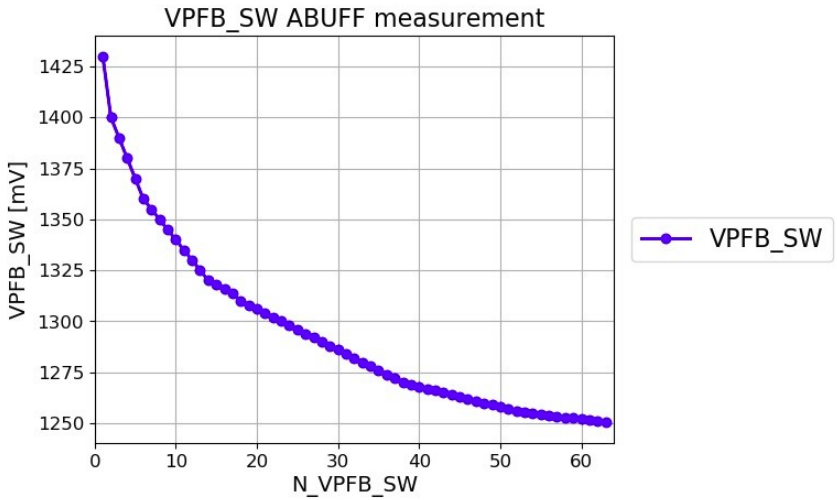
VPFB_SW simulation

RD50-MPW2 bias voltages measurements

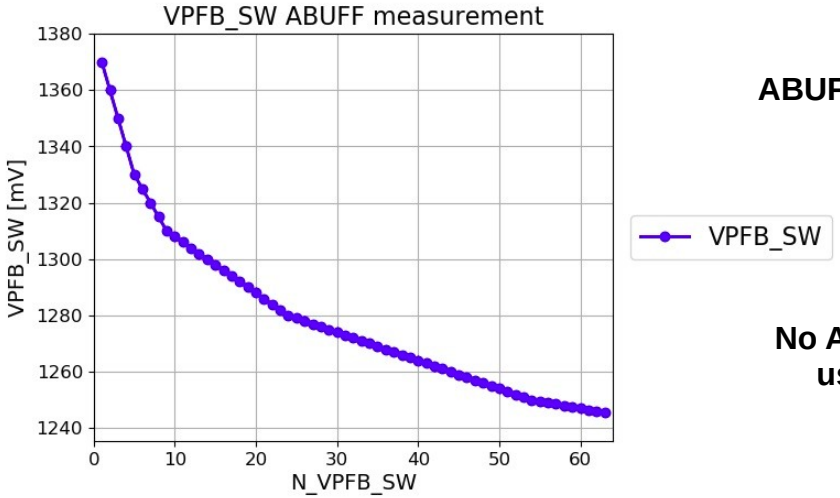
- Measurement details: **VPFB_SW (sets I_{FB} of switched-reset pixels).**
  - Measurement with on-board **ABUFF output with scope**..
  - Bias register programmed from 0 to 63.



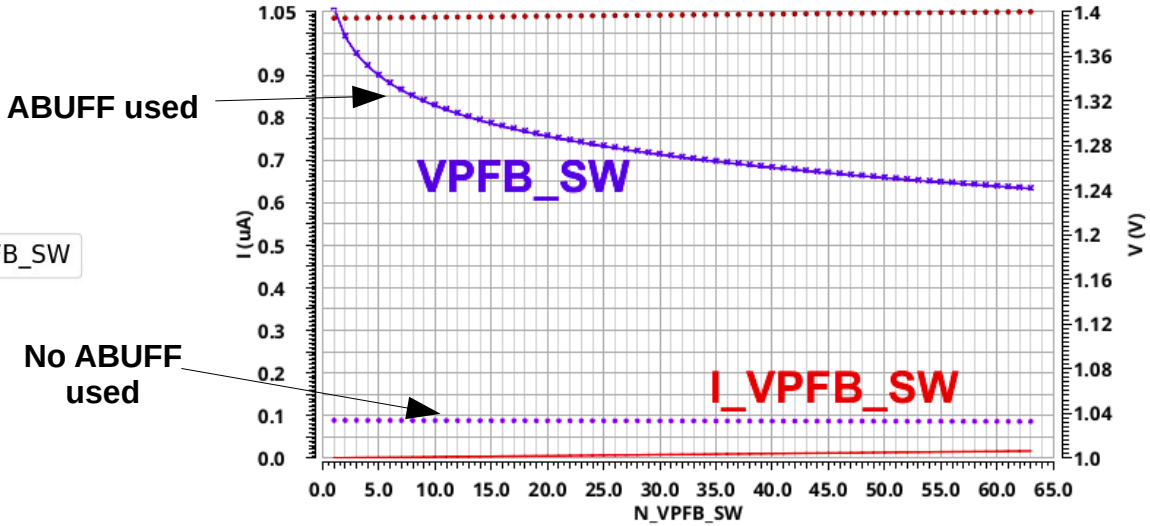
VPFB_SW ABUFF measurement (RD50-MPW2-1 W7).



VPFB_SW ABUFF measurement (RD50-MPW2-3 W14).



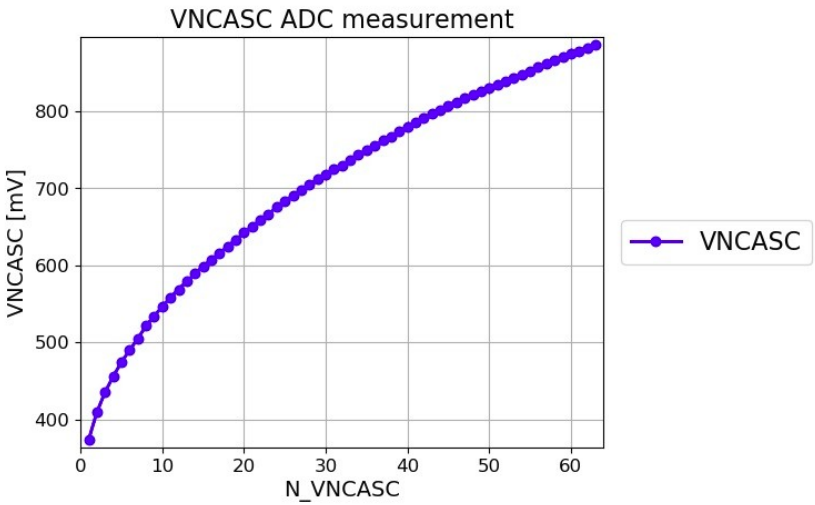
VPFB_SW ABUFF measurement (RD50-MPW2-2 W10).



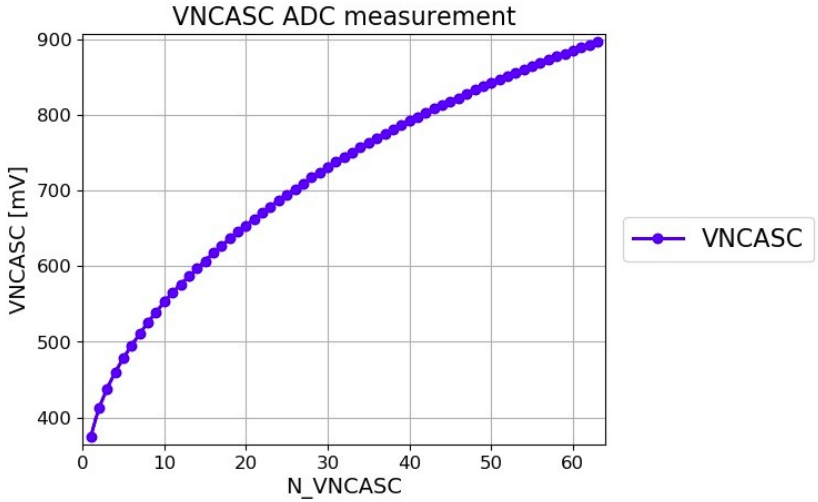
VPFB_SW simulation

RD50-MPW2 bias voltages measurements

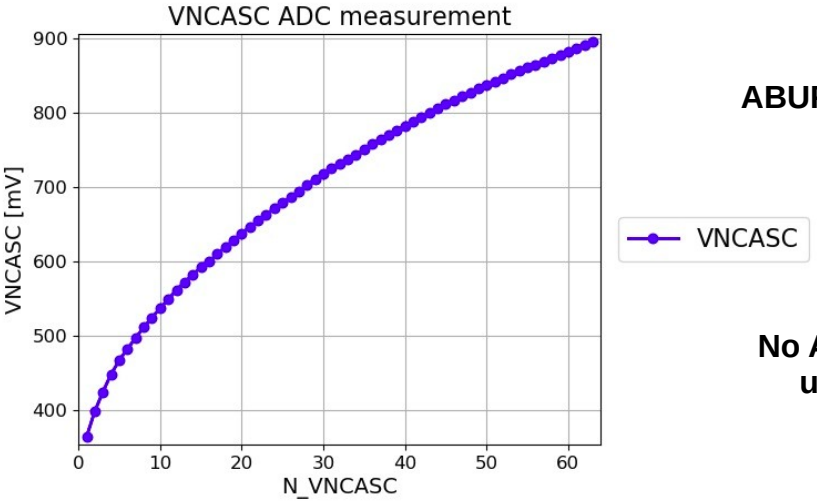
- Measurement details: **VNCASC (bias the cascode transistor of CSAs).**
  - Measurement with on-board **ADC**.
  - Bias register programmed from 0 to 63.



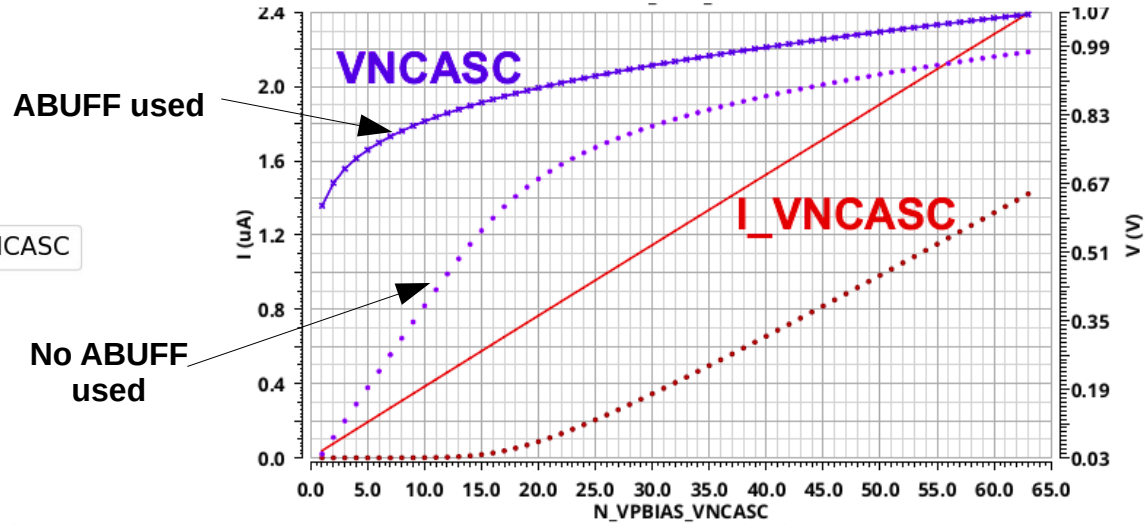
VNCASC ADC measurement (RD50-MPW2-1 W7).



VNCASC ADC measurement (RD50-MPW2-3 W14).



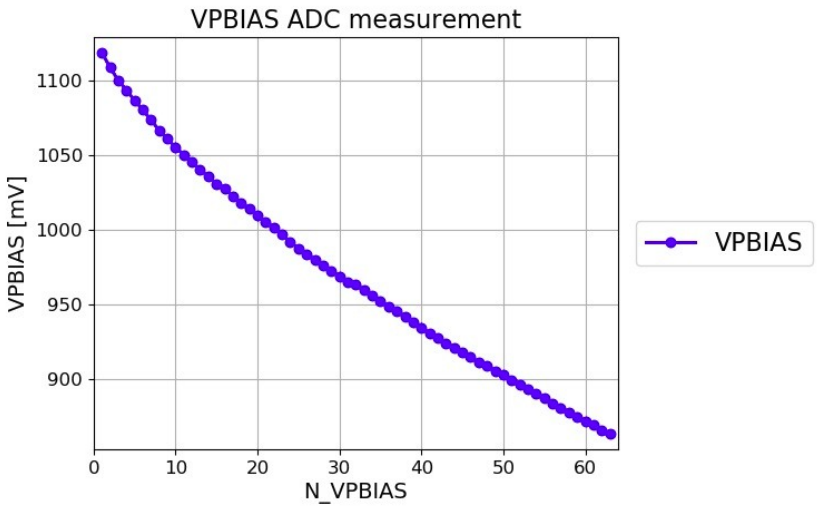
VNCASC ADC measurement (RD50-MPW2-2 W10).



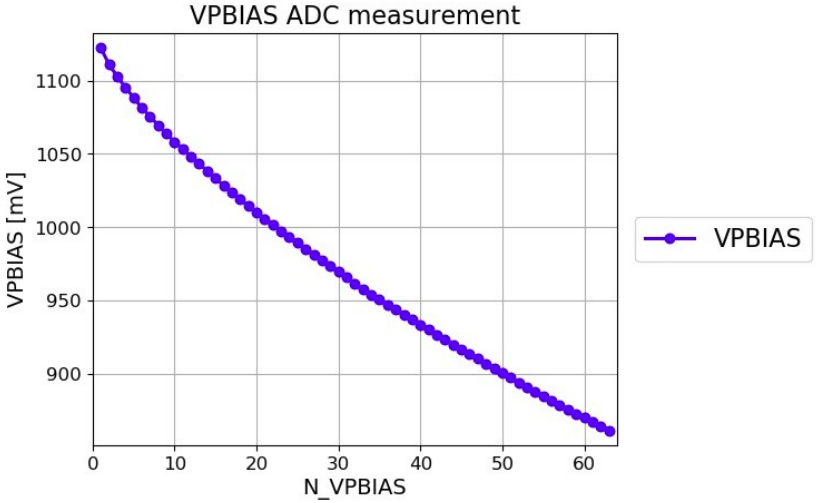
VNCASC simulation

RD50-MPW2 bias voltages measurements

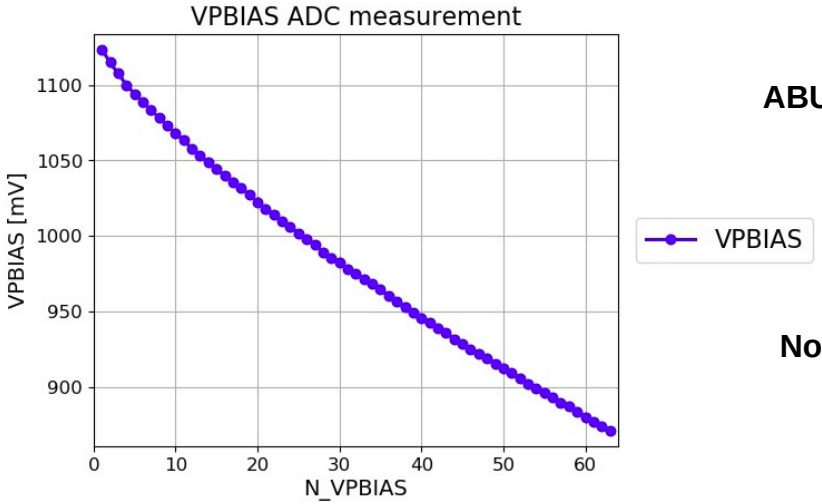
- Measurement details: **VPBIAS (sets current of the load of CSAs).**
  - Measurement with on-board **ADC**.
  - Bias register programmed from 0 to 63.



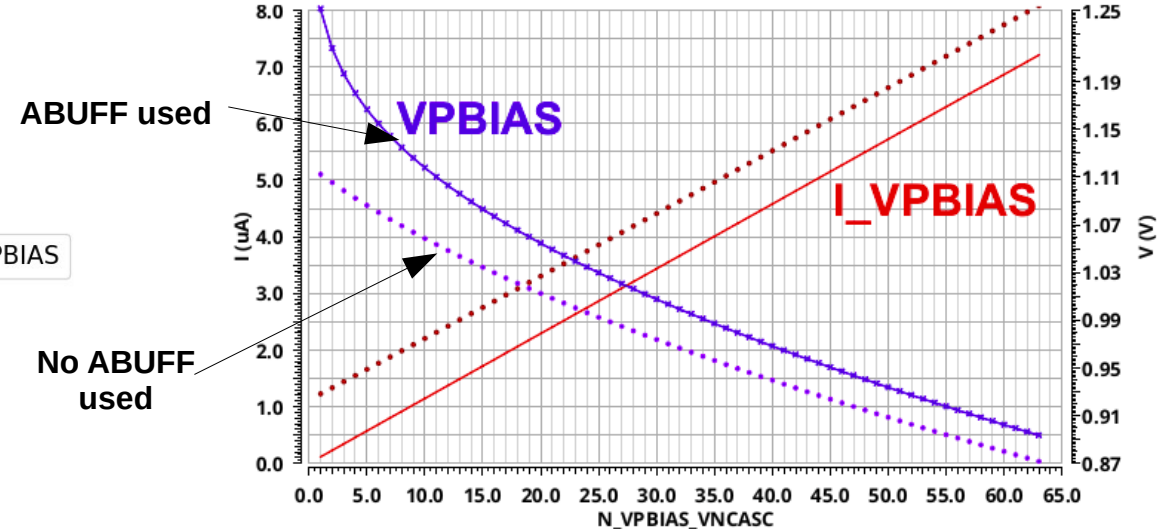
VPBIAS ADC measurement (RD50-MPW2-1 W7).



VPBIAS ADC measurement (RD50-MPW2-3 W14).



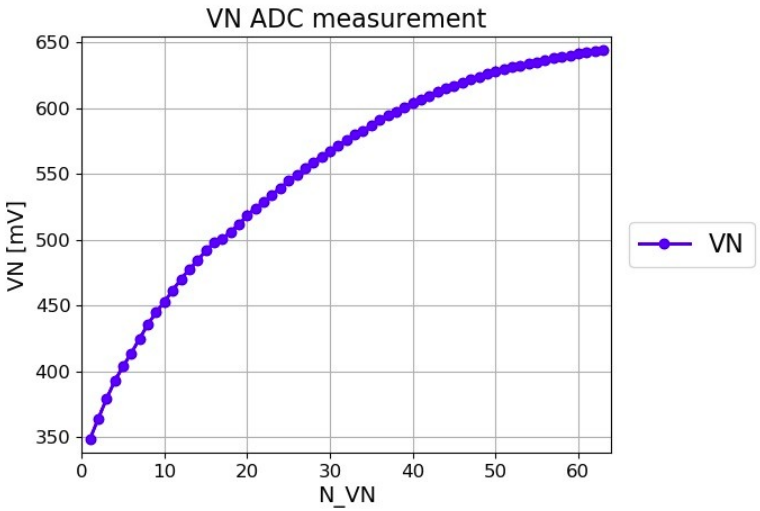
VPBIAS ADC measurement (RD50-MPW2-2 W10).



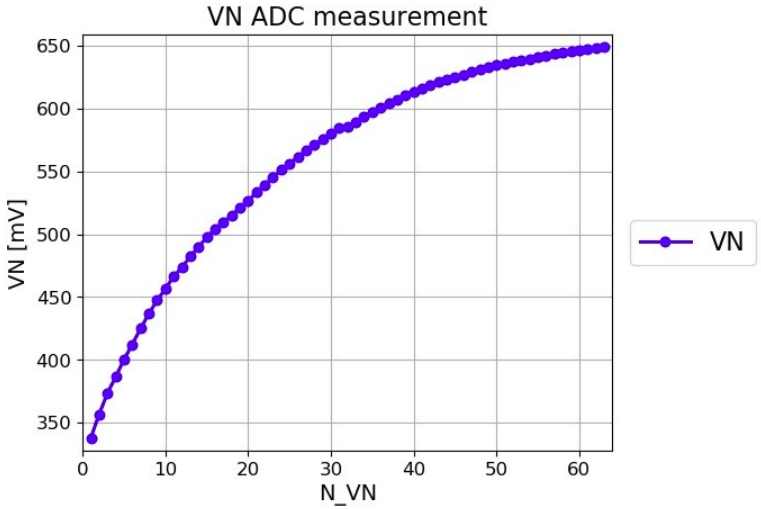
VPBIAS simulation

RD50-MPW2 bias voltages measurements

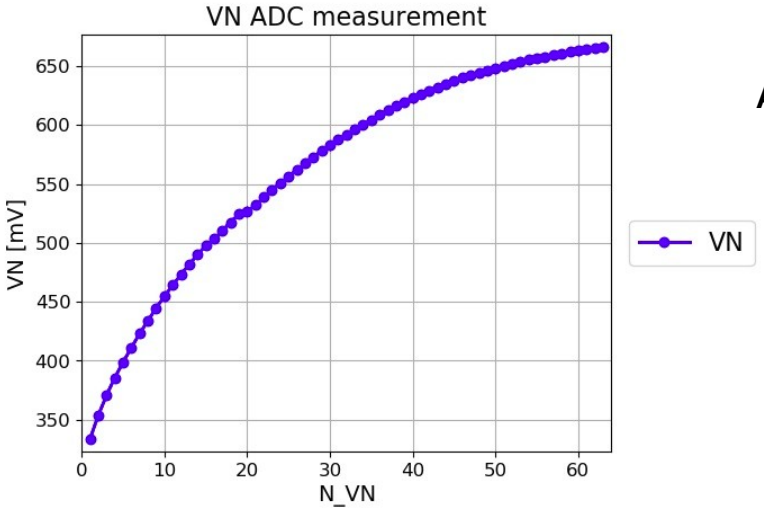
- Measurement details: **VN (sets current of CSAs).**
  - Measurement with on-board **ADC**.
  - Bias register programmed from 0 to 63.



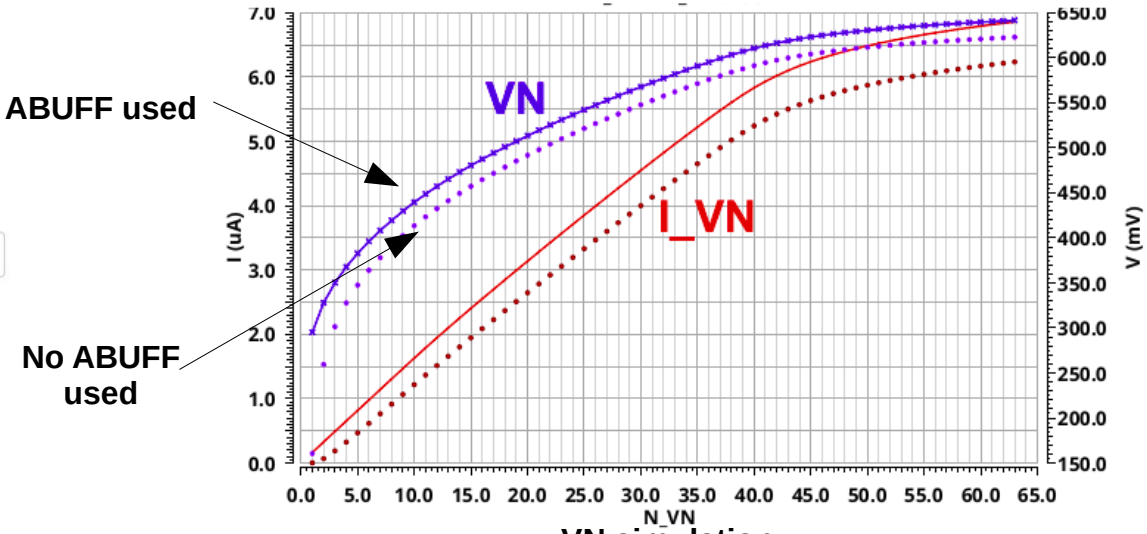
VN ADC measurement (RD50-MPW2-1 W7).



VN ADC measurement (RD50-MPW2-3 W14).



VN ADC measurement (RD50-MPW2-2 W10).



VN simulation

RD50-MPW2 current consumption measurement

- Measurement details: RD50-MPW2-2 (W10)
  - RD50-MPW2 voltage levels (V) and current levels (mA).
  - **Registers** of device **not configured from DAQ**.
  - **ABUFF powered**.

```
root@RD50_MPW2_DAQ_v2:~/Apps# python Meas_curr_RD50_MPW2.py --temp -v
#######################################################
# RD50_MPW2 power levels current measurement started #
#######################################################
CaR temperature (C): 36.875000
P1V8A_NW_RING (PWR_OUT_1) voltage (V): 1.837500
P1V8A_NW_RING (PWR_OUT_1) current (mA): 0.000000
P1V8D_VDD_IO (PWR_OUT_2) voltage (V): 1.841250
P1V8D_VDD_IO (PWR_OUT_2) current (mA): 0.300000
P1V8A_VSENSBIAS (PWR_OUT_3) voltage (V): 1.838750
P1V8A_VSENSBIAS (PWR_OUT_3) current (mA): 0.500000
P1V8A_VDDA (PWR_OUT_4) voltage (V): 1.823750
P1V8A_VDDA (PWR_OUT_4) current (mA): 6.800000
P1V8D_VDDC (PWR_OUT_5) voltage (V): 1.822500
P1V8D_VDDC (PWR_OUT_5) current (mA): 4.500000
P1V3A_VSSA (PWR_OUT_6) voltage (V): 1.348750
P1V3A_VSSA (PWR_OUT_6) current (mA): 0.800000
P1V8D_VDDD (PWR_OUT_7) voltage (V): 1.845000
P1V8D_VDDD (PWR_OUT_7) current (mA): 0.500000
P1V8A_BG_VDD (PWR_OUT_8) voltage (V): 1.843750
P1V8A_BG_VDD (PWR_OUT_8) current (mA): 0.800000
#######################################################
# RD50_MPW2 power levels current measurement finished #
#######################################################
root@RD50_MPW2_DAQ_v2:~/Apps#
```

RD50-MPW2 current consumption. No registers not configured. ABUFF powered.

Name	Description	Voltage	Current
NW_RING	Nwell guard ring bias	1.8 V	Leakage
VDD_IO	Pads protection diodes cathode bias	1.8 V	
VSENSBIAS	DNWELL bias (cathode of sensing diode	1.8 V	~ nA
VDDA	Analog circuits power supply	1.8 V	< 5.5 mA
VDDC	In-pixel comparators power supply	1.8 V	< 0.5 mA
VSSA	CSAs power supply	1.3 V	< 0.5 mA
VDDD	Digital circuits power supply	1.8 V	< 100 µA
BG_VDD	Bandgap power supply	1.8 V	~ 100 µA

RD50-MPW2 current consumption from pad description.

Higher values of current measured than expected

RD50-MPW2 current consumption measurement

- Measurement details: RD50-MPW2-2 (W10)
  - RD50-MPW2 voltage levels (V) and current levels (mA).
  - **Registers** of device **configured from DAQ**.
  - **ABUFF powered**.

```
root@RD50_MPW2_DAQ_v2:~/Apps# python Meas_curr_RD50_MPW2.py --temp -v
#####################################################
# RD50_MPW2 power levels current measurement started #
#####################################################
CaR temperature (C): 37.187500
P1V8A_NW_RING (PWR_OUT_1) voltage (V): 1.838750
P1V8A_NW_RING (PWR_OUT_1) current (mA): 0.300000
P1V8D_VDD_IO (PWR_OUT_2) voltage (V): 1.842500
P1V8D_VDD_IO (PWR_OUT_2) current (mA): 0.000000
P1V8A_VSENSBIAS (PWR_OUT_3) voltage (V): 1.840000
P1V8A_VSENSBIAS (PWR_OUT_3) current (mA): 0.500000
P1V8A_VDDA (PWR_OUT_4) voltage (V): 1.822500
P1V8A_VDDA (PWR_OUT_4) current (mA): 6.500000
P1V8D_VDDC (PWR_OUT_5) voltage (V): 1.820000
P1V8D_VDDC (PWR_OUT_5) current (mA): 4.800000
P1V3A_VSSA (PWR_OUT_6) voltage (V): 1.347500
P1V3A_VSSA (PWR_OUT_6) current (mA): 0.500000
P1V8D_VDDD (PWR_OUT_7) voltage (V): 1.846250
P1V8D_VDDD (PWR_OUT_7) current (mA): 0.300000
P1V8A_BG_VDD (PWR_OUT_8) voltage (V): 1.843750
P1V8A_BG_VDD (PWR_OUT_8) current (mA): 0.800000
#####################################################
# RD50_MPW2 power levels current measurement finished #
#####################################################
root@RD50_MPW2_DAQ_v2:~/Apps#
```

RD50-MPW2 current consumption. Registers configured. ABUFF powered.

Name	Description	Voltage	Current
NW_RING	Nwell guard ring bias	1.8 V	Leakage
VDD_IO	Pads protection diodes cathode bias	1.8 V	
VSENSBIAS	DNWELL bias (cathode of sensing diode	1.8 V	~ nA
VDDA	Analog circuits power supply	1.8 V	< 5.5 mA
VDDC	In-pixel comparators power supply	1.8 V	< 0.5 mA
VSSA	CSAs power supply	1.3 V	< 0.5 mA
VDDD	Digital circuits power supply	1.8 V	< 100 µA
BG_VDD	Bandgap power supply	1.8 V	~ 100 µA

RD50-MPW2 current consumption from pad description.

Similar values of current measured as previous case

RD50-MPW2 current consumption measurement

- Measurement details: RD50-MPW2-2 (W10)
  - RD50-MPW2 voltage levels (V) and current levels (mA).
  - **Registers** of device **configured from DAQ**.
  - **ABUFF powered down**.

```
root@RD50_MPW2_DAQ_v2:~/Apps# python Meas_curr_RD50_MPW2.py --temp -v
#####################################################
# RD50_MPW2 power levels current measurement started #
#####################################################
CaR temperature (C): 37.187500
P1V8A_NW_RING (PWR_OUT_1) voltage (V): 1.837500
P1V8A_NW_RING (PWR_OUT_1) current (mA): 0.300000
P1V8D_VDD_IO (PWR_OUT_2) voltage (V): 1.843750
P1V8D_VDD_IO (PWR_OUT_2) current (mA): 0.000000
P1V8A_VSENSBIAS (PWR_OUT_3) voltage (V): 1.840000
P1V8A_VSENSBIAS (PWR_OUT_3) current (mA): 0.000000
P1V8A_VDDA (PWR_OUT_4) voltage (V): 1.838750
P1V8A_VDDA (PWR_OUT_4) current (mA): 1.000000
P1V8D_VDDC (PWR_OUT_5) voltage (V): 1.821250
P1V8D_VDDC (PWR_OUT_5) current (mA): 5.000000
P1V3A_VSSA (PWR_OUT_6) voltage (V): 1.346250
P1V3A_VSSA (PWR_OUT_6) current (mA): 0.800000
P1V8D_VDDD (PWR_OUT_7) voltage (V): 1.846250
P1V8D_VDDD (PWR_OUT_7) current (mA): 0.300000
P1V8A_BG_VDD (PWR_OUT_8) voltage (V): 1.842500
P1V8A_BG_VDD (PWR_OUT_8) current (mA): 0.800000
#####################################################
# RD50_MPW2 power levels current measurement finished #
#####################################################
root@RD50_MPW2_DAQ_v2:~/Apps#
```

RD50-MPW2 current consumption. Registers configured. ABUFF powered down.

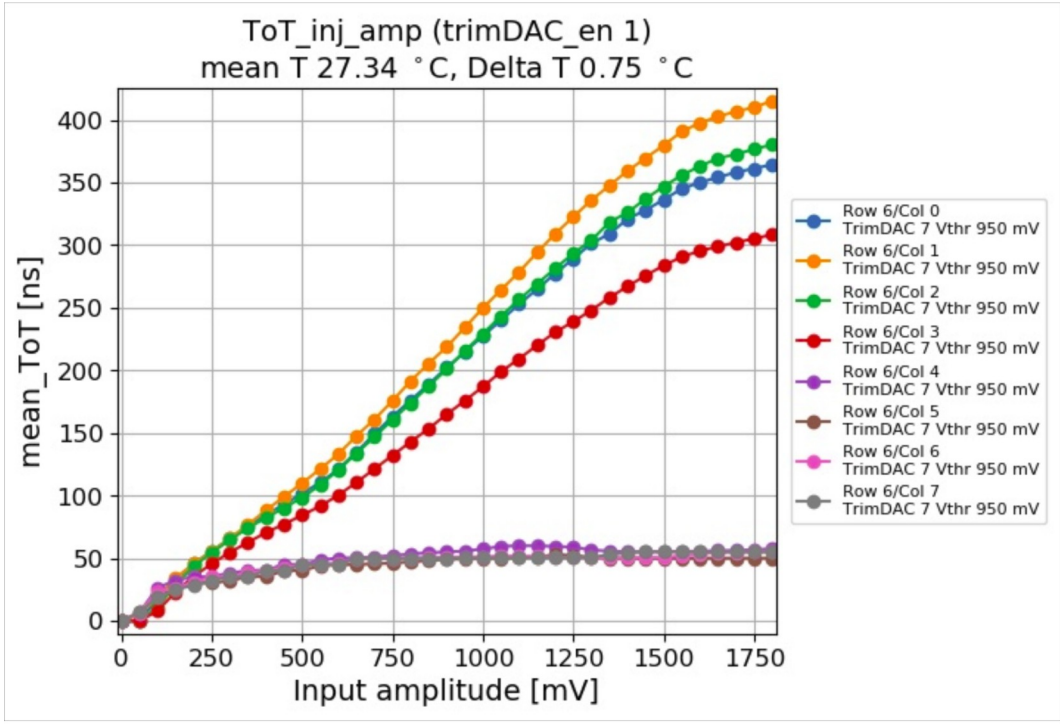
Name	Description	Voltage	Current
NW_RING	Nwell guard ring bias	1.8 V	Leakage
VDD_IO	Pads protection diodes cathode bias	1.8 V	
VSENSBIAS	DNWELL bias (cathode of sensing diode	1.8 V	~ nA
VDDA	Analog circuits power supply	1.8 V	< 5.5 mA
VDDC	In-pixel comparators power supply	1.8 V	< 0.5 mA
VSSA	CSAs power supply	1.3 V	< 0.5 mA
VDDD	Digital circuits power supply	1.8 V	< 100 µA
BG_VDD	Bandgap power supply	1.8 V	~ 100 µA

RD50-MPW2 current consumption from pad description.

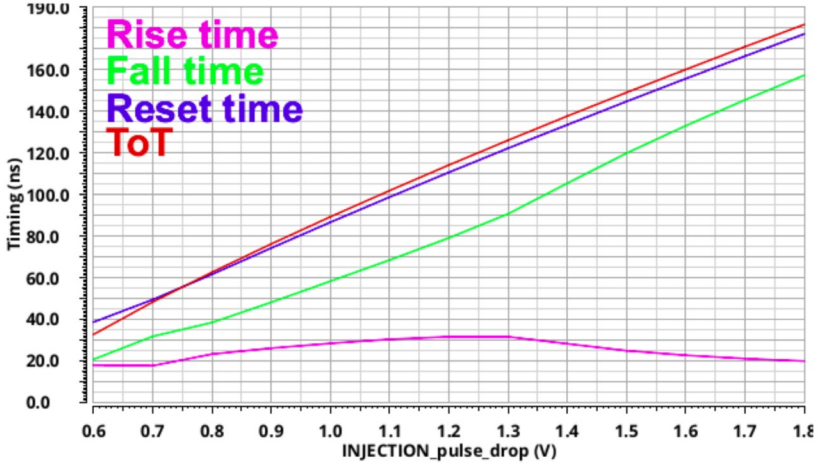
Current consumption at VDDA reduced 5 mA with ABUFF off as expected

RD50-MPW2 ToT measurement

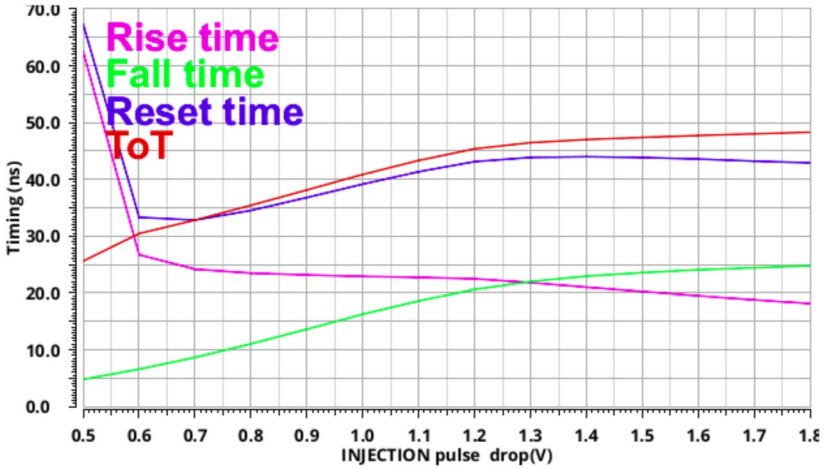
- Measurement details:
  - 400 test pulses generated (100 us of width and 1 ms of period). Amplitude 0 mV to 1800 mV.
  - Different types of pixels measured: **R6/C0-C3 (CR pixel) and R6/C4-C7 (SR pixel).**
  - Mean of ToT calculated for each injection amplitude.
  - Nominal values of bias voltage registers. BL 900 mV. TH 950 mV.
  - TrimDAC enabled and programmed to 7.



R6/C0-C3 (CR) and R6/C4-C7 (SR) mean ToT (ns) versus input voltage pulse amplitude (mV).



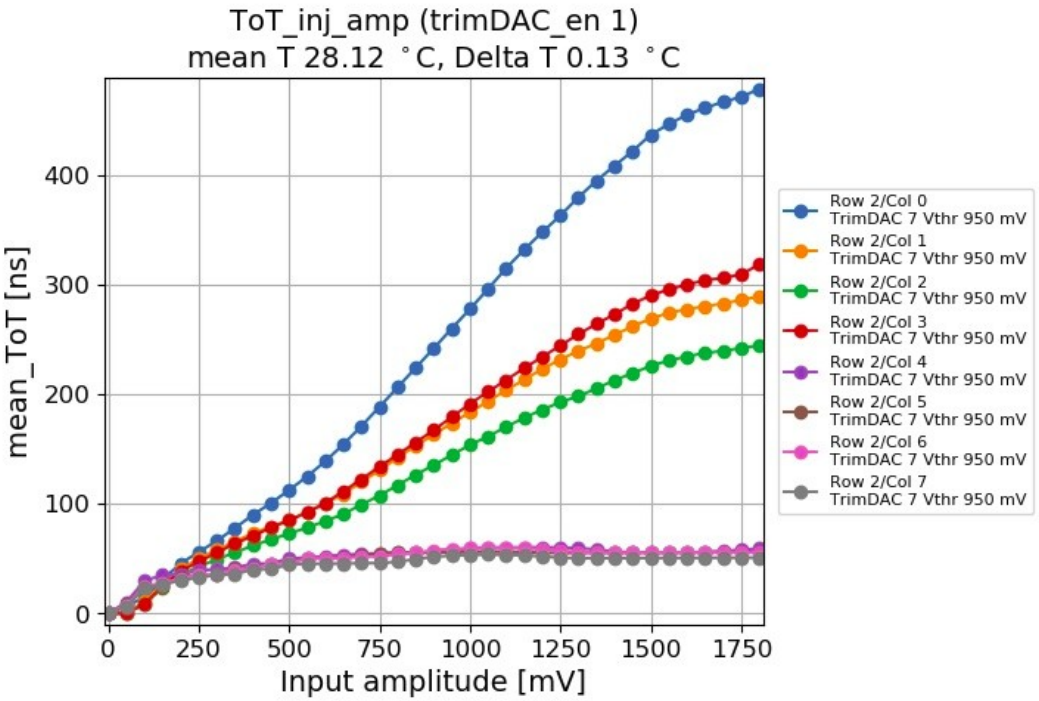
Simulated ToT (red) with voltage injections for a CR pixel.



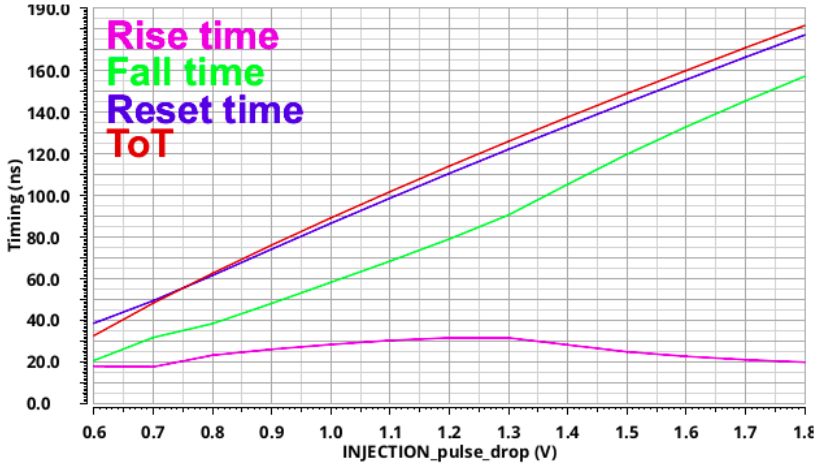
Simulated ToT (red) with voltage injections for a SR pixel.

RD50-MPW2 ToT measurement

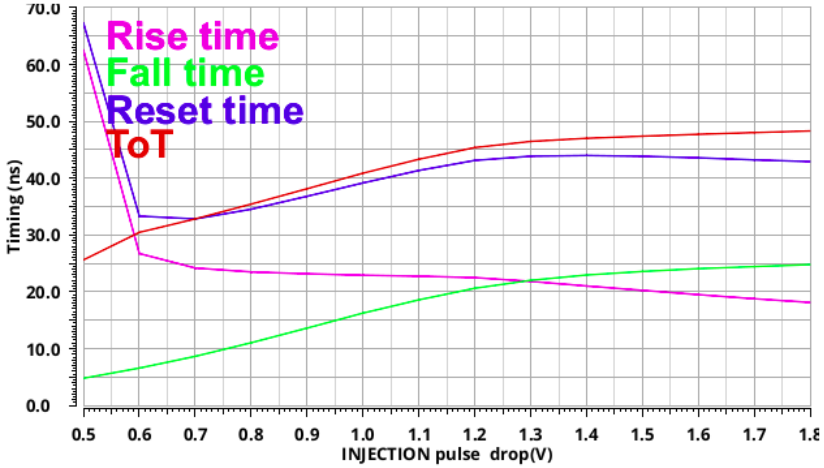
- Measurement details:
  - 400 test pulses generated (100 us of width and 1 ms of period). Amplitude 0 mV to 1800 mV.
  - Different types of pixels measured: **R2/C0-C3 (CR pixel) and R2/C4-C7 (SR pixel).**
  - Mean of ToT calculated for each injection amplitude.
  - Nominal values of bias voltage registers. BL 900 mV. TH 950 mV.
  - TrimDAC enabled and programmed to 7.



R2/C0-C3 (CR) and R2/C4-C7 (SR) mean ToT (ns) versus input voltage pulse amplitude (mV).



Simulated ToT (red) with voltage injections for a CR pixel.



Simulated ToT (red) with voltage injections for a SR pixel.

Next steps

- RD50 workshop talk about active matrix, bandgap and SEU memory.
- After RD50 Workshop: follow agreed measurements of excel file.
  - I-V measurement of active matrix.
  - Measurement of bias voltages vs. different values programmed using ABUFF_OUT.
  - Measurements with HV applied.
  - Measurements with three different chip boards (with MPW2 devices from different wafers with different resistivities).
  - ...

RD50-MPW2 active pixel matrix measurements

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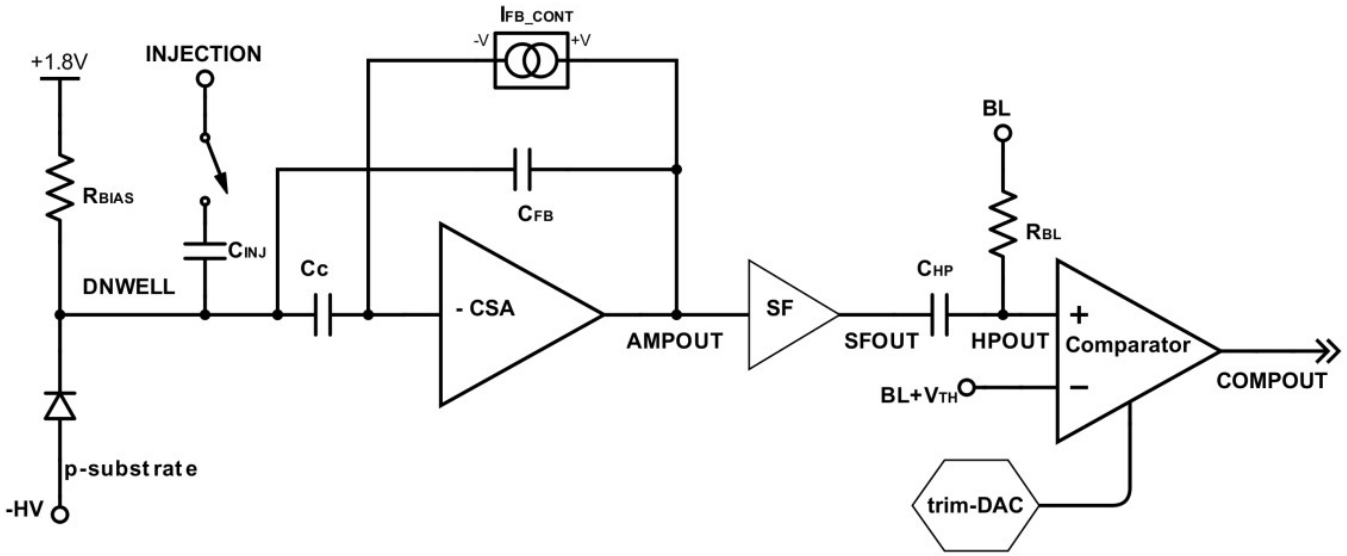

Figure 5.2. Schematic diagram of the continuous-reset pixel

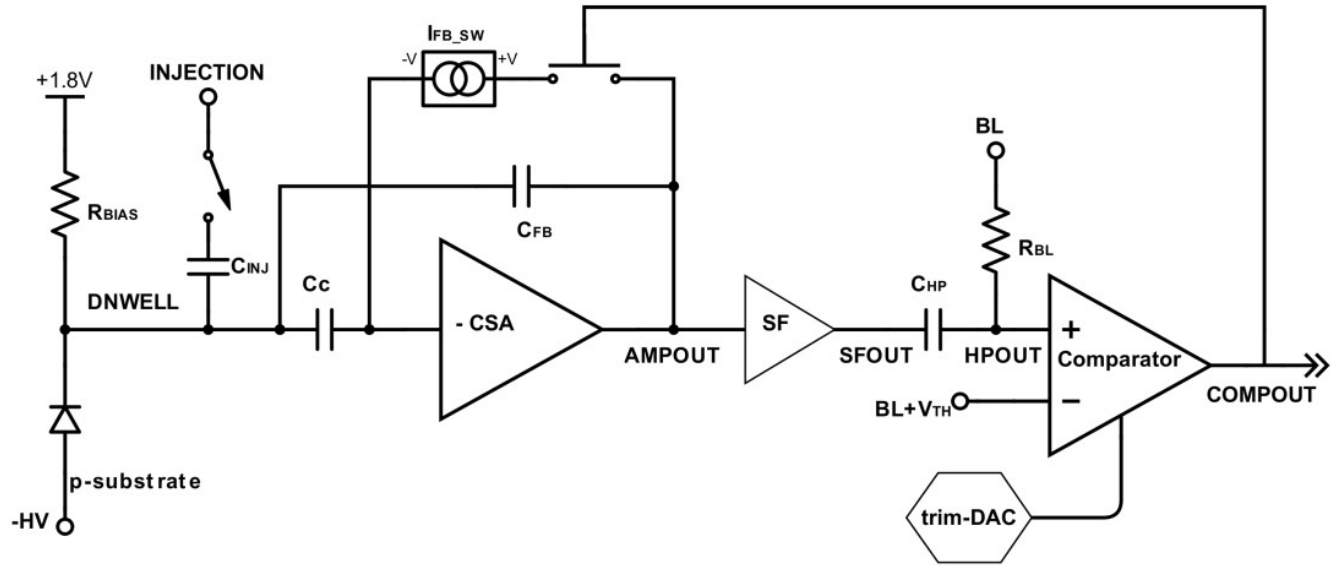

Figure 5.9. Schematic diagram of the switched-reset pixel