RD50-MPW3: ideas for the FEI3 pixel matrix

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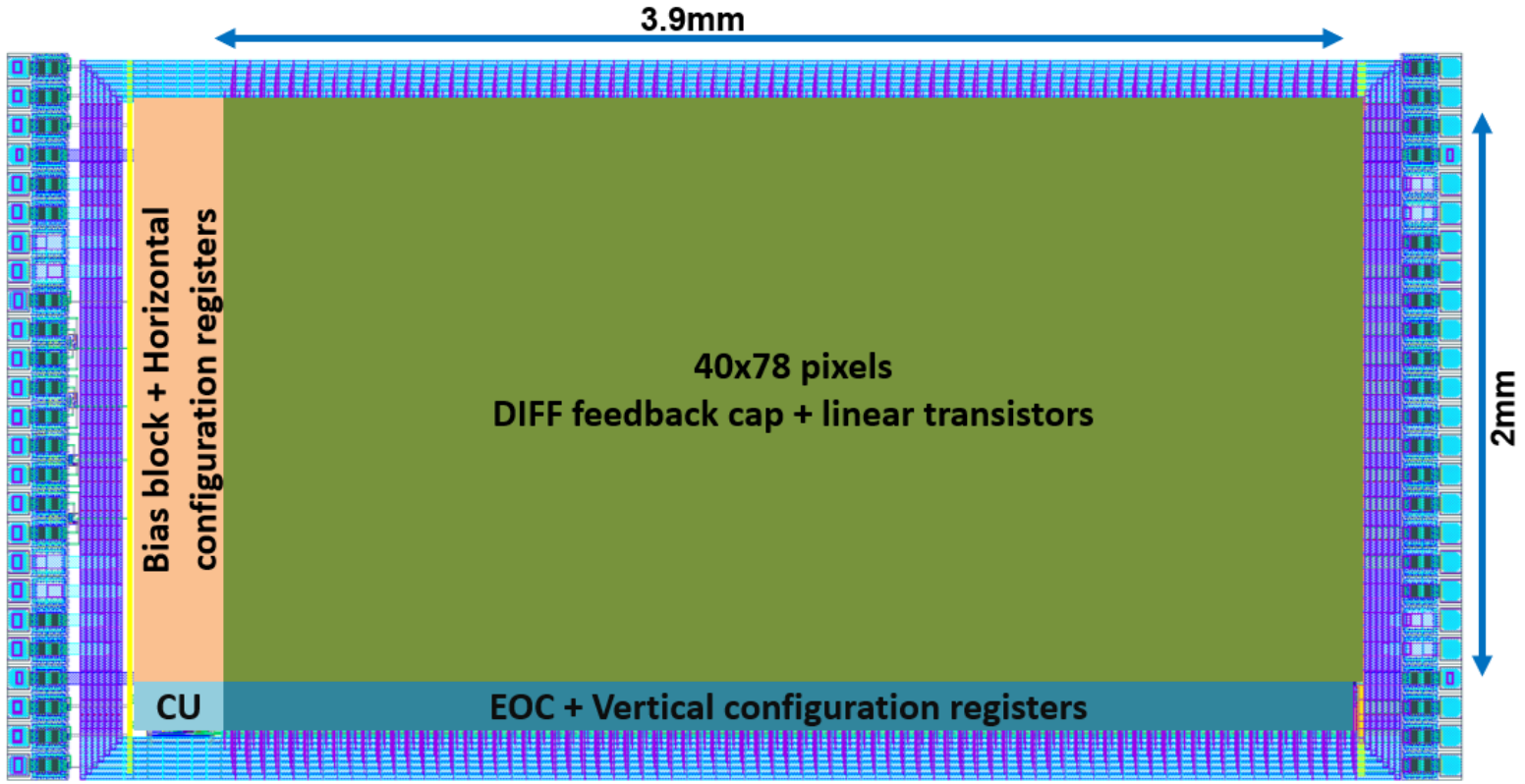
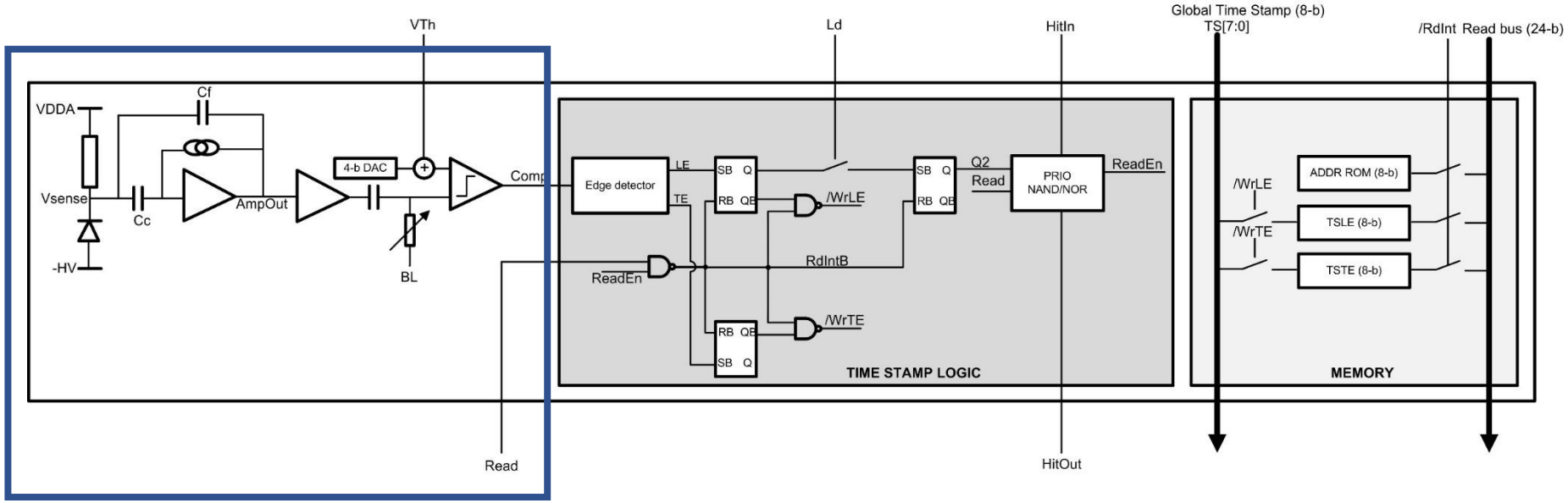
RD50-MPW1 (FEI3 pixel matrix)



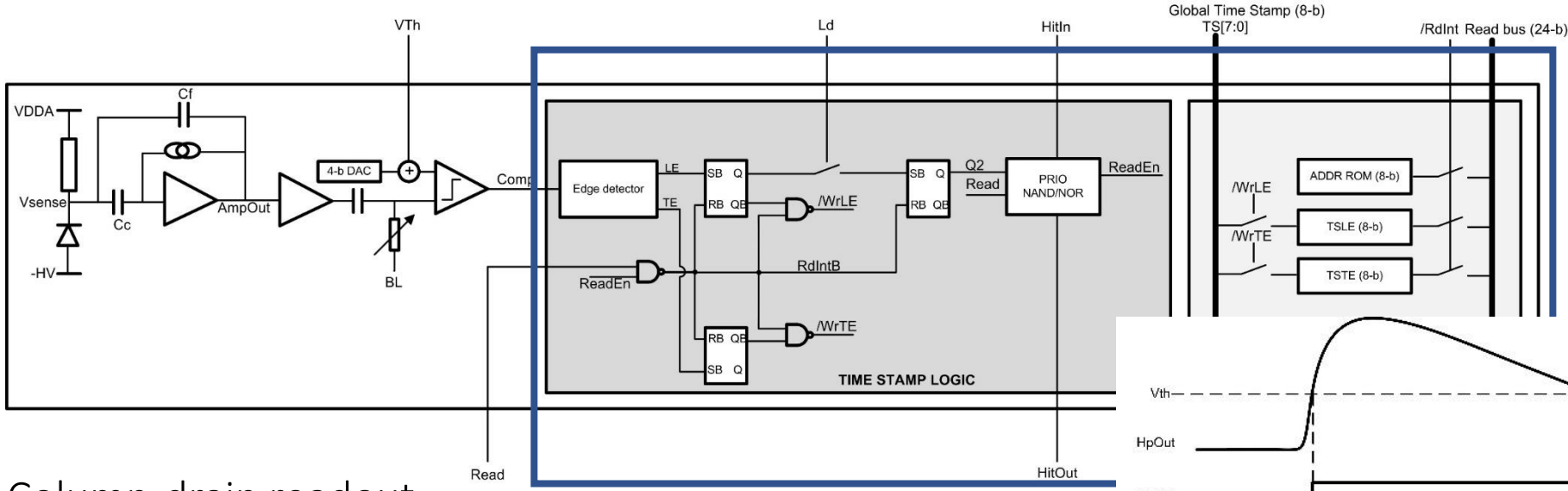
- Pixel size of 50x50µm^2
- Analog and digital front-end electronics on pixel
- CU and configuration registers compatible with H35DEMO

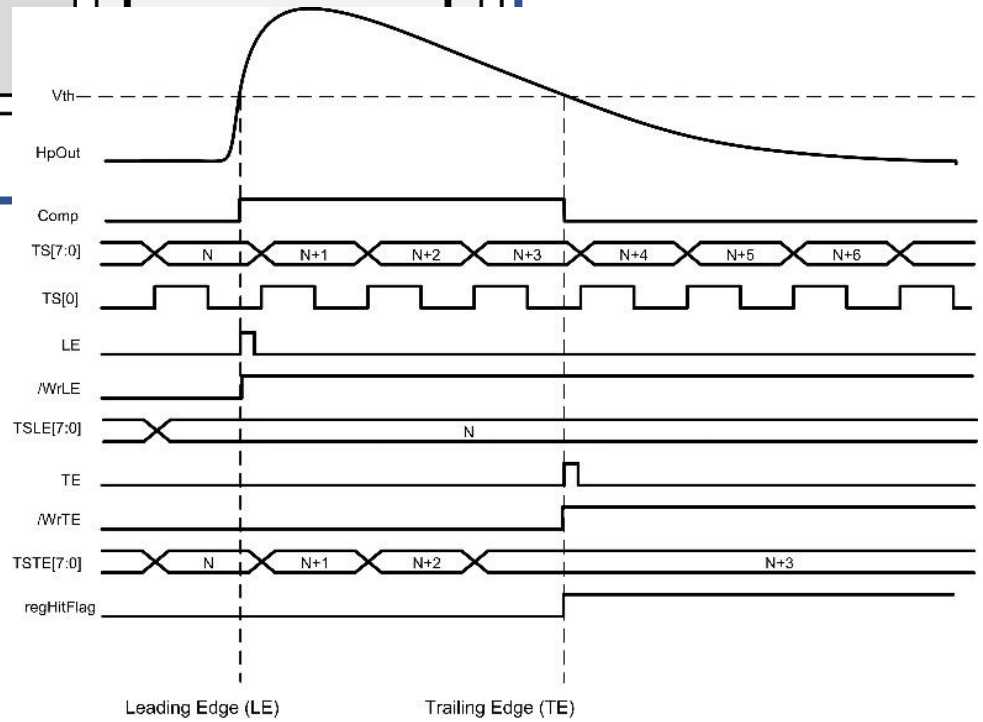
FEI3 pixel – analog front-end electronics



- Continuous discharging integrator with programmable discharging current.
- Base line (BL) and CR-RC filter adjustable.
- Global threshold.
- 4-bits DAC to fine tuning on pixel threshold level.
- Total power consumption: 33µW approx.

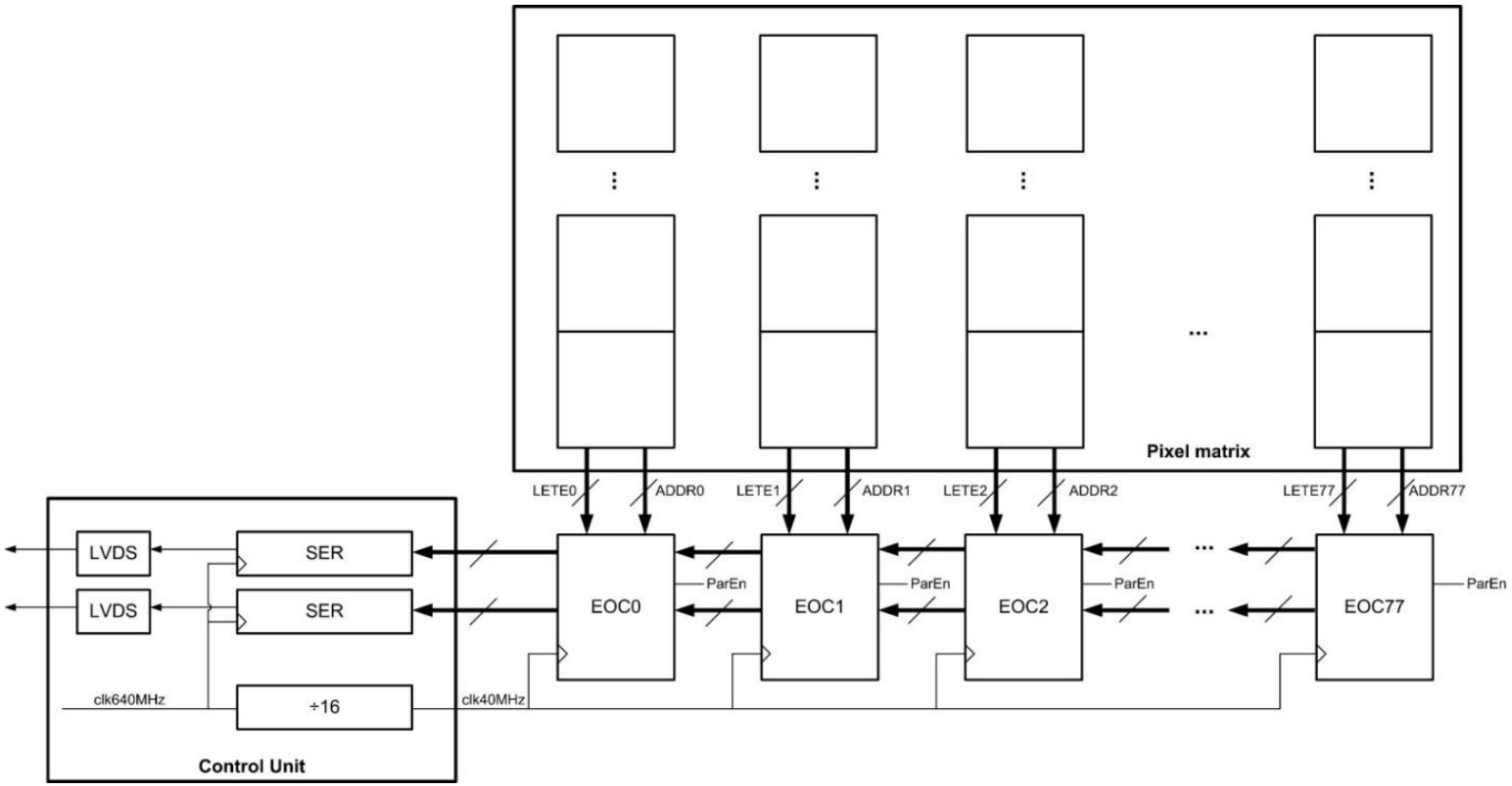
FEI3 pixel – analog front-end electronics





- Column-drain readout
- Global 8-bit gray encoded time stamp (40MHz)
- For each hit:
  - Leading edge (LE): 8-bit DRAM memory
  - Trailing Edge (TE): 8-bit DRAM memory
  - Address: 6-bit ROM memory
- TOT = LE – TE (off-chip)
- Hit flag + priority encoded scheme

FEI3 pixel matrix -readout



- Continuous readout.
- Data transferred from one End of Column (EOC) to the next one until arrives at the control unit where is serialized.
- Readout sequence:

  1) ADDR, LE and TE of the hit pixel with highest priority in a column stored into the End Of Column (EOC) cell. Duration: 1 clock cycle.

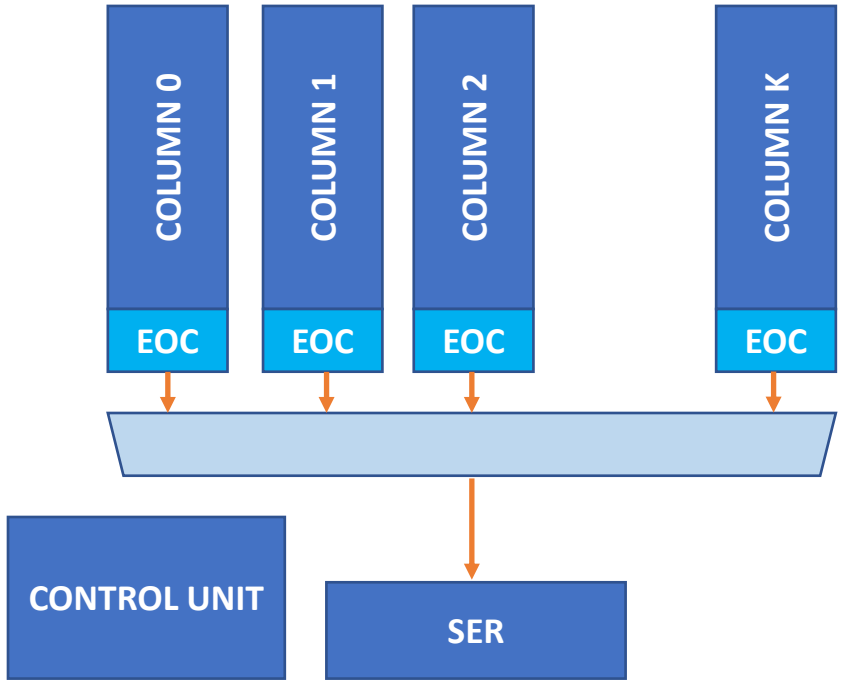
  2) CU reads sequentially the data stored in each EOC at 40MHz. Duration: 78 clock cycle.
- 2 LVDS ports at 640MHz.

Limitations

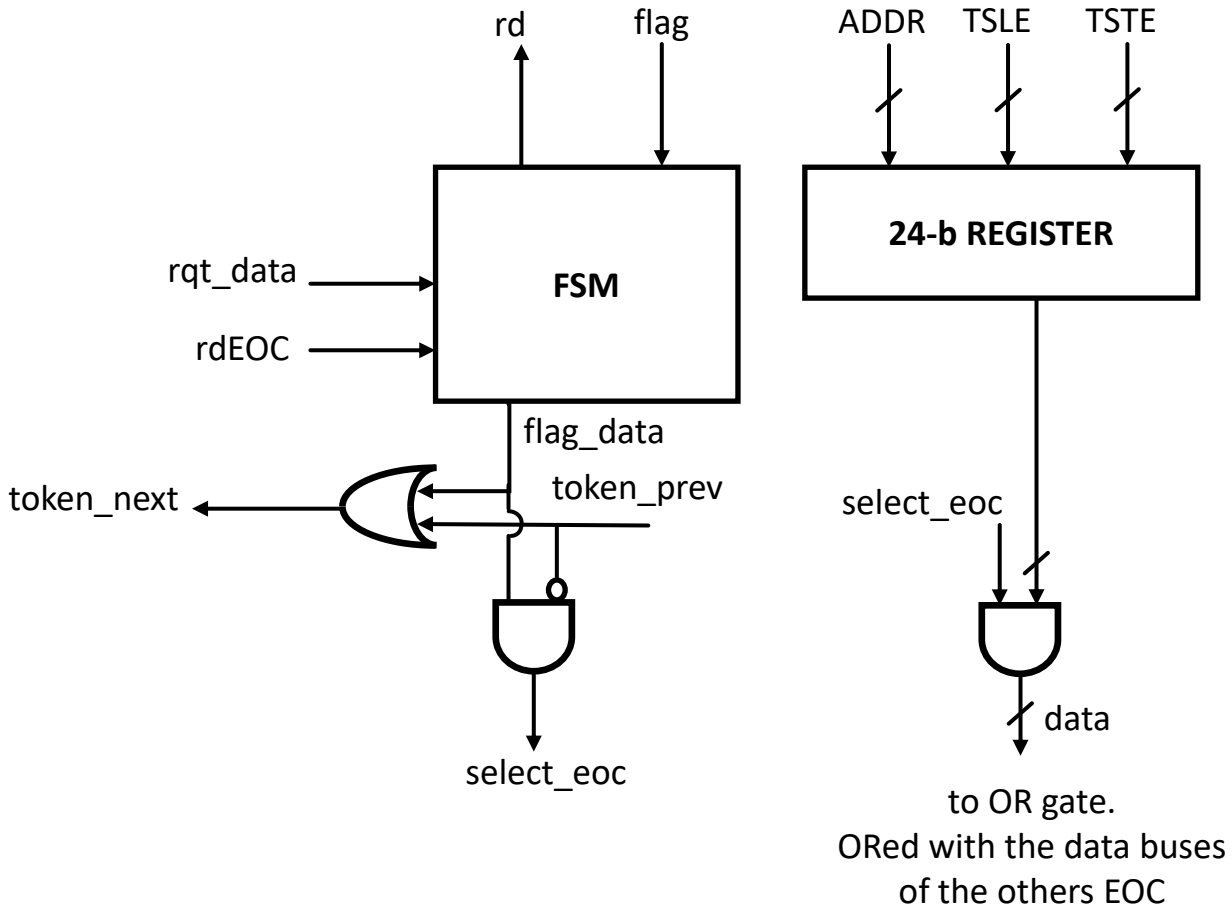
- Limitations:
  - 2 serial TX channels operating at 640Mbps.
  - No synchronization frame.
  - Bare data, no SOF and EOF.
  - Every column is given a time slot even not having data to transmit → only one pixel per column is readout every 25ns * number of columns.
  - Columns with no hits are also readout (transmission of zeros!).

Architecture 1

- Time slot only given to those columns with data
- Readout performed in two steps:
  - Data readout (from pixel to EOC):
    - control unit asks to EOC to readout data from the pixel.
    - EOC checks ORed hit flag in the column. It reads the pixel with its hit flag asserted and with the highest priority.
    - data transmission from pixel to column takes one clock cycle.
    - read data stored temporally in the EOC. A token flag is set to high indicating data to be readout.
  - Data transmission:
    - only EOC with token flag asserted are readout.
    - priority-encoded scheme readout. EOC with higher priority read first.
    - data of one EOC is packed and serialized (it may take few clock cycles depending on the transmission rate).
- Limitations: pixel can not process another hit until its data has not been readout and transmitted.

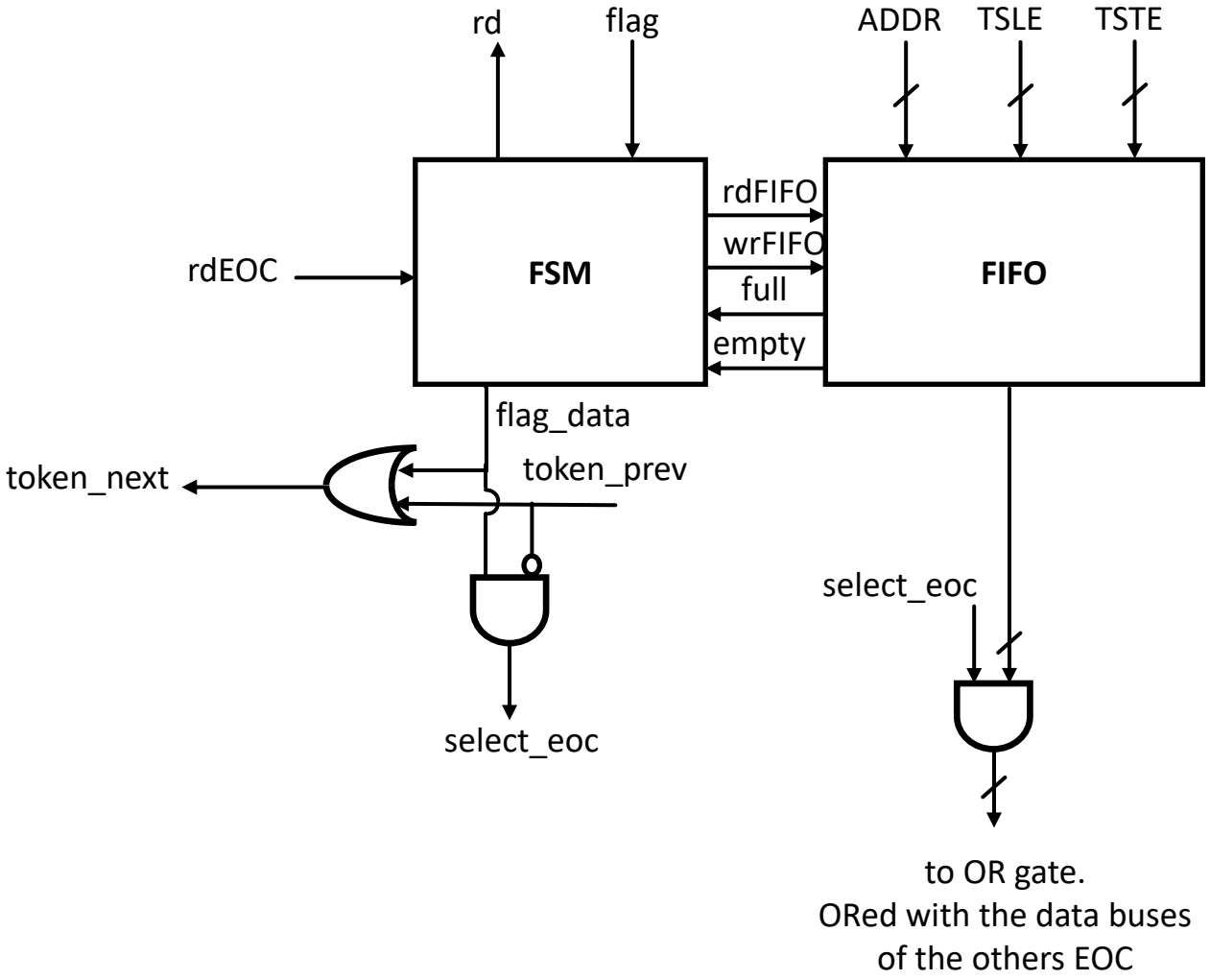


Architecture 1

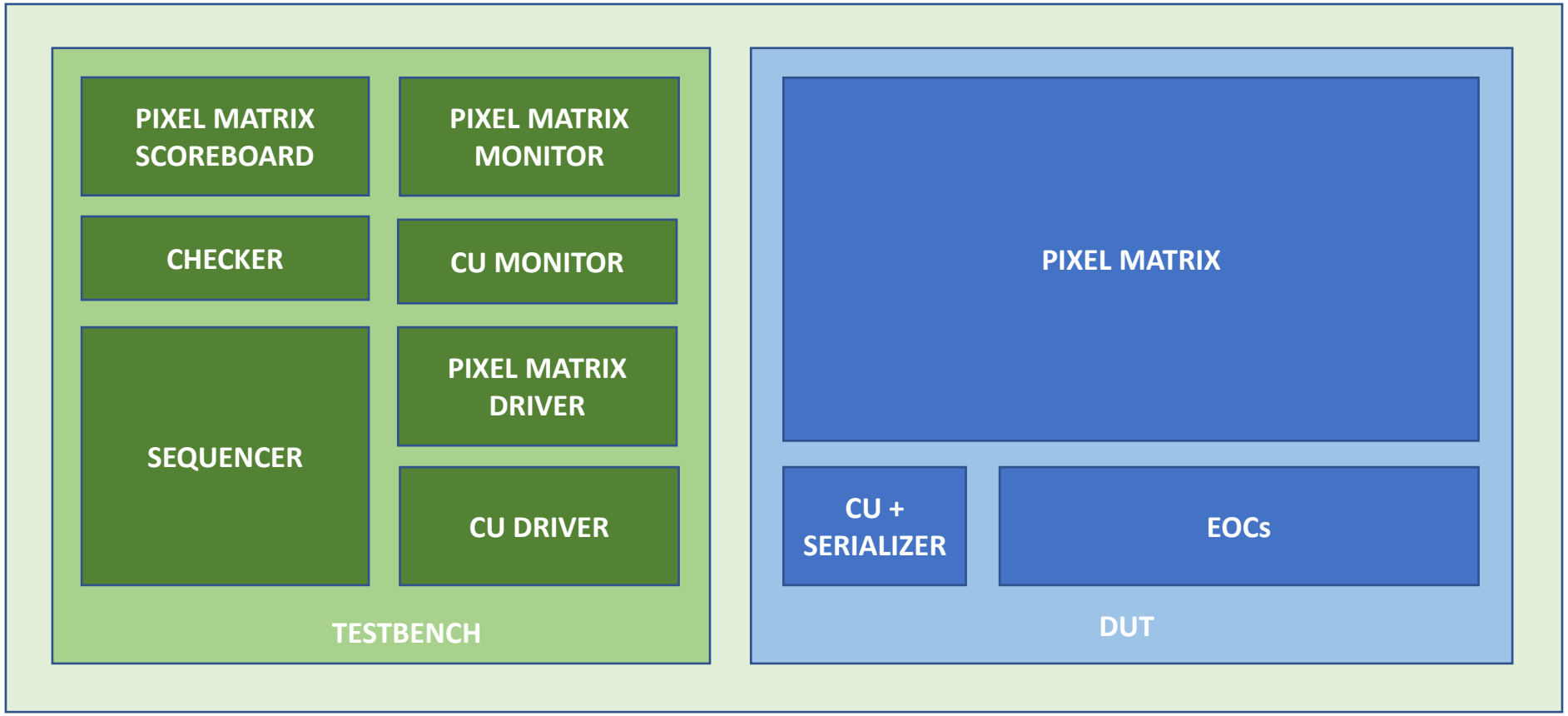


Architecture 2

- Register replaced by a FIFO.
- FSM continuously fills the FIFO with data from the pixels.
- FIFO acts as a temporal buffer and data is transmitted from pixel to EOC as soon as is available and the FIFO is not full.
- Control unit only reads one entry from the FIFO and then the token is passed to the next EOC with data to be readout.



Architecture exploration enviroment



It will be reused for verification

Steps to follow

- Write a functional model of:
  - pixel
  - pixel matrix
  - Periphery electronics (diferent architectures)
- Write verification enviroment. UVM methodology?