Contribution ID: **19** Type: **not specified**

Semiconductor process selection from ESD perspective: FinFET, SOI or CMOS?

Tuesday 22 September 2020 16:10 (30 minutes)

Many fabless companies struggle with the selection of their next process platform: FinFET or thin film SOI or in CMOS?
Though on-chip protection against Electrostatic discharge (ESD) should not determine the choice of technology, it can impact design choices and ultimately cost of the product. For efficient ESD protection, 2 elements are important: the ESD strategy, and the vulnerability of the circuit. The clamp design lays bare the underlying technology restrictions: the SOI BOX limits heat dissipation, even worse in FinFET designs. Techniques to circumvent the issue lead to unacceptable DRC/LVS violations. Also, the transistor characteristics under ESD conditions are heavily influenced by the Fins and BOX. Design margins are shrinking, and I/O topological decisions have different results in FinFETs, SOI or CMOS.
In the presentation device architecture and measurement data is used to compare 16nm FinFET, 22nm CMOS and 22nm SOI from the perspective of ESD robustness and I/O design.

Presenter: Mr VAN CAMP, CTO SOFICS, Benjamin (SOFICS solutions for ICs)

Session Classification: Micro-electronic user group