Future Trends in Microelectronics

A.Marchioro / June 18, 2022

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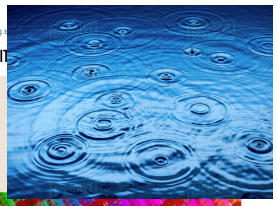
Quiz?

What is the item produced in the largest number today?

- Annual worldwide precipitation:
  - 5.4e14 m3 of rain
- Diameter of average drop: 2.5 mm
- Drop volume: 8.2e6
- Total number of water drops: 8.2e21

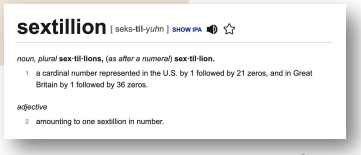


CHM Computer History Museum

EXPLORE CONNECT VISIT

13 SEXTILLION & COUNTING: THE LONG & WINDING ROAD TO THE MOST FREQUENTLY MANUFACTURED HUMAN ARTIFACT IN HISTORY

By David Laws | April 02, 2018



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Topics

- Refresher: what is a MOS transistor and how does it work?
- Past predictions
  - How good are we at "forecasting (*imagining?*) the future"?
- Revisit the major innovations that allowed VLSI scaling to go-on for 50+ years
- Sub 10 nm devices are now on the market
  - … and few atomic layers are left
  - are we approaching the end of the road?
- Possible innovations allowing growth for another generation
  - (Several) new devices current research
  - Innovative circuit from
- What use to make of sub-10nm transistors in HEP

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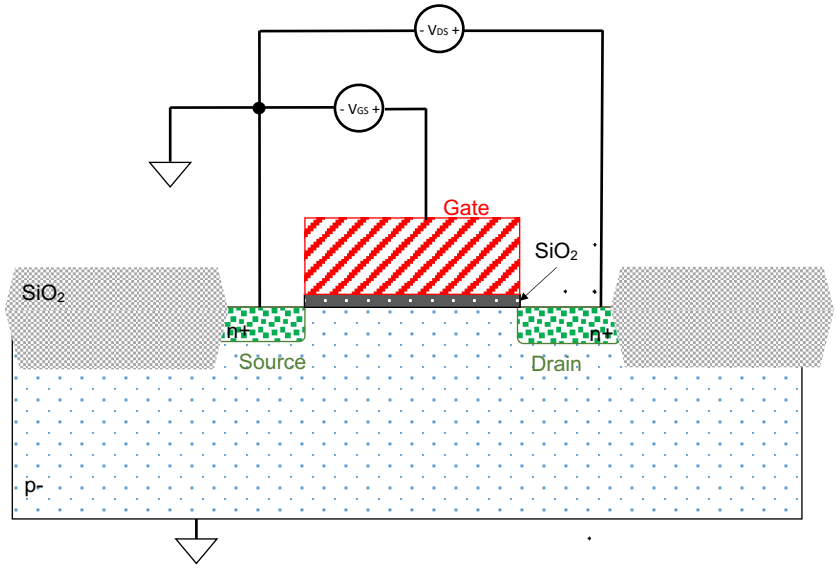
MOS Transistor



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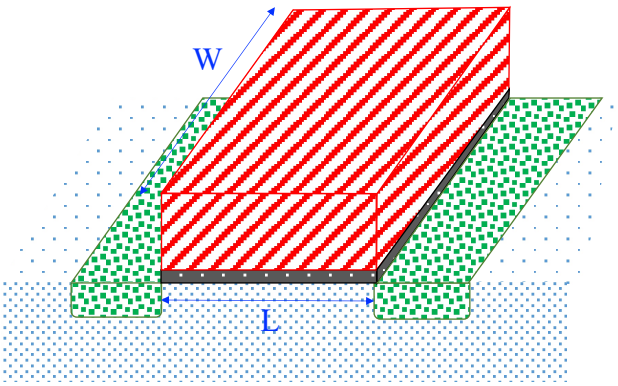
MOS Transistor Nomenclature



L is the defining parameter of a given CMOS technology.

Called the channel length, it is (actually was …) the smallest dimension that could be fabricated in an integrated circuit.

L is the distance that charge carriers have to traverse to bring current between the two terminals of a transistor.

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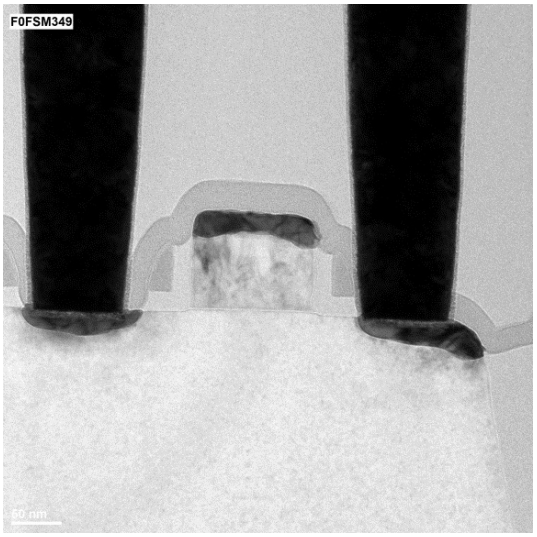
Real NMOS Transistor



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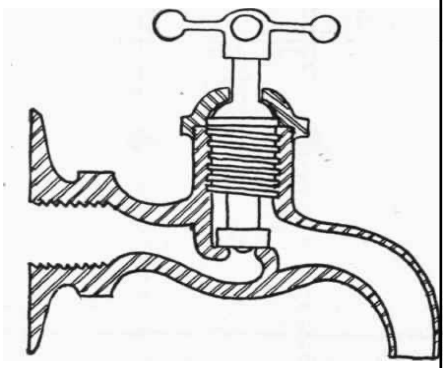
What do we want from a transistor anyway? (sorry analog engineers…)

- A transistor (a digital transistor) is a device that "should" have the following characteristics:
  - works as a switch (on or off)
  - three terminals: an input, an output, a control
  - makes a "sharp" transition between the two states (open or closed) in a time as short as possible (i.e. carry charge quickly through it)
  - no leakage current when off (I_{on}/I_{off} >[>] 10^6)
  - … while delivering high current when on (drive strongly the load), $I_{on,min}$ ~ 1mA/um
  - control terminal induces a transition between the two states with a voltage drive (V_{tr}) as small as possible: $P = ½ C V_{dd}^2$ (today V_{tr} ~ 1/2 V_{dd})
  - control terminal should not be influenced by input/output terminal(s)
  - be physically small (otherwise other "parasitics" ruin the party)
  - must have complementary type (i.e. a second type which is turned on when the first is turned off using the same "control").
- "Good analog" characteristics are desirable but by far not necessary or even important for the the majority of applications.
  In fact modern deep-submicron devices have "horrible" analog characteristics and analog designers have a hard time to achieve what was "easy" 20 years ago



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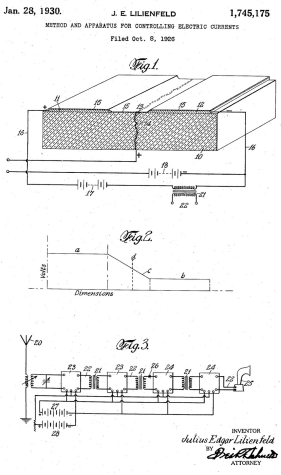
Lilienfeld (1926)



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Lilienfeld: right and wrong

Over both of the coatings 11 and 12, the intermediate upper surface portion of the glass 10, and the edge of the foil 13 is provided a film or coating 15 of a compound having the property of acting in conjunction with said metal foil electrode as an element of uni-directional conductivity. That is to say, this coating is to be electrically conductive and possess also the property, when associated with other suitable conductors, of establishing at the surface of contact a considerable drop of potential. The thickness of the film, moreover, is minute and of such a degree that the electrical conductivity therethru would be influenced by applying thereto an electrostatic force. A suitable material for this film and especially suitable in conjunction with aluminum foil, is a compound of copper and sulphur. A convenient way of providing the film over the coatings

J.E. Lilienfeld patent, page 2

The basis of the invention resides apparently in the fact that the conducting layer at the particular point selected introduces a resistance varying with the electric field at this point; and in this connection it may be assumed that the atoms (or molecules) of a conductor are of the nature of bipoles. In order for an electron, therefore, to travel in the electric field, the bipoles are obliged to become organized in this field substantially with their axes parallel or lying in the field of flow. Any disturbance in this organization, as by heat movement, magnetic field, electrostatic cross-field, etc., will serve to increase the resistance of the conductor; and in the instant case, the conductivity of the layer is influenced by the electric field. Owing to the fact that this layer is extremely thin the field is permitted to penetrate the entire volume thereof and thus will change the conductivity throughout the entire cross-section of this conducting portion.

J.E. Lilienfeld patent, page 3

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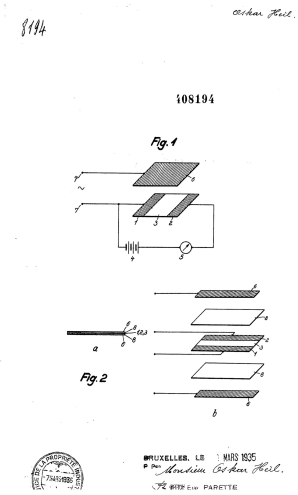
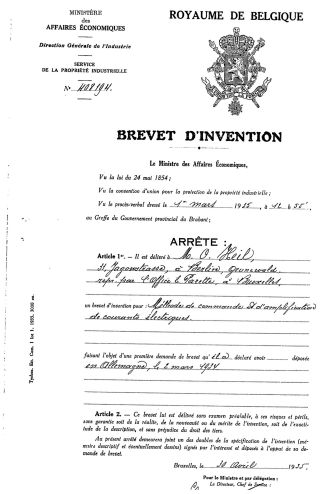
O. Heil (1935)





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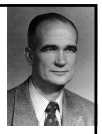
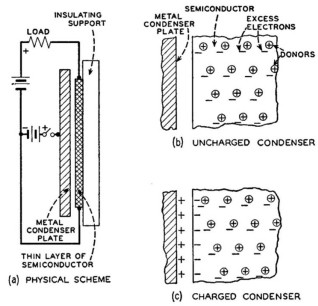
W. Shockley (1950)



from W. Shockley, "Electrons and Holes in Semiconductors, 1950, p30



Experiments have been carried out with layers of various semiconductors, and effects of the sort discussed have been observed. However, the degree of modulation has been somewhat less than that calculated above. For layers of germanium about 5000A thick, in which the mobility was only about 40 cm^2/volt sec, it was apparent upon analysis of the data that only about 10 per cent of the induced charges (holes in this instance since the evaporated germanium was *p*-type) were effective in changing the conductance.[4] This reduced effectiveness can be accounted for on the basis of a theory dealing with the behavior of the current carriers at a semiconductor surface.

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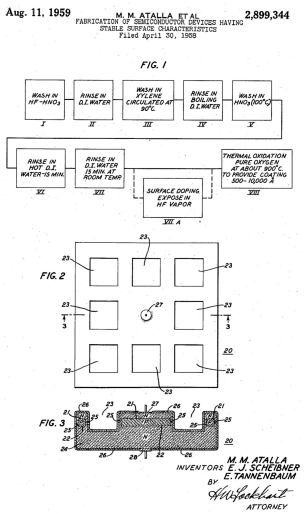
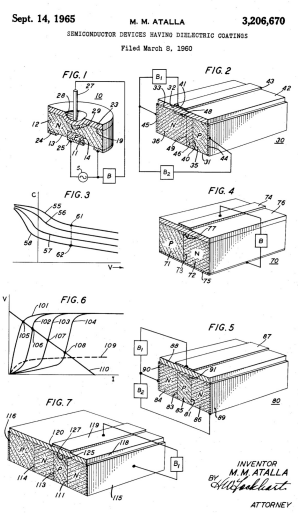
Atalla (1959 & 1965)





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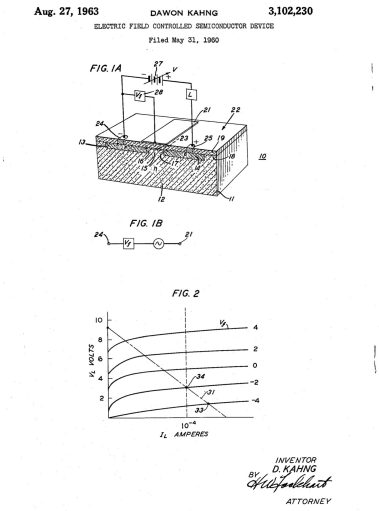
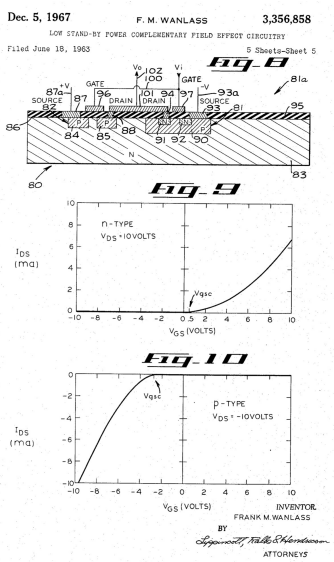
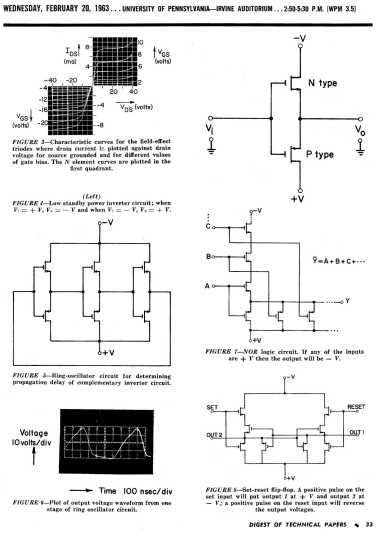
Kahng (1963)



13

Wanlass, Sah (1963) MOS -> CMOS





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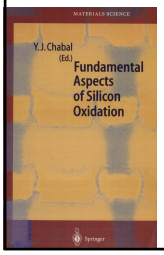
Si and SiO_2 – The chicken and the egg



An ideal interface is one where all of the atomic bonds are satisfied through couplings between the two layers. The successful MOSFET is very sensitive to the degree of interface perfection. Silicon dioxide on silicon is the combination of materials that comes closest to this ideal, with only one electrically active imperfection (defect) for every 100000 surface atoms. This is truly remarkable when one realizes that the two materials are so different, the oxide being an amorphous insulator and the silicon a high quality, single crystal, semiconductor. Hans Quiesser, in his exciting book, Conquest of the Microchip [14], describes the early difficulties of surface passivation and writes: "what finally saved the day was that an incredibly stable oxide of silicon can be wrapped around the crystal to protect it." Another historical account, The History of Engineering & Science in the Bell System [15], describes "surface state problems were resolved by an unexpected discovery .... Kahng and Atalla found that silicon and clean, thermally grown SiO_2 interfaces contain sufficiently small surface states to realize a true field effect transistor in silicon." The

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Self-Aligned Gates

Solid-State Electronics Pergamon Press 1968. Vol. 11, pp. 653–660. Printed in Great Britain

METAL–NITRIDE–OXIDE–SILICON FIELD-EFFECT TRANSISTORS, WITH SELF-ALIGNED GATES*

J. C. SARACE,† R. E. KERWIN, D. L. KLEIN‡ and R. EDWARDS
Bell Telephone Laboratories, Inc.,
Murray Hill, New Jersey, U.S.A.

(*Received* 2 *January* 1968; *in revised form* 16 *February* 1968)

Abstract—Silicon insulated-gate field-effect transistors (FETs) have been fabricated by processes involving relatively non-critical photoresist and self-limiting etching steps. Important features of the method include the formation of the gate insulator under extremely clean conditions, incorporation of an alkali ion barrier (silicon nitride) to achieve stable device characteristics and automatic alignment of the gate electrode with respect to source and drain. The gate insulator, comprising 600 Å of grown silicon dioxide covered with 400 Å of silicon nitride, is formed at the beginning of fabrication. Thus, the Si-SiO_2 interface is established at a point where the best state-of-the-art cleaning techniques can be applied to the starting material. A thick (8000 Å) layer of SiO_2 is pyrolytically deposited over the nitride to minimize contact capacitances in the finished structure. This must be removed from the active device region, and advantage is taken of the difference in etch rate between SiO_2 and silicon nitride to ensure a well-controlled gate insulator thickness. Thus the nitride layer serves the dual function of providing a barrier to mobile ions in the completed structure, and of acting as an etch-resistant layer during fabrication to achieve control over geometry.

A polycrystalline layer of silicon is used to form the gate electrode, which is shaped early in the process, and is used to define the limits of the source and drain windows. This aspect of the fabrication assures self-alignment of the gate electrode with respect to source and drain. During the diffusion of source and drain regions the polycrystalline silicon is rendered sufficiently conductive that no metallization of the gate electrode is required, except at one end for contacting purposes. This eliminates the need for a critical photoresist alignment.

Both *n* and *p* induced-channel (enhancement) devices have been made with this process. Turn-on voltages at 10 μA drain current of +1.35 V (*n*-channel) and −2.6 V (*p*-channel) with less than 12 per cent spread over a slice were obtained. Analysis of the device characteristics indicates field-effect mobilities of 335 and 233 cm^2/V-sec for the *n*- and *p*-channel devices respectively. Aging behavior under bias at 300°C indicates the presence of residual mobile positive charge of the order of 1.5×10^{11} charges/cm^2, resulting in turn-on voltage shifts of less than 1 V over several hundred hr with +10 V applied to the gate.

Résumé—Les transistors d'effet de champ à porte isolée ont été fabriqués par des procédés comprenant des étapes de corrosion auto-limitatives et une photo-résistance non-critique. Parmi les importantes caractéristiques de la méthode sont incluses la formation de l'isolement de porte sous des conditions extrêmement propres, l'incorporation d'une barrière alcaline d'ion (silicium nitré) pour pouvoir atteindre des caractéristiques de dispositif stable et un alignement automatique de l'électrode de porte par rapport à la source et au drain. L'isolement de porte, comprenant 600 Å de bioxide de silicium développé couvert le 400 Å de silicium nitré est formé au début de la fabrication. Donc, l'interface Si–O_2Si est établi à un point où les techniques de nettoyage les plus avancées peuvent être appliquées au matériau de départ. Une épaisse couche (800 Å) de O_2Si est déposée pyrolitiquement sur l'ensemble pour minimiser les capacités de contact dans la structure finale. Celle-ci doit être retirée de la région active du dispositif et on profite de la différence du taux de corrosion entre PO_2Si et le silicium nitré

* Presented at the Metallurgical Society (AIME) Meeting, New York, August (1967).
† Present address: RCA Laboratories, Princeton, New Jersey.
‡ Present address: IBM Corporation, East Fishkill Facilities.

METAL-NITRIDE-OXIDE-SILICON FIELD-EFFECT TRANSISTORS, SELF-ALIGNED GATES 655

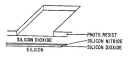


FIG. 1. Definition of general gate area.

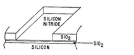


FIG. 2. Upper silicon dioxide layer removed in gate area.

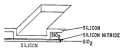


FIG. 3. Silicon evaporation in gate area.

FIG. 4. Definition of source and drain areas.

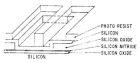


FIG. 5. Silicon removal from source and drain areas.

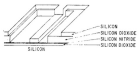
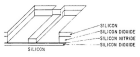


FIG. 6. Excess silicon dioxide removed from source and drain areas.



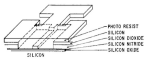


FIG. 7. Definition of contact pads on upper surface.

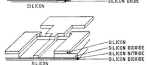


FIG. 8. Excess silicon removed from top surface.

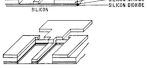


FIG. 9. Silicon nitride and silicon dioxide removed from source and drain.

Note: In his recent book "Silicio", F. Faggin gives a slightly different story of who actually invented what

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Problems and Predictions

"Prediction is very difficult, especially about the future"

Niels Bohr

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Past predictions (1971)

Solid-State Electronics, 1972, Vol. 15, pp. 819–829. Pergamon Press. Printed in Great Britain

FUNDAMENTAL LIMITATIONS IN MICROELECTRONICS – I. MOS TECHNOLOGY*

B. HOENEISEN and C. A. MEAD
California Institute of Technology, Pasadena, California 91109, U.S.A.

(*Received* 11 *August* 1971; *in revised form* 8 *November* 1971)

The minimum channel length of a 2V transistor is $\approx 0.4\,\mu$m. This length is a factor of 10 smaller than the channel of the smallest present day devices. The mask alignment tolerances required to manufacture such a device are within the capabilities of electron beam pattern generation techniques. Thus we can envision fully dynamic or complementary integrated silicon chips with up to $\approx 3 \times 10^7$ MOS transistors per cm², operating in the 10 to 30 MHz range, as shown in Fig. 1.

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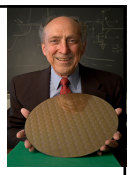
The foundation paper (1974)



IEEE JSSC, VOL. SC-9, NO. 5, Oct. 1974

Design of Ion-Implanted MOSFET's with Very Small Physical Dimensions

ROBERT H. DENNARD, MEMBER, IEEE, FRITZ H. GAENSSLEN, HWA-NIEN YU, MEMBER, IEEE, V. LEO RIDEOUT, MEMBER, IEEE, ERNEST BASSOUS, AND ANDRE R. LEBLANC, MEMBER, IEEE

Classic Paper

This paper considers the design, fabrication, and characterization of very small MOSFET switching devices suitable for digital integrated circuits using dimensions of the order of 1 μ. Scaling relationships are presented which show how a conventional MOSFET can be reduced in size. An improved small device structure is presented that uses ion implantation to provide shallow source and drain regions and a nonuniform substrate doping profile. One-dimensional models are used to predict the substrate doping profile and the corresponding threshold voltage versus source voltage characteristic. A two-dimensional current transport model is used to predict the relative degree of short-channel effects for different device parameter combinations. Polysilicon-gate MOSFET's with channel lengths as short as 0.5 μ were fabricated, and the device characteristics measured and compared with predicted values. The performance improvement expected from using these very small devices in highly miniaturized integrated circuits is projected.

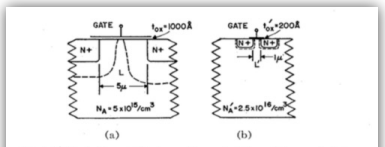


Fig. 1. Illustration of device scaling principles with $\kappa = 5$. (a) Conventional commercially available device structure. (b) Scaled-down device structure.

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Pre-Dennard Scaling

RADIO CORPORATION OF AMERICA
RCA LABORATORIES

SPECIAL SCIENTIFIC REPORT

INVESTIGATIONS OF FUNDAMENTAL LIMITATIONS DETERMINING THE ULTIMATE SIZE OF MICROSTRUCTURES

CONTRACT NO. AF19(604)-8040

PREPARED FOR
ELECTRONICS RESEARCH DIRECTORATE
AIR FORCE CAMBRIDGE RESEARCH LABORATORIES
OFFICE OF AEROSPACE RESEARCH
UNITED STATES AIR FORCE
BEDFORD, MASSACHUSETTS

PROJECT NO. 5633
TASK NO. 56332

REPORT DATE: FEBRUARY 28, 1962

DAVID SARNOFF RESEARCH CENTER
PRINCETON, NEW JERSEY

Summarizing the scaling laws for field-effect devices, with limitations cited above:

length	(1)
area	(2)
doping	(-1)
fixed charge	(2)
electric field	(0)
voltage	(1)
capacitance	(1)

current	(1)
resistance	(0)
time constant, RC	(1)
power	(2)
area power density	(0).

These relations and limitations will be discussed quantitatively following a review of bipolar transistor scaling relationships.

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Past predictions (1989)

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 36, NO. 9, SEPTEMBER 1989

MOSFET Scaling Limits Determined by Subthreshold Conduction

JOSEPH M. PIMBLEY, MEMBER, IEEE, AND JAMES D. MEINDL, FELLOW, IEEE

mation and ultrathin (< 50 Å) gate insulators. With vanishingly small (< 50 Å) junction depth, a 30-Å gate oxide dielectric and a channel acceptor concentration of 2 × 10^{18} per cubic centimeter, one may achieve acceptably low subthreshold conduction at effective channel lengths down to 0.06 μm at an operating temperature of 300 K.

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Past predictions (2001)

PROCEEDINGS OF THE IEEE, VOL. 89, NO. 3, MARCH 2001

Device Scaling Limits of Si MOSFETs and Their Application Dependencies

DAVID J. FRANK, MEMBER, IEEE, ROBERT H. DENNARD, FELLOW, IEEE,
EDWARD NOWAK, MEMBER, IEEE, PAUL M. SOLOMON, FELLOW, IEEE, YUAN TAUR, FELLOW, IEEE,
AND HON-SUM PHILIP WONG, FELLOW, IEEE

The scale length theory that has been presented here provides a useful framework within which to understand the tradeoff between channel length and short channel effects. Using this theory in conjunction with the various limiting effects, we have projected that bulk-like CMOS should be extendible down to about 14-nm nominal channel length for high-performance logic and ~35 nm for very low power applications, with intermediate applications falling in between.

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Brief review of breakthroughs in the last 20 years

- Lithography
  - Computational lithography
  - Immersion lithography
  - EUV
  - …
- Strained Silicon
- High-K Metal Gate
- FinFET

23

Problem #1: velocity saturation

Modern transistors operate here.

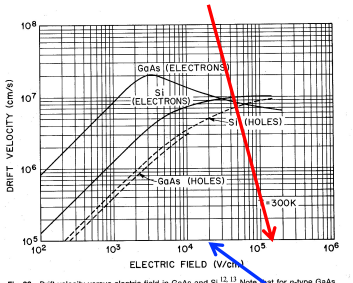


Fig. 23 Drift velocity versus electric field in GaAs and Si.[12, 13] Note that for *n*-type GaAs, there is a region of negative differential mobility.

Si Detectors operate here

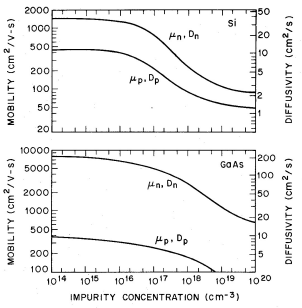


Fig. 3 Mobilities and diffusivities in Si and GaAs at 300 K as a function of impurity concentration.[4, 5]

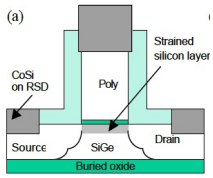
from S. Sze, Semiconductor Devices

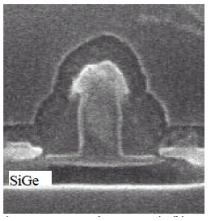
24

Faster carriers: Strained Silicon (1)

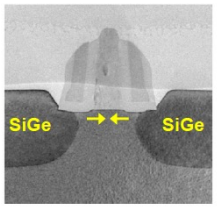
NMOS (strain)

PMOS (compress)





from B.H. Lee et al., IEDM 2002

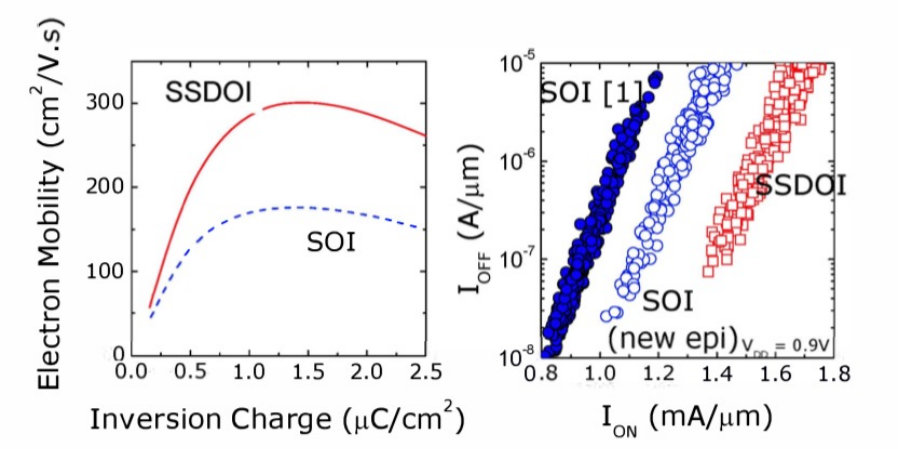


from T. Ghani et al., IEDM 2003

improvement. Dramatic (>50%) strain induced hole channel mobility improvement is demonstrated for our devices with 17% Ge composition. Fig. 2 shows significant improvement

25

Strained Silicon (2)

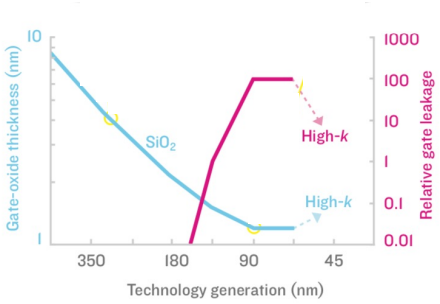


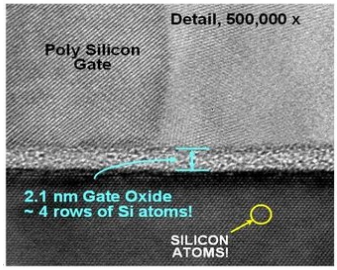
from A. Khakifirooz et al., Symp VLSI Tech 2012

26

Problem #2: leakage through gate oxide

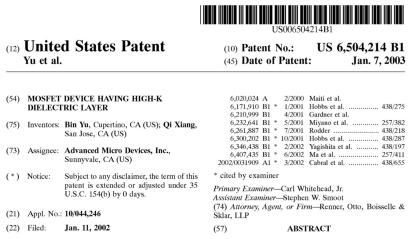
from M. Bohr et al., IEEE Spectrum Oct. 2007





Gate oxide in a 130nm technology

High-K gate dielectric



US006504214B1

(12) **United States Patent**
Yu et al.

(10) **Patent No.: US 6,504,214 B1**
(45) **Date of Patent: Jan. 7, 2003**

(54) **MOSFET DEVICE HAVING HIGH-K DIELECTRIC LAYER**

(75) Inventors: **Bin Yu**, Cupertino, CA (US); **Qi Xiang**, San Jose, CA (US)

(73) Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/044,246**

(22) Filed: **Jan. 11, 2002**

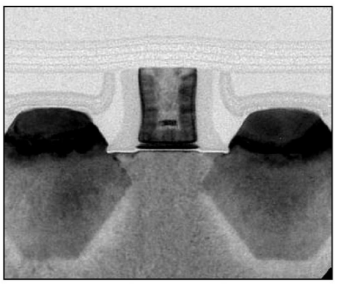
6,020,024	A	2/2000	Maiti et al.
6,171,910	B1 *	1/2001	Hobbs et al. 438/275
6,210,999	B1	4/2001	Gardner et al.
6,232,641	B1 *	5/2001	Miyano et al. 257/382
6,261,887	B1 *	7/2001	Rodder 438/238
6,300,202	B1 *	10/2001	Hobbs et al. 438/287
6,346,438	B1 *	2/2002	Yagishita et al. 438/197
6,407,435	B1 *	6/2002	Ma et al. 257/411
2002/0031909	A1 *	3/2002	Cabral et al. 438/655

* cited by examiner

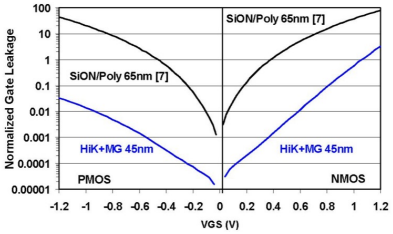
Primary Examiner—Carl Whitehead, Jr.
Assistant Examiner—Stephen W. Smoot
(74) *Attorney, Agent, or Firm*—Renner, Otto, Boisselle & Sklar, LLP

(57) **ABSTRACT**

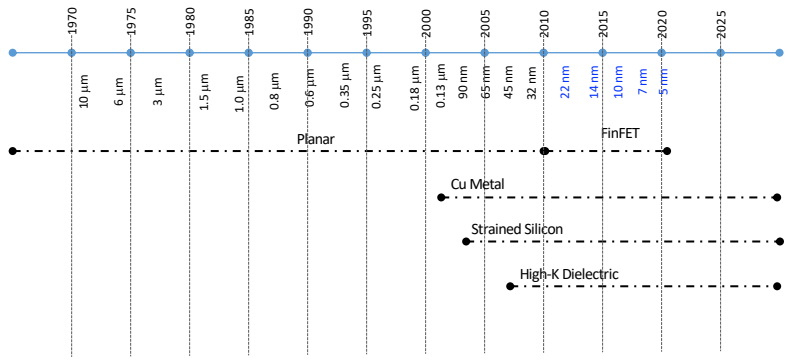
greater detail below. Although other materials can be selected for the gate dielectric **34**, hafnium oxide (e.g., HfO_2), zirconium oxide (e.g., ZrO_2), cerium oxide (e.g., CeO_2), aluminum oxide (e.g., Al_2O_3), titanium oxide (e.g., TiO_2), yttrium oxide (e.g., Y_2O_3) and barium strontium titanate (BST) are example suitable materials for the gate dielectric **34**. In addition, all binary and ternary metal oxides and ferroelectric materials having a K higher than, in one embodiment, about twenty (20) can be used for the gate dielectric **34**.



from K. Mistry et al., IEDM 2007



CMOS Timeline



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What is actually "wrong" with infinite scaling?

- The 1974 Scaling theory (Dennard et al.) essentially looked at the transistor as a two-dimensional (planar) structure.
  - This worked ok up until about 2010
- Classical scaling is only as good as one manages to keep effects in the third dimension ("short channel effects") small, but it fails to describe the behavior of a MOS device when all dimensions are reduced, and doping are increased, and voltages are not reduced (enough).

30

Raising from the surface

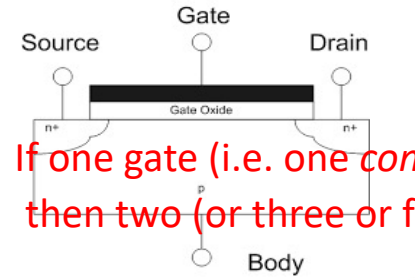
31

Short channel effects

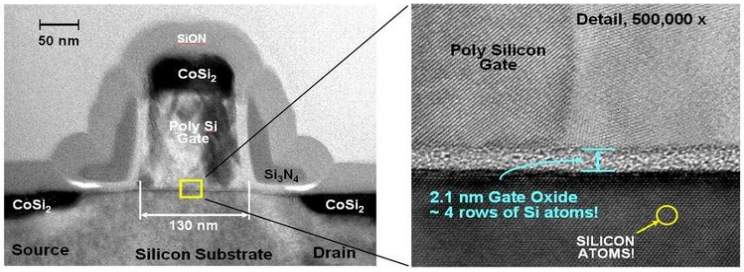
- When the channel (L) of a MOSFETS becomes shorter than about .35 um, the following phenomena start appearing:
  - Velocity Saturation
  - Hot Carrier Degradation
  - Drain Induced Barrier Lowering (DIBL)
  - V_t dependence on L
  - …

32

How to get to FINFETs



If one gate (i.e. one *control surface*) is good, then two (or three or four) are even better



33

Toshiba 1983

Solid-State Electronics Vol. 27, Nos. 8/9, pp. 827–828, 1984
Printed in Great Britain

0038-1101/84 $3.00 + .00
© 1984 Pergamon Press Ltd.

CALCULATED THRESHOLD-VOLTAGE CHARACTERISTICS OF AN XMOS TRANSISTOR HAVING AN ADDITIONAL BOTTOM GATE

(*Received* 30 *May* 1983; *in revised form* 24 *August* 1983)

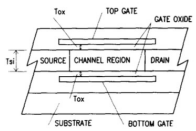


Fig. 1. Schematic cross-sectional structure of an XMOS transistor having an additional bottom gate which is symmetrically placed to a top gate with a channel region between them. "X" originates from Greek capital letter of xi as this structure resembles its shape.

Electronic Device Division, Electrotechnical Laboratory, Sakura-mura, Ibaraki, 305, Japan

T. SEKIGAWA and Y. HAYASHI

IBM 1994

Figure 1: Schematic views of the double-gate SOI MOSFET's.

Hitachi 1991

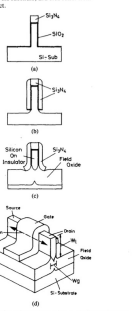
IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 38, NO. 6, JUNE 1991 1419

Impact of the Vertical SOI "DELTA" Structure on Planar Device Technology

Digh Hisamoto, *Member, IEEE*, Toru Kaga, *Member, IEEE*, and Eiji Takeda, *Senior Member, IEEE*

Abstract—A fully depleted lean channel transistor (DELTA) with its gate incorporated into a new vertical ultra-thin SOI structure is presented. In the deep-submicrometer region, selective oxidation produces and isolates an ultra-thin SOI MOSFET that has high crystalline quality, as good as that of conventional bulk single-crystal devices. Experiments and three-dimensional simulations have shown that this new gate structure effectively suppresses leakage, and that the vertical ultra-thin SOI structure provides expected device characteristics, reduction in short-channel effects, minimized subthreshold swing, and high transconductance.

is required. Moreover, it is evident that these structures are difficult to contact to the substrate, and thus suffer from a substrate floating effect.



(a)–(c) Process flow of selective oxidation. (d) Schematic cross section of DELTA.

Berkely 2000

2320 IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 47, NO. 12, DECEMBER 2000

FinFET—A Self-Aligned Double-Gate MOSFET Scalable to 20 nm

Digh Hisamoto, *Member, IEEE*, Wen-Chin Lee, Jakub Kedzierski, Hideki Takeuchi, Kazuya Asano, *Member, IEEE*, Charles Kuo, Erik Anderson, Tsu-Jae King, Jeffrey Bokor, *Fellow, IEEE*, and Chenming Hu, *Fellow, IEEE*

Abstract—MOSFETs with gate length down to 17 nm are reported. To suppress the short channel effect, a novel self-aligned double-gate MOSFET, FinFET, is proposed. By using boron-doped $Si_{0.4}Ge_{0.6}$ as a gate material, the desired threshold voltage was achieved for the ultrathin body device. The quasiplanar nature of this new variant of the vertical double-gate MOSFETs can be fabricated relatively easily using the conventional planar MOSFET process technologies.

Index Terms—Fully depleted SOI, MOSFET, poly SiGe, short-channel effect.

I. INTRODUCTION

TO DEVELOP sub-50-nm MOSFETs, the double-gate structure has been widely studied. This is because

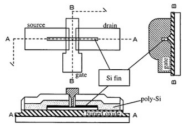


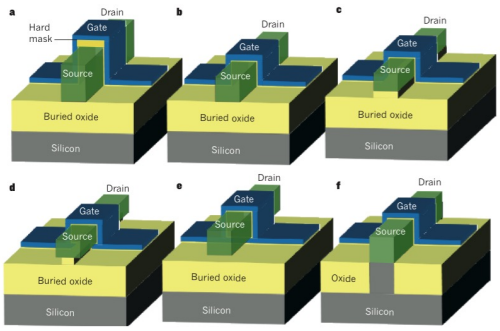
Fig. 1. FinFET typical layout and schematic cross sectional structures.

(*) A Japanese 1980 patent pre-dates all these publications but its content and validity is confusing.

34

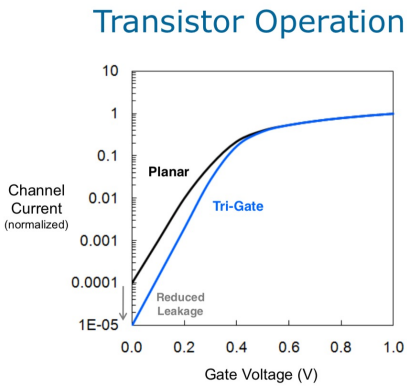
Multi-gate devices

- Intel: Tri-gate
- TSMC, GF, Samsung: Finfets



from: Ferain, "Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors ",

Subthreshold slope improvement

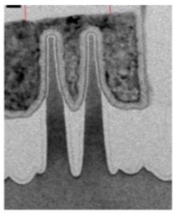


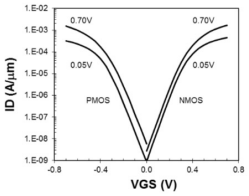
Intel @ 22 nm

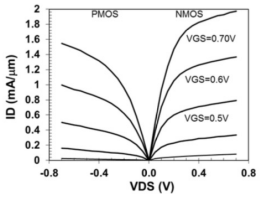
from: M. Bohr (Intel) , Intel's Revolutionary 22 nm Transistor Technology, May 2011

10 nm Finfet

from: A. Auth (Intel), A 10nm High Performance and Low Power CMOS Technology…, IEDM 2017



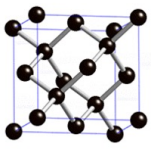


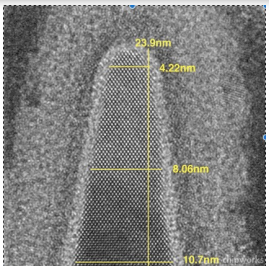


FinFET dimensions

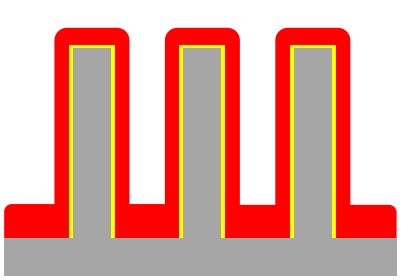
From the ITRS 2011 report

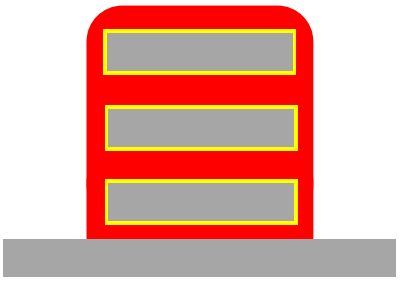
Year of Production	*2013*	*2015*	*2017*	*2019*	*2021*	*2023*	*2025*	*2028*
FinFET Fin Width (new) (nm)	**7.6**	**7.2**	**6.8**	**6.4**	**6.1**	**5.7**	**5.4**	**5.0**

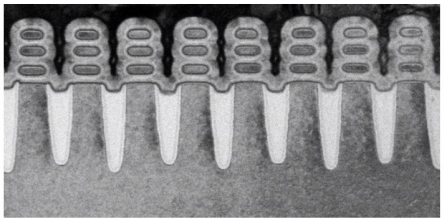


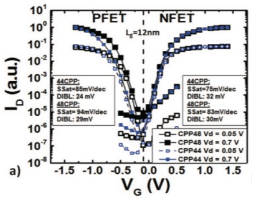


Nanosheet: a horizontal FinFET !





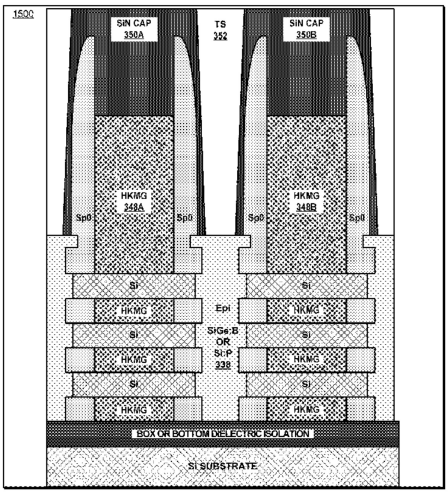




From N. Loubet – IBM – Stacked Nanosheet Gate-All-Around Transistor to Enable Scaling Beyond FinFET – VLSI Symp 2017

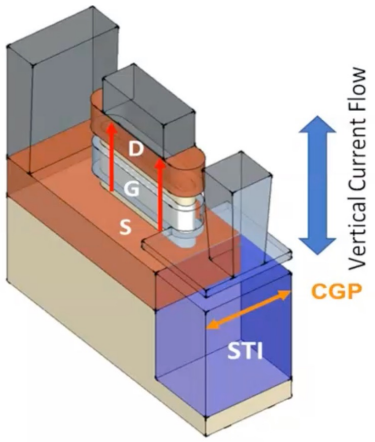
Nanosheet process flow

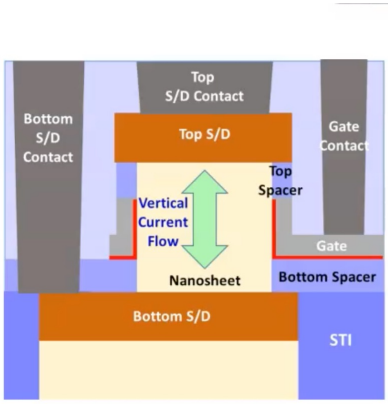
from US Patent 11,121,233 B2, owned by Tessera Tech (*)



IEDM-2021 paper 26.1

Vertical-Transport Nanosheet Technology for CMOS Scaling beyond Lateral-Transport Devices (IBM 2021)





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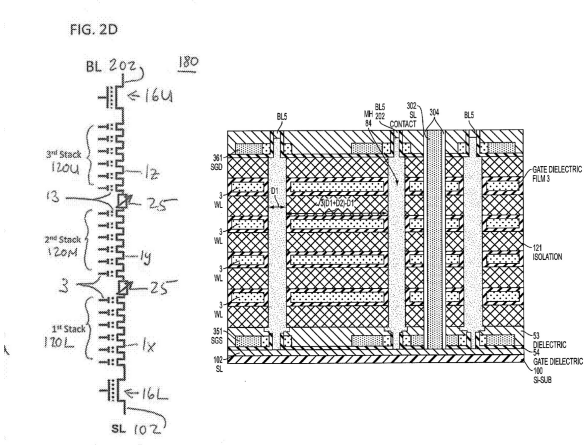
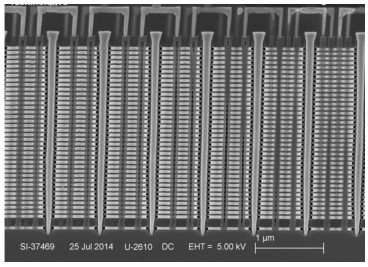
Other 'vertical' transistors

US Patent 2014/0273373A1, Samsung





3D Flash Memory, 2018

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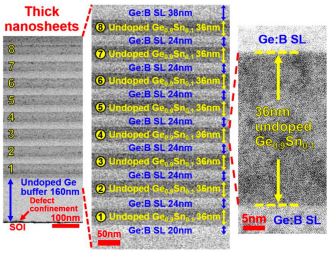
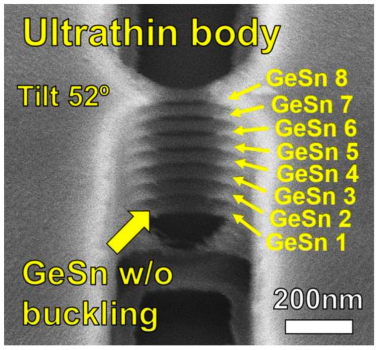
IEDM-2021 Paper 26.4

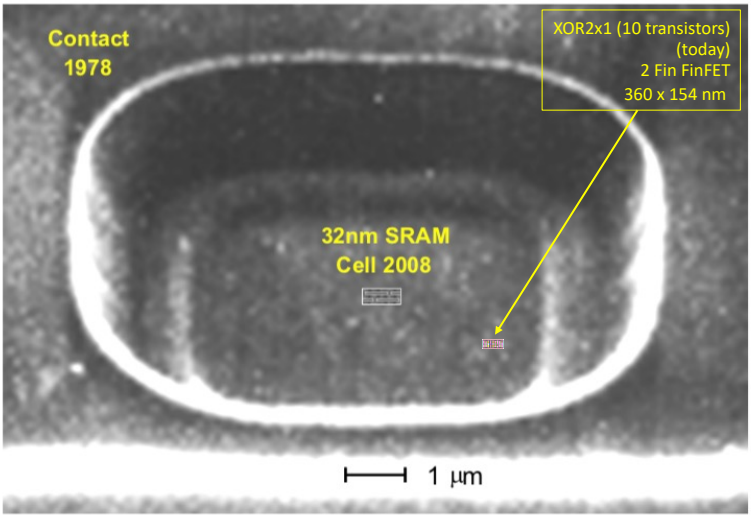
"Highly Stacked 8 Ge0.9Sn0.1 Nanosheet pFETs with Ultrathin Bodies …", NTU





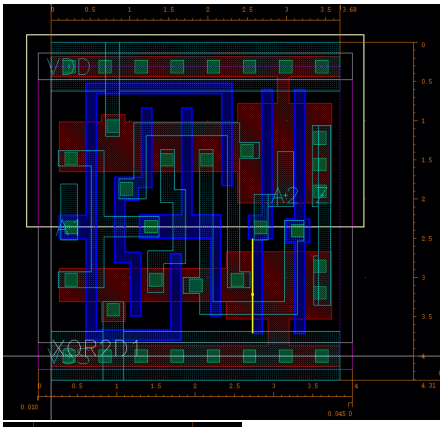
3nm Ultrathin Bodies

50 years: 1978 to 2028

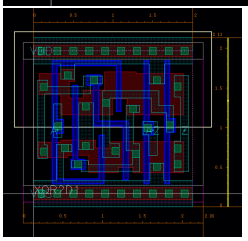


… more details

130 nm



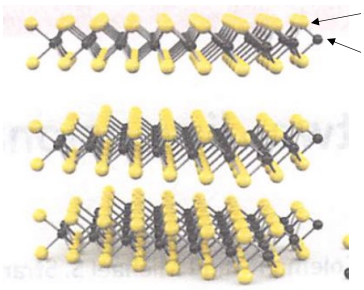
65 nm



7 nm

and what about “beyond” Nanosheets ?

Transition-Metal-Dichalcogenides



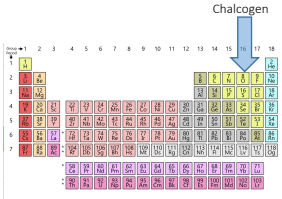
S, Se, Te

Mo, W, etc.

Advantages:

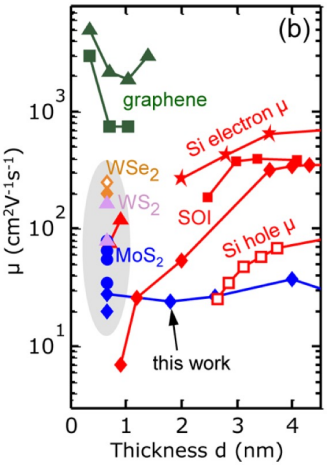
- Monolayer Channel thickness, C/2 = 0.615 nm
- High mobility
- Large bandgap, good SC effects control

Note: no doping as in Silicon
- NMOS is obtained with MoS_2
- PMOS is obtained with WSe_2



from: A. H. Wang et al., Electronics and optoelectronics of two-dimensional transition metal dichalcogenides, Nature Nanotech 7, Nov 2012

Why bother with these materials?



from: Improved Contacts to MoS2 Transistors by Ultra-High Vacuum Metal Deposition, Nano Lett. 2016, 16, 3824-3830

Answer: for extremely thin sheets the mobility of TMD materials is better than the one of Silicon (for the same thickness)

47

and yet...

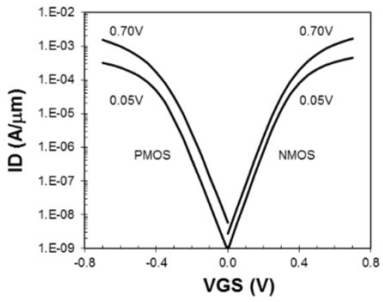
https://en.wikichip.org/wiki/technology_node

Number of Semiconductor Manufacturers with a Cutting Edge Logic Fab

SilTerra										
X-FAB										
Dongbu HiTek										
ADI	ADI									
Atmel	Atmel									
Rohm	Rohm									
Sanyo	Sanyo									
Mitsubishi	Mitsubishi									
ON	ON									
Hitachi	Hitachi									
Cypress	Cypress	Cypress								
Sony	Sony	Sony								
Infineon	Infineon	Infineon								
Sharp	Sharp	Sharp								
Freescale	Freescale	Freescale								
Renesas (NEC)	Renesas	Renesas	Renesas	Renesas						
Toshiba	Toshiba	Toshiba	Toshiba	Toshiba						
Fujitsu	Fujitsu	Fujitsu	Fujitsu	Fujitsu						
TI	TI	TI	TI	TI						
Panasonic	Panasonic	Panasonic	Panasonic	Panasonic	Panasonic					
STMicroelectronics	STM	STM	STM	STM	STM					
HLMC	HLMC		HLMC	HLMC	HLMC					
UMC	UMC	UMC	UMC	UMC	UMC			UMC		
IBM	IBM	IBM	IBM	IBM	IBM	IBM				
SMIC	SMIC	SMIC	SMIC	SMIC	SMIC			SMIC		
AMD	AMD	AMD	GlobalFoundries	GF	GF	GF	GF	GF		
Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung
TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC
Intel	Intel	Intel	Intel	Intel	Intel	Intel	Intel	Intel	Intel	Intel
180 nm	130 nm	90 nm	65 nm	45 nm/40 nm	32 nm/28 nm	22 nm/20 nm	16 nm/14 nm	10 nm	7 nm	5 nm

Classical "L" | "Scaled "L"

48



New Ideas

Negative Capacitance Transistors (Ferroelectric Transistors)

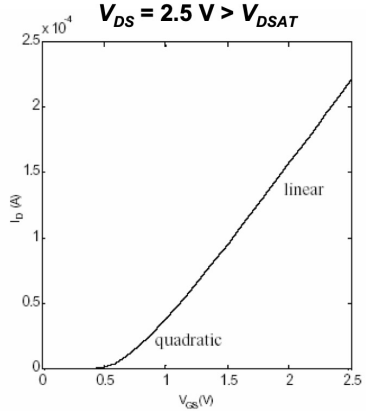
Adiabatic Circuits

Tunneling Transistors

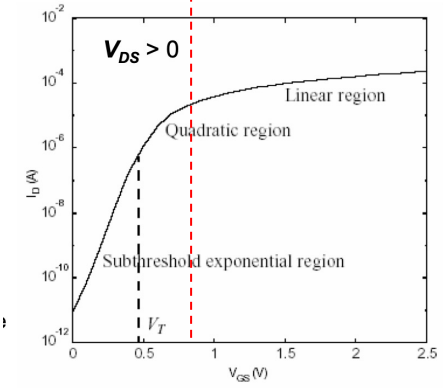
Turning on a MOSFET

Short-channel MOSFET

$V_{DS} = 2.5\ V > V_{DSAT}$



Max V_{dd} in < 28nm



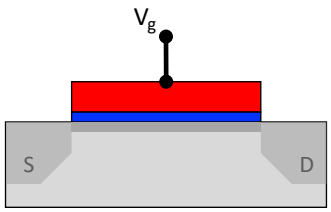
What does Boltzmann have to do with microelectronics?

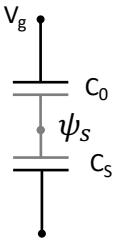
$$SS = \frac{\partial V_g}{\partial(logI_d)} = \frac{\partial V_g}{\partial \psi_s} * \frac{\partial \psi_s}{\partial(logI_d)}$$

$$\min\left(\frac{\partial \psi_s}{\partial(logI_d)}\right) = Ln(10) * \frac{k_B T}{q} \approx 60 \frac{mV}{decade}$$

$$\frac{\partial V_g}{\partial \psi_s} = 1 + \frac{C_S}{C_o}$$

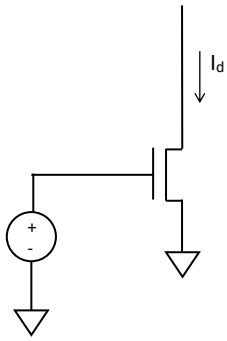
for a full derivation of this formula, see Y. Tsividis' book, page 208

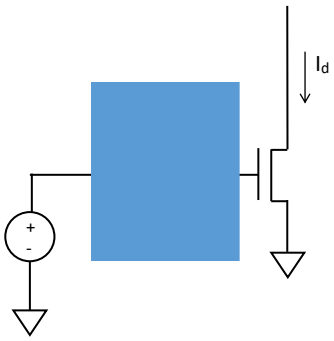




51

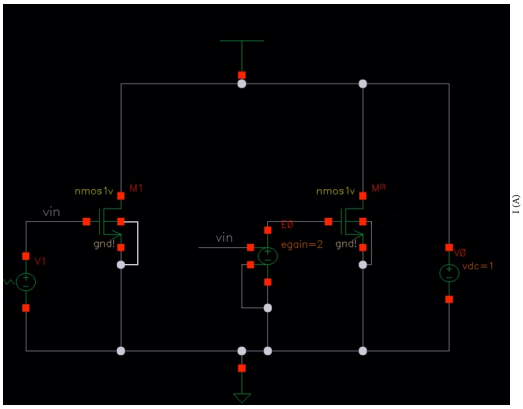
[A little Gedankenexperiment (1)]

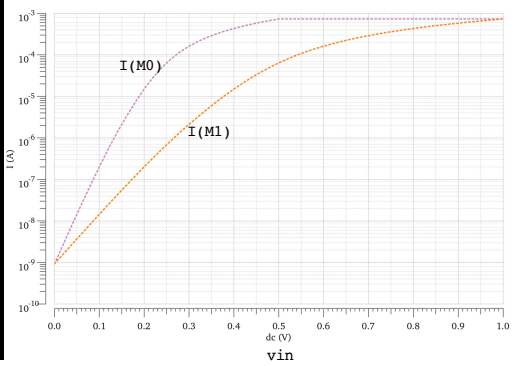




52

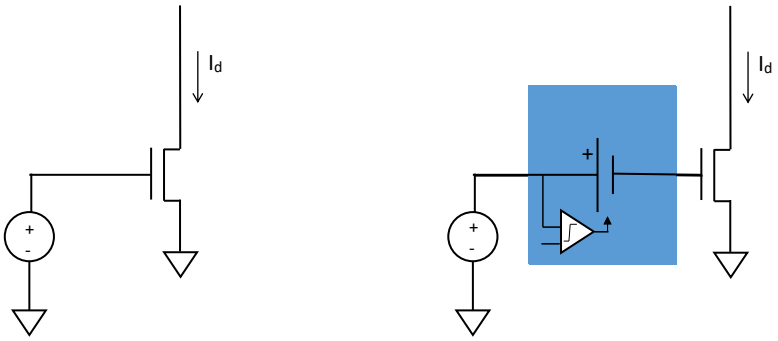
[A little Gedankenexperiment(2)]





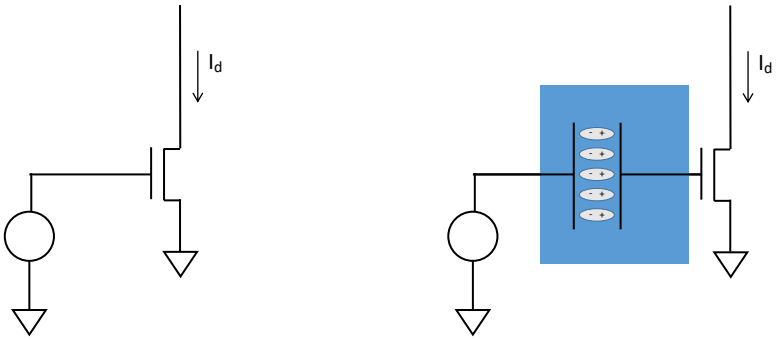
53

[A little Gedankenexperiment (3)]



54

[A little Gedankenexperiment (4)]



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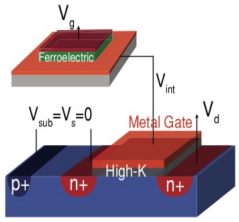
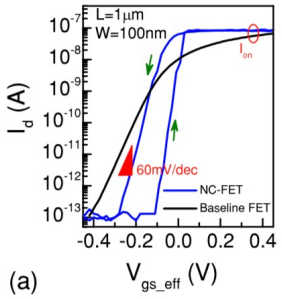
A real exercise

PZT (Lead-Zirconate-Titanate) capacitor





from: A. Saeidi et al, , "Negative Capacitance as Digital and Analog Performance Booster for Complementary MoS Transistors", EPFL, arXiv:1804.09622v2

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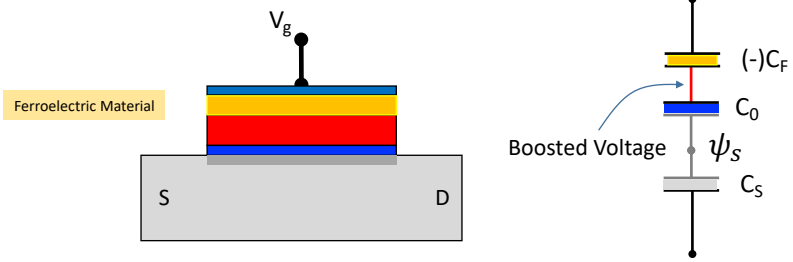
NC gate stack



@IEDM 2018, Negative Capacitance devices occupied 3 sessions and are mentioned in 16 papers

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Adiabatic Logic Circuit

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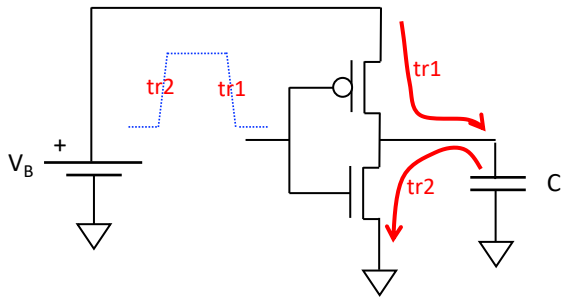
CMOS Logic: charging and discharging capacitors



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Charging a Capacitor

- A capacitor charged from a battery has a total charge:

$$Q = C * V_B$$

and the energy required to charge it is:

$$E = (C * V_B) * V_B = C * V_B^2$$

- The energy stored on a capacitor C is instead:

$$E_C = \frac{1}{2} C * V_B^2$$

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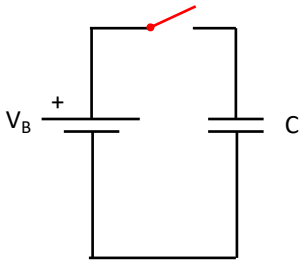
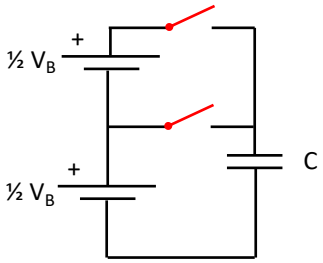
Charging capacitors with minimal effort



$$E_C = \frac{1}{2} C\, V_B^2$$

$$E_{wasted} = \frac{1}{2} C\, V_B^2$$



$$E_C = \frac{1}{2} C\, V_B^2$$

$$E_{wasted} = \frac{1}{2} C\, (\frac{V_B}{2})^2 + \frac{1}{2} C\, (\frac{V_B}{2})^2 = \frac{1}{4} C\, V_B^2$$

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Other non-Boltzmann limited devices

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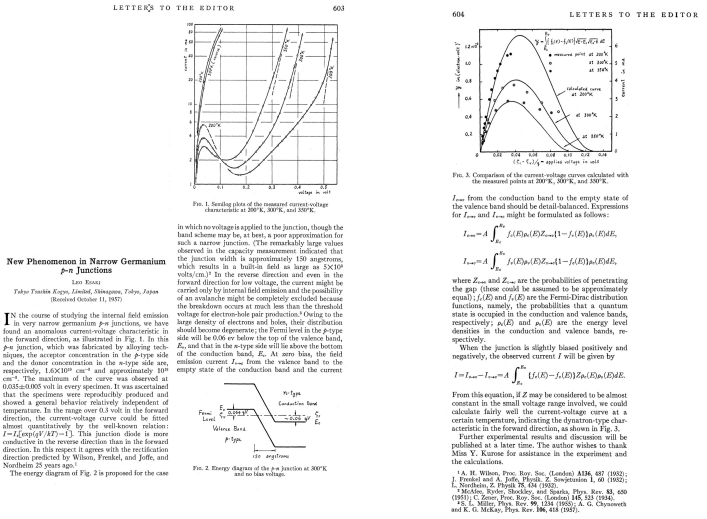
Tunnel diode

from: L. Esaki, "New Phenomenon in Narrow Germanium p-n Junctions", Phys. Rev. 1957



LETTERS TO THE EDITOR 603

New Phenomenon in Narrow Germanium p-n Junctions

LEO ESAKI

Tokyo Tsushin Kogyo, Limited, Shinagawa, Tokyo, Japan

(Received October 11, 1957)

IN the course of studying the internal field emission in very narrow germanium p-n junctions, we have found an anomalous current-voltage characteristic in the forward direction, as illustrated in Fig. 1. In this p-n junction, which was fabricated by alloying techniques, the acceptor concentration in the p-type side and the donor concentration in the n-type side are, respectively, 1.6×10^{19} cm^{-3} and approximately 10^{19} cm^{-3}. The maximum of the curve was observed at 0.035±0.005 volt in every specimen. It was ascertained that the specimens were reproducibly produced and showed a general behavior relatively independent of temperature. In the range over 0.3 volt in the forward direction, the current-voltage curve could be fitted almost quantitatively by the well-known relation: $I=I_s[\exp(qV/kT)-1]$. This junction diode is more conductive in the reverse direction than in the forward direction. In this respect it agrees with the rectification direction predicted by Wilson, Frenkel, and Joffe, and Northeim 25 years ago.[1]

The energy diagram of Fig. 2 is proposed for the case in which no voltage is applied to the junction, though the band scheme may be, at best, a poor approximation for such a narrow junction. (The remarkably large values observed in the capacity measurement indicated that the junction width is approximately 150 angstroms, which results in a built-in field as large as 5×10^5 volts/cm.[2] In the reverse direction and even in the forward direction for low voltage, the current might be carried only by internal field emission and the possibility of an avalanche might be completely excluded because the breakdown occurs at much less than the threshold voltage for electron-hole pair production.[3] Owing to the large density of electrons and holes, their distribution should become degenerate; the Fermi level in the p-type side will be 0.06 ev below the top of the valence band, E_v, and that in the n-type side will lie above the bottom of the conduction band, E_c. At zero bias, the field emission current $I_{e\to c}$ from the valence band to the empty state of the conduction band and the current

FIG. 2. Energy diagram of the p-n junction at 300°K and no bias voltage.

FIG. 3. Comparison of the current-voltage curves calculated with the measured points at 200°K, 300°K, and 350°K.

604 LETTERS TO THE EDITOR

$I_{c\to e}$ from the conduction band to the empty state of the valence band should be detail-balanced. Expressions for $I_{e\to c}$ and $I_{c\to e}$ might be formulated as follows:

$$I_{e\to c}=A\int_{E_c}^{E_c'} f_e(E)\rho_e(E)Z_{e\to c}\{1-f_c(E)\}\rho_c(E)dE,$$

$$I_{c\to e}=A\int_{E_v}^{E_v'} f_c(E)\rho_c(E)Z_{c\to e}\{1-f_e(E)\}\rho_e(E)dE,$$

where $Z_{e\to c}$ and $Z_{c\to e}$ are the probabilities of penetrating the gap (these could be assumed to be approximately equal); $f_e(E)$ and $f_c(E)$ are the Fermi-Dirac distribution functions, namely, the probabilities that a quantum state is occupied in the conduction and valence bands, respectively; $\rho_c(E)$ and $\rho_e(E)$ are the energy level densities in the conduction and valence bands, respectively.

When the junction is slightly biased positively and negatively, the observed current I will be given by

$$I=I_{e\to c}-I_{c\to e}=A\int_{E_v}^{E_c'}\{f_e(E)-f_c(E)\}Z\rho_c(E)\rho_e(E)dE.$$

From this equation, if Z may be considered to be almost constant in the small voltage range involved, we could calculate fairly well the current-voltage curve at a certain temperature, indicating the dynatron-type characteristic in the forward direction, as shown in Fig. 3.

Further experimental results and discussion will be published at a later time. The author wishes to thank Miss Y. Kurose for assistance in the experiment and the calculations.

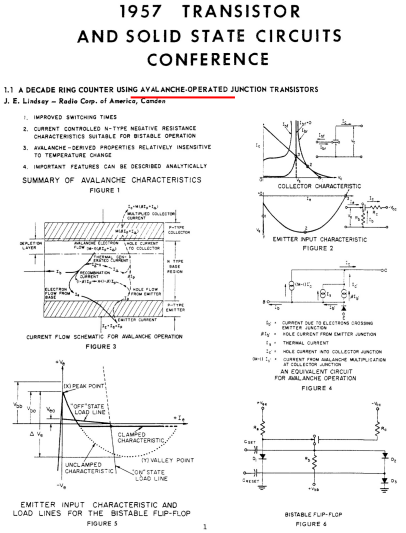
[1] A. H. Wilson, Proc. Roy. Soc. (London) **A136**, 487 (1932); J. Frenkel and A. Joffe, Physik. Z. Sowjetunion **1**, 60 (1932); L. Nordheim, Z. Physik **75**, 434 (1932).

[2] W. Shockley and W. T. Read, Jr., Phys. Rev. **83**, 650 (1951); C. Lanet, Proc. Phys. Soc. (London) **A65**, 533 (1952).

[3] S. L. Miller, Phys. Rev. **99**, 1234 (1955); A. G. Chynoweth and K. G. McKay, Phys. Rev. **106**, 418 (1957).

Devices with internal gain

from: J. Lindsay, "A decade ring counter usign avalanche operated junction transistors", IEEE 1957 Transistor and Solid State Circuit Conference



1957 TRANSISTOR AND SOLID STATE CIRCUITS CONFERENCE

1.1 A DECADE RING COUNTER USING AVALANCHE-OPERATED JUNCTION TRANSISTORS

J. E. Lindsay – Radio Corp. of America, Camden

1. IMPROVED SWITCHING TIMES
2. CURRENT CONTROLLED N-TYPE NEGATIVE RESISTANCE CHARACTERISTICS SUITABLE FOR BISTABLE OPERATION
3. AVALANCHE-DERIVED PROPERTIES RELATIVELY INSENSITIVE TO TEMPERATURE CHANGE
4. IMPORTANT FEATURES CAN BE DESCRIBED ANALYTICALLY

SUMMARY OF AVALANCHE CHARACTERISTICS
FIGURE 1

CURRENT FLOW SCHEMATIC FOR AVALANCHE OPERATION
FIGURE 3

COLLECTOR CHARACTERISTIC

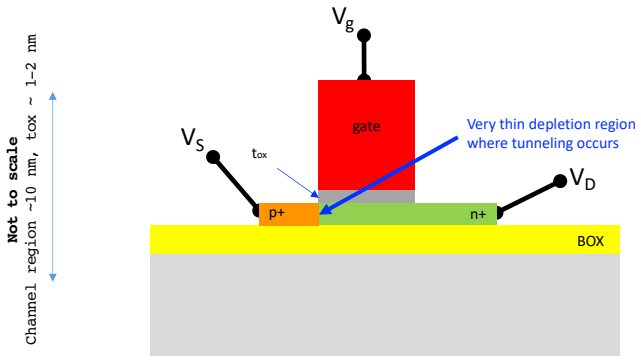
EMITTER INPUT CHARACTERISTIC
FIGURE 2

AN EQUIVALENT CIRCUIT FOR AVALANCHE OPERATION
FIGURE 4

EMITTER INPUT CHARACTERISTIC AND LOAD LINES FOR THE BISTABLE FLIP-FLOP
FIGURE 5

BISTABLE FLIP-FLOP
FIGURE 6

Tunneling Transistors: Principle



- Very highly doped S and D
- $V_S < V_D$

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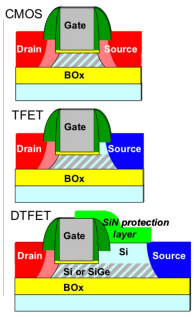
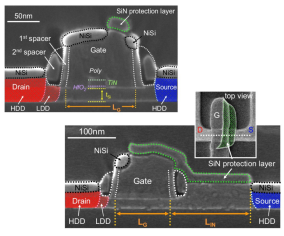
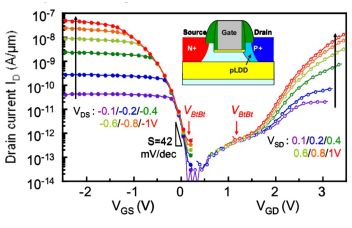
Tunneling Transistors: Example

from: F. Mayer et al., "Impact of SOI, Si1-xGexOI and GeOI substrates on CMOS compatible Tunnel FET performance", IEDM 2008







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Summary: low supply voltage devices

- Currently with devices powered between 0.8 and 1.2 V, we use about 400-500 mV (~70-80 mV/dec * 6 dec) to turn them on.
- If one could reduce reduce the "transition region" to about 50 mV (SS ~ 50/6 = 8-10 mV/dec)
  - Then it would be conceivable to have a digital logic supply at 150 mV therefore saving:

$$\text{Power saving: } (1.0)^2 / (0.15)^2 = 44 \text{ times}$$

(i.e. you could recharge your mobile phone less than once per month)

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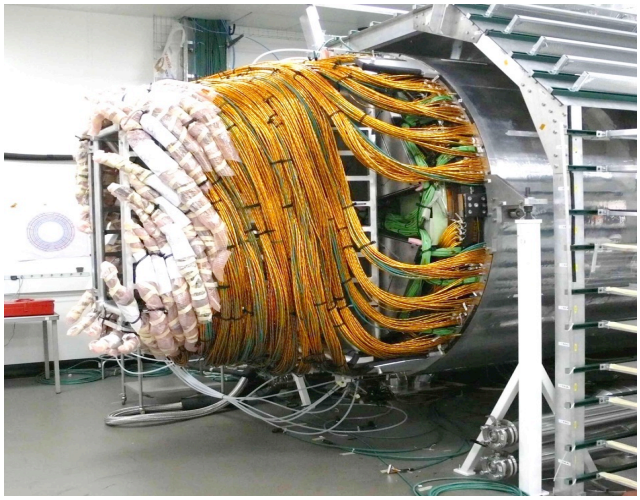
… and for the CMS tracker…



… in fact the CMS tracker used 2.5V transistors. If we could use 0.25V transistors the savings in power would be $(2.5)^2 / (0.25)^2 = 100$ times less cables!!!

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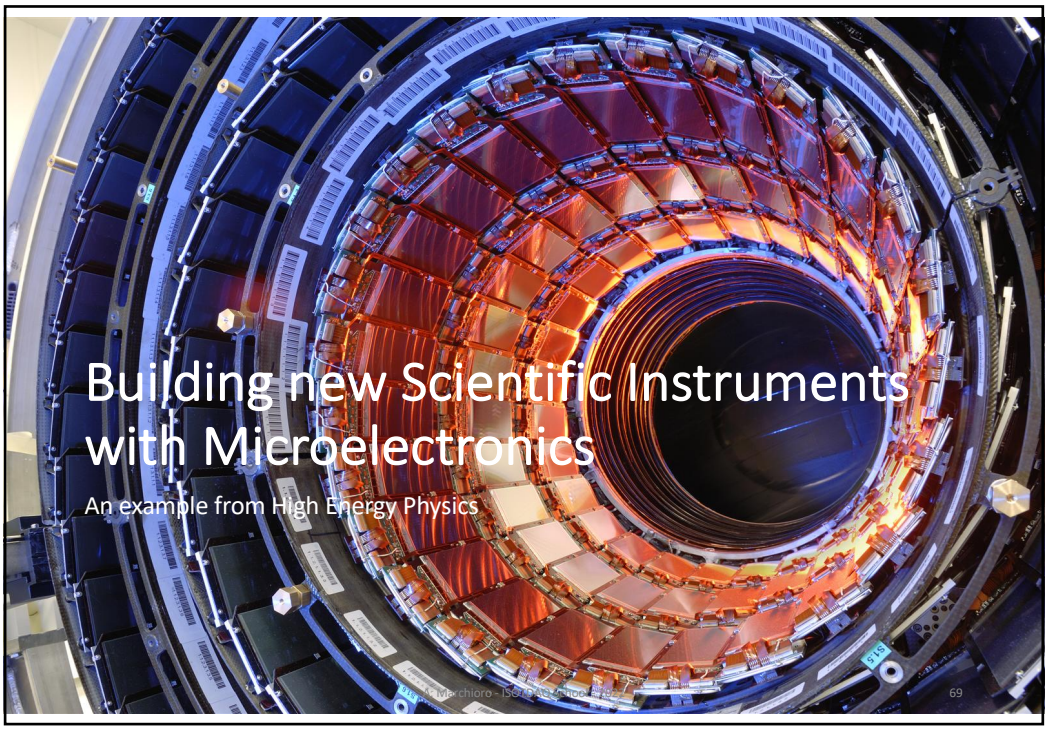

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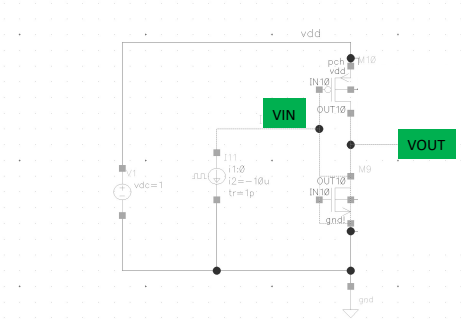
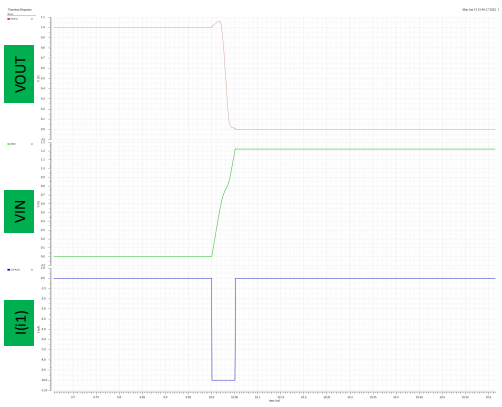
How many electrons are needed to switch a logic gate ?





- **65 nm: 10uA x 50ps ~ 3000 e⁻**
- **28 nm: ~ 850 e⁻**

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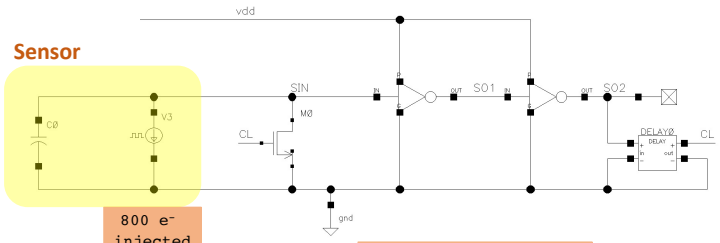
Digital Amplifier for small cell Si sensor



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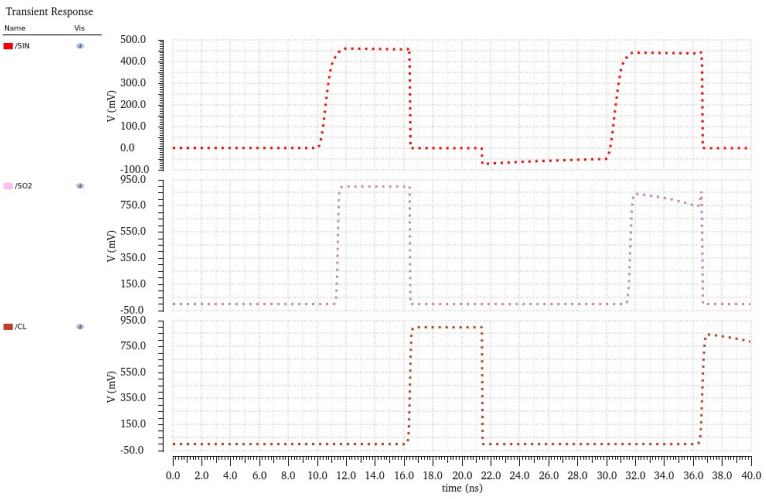
Digital Amplifier (2)



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And what about 5 nm?

- A 5 nm "transistor" switches with < ~100 e^- input signal
- That is the signal produced by a MIP particle in about 1um of silicon

Significant issues still exist in the integration of an appropriate sensor with very low parasitic capacitances (intrinsic and extrinsic), but from the point of view of the sensing electronics, it may well be possible to design a pixelized detector with sufficiently small cells to be read out entirely by simple inverters.

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Conclusions

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Take home message

- ”Brute-force” growth (was called “scaling”) is being replaced by “more-sweat” growth
  - More sweat also implies more investments, much more investments (especially human)!
- But lots of opportunities are still open for creative designers.
- Much functionality can still be added to instrumentation for physics and other sciences
  - The impact of “digital” is still very small in HEP, replace “quantity” of data with “quality” of data
  - Beware, gain in analog may even be < 1
- More exotic technologies (TSVs, 3D, wafer stacking, adv. packaging...) ~~may~~ will become available also for low-volume, but history teaches that one should bet on mainstream opportunities
- New engineering “structures” ~~may be~~ mandatory to exploit the above!

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Thank you

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