

# FastCaloSim-GPU

HSF Simulation Working Group Meeting  
R&D on accelerators and simulations

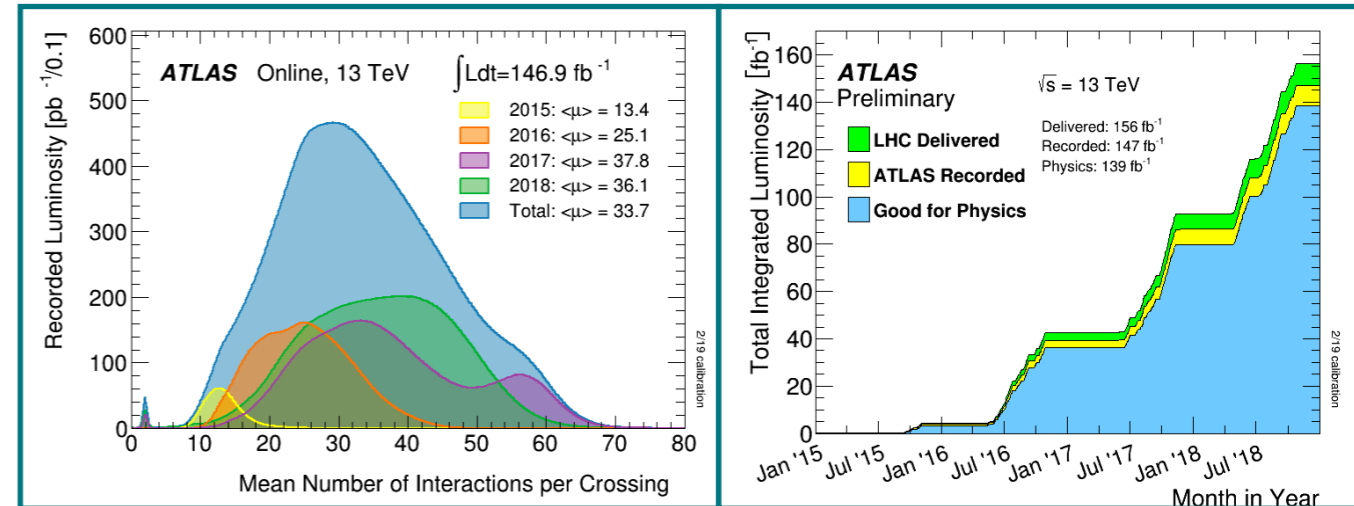
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June 24, 2020





# Motivation

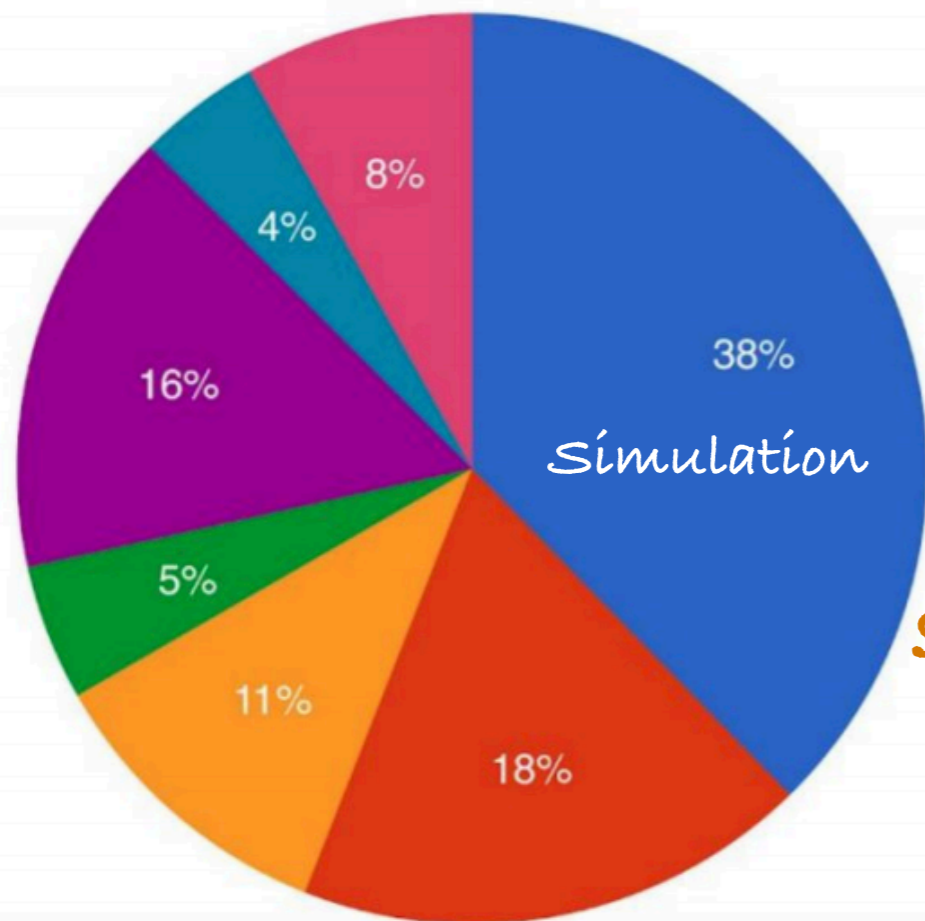
## In a nutshell



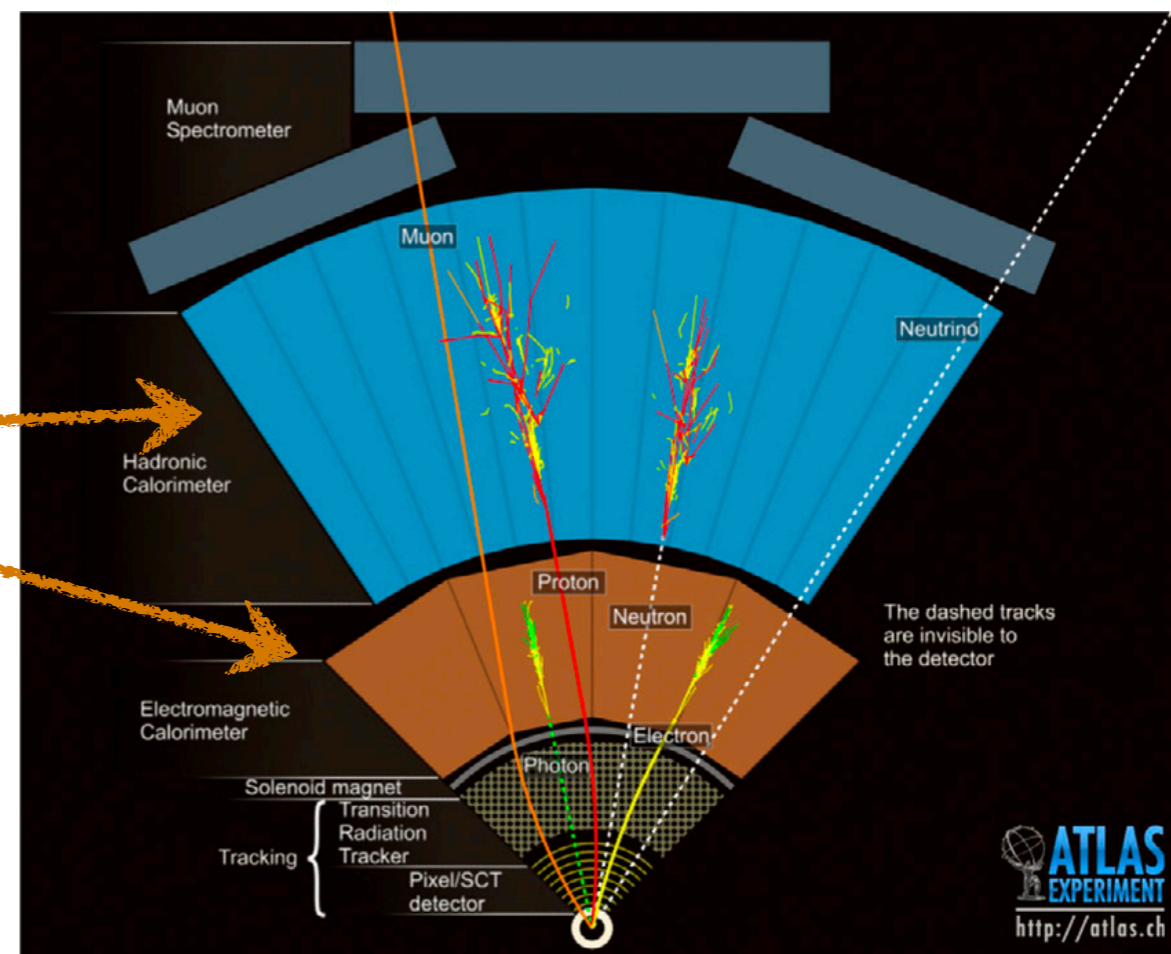
[AtlasPublic/LuminosityPublicResultsRun2](https://atlaspublic.cern.ch/LuminosityPublicResultsRun2)

$$\sqrt{\frac{1}{N_{MC}} \frac{1}{\sigma \int L dt}} \lesssim 1\% \sim 10^{18} \text{ sim'd events needed for Run-2 dataset}$$

Wall clock consumption per workflow



> 90% of time spent here



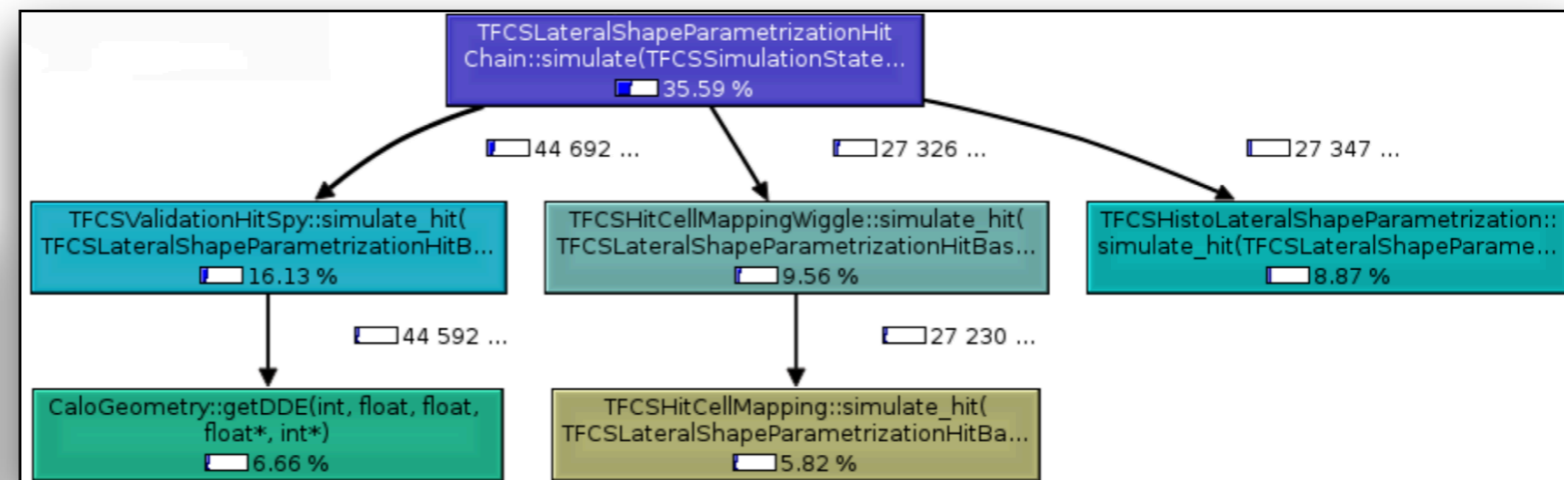
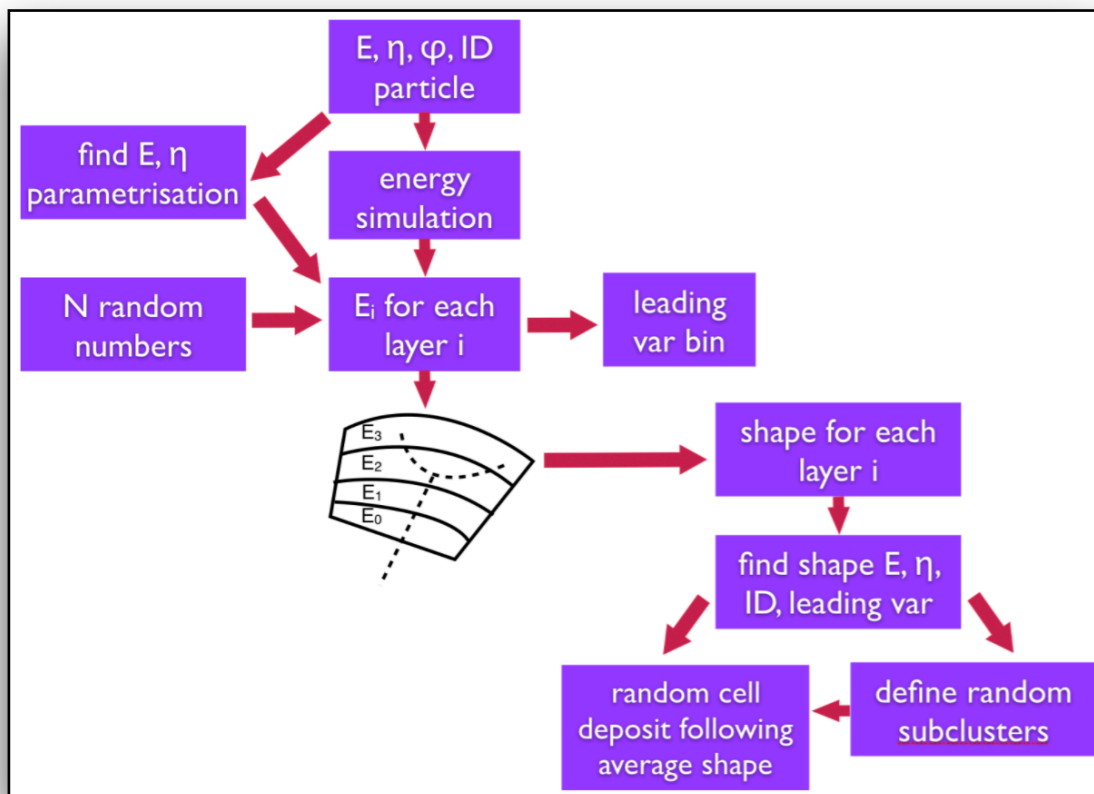


# FastCaloSim(V2)

## GPU simulation port strategy

No data dependence; Can parallelize hit-processing

### Simulation schematic



### ⊕ GPU-based geometry

- ⊖ ~200k cells in 24 layers (about 20MB)
- ⊖ Flatten and simplify for GPU-friendly data structures, e.g. non-standard layouts not supported

### ⊕ Multi-stage kernels

- ⊖ Block-/work-group-wise atomic update for shared memory
- ⊖ Reduction of results from all blocks/work-groups

### ⊕ Offload

- ⊖ [Device] Geometry-based calculations, e.g. extrapolation, hit cells
- ⊖ [Device] RNG, e.g. energy and hit distributions
- ⊖ [Shared] Histogram data, e.g. cell counts and energies



# Portability

## Target multiple backends

- ⊕ Investigating a number of different parallel computing platforms
  - ⊖ CUDA (NVIDIA) → industry “standard” and initial target from BNL CSI; only NVIDIA devices
  - ⊖ Kokkos (Sandia, LANL, ORNL) → CUDA, HPX, OpenMP and pthreads; CUDA wrapper
  - ⊖ SYCL (Intel, Codeplay) → SPIR-V-compatible devices, OpenMP/CL, CUDA\*; code rewrite, utilizing DPC++ extensions, e.g. USM, sub-groups

### Geometry transfer

Device	malloc_shared [ms]	malloc_device [ms]
Host	0.01114258	0.00351570
CPU	0.00347361	0.00337206
Intel Gen9	0.00421972	0.00366639
CUDA	0.00775582	0.00449499

nvprof					
CUDA	time / ms	calls	avg / us	min / us	max / us
clean	38.6	19975	1.93	1.85	2.3
sim_a	391.7	19975	19.6	12.7	50
sim_ct	49.7	19975	2.49	2.43	2.84
mem d->h	37.9	39950	0.95	0.895	1.76
nvprof (NVIDIA RTX 2080 Super)					
Kokkos/CUDA	time / ms	calls	avg / us	min / us	max / us
clean	61.874	19975	3.097	2.944	3.296
sim_a	366.03	19975	18.324	12.672	47.968
sim_ct	70.973	19975	3.553	3.328	3.776
mem d->h	38.669	40193	0.962	0.895	2.4
rocprofiler (AMD Vega 56)					
Kokkos/HIP	time / ms	calls	avg / us		
clean	177.565	19975	8.889		
sim_a	26042.777	19975	1303.768		
sim_ct	220.934	19975	11.06		
mem d->h	55.817		2.794		

Benchmarks from C.Leggett:

- 10k single-electron events within  $0.20 < \eta < 0.25$ ; single layer (EMB).
- N.B. Geo-load not included in “mem d->h”.

Benchmarks from vrp (SYCL port):

- ~200k cells, ~20MB
- “Node 1” (white cells) and “Node 2” (grey cells).
- N.B. Gen9 uses Unified Memory Architecture (UMA).



# Reproducibility

e.g. `SyclRng/SimHitRng_test`

```
$ cmake <...> -DSYCL_RNG_CPU=on <...> && cmake --build .
$ ./generic/test/FastCaloSycl/SimHitRng_test
SimHitRng BEGIN
test1()
SimHitRng device:
"Intel(R) Xeon(R) CPU E3-1585 v5 @ 3.50GHz"

Device random number memory allocated...
  allocd_num_hits: 1000
  size: 4 kb

Generated random numbers...
<...>
test_random_num[384] = [0.679990]
test_random_num[474] = [0.388999]
test_random_num[19] = [0.249990]
test_random_num[999] = [0.578832]
test_random_num[215] = [0.999082]
test_random_num[227] = [0.199966]
<...>
```

```
$ cmake <...> -DSYCL_RNG_GPU=on <...> && cmake --build .
$ ./generic/test/FastCaloSycl/SimHitRng_test
SimHitRng BEGIN
test1()
SimHitRng device:
"Intel(R) Gen9 HD Graphics NEO"

Device random number memory allocated...
  allocd_num_hits: 1000
  size: 4 kb

Generated random numbers...
<...>
test_random_num[999] = [0.578832]
test_random_num[474] = [0.388999]
test_random_num[215] = [0.999082]
test_random_num[227] = [0.199966]
test_random_num[19] = [0.249990]
test_random_num[384] = [0.679990]
<...>
```

All supported devices on given machine generate same random numbers (to precision shown), e.g. Intel CPU and Iris GPU. No MKL support for CUDA; workaround by using CPU device.



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# FastCaloSync1 github project

<https://github.com/vpascuzz/FastCaloSim-GPU/tree/dpcpp>

Forked from a private repo;  
send me your github account ID if you want access.



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# Backup



# FastCaloSycl

## What is it?

- ⊕ Port CPU-intensive code from Simulation/ISF/ISF FastCaloSim
- ⊕ Using Intel/llvm (DPC++), oneMKL
- ⊕ Investigation of SYCL as an accelerator  
“portability solution” using FastCaloSim(V2) as a testbed



# Package (re-)structure

## FastCaloSycl overview

### ⊕ Refactored code, added new data structures

- ⊖ Comprises several libraries: `FastCaloSycl`, `SyclGeo`, `SyclCommon` and `SyclTest`
- ⊖ Serialization for GPU-friendly structures
- ⊖ Simulation kernel function object
- ⊖ MKL-based random number generator

### ⊕ Updated cmake configuration

1. `SyclGeo: SYCL_TARGET_{CUDA, DEFAULT, CPU, GPU}`
2. `SyclRng*: SYCL_RNG_{CUDA, DEFAULT, CPU, GPU}`



*Possible to use distinct devices for geometry and RNG*



# Package (re-)structure (II)

FastCaloSimAnalyzer > FastCaloSycl > M CMakeLists.txt

```
1 # Copyright (C) 2002-2020 CERN for the benefit of the ATLAS collaboration
2
3 cmake_minimum_required(VERSION 3.10)
4
5 add_library(${FastCaloSycl_LIB} SHARED)
6
7 set(CMAKE_C_COMPILER "clang")
8 set(CMAKE_CXX_COMPILER "clang++")
9
10 set(SYCL_TARGET_DEFAULT OFF CACHE BOOL "Use the default device for simulation")
11 set(SYCL_TARGET_CPU OFF CACHE BOOL "Use the CPU device for simulation")
12 set(SYCL_TARGET_GPU OFF CACHE BOOL "Use the GPU device for simulation")
13 set(SYCL_TARGET_CUDA OFF CACHE BOOL "Enable CUDA backend for simulation")
14
15 add_definitions(-DUSE_SYCL)
16
```

} Select device to hold geometry, run non-RNG calculations

FastCaloSimAnalyzer > FastCaloSycl > SyclRng > M CMakeLists.txt

```
1 # Copyright (C) 2002-2020 CERN for the benefit of the ATLAS collaboration
2
3 cmake_minimum_required(VERSION 3.10)
4
5 add_library(SyclRng SHARED)
6
7 set(CMAKE_C_COMPILER "clang")
8 set(CMAKE_CXX_COMPILER "clang++")
9
10 set(CMAKE_CXX_FLAGS "-g -O2 -fsycl -std=c++17 -Wno-unknown-cuda-version")
11
12 set(SYCL_RNG_DEFAULT OFF CACHE BOOL "Use default device for RNG")
13 set(SYCL_RNG_CPU OFF CACHE BOOL "Use CPU device for RNG")
14 set(SYCL_RNG_GPU OFF CACHE BOOL "Use GPU device for RNG")
15
16 if (SYCL_RNG_DEFAULT)
17   message(STATUS "Targetting default SYCL device for RNG")
18   add_definitions(-DSYCL_RNG_DEFAULT)
19 elseif (SYCL_RNG_CPU)
20   message(STATUS "Targetting CPU SYCL device for RNG")
21   add_definitions(-DSYCL_RNG_CPU)
22 elseif (SYCL_RNG_GPU)
23   message(STATUS "Targetting GPU SYCL device for RNG")
24   add_definitions(-DSYCL_RNG_GPU)
25 endif()
```

} Select device to perform RNGation



# Class overview

- ⊕ `SyclGeo::GeoRegion`
  - ⊖ Data class to represent a region of the calorimeter
  - ⊖ Comprises cells (i.e. `CaloDetDescrElement`), extents
  - ⊖ Converts `TObject`-derived data structure(s) to standard-layout\* class for device
- ⊕ `SyclGeo::Geo`
  - ⊖ Holds full calorimeter geometry
  - ⊖ Allocates device-side memory, and performs loading of host-side to device-side memory using USM
  - ⊖ Device-side geometry stored in struct, `Geo::DeviceGeo`
- ⊕ `SyclRng::SimHitRng`
  - ⊖ Used for sampling number of hits, particle energies
  - ⊖ RNG done on device (host, SPIRV) with MKL
- ⊕ `SyclCommon::DeviceCommon`
  - ⊖ Access `cl::sycl::queues` and associated `cl::sycl::devices`, and `CUDASelector` class
  - ⊖ Various `cl::sycl::experimental::printf()` definitions
- ⊕ `SyclCommon::Props`
  - ⊖ Contains constants and simulation-related structures
- ⊕ `FastCaloSycl::SimEvent`
  - ⊖ Performs simulation using above classes
  - ⊖ Kernel function object; class implementing `void operator() (...)`; target callable object is called within command group scope

\* While DPC++ claims to support non-standard layouts, virtual functions are not [yet] callable in SYCL kernels.



# Device-exclusive memory

## SyclRng::SimHitRng

```
59 bool SimHitRng::Alloc(unsigned long ncells, unsigned short max_unique_hits) {
60     // Don't reallocated if memory is already allocated.
61     if (is_initialized_) {
62         return true;
63     }
64
65     // Allocate device-side memory for random numbers array.
66     random_nums_ =
67         (float*)malloc_device(alloca_num_hits_ * sizeof(float), device_, ctx_);
68     if (!random_nums_) {
69         std::cout << "Cannot allocate device-side memory for random numbers!"
70                 << std::endl;
71         return false;
72     }
73     // Allocate memory for energy in cells
74     cells_energy_ = (float*)malloc_device(ncells * sizeof(float), device_, ctx_);
75     if (!cells_energy_) {
76         std::cout << "Cannot allocate device-side memory for cell energy!"
77                 << std::endl;
78         return false;
79     }
80     // Allocate memory for cell properties
81     cell_props_ = (fastcalosycl::CellProps*)malloc_device(
82         max_unique_hits * sizeof(fastcalosycl::CellProps), device_, ctx_);
83     if (!cell_props_) {
84         std::cout << "Cannot allocate device-side memory for cell properties!"
85                 << std::endl;
86         return false;
87     }
88     // Allocate memory for unique hits counter
89     num_unique_hits_ = (int*)malloc_device(sizeof(int), device_, ctx_);
90     if (!num_unique_hits_) {
91         std::cout << "Cannot allocate device-side memory for unique hits counter!"
92                 << std::endl;
93         return false;
94     }
95     is_initialized_ = true;
96     return true;
97 }
```

RNGation performed exclusively on device;

Copy to host if/when needed:  
`cl::sycl::queue::memcpy()`



# Unit tests

## Test library functionality

- ⊕ `SimHitRng_test`
  - ⊖ Test pseudo-random number generation on device
  
- ⊕ `GeoRegion_test`
  - ⊖ Read in geometry via [CaloGeometryFromFile](#) object (virtual interface)
  - ⊖ Test pointer arithmetic; ensure cells are correct
  
- ⊕ `Geo_test`
  - ⊖ Extension of `GeoRegion_test`
  - ⊖ Copies geometry (`CaloDetDescrElements`, `GeoRegions`) to device
  - ⊖ Perform cell and region cross-checks



# Status and TODO

- ⊕ All necessary pieces tested and in place
- ⊕ Start simulating
  - ⊖ Finish implementing `FastCaloSycl::SimEvent` // TODO
  - ⊖ Perform histogramming on GPU // TODO
- ⊕ Benchmarking
  - ⊖ Against Intel CPU and iGPU, and native CUDA versions // TODO
    - ⊖ Expect results by end of the month
  - ⊖ Should have access to Intel DG (dGPU) cards soon (more of apples-to-apples comparison, e.g. no shared silicon between host-device memory)