

Low-Voltage Analog CMOS Design in scaled CMOS technology

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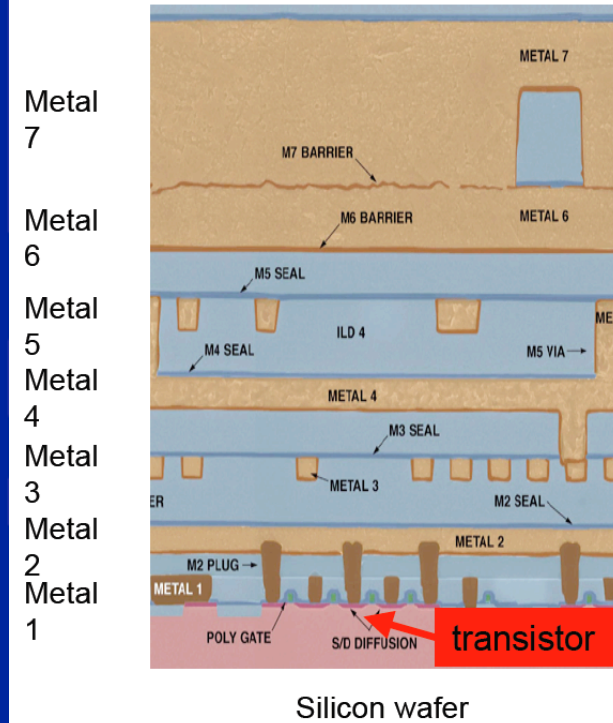
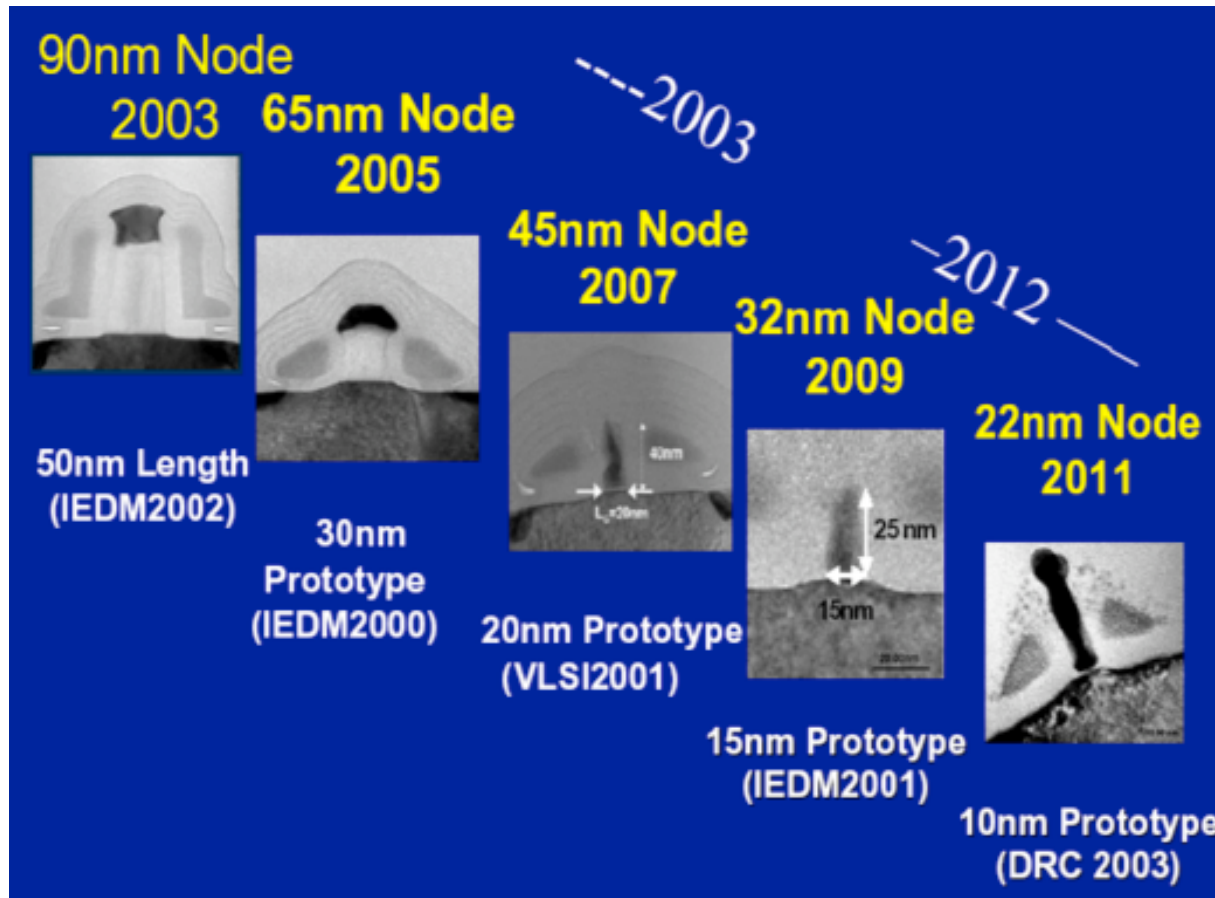


LV Analog Design in scaled CMOS technology

Outline

- Introduction
 - CMOS technology scaling trends ←←←
 - What is LV
 - LV Analog design
 - LV at transistor level
 - LV at circuit level
 - Opamp design
 - Basic bandgap design
 - LV at system level
 - Active-RC filter design
 - Gm-C filter design
 - SC circuit design

CMOS Technology scaling



CMOS Technology scaling

Parameter of the digital NFET in IBM CMOS*

Node	Nm	250	180	130	90	65	↓↓
L_{GATE}	Nm	180	130	92	63	43	
$t_{ox(inv.)}$	Nm	6.2	4.45	3.12	2.2	1.8	↓↓
Peak g_m	$\mu S/\mu m$	335	500	720	1060	1400	↑↑
g_{ds}^{**}	$\mu S/\mu m$	22	40	65	100	230	↑↑↑
g_m/g_{ds}	-	15.2	12.5	11.1	10.6	6.1	↓↓
V_{DD}	V	2.5	1.8	1.5	1.2	1	↓↓↓
V_{TH}	V	0.44	0.43	0.34	0.36	0.24	↓↓
f_T	GHz	35	53	94	140	210*	↑↑↑

- * projected
- ** at peak g_m

1

2

3

- The above trends affects:
 - Analog block **functionality**
 - Analog block **performance**

▪ _____

Table 2. Projected mixed-signal device parameters necessary for continuous design progress.

Technology node (year)	130 nm (2001)	90 nm (2004)	65 nm (2007)	45 nm (2010)	32 nm (2013)	22 nm (2016)	Note
Digital supply voltage (V)	0.9-1.3	0.7-1.0	0.5-0.7	0.4-0.6	0.3-0.5	0.3-0.4	
Analog supply voltage (V)	3.3-1.8	2.5-1.8	2.5-1.8	1.8-1.0	1.8-1.0	1.5-1.0	
NMOS RF device							
f_{\max} (GHz)	≥ 160	≥ 175	≥ 190	200-230	230-260	260-290	
g_m/g_{ds} at $L_{\min\text{-digital}}$	≥ 20	≥ 20	≥ 20	≥ 20	≥ 20	≥ 20	
g_m/g_{ds} at $10 \times L_{\min\text{-digital}}$	≥ 100	≥ 100	≥ 100	≥ 100	≥ 100	≥ 100	
input 1/f noise ($\mu V^2 \times \mu m^2/Hz$)	≤ 500	≤ 300	≤ 200	≤ 150	≤ 100	≤ 75	1
$3\sigma V_{th}$ matching (mV $\times \mu m$)	≤ 15	≤ 12	≤ 9	3	2.5	2.0	1
NMOS analog device							
analog V_{th} (V)	0.5-0.2	0.4-0.2	0.4-0.2	0.3-0.1	0.3-0.1	0.2-0.1	
g_m/g_{ds} at $10 \times L_{\min\text{-digital}}$	≥ 200	≥ 200	≥ 200	≥ 200	≥ 200	≥ 200	
input 1/f noise ($\mu V^2 \times \mu m^2/Hz$)	$\leq 1,000$	≤ 500	≤ 300	≤ 150	≤ 100	≤ 100	1
$3\sigma V_{th}$ matching (mV $\times \mu m$)	≤ 21	≤ 15	≤ 15	≤ 9	≤ 9	≤ 7.5	1
Capacitor							
density (fF/ μm^2)	≥ 2	≥ 3	≥ 4.5	7	10	15	
$Q(1/k(2 \times \mu m^2 \times GHz))$	≥ 200	≥ 300	≥ 450	≥ 700	$\geq 1,000$	$\geq 1,500$	2
voltage linearity (ppm/ V^2)	≤ 100	≤ 100	≤ 100	≤ 100	≤ 100	≤ 100	
leakage (fA/[pF $\times V$])	≤ 7	≤ 7	≤ 7	≤ 7	≤ 7	≤ 7	
3σ matching (% $\times \mu m^2$)	≤ 4.5	≤ 3	≤ 2.5	≤ 2	≤ 1.5	≤ 1	
Resistor							
resistance (Ω/\square)	100	100	100	100	100	100	3
$Q(k(2 \times \mu m^2 \times GHz))$	1,000	1,500	2,000	3,000	4,500	6,000	4
temperature linearity (ppm/ $^{\circ}C$)	60	50	40	30	30	30	
3σ matching (% $\times \mu m$)	9	8	7	6	6	6	
1/f current noise per current ² ($1/[\mu m^2 \times Hz]$)	10^{-18}	10^{-18}	10^{-18}	4×10^{-19}	3×10^{-19}	2×10^{-19}	
Inductor							
density (nH/ μm^2)	0.03	0.03	0.03	0.025	0.02	0.015	
Q_{3dB}	12	16	22	30	40	50	5

¹Optimum value in the possible range of operating points (V_{SS} - V_{DD}). ² $Q = C^2/[C_{\square,par} \times R_{\square,par}]$. ³Multiple resistance values are desirable; all further parameters are specified at $100 \Omega/\square$. ⁴ $Q = R_{\square}/C_{\square,par}$. ⁵Self-oscillation frequency at half bandwidth.

CMOS Technology scaling

Advanced MOS Behaviour

- Transistor performance deviation from the previously described modeling in:
 - scaled-down technology (i.e. with gate length $<1\mu\text{m}$)
 - with thin gate oxide ($t_{\text{ox}} < 50\text{nm}$)

- Large-signal behaviour deviation
 - Gate leakage current
 - V_{TH} variations
 - V-to-I characteristic

 - Device Matching

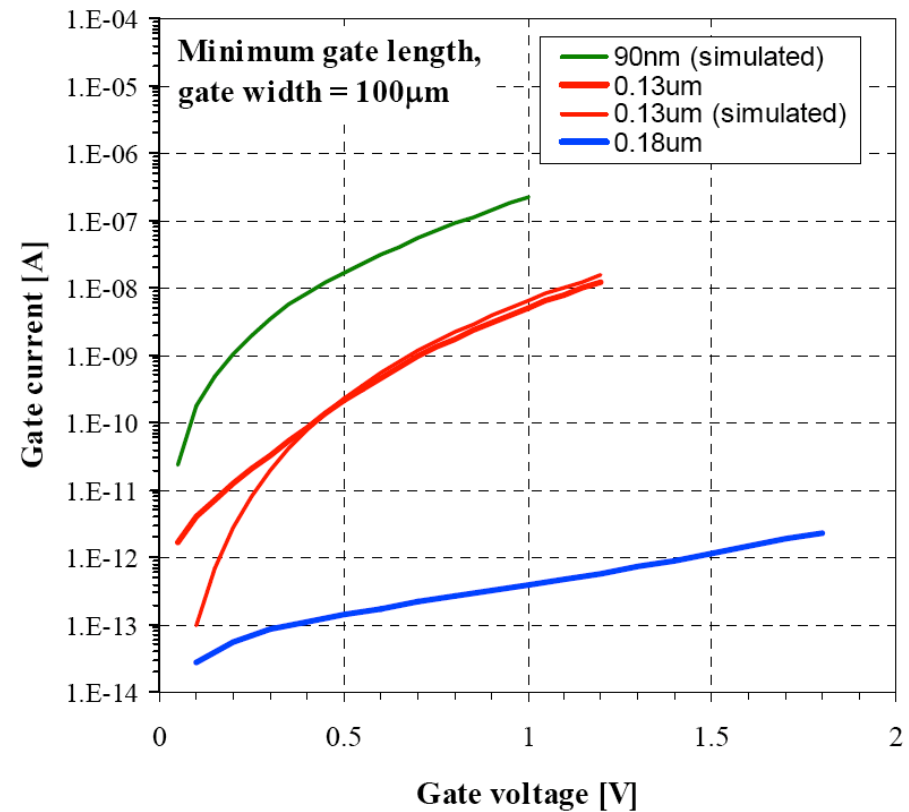
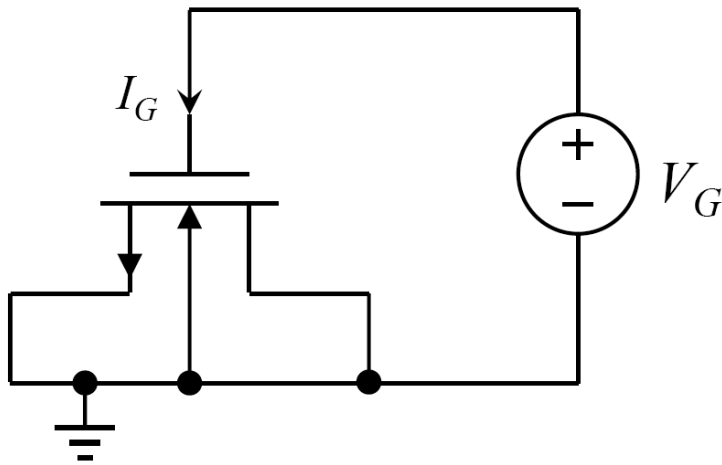
- Small-signal behaviour deviation
 - g_m -vs.-I
 - g_{ds}
 - $A_o = g_m / g_{\text{ds}}$

 - Noise (Thermal & $1/f$)

CMOS Technology scaling

Gate Leakage Current

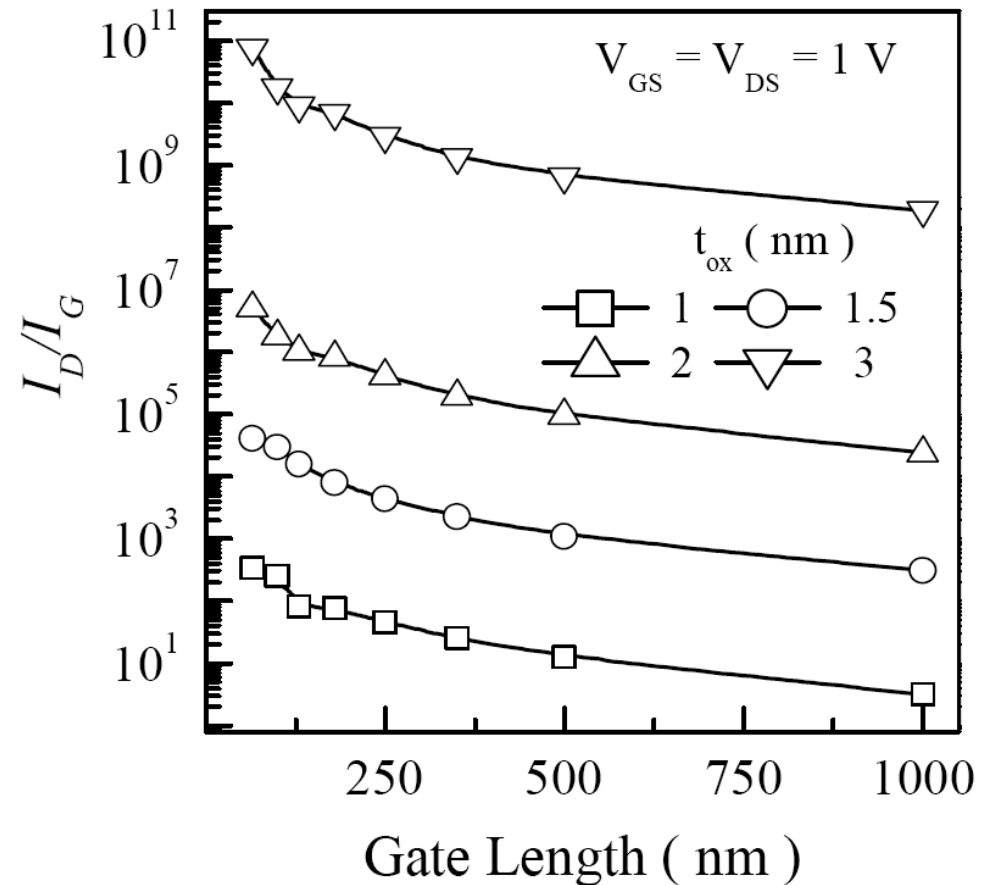
- Gate current can NOT be neglected in scaled down technologies.
- Dominated by tunneling current
 - => Relatively insensitive to device temperature



CMOS Technology scaling

Gate Leakage Current – Bias level

- $I_G \approx$ device area ($\approx W \cdot L$)
- $L_G \uparrow$ & $I_D \downarrow$
 - $I_G \uparrow$
 - $\rightarrow I_D / I_G \downarrow$
 - In **long** L devices
 - a considerable fraction of I_G in I_D
 - critical for S&H and MOS DACs
 - In **short** L devices
 - I_G reduces 😊
 - Output resistance reduces 😞
 - \rightarrow tradeoff between gate current and output resistances



○ @ **ScalTech** $\rightarrow V_{ov} \downarrow \rightarrow (W/L) \uparrow$ (for same g_m) $\rightarrow I_G \uparrow$

CMOS Technology scaling

Gate Leakage Current

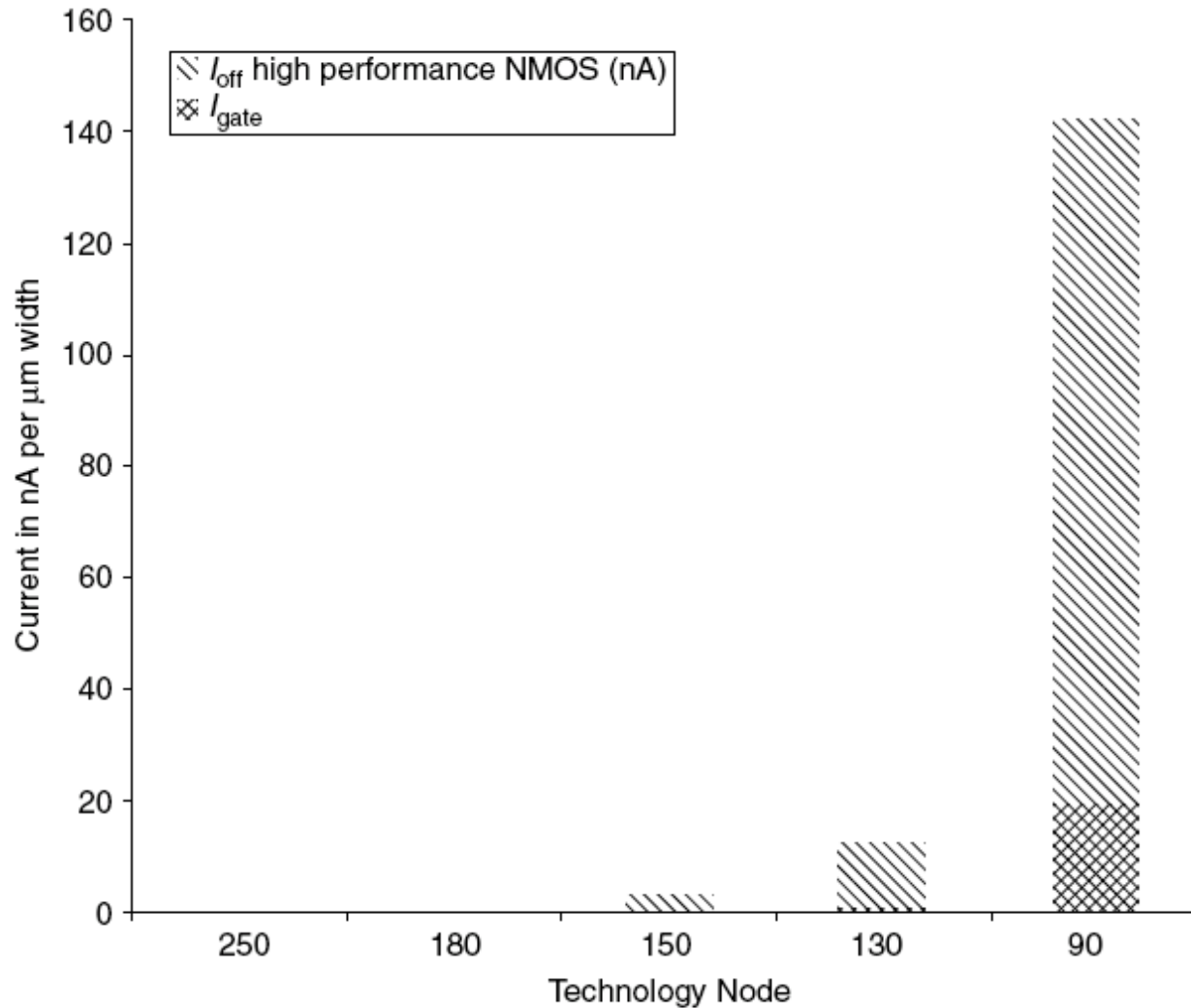
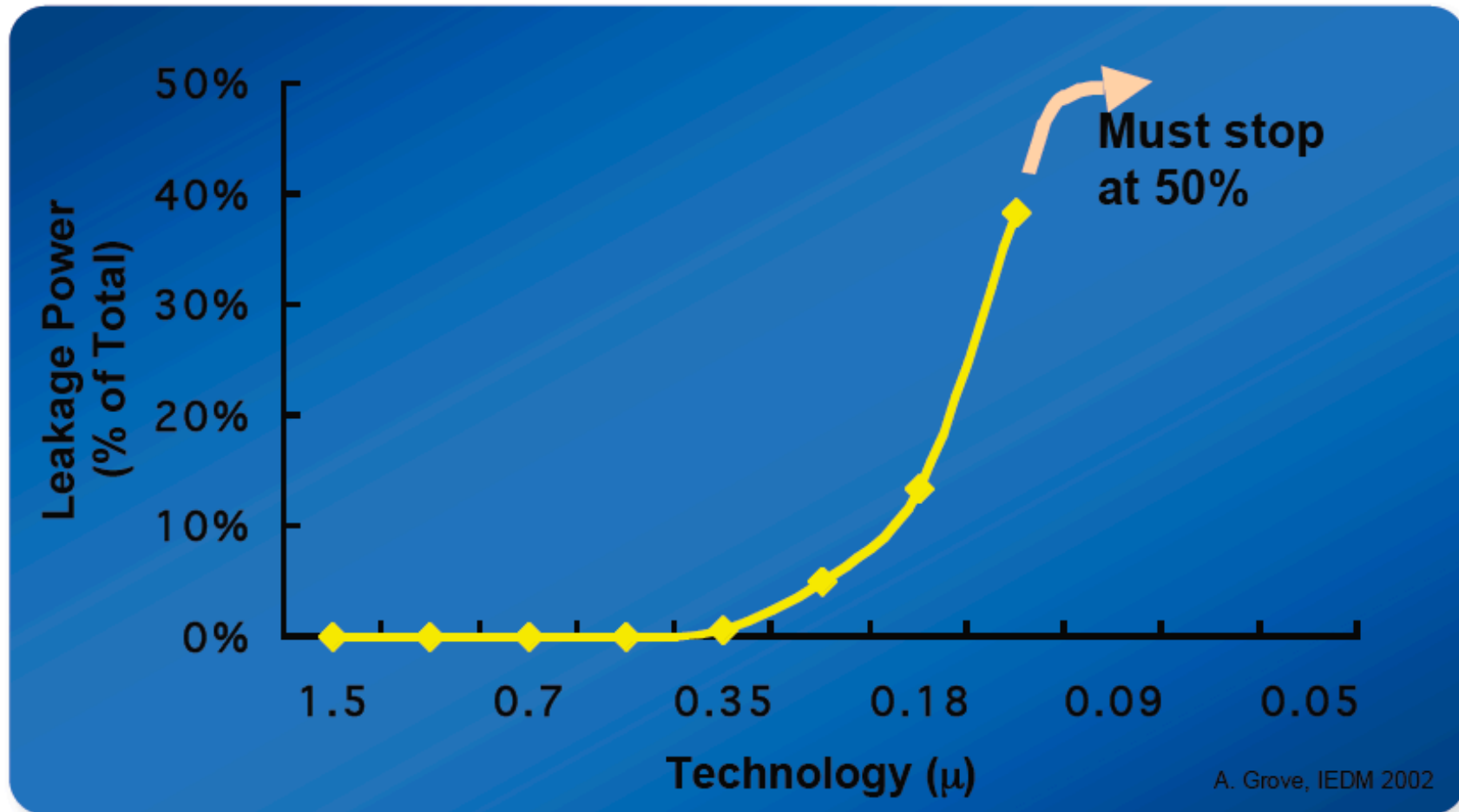


Figure 1.2 I_{gate} and subthreshold leakage versus technology.

CMOS Technology scaling

Leakage Current

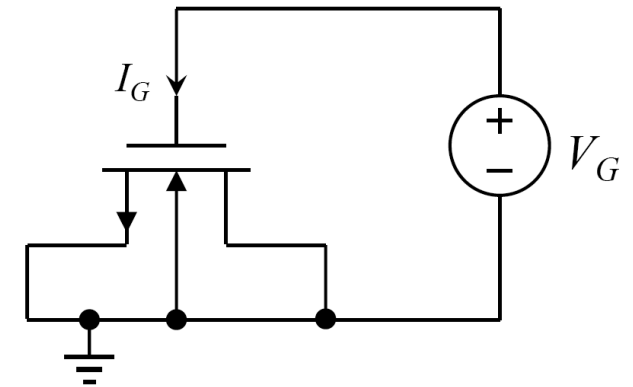


Leakage power limits Vt scaling

CMOS Technology scaling

Gate Leakage Current – Frequency behaviour

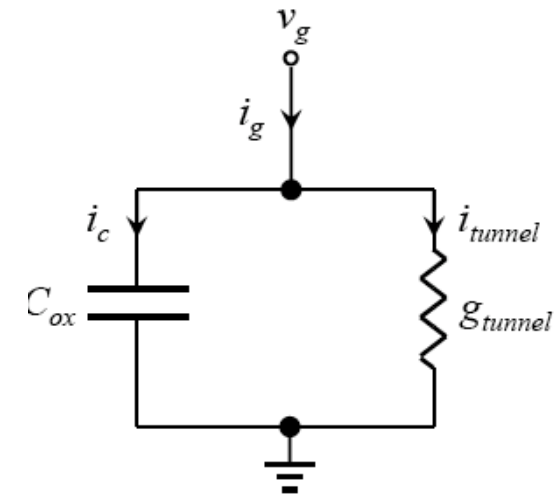
- Small signal equivalent circuit assuming low to moderate frequencies and strong inversion
- At a given frequency
 - similar impedance of the two branches
 - i_c and i_{tunnel} will be equal in magnitude



$$\omega_{gate} \cdot C_{ox} = g_{tunnel}$$

$$f_{gate} = \frac{1}{2 \cdot \pi} \cdot \frac{g_{tunnel}}{C_{ox}}$$

- For $f > f_{gate}$
 - $\rightarrow i_c > i_g$



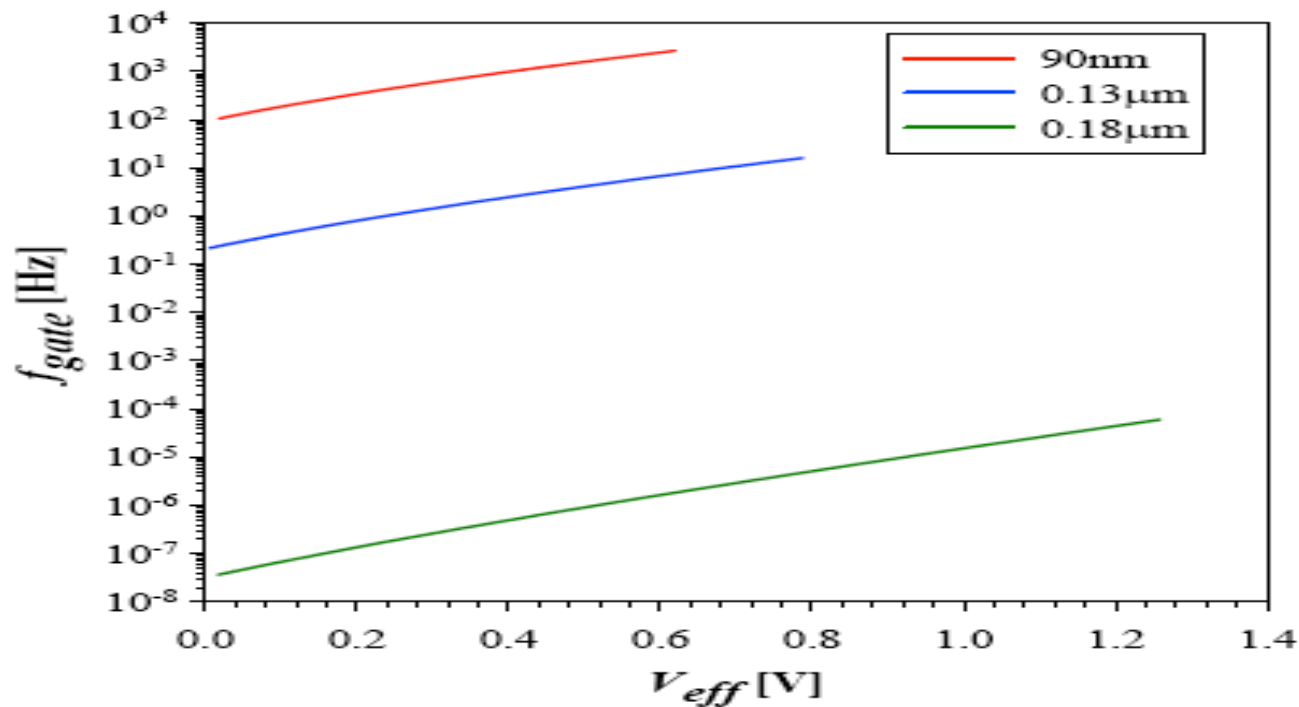
CMOS Technology scaling

Gate Leakage Current – Frequency behaviour: f_{gate} versus technology

- f_{gate} is almost gate area independent
 - An approximate expression:

$$f_{gate} \cong K_{fg} \cdot V_{gs}^2 \cdot e^{t_{ox} \cdot (V_{gs} - 13.6)}$$

- t_{ox} is the oxide thickness in nm
- K_{fg} is $1.5 \cdot 10^{16}$ for NMOS and $0.5 \cdot 10^{16}$ for PMOS



CMOS Technology scaling

V_{TH} deviations

- In scaled technologies V_{TH} strongly changes
 - Technology scaling
 - Thinner oxide
 - Systematic variation
 - Short & Narrow channel effects (W&L effects)
 - Design
 - Shallow Trench Insulator (STI) effects
 - Layout
 - Statistical variation
 - Mismatch
 - Design & Layout

CMOS Technology scaling

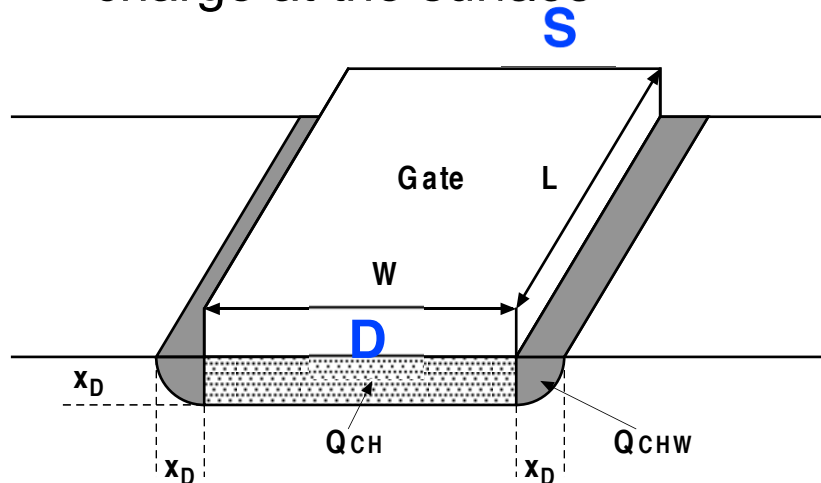
V_{TH} Variation

- V_{TH} depends on
 - Device sizes (W & L)
 - Narrow channel effects
 - Short channel effects
 - → V_{TH0} model
 - Accurate electric field evaluation
 - Vertical Electrical Field Effect
 - Lateral Electrical Field Effect (Velocity saturation)
 - → mobility model
 - Layout design
 - STI effects
 - → V_{TH0} model

CMOS Technology scaling

V_{TH} Variation - Narrow Channel Effects

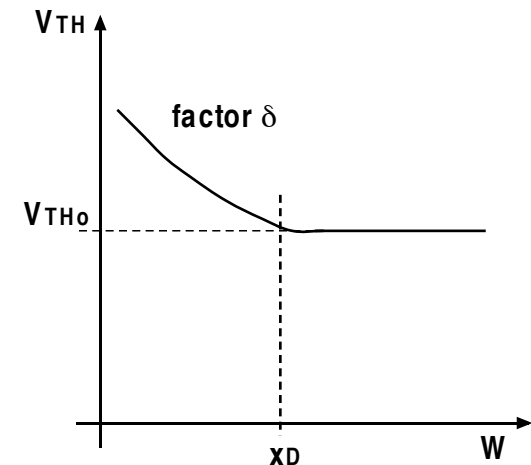
- The depletion layer, which determines the V_{TH} , is not limited to the charge in the area under the gate (Q_{CH})
- On both ends additional charges (Q_{CHW}) is required to terminate the depletion charge at the surface



- For **large W** , Q_{CHW} additional charges are negligible
- For **narrow W** , Q_{CHW} becomes important !!!
 - The effective value of V_{TH} increases

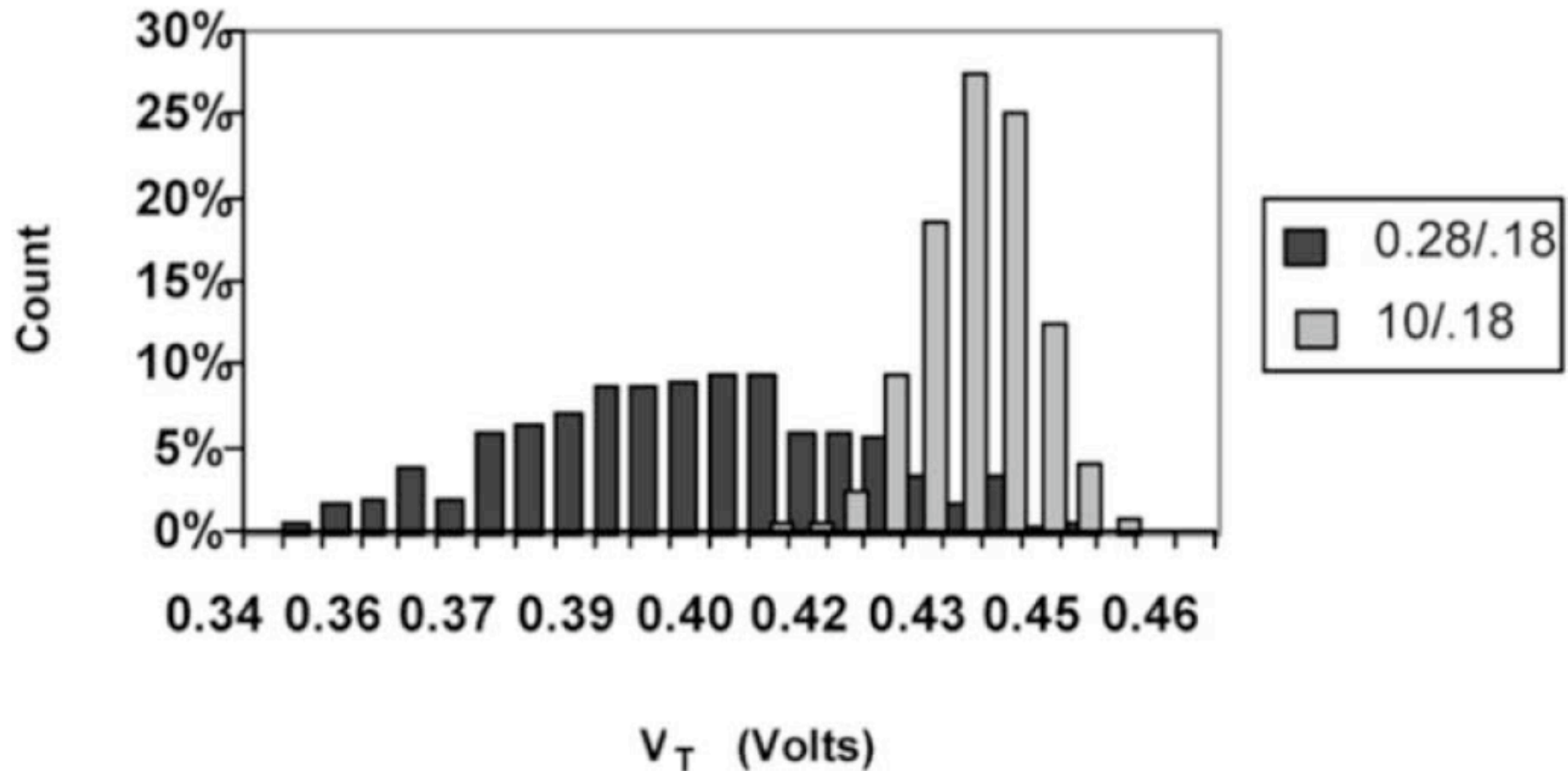
$$\Delta V_{TH} = \frac{\delta}{4} \cdot \frac{\pi \cdot \epsilon_{Si} \cdot (2 \cdot |\phi_F| - V_{BS})}{W \cdot C_{OX}}$$

- Parameter δ (DELTA) is a fitting parameter



CMOS Technology scaling

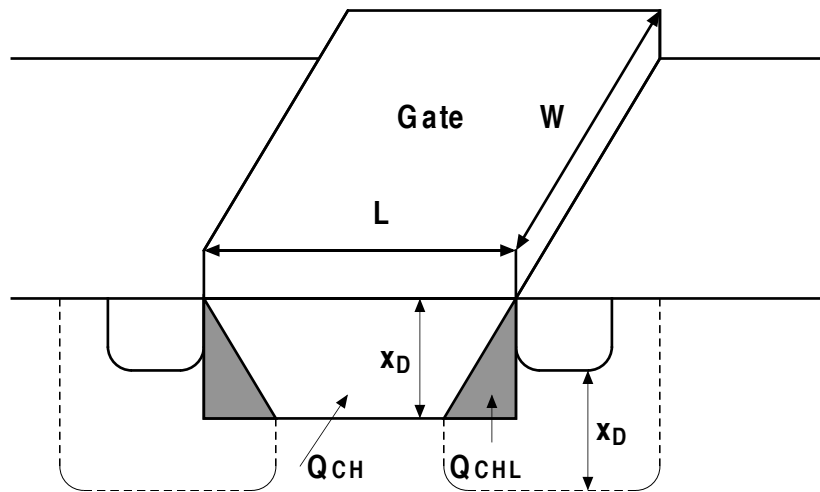
V_{TH} Variation - Narrow Channel Effects



CMOS Technology scaling

V_{TH} Variation - Short Channel Effects

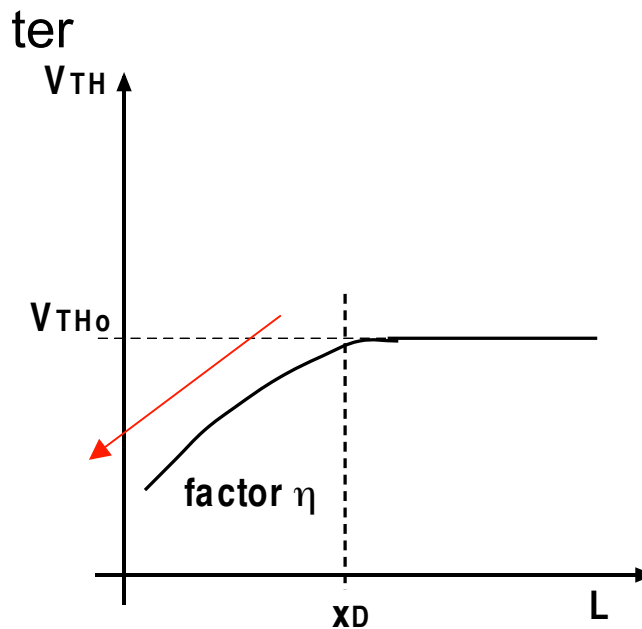
- The depletion layer under the gate includes all the charge from S to D.
- At both D and S, part of the charge (Q_{CHL}) is not directly controlled by G
 - It depends on D and S
- Q_{CHL} has not to be included in the calculation of V_{TH} .



- This effects reduces the value of V_{TH}

$$\Delta V_{TH} = -8.15 \cdot 10^{-20} \cdot \eta \cdot \frac{V_{DS}}{L^3 \cdot C_{ox}}$$

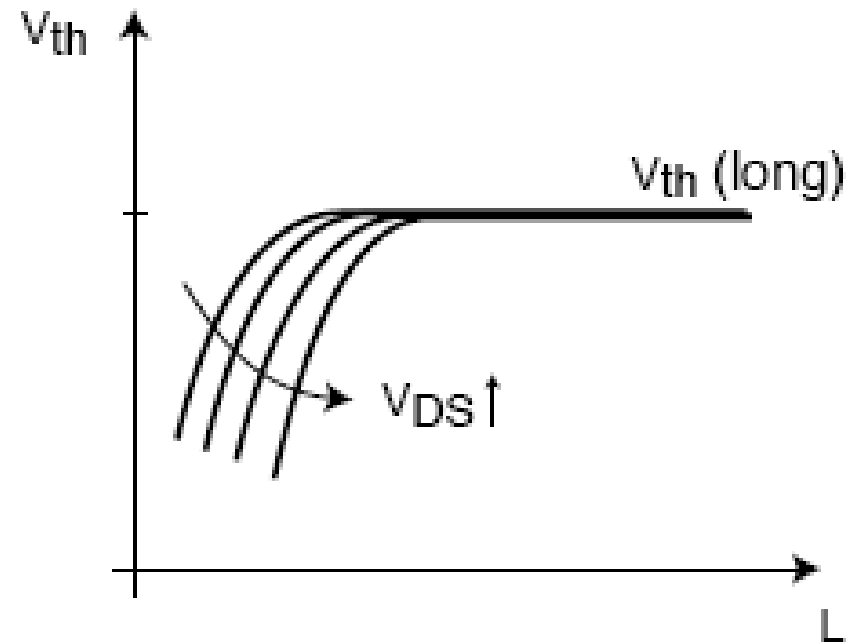
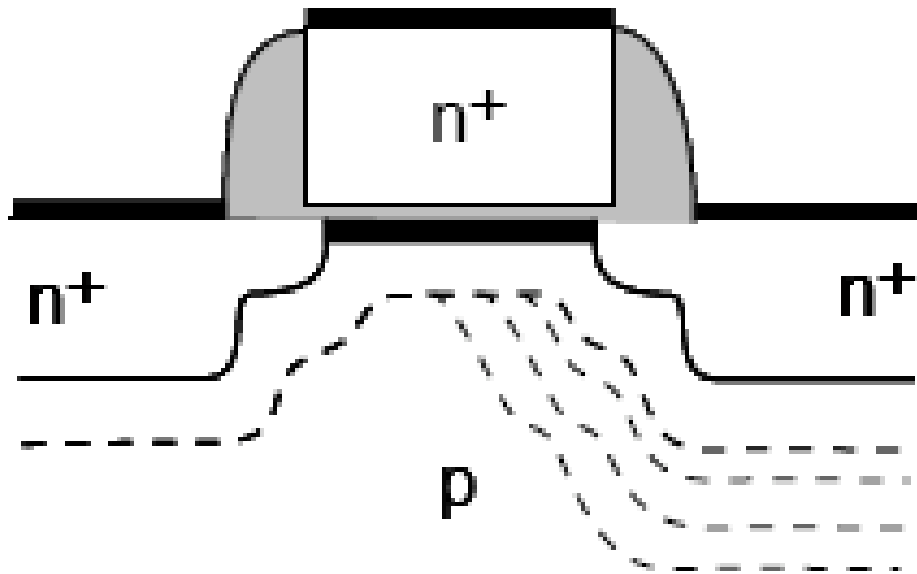
- Parameter η (ETA) is a fitting parameter



CMOS Technology scaling

Drain Induced Barrier Lowering (DIBL)

- For short L , V_S and V_D influence the channel surface potential and tends to make it larger than what would be obtained from the long-channel approximation
 - $\rightarrow I_D$ Increase, particularly in weak and moderate inversion
- Depletion region associated with drain junction expands as $V_{DS} \uparrow$
 - \rightarrow additional V_{TH} reduction



CMOS Technology scaling

V_{TH} reduction protection

- Short channel & DIBL effect
 - → V_{TH} reduction
 - V_{TH} reduction could reach very low V_{TH} values
 - Critical for leakage current, etc....
 - To avoid V_{TH} reduction
 - → Additional technological steps
 - A modified doping profile at the channel edges, like HALO
 - → This maintains a certain V_{TH} value
 - → Channel length reduction → larger V_{TH}

CMOS Technology scaling

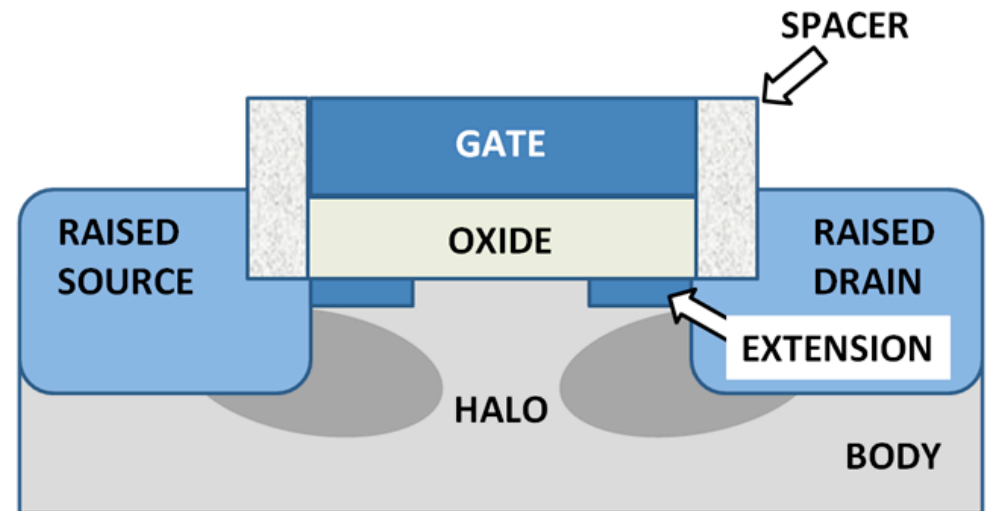
Junction design

- S-to-B & D-to-B junctions affect device performance

- I-V characteristics
- output resistance
- junction cap loading effect
 - → speed
- junction leakage
 - → stand-by power cons

- MOSFET improvement

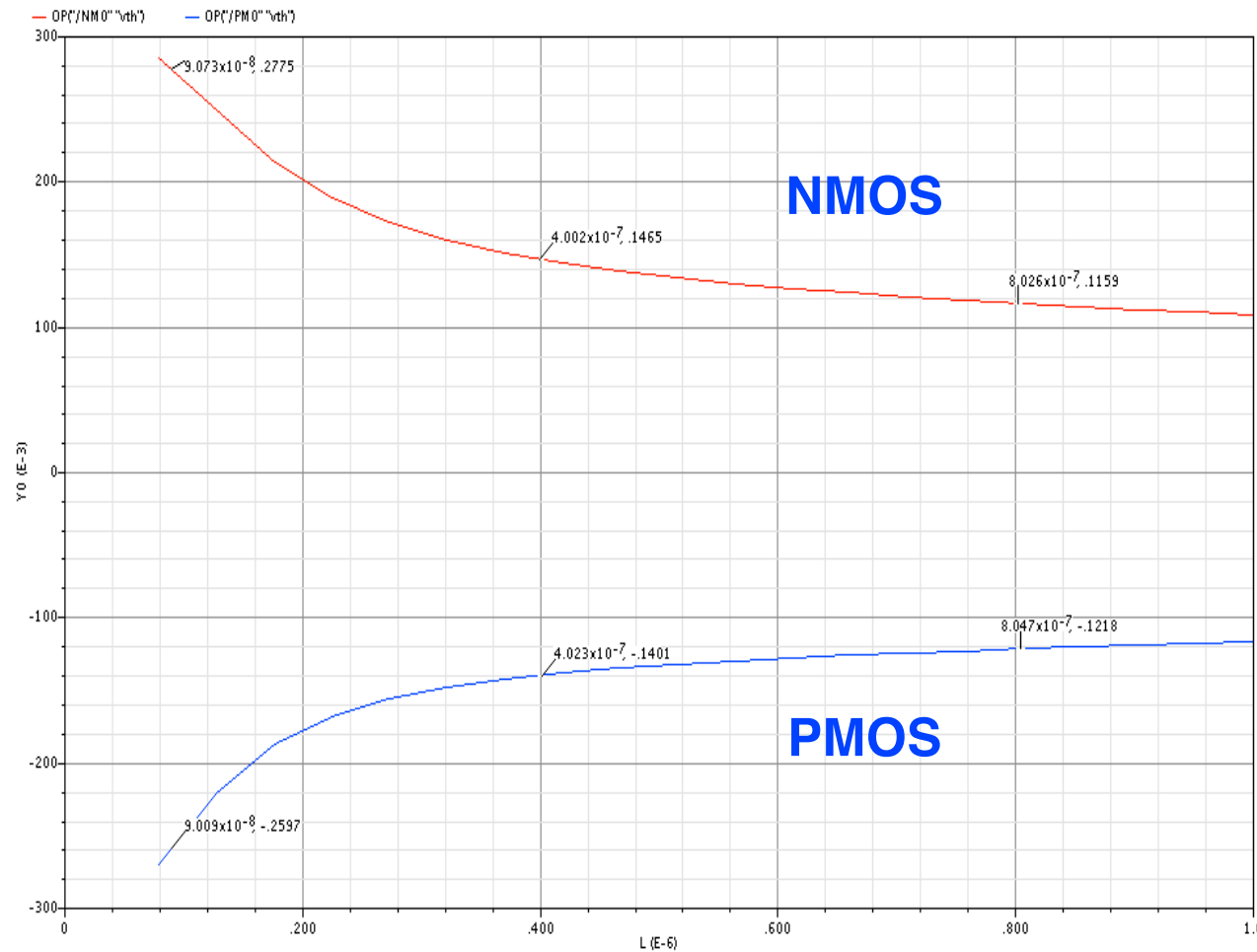
- Shallow junction extensions
- Raised source and drain
- Halo implant
 - → Short channel & DIBL effect reduction
 - → V_{TH} increase



CMOS Technology scaling

Variation of the Threshold Voltage - HALO Effect

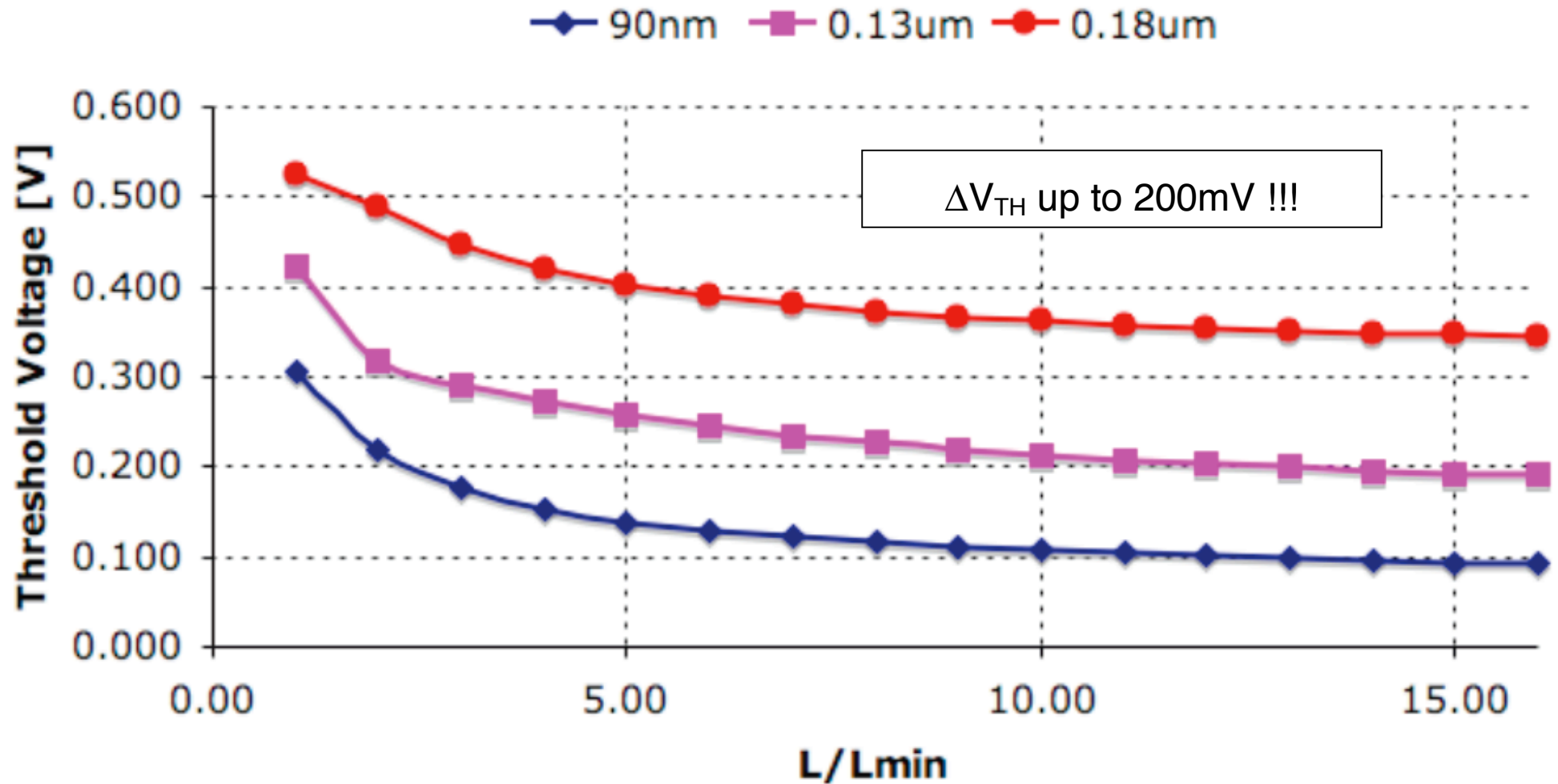
- 90nm CMOS technology
 - PMOS & NMOS threshold voltage vs. gate length



CMOS Technology scaling

Simulated threshold voltage

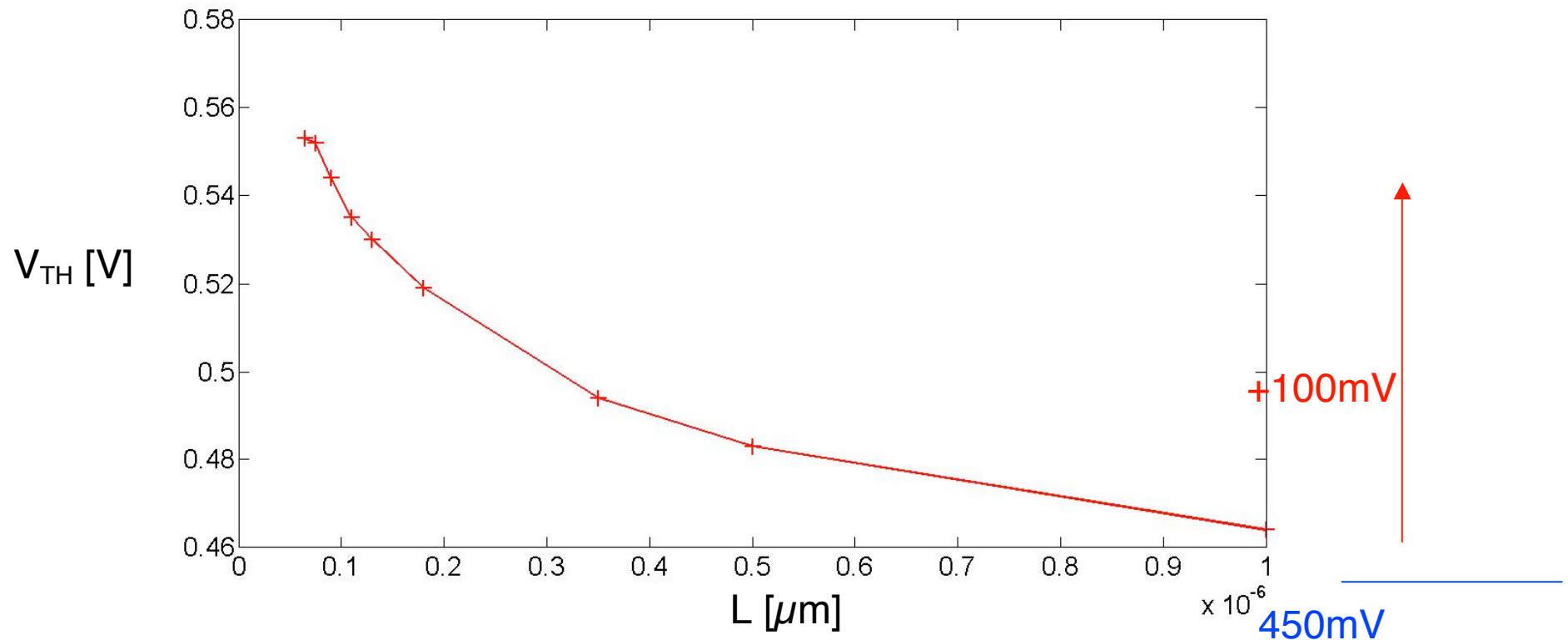
- 2 μm wide NMOS with varying length



CMOS Technology scaling

V_{TH} dependence on MOS gate length (L) – (65nm node)

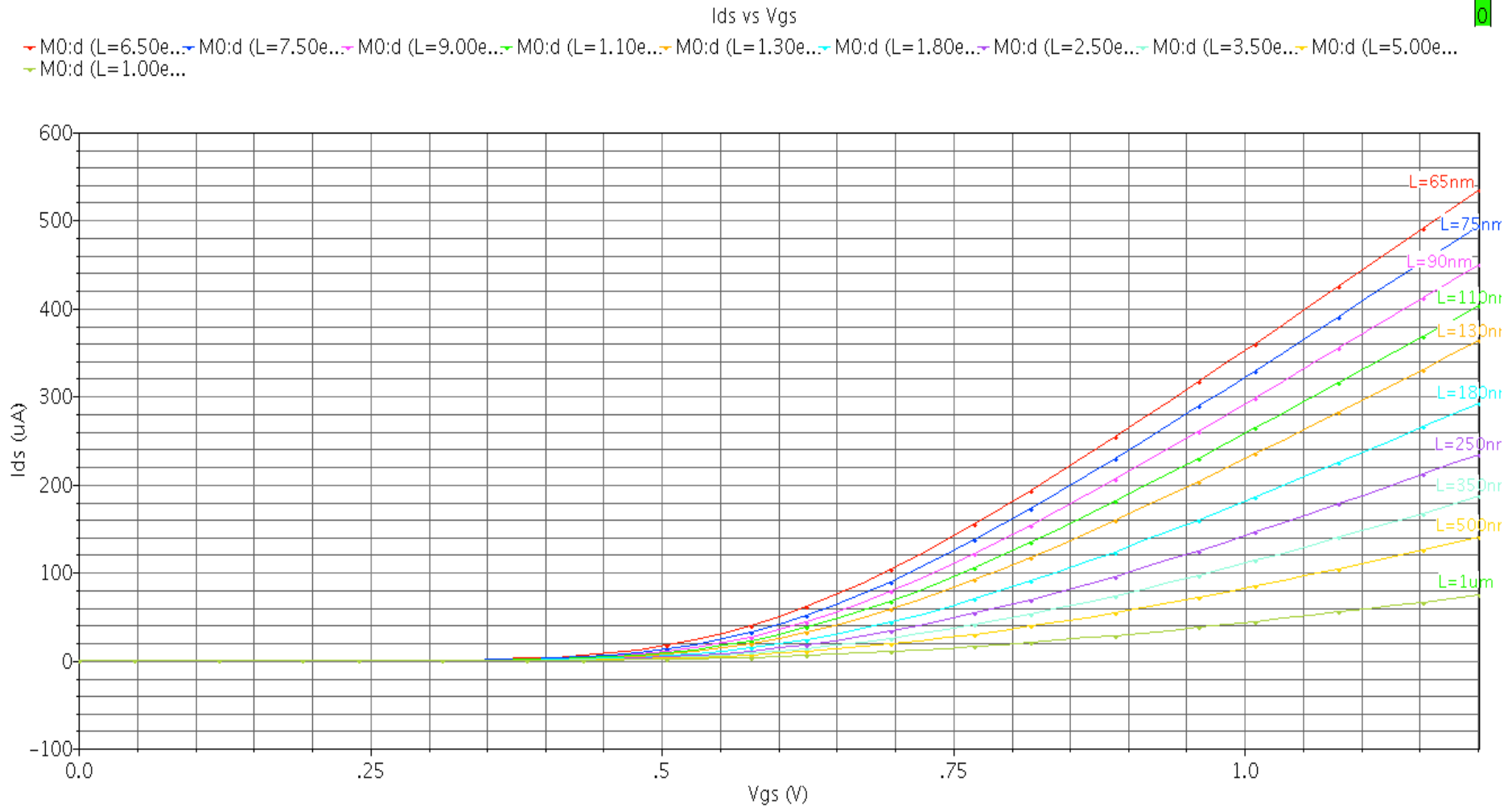
- V_{TH} changes for different L values
 - ΔV_{TH} can be up to 80mV for a nominal value of 550mV
 - → Matched devices need to have the same W&L values
 - Having the same (W/L) ratio is not sufficient



CMOS Technology scaling

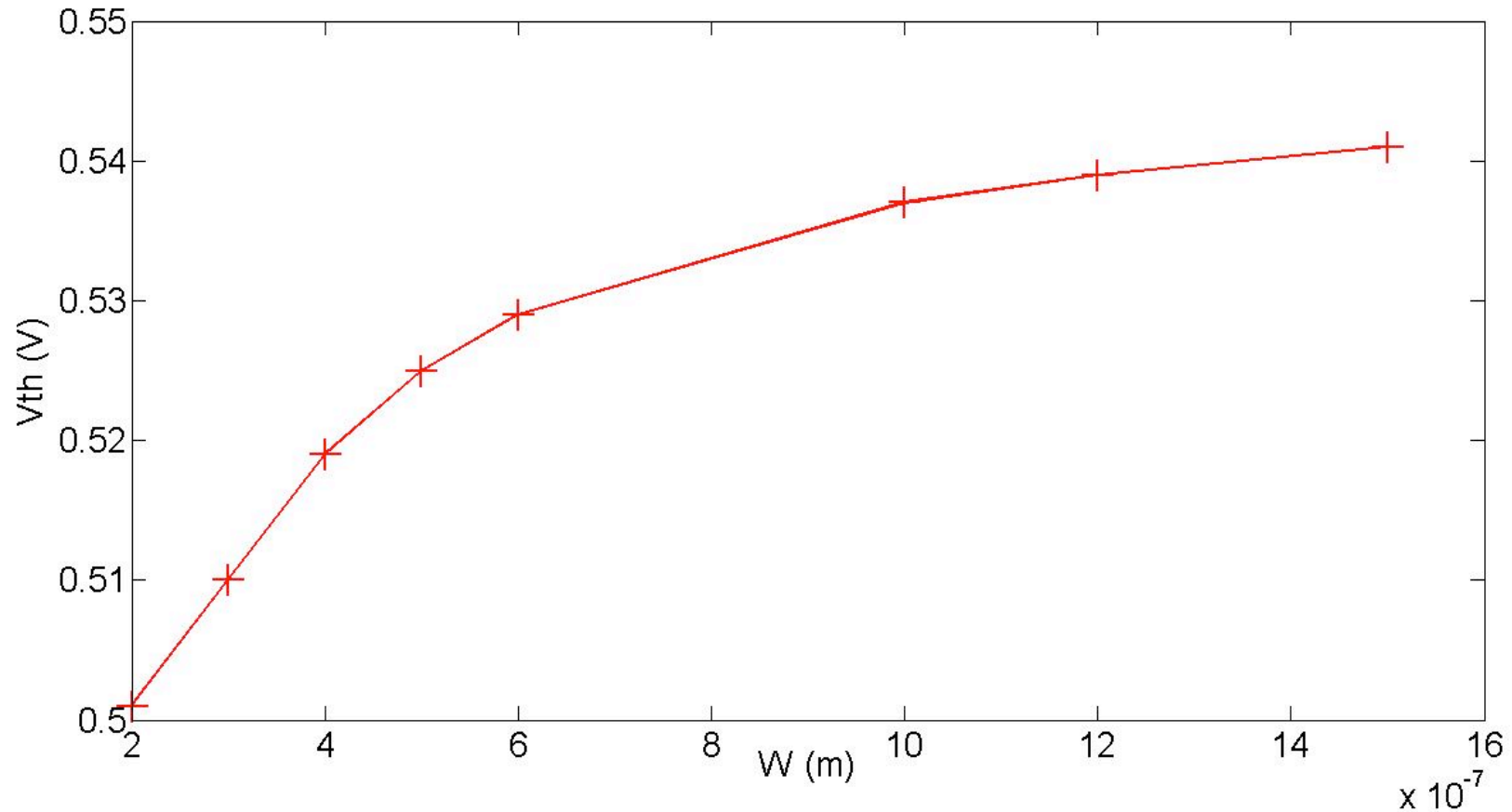
V_{TH} dependence on MOS gate length (L)

■ I_D vs. V_{GS}



CMOS Technology scaling

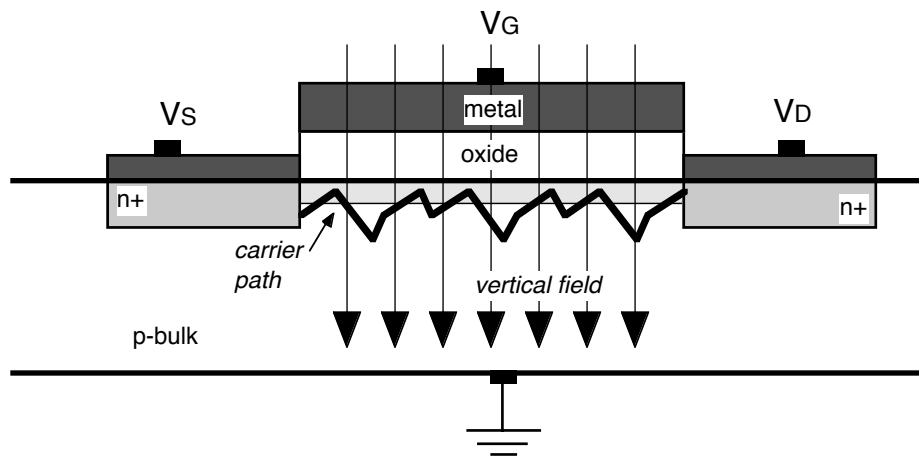
V_{TH} dependence on MOS gate width (W)



CMOS Technology scaling

V_{TH} Variation - Vertical Electrical Field Effects

- The vertical field in the channel reduces the mobility in the channel.
- Increasing V_{GS} increases the field perpendicular to the carrier flow in the channel. This reduces the mobility.



- A transverse field reduces the mobility

$$\mu = \frac{\mu_0}{1 + \theta(V_{GS} - V_{TH})}$$

- θ depends on the oxide thickness and is typically **approximated** by:

$$\theta = \frac{2.3}{t_{ox}} [nm]$$

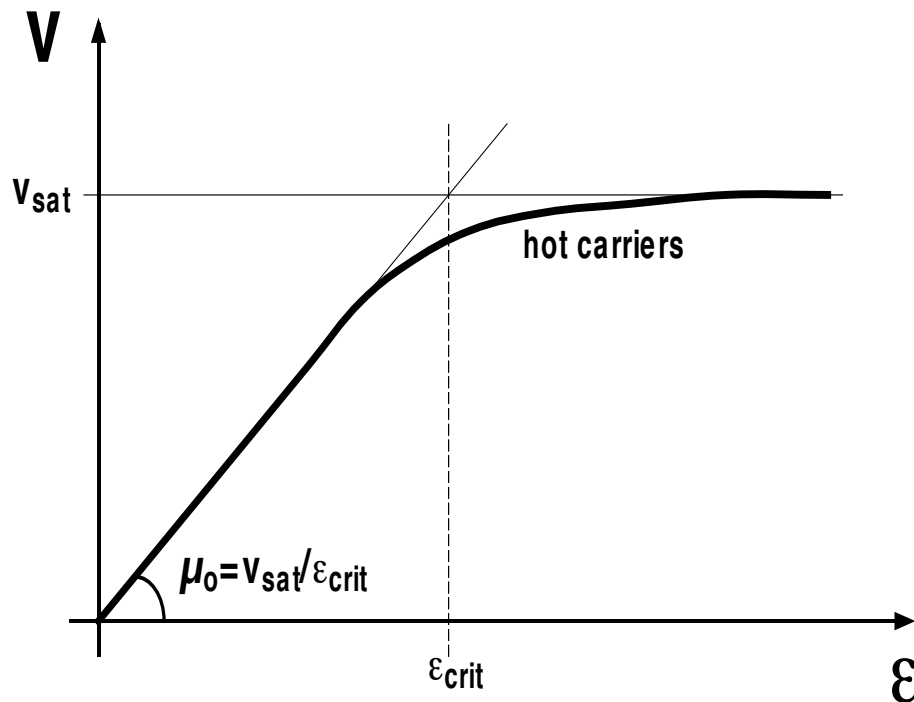
- This effects strongly depends on channel length and oxide thickness (Even long-channel & thin oxide devices suffer from this problem !!).
- g_m is lower than expected (up to 50% less, for large V_{Dsat})
 - $\rightarrow g_m$ increases more slowly than $\sqrt{I_D}$

CMOS Technology scaling

V_{TH} Variation - High-Lateral Electrical Field Effects - (Velocity saturation)

- The mobility is a measure of the carrier velocity acquired by the applied electric field, i.e.

the mobility is the velocity per unit electric field



- For **LOW** value of electric field (ϵ)
 - the velocity (v) increases proportionally

$$\mu_0 = \frac{V_{sat}}{\epsilon_{crit}}$$

- For **LARGE** electric field,
 - the velocity does not increase proportionally
 - tends to saturate to the saturation velocity (v_{sat})

$$v_{sat} \approx 10^5 \text{ m/s}$$

- Carriers at v_{sat} are called hot electron
- In SPICE this effect is evaluated with a series of correlated fitting parameters (U_0 , U_{CRIT} , U_{EXP} , U_{TRA} , V_{MAX})

CMOS Technology scaling

V_{TH} Variation - High-Lateral Electrical Field Effects - (Velocity saturation)

- For **SMALL L** → the model with constant mobility is no longer valid

- The current is derived by replacing ϵ with v_{sat}/μ_0

$$I_D = W \cdot Q_m \cdot v_{sat} \quad (Q_m = \text{total mobile charge in the channel})$$

- The current can also be expressed as:

$$I_D = W \cdot C_{ox} \cdot (V_{GS} - V_{TH}) \cdot v_{sat}$$

- The saturation is **NOT** defined as the point with zero mobile charge Q_m
 - The saturation is the point where the carriers reach the saturation velocity

- The transconductance

$$g_m = \frac{\partial I_D}{\partial (V_{GS} - V_{TH})} \cong W \cdot C_{ox} \cdot v_{sat}$$

- The transition frequency at long channel

$$f_{max} = \frac{1}{2 \cdot \pi} \cdot \frac{g_{msat}}{C_{GS}} = \frac{1}{2 \cdot \pi} \cdot \frac{\mu}{L_{eff}^2} \cdot (V_{GS} - V_{TH})$$

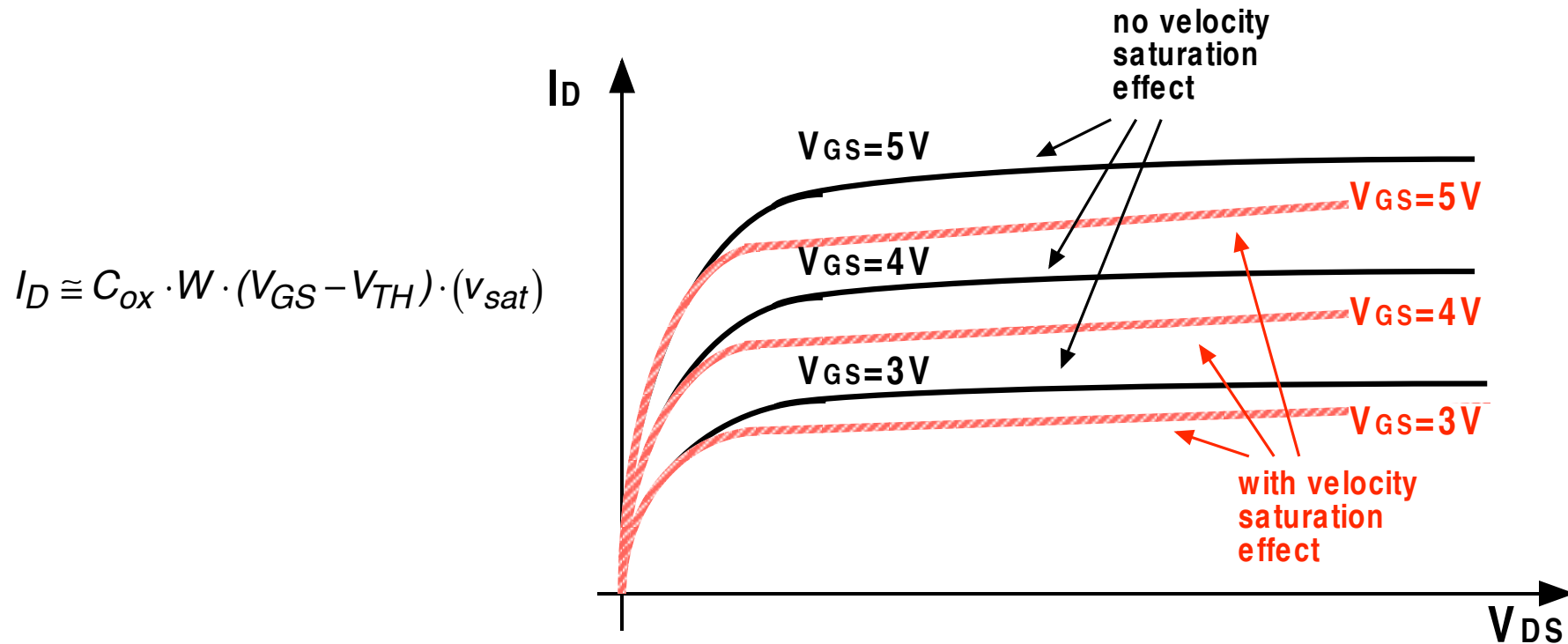
- The transition frequency at short channel

$$f_{max} = \frac{1}{2 \cdot \pi} \cdot \frac{g_{msat}}{C_{GS}} = \frac{1}{2 \cdot \pi} \cdot \frac{v_{sat}}{L_{eff}}$$

CMOS Technology scaling

High-Lateral Electrical Field Effects - (Velocity saturation)

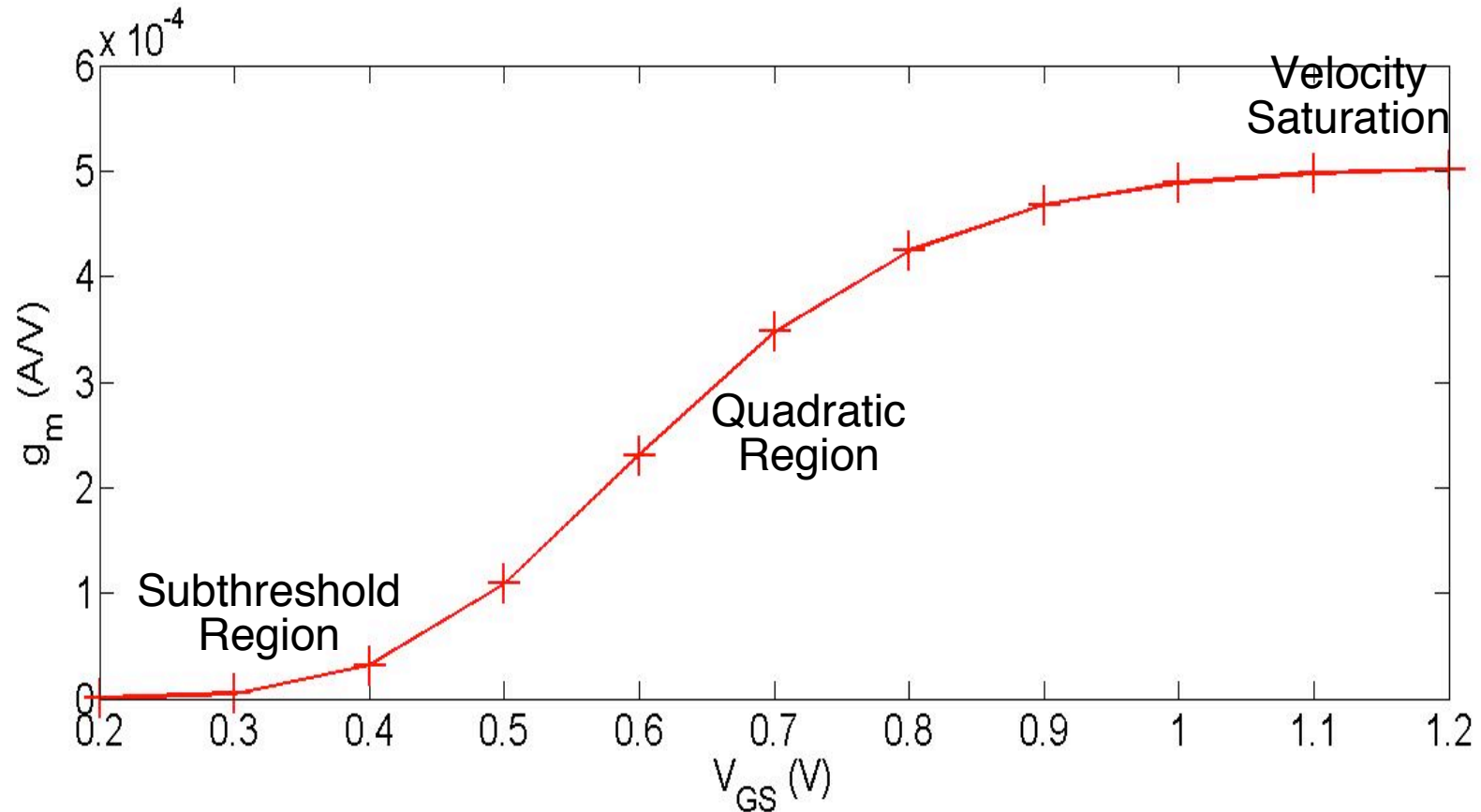
$$I_D = \frac{\mu \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH}) \cdot V_{DSsat}}{1 + \frac{V_{DSsat}}{L \cdot \epsilon_{sat}}} \cong C_{ox} \cdot W \cdot (V_{GS} - V_{TH}) \cdot (\mu \cdot \epsilon_{sat}) \cong C_{ox} \cdot W \cdot (V_{GS} - V_{TH}) \cdot (v_{sat})$$



CMOS Technology scaling

Velocity saturation effects

- Transconductance dependence



CMOS Technology scaling

Accurate Mobility Model

- The mobility is given by:

$$\mu = \mu_o \cdot \left(\frac{T}{T_{REF}} \right)^{2/3} \cdot \left(1 + \frac{\epsilon_x}{\epsilon_{crit}} \right)^{-m} \cdot \left(\frac{1}{1 + \frac{V_{DS}}{L \cdot \epsilon_{sat}}} \right)$$

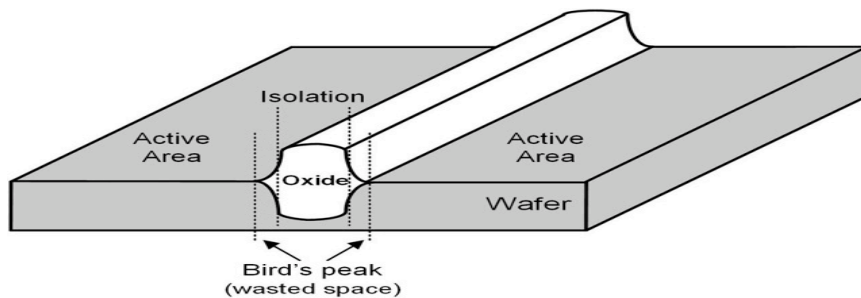
- The mobility depends on:

- Temperature $\left(\frac{T}{T_{REF}} \right)^{2/3}$
- Vertical field $\left(1 + \frac{\epsilon_x}{\epsilon_{crit}} \right)^{-m}$
- Lateral field $\left(\frac{1}{1 + \frac{V_{DS}}{L \cdot \epsilon_{sat}}} \right)$

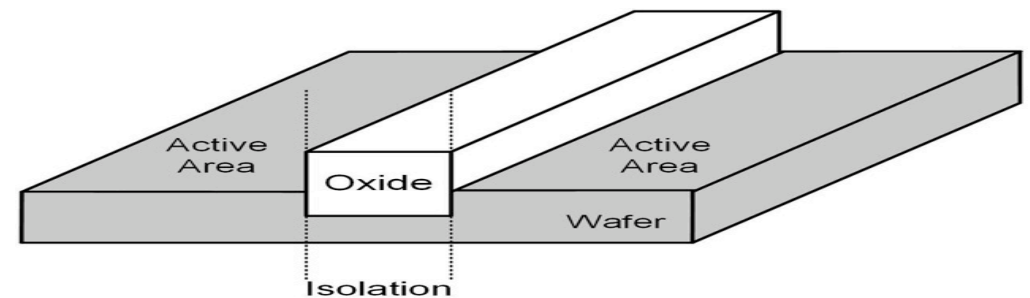
CMOS Technology scaling

Shallow Trench Isolation (STI)

- STI is a method used to electronically isolate microstructures in semiconductors and microelectromechanical systems (MEMS) devices.
- STI isolates each transistor from its adjacent transistor in order to prevent current leakage.
- Preferred method (compared to LOCOS-Local Oxidation of Silicon) for this electronic isolation for microstructures approaching $0.35\ \mu\text{m}$ and smaller.
- STI isolates MOS structures, with minimal area, than LOCOS-Local Oxidation of Silicon
 - → structure density can be maximized.



Cross section of an isolation barrier created using the LOCOS process. The sloped "bird's beak" regions are wasted space

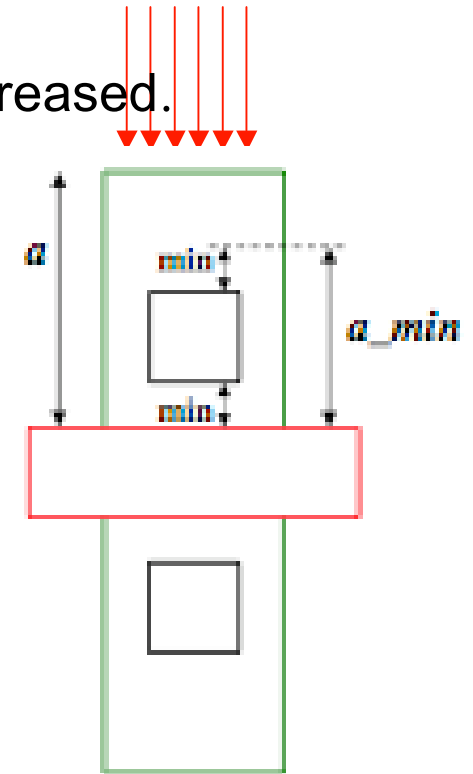


Cross section of a wafer during the STI process; the raised oxide profile will subsequently be nearly flattened by CMP

CMOS Technology scaling

Shallow Trench Isolation (STI) - Global statements

- Compressive stress in MOS channels relaxes when "a" is increased.
- Stress only affects carriers low field mobility: μ_0
 - → directly modifying all conduction parameters, such as Beta0, Ion, Ilin, gm, because:
$$I_{DS}(V_{GS}, V_{DS}) \propto \mu_0$$
- Stress impact on Vt, Theta1, Theta2 is completely negligible.



- Empirical model

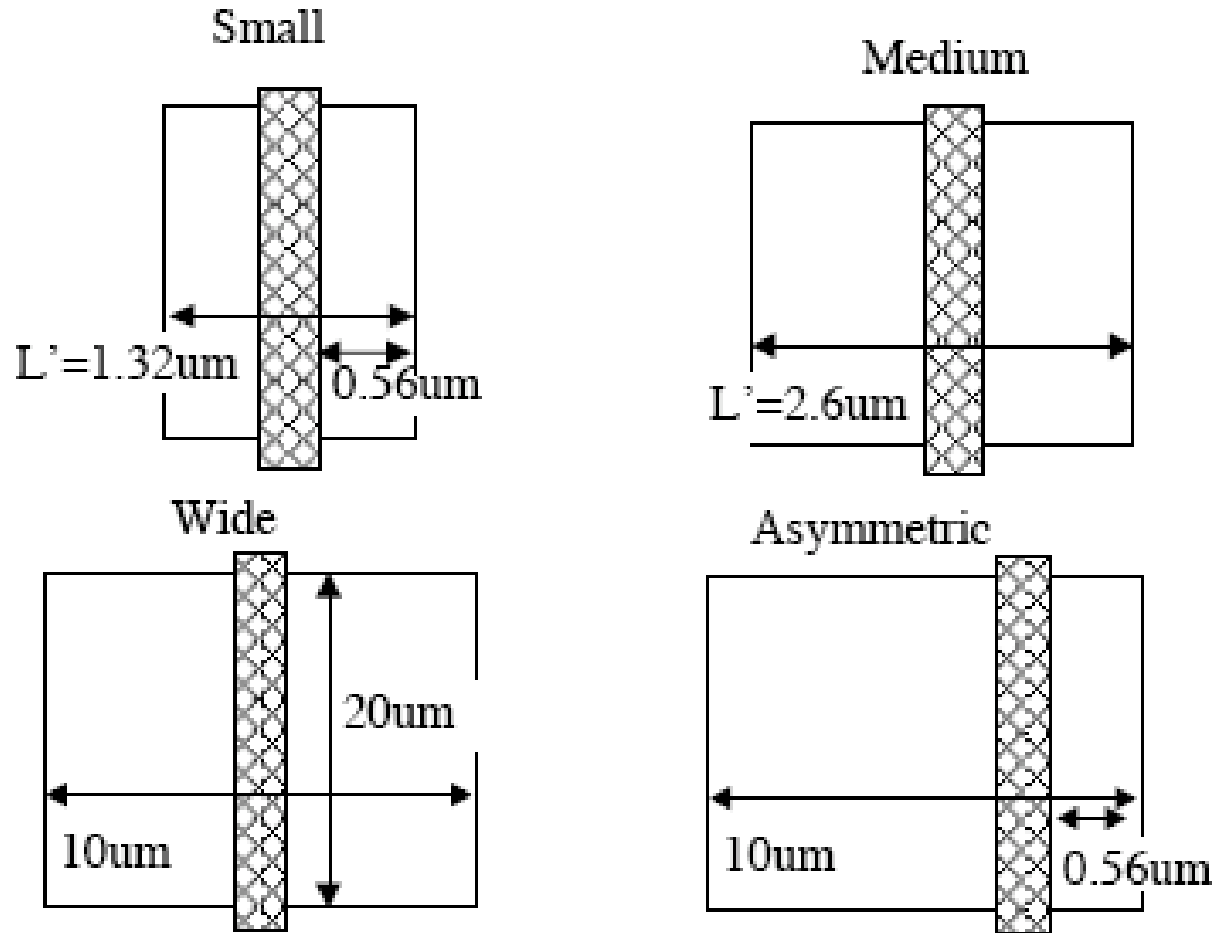
$$\mu_0(a) = \mu_{0SPICE} \cdot \left[1 + Var_max(L,W) \cdot \left(\frac{a - a_{min}}{a} \right) \right]$$

- NMOS : $Var_max \approx +12\%$
- PMOS : $Var_max \approx -12\%$
- μ_0 variation can be moved as V_{TH} variation

CMOS Technology scaling

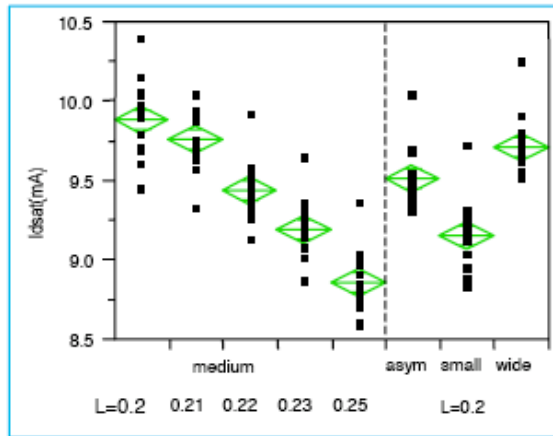
Shallow Trench Isolation (STI) - Variation of the Threshold Voltage

- Test devices

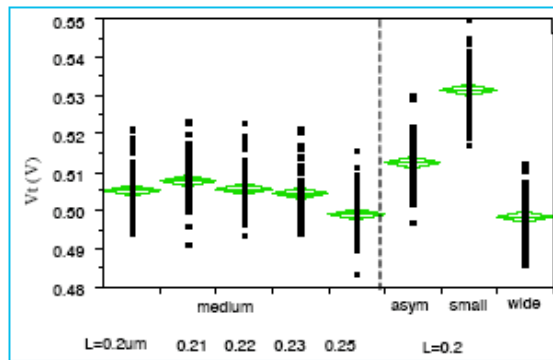


CMOS Technology scaling

Shallow Trench Isolation (STI) - Experimental results

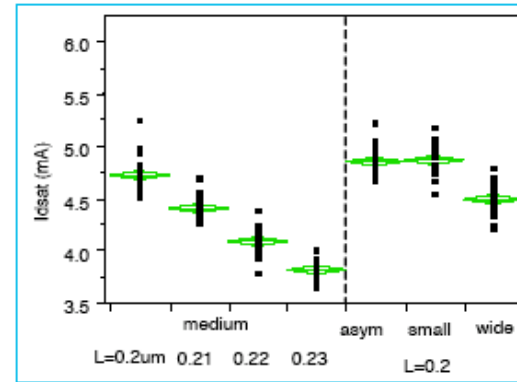


(a)

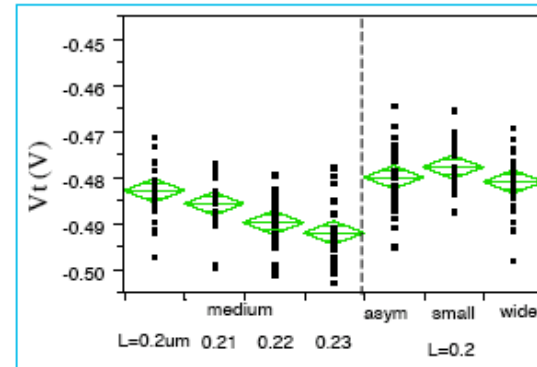


(b)

Fig 3. NMOS Idsat and Vt vs. device layout. The degradation in Idsat of a small overlap 0.2um transistor is equivalent to a 30 nm increase in gate length.

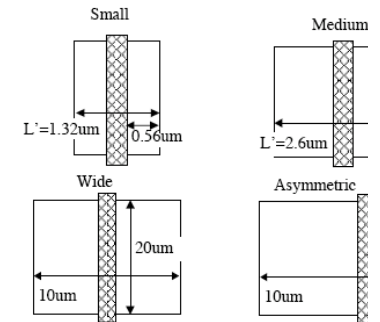


(a)



(b)

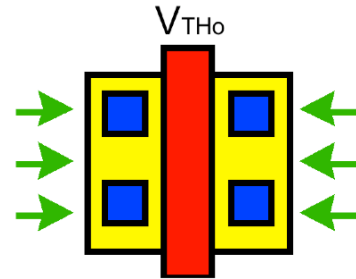
Fig 5. PMOS Idsat and Vt layout dependence.



CMOS Technology scaling

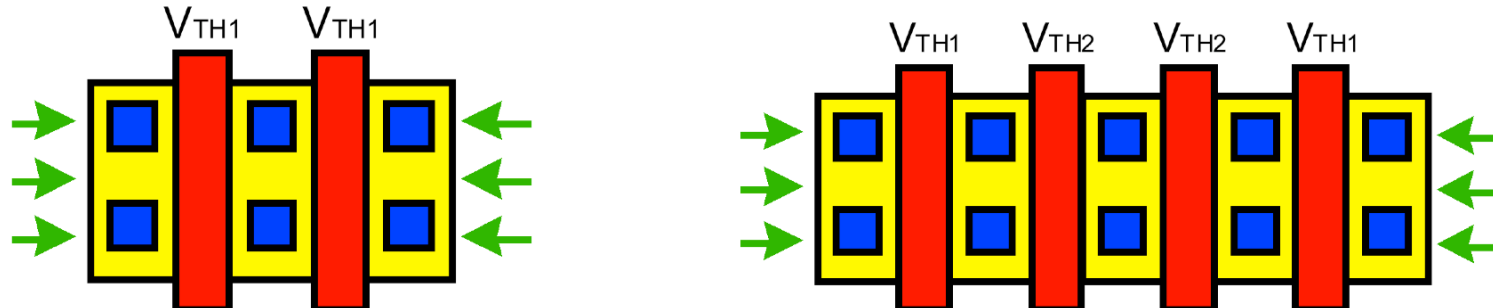
Shallow Trench Isolation (STI) - Simulation issues

- Technology models are extracted from the unitary transistor



- Both sides are affected by STI

- Stacked transistors may have different V_{TH}



- “Internal” devices do not see STI and are well matched (same V_{TH2})
 - Good for current mirrors (current steering DAC)
- BUT they are not modeled (post-layout in some Design Kits)
 - For matched devices (current mirror, etc..) use external dummy devices

CMOS Technology scaling

V_{TH} Mismatch*

TABLE II

THRESHOLD VOLTAGE MISMATCH STANDARD DEVIATIONS IN STRONG INVERSION ($\sigma_{\Delta V_t}$) AND SUBTHRESHOLD V_{gs} MISMATCH ($\sigma_{\Delta V_{gs}}$ at $I_d = 10 \text{ pA}/(W/L)$) AND THE CORRELATIONS BETWEEN THE MISMATCH OBSERVATIONS FOR A RANGE OF TRANSISTOR DIMENSIONS

Area

drawn_W (μm)	drawn_L (μm)	$\sigma_{\Delta V_t}$ (strong inversion) (mV)	$\sigma_{\Delta V_{gs}}@[I_d=10\text{pA}/(W/L)]$ (mV)	Correlation factor R^2
10	4	0.7	2.1	0.07
2	10	1.1	3.0	0.05
10	1	1.7	4.5	0.03
0.4	10	2.5	5.1	0.24
2	1	5.4	10	0.09
0.32	4	4.0	6.6	0.32
2	0.2	12	27	0.26
0.4	1	8.9	12	0.25
0.4	0.24	23	38	0.32
0.32	0.2	27	44	0.45

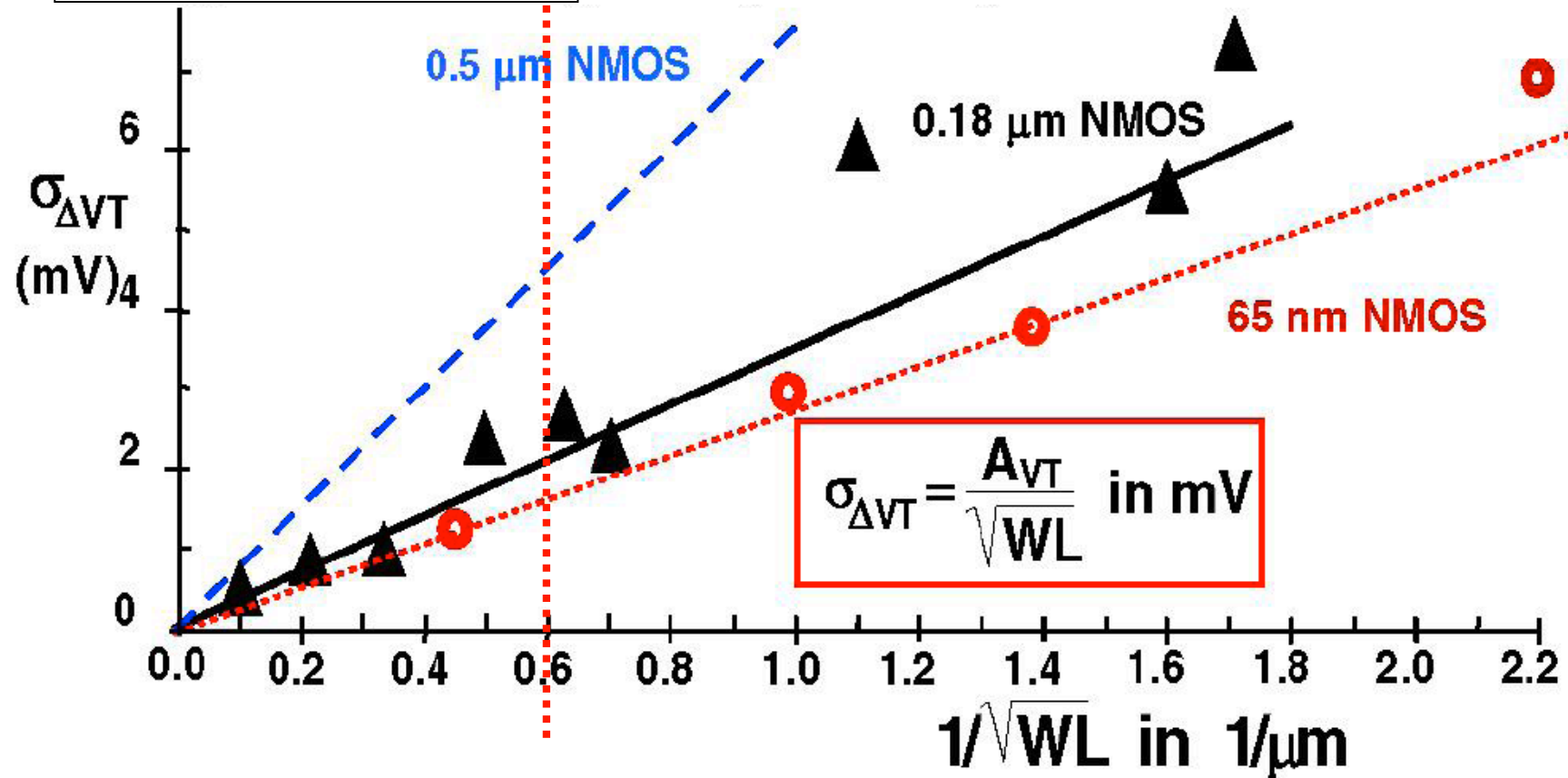
*Pineda de Gyvez, Tuinhout, "Threshold Voltage Mismatch and Intra-Die Leakage Current in Digital CMOS Circuits", IEEE JSSC Jan. 2004



CMOS Technology scaling

V_{TH} Mismatch

For a given (W·L)
scaled technologies
give better matching



CMOS Technology scaling

Mismatch for subthreshold and saturation region

- Matching in saturation is better than in WI

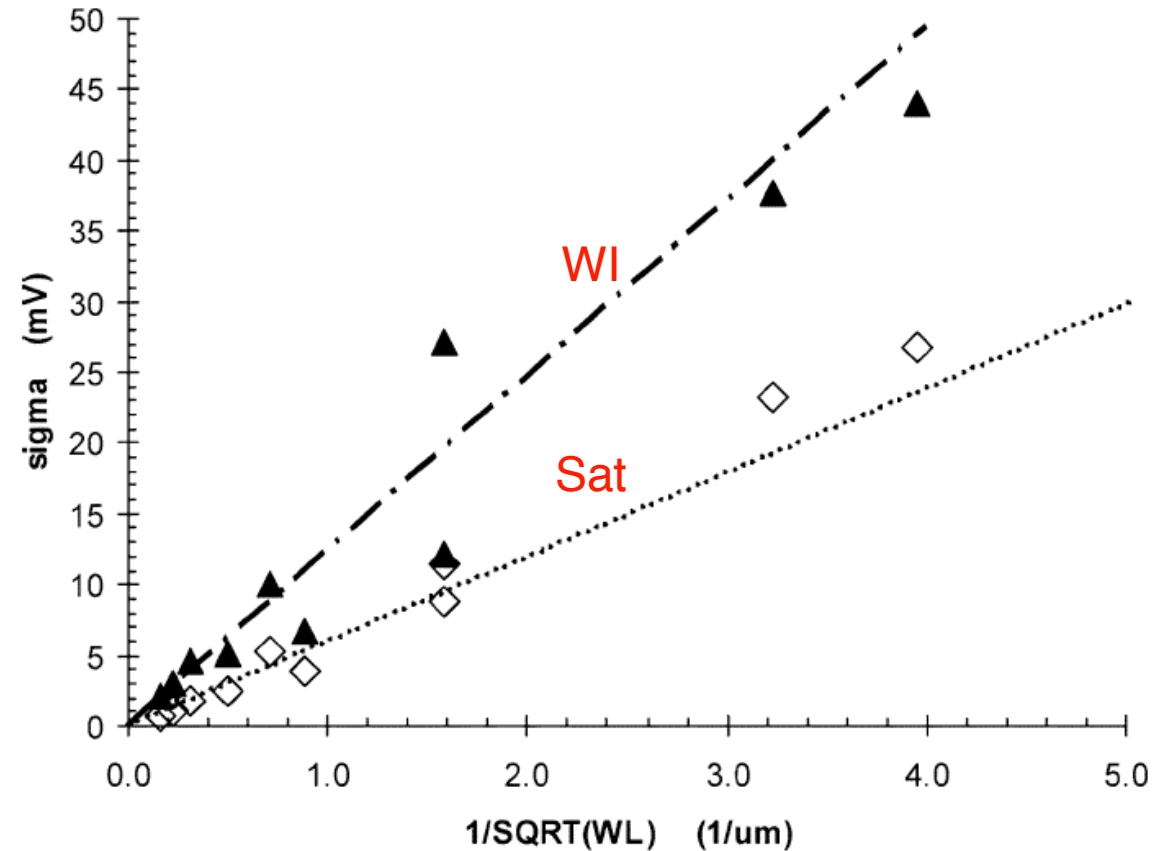


Fig. 12. Mismatch area scaling graph. Diamonds: strong inversion (linear region) V_t mismatch. Triangles: subthreshold V_{gs} mismatch (at 10 pA/square). The 6 $mV\mu m$ and 12.5 $mV\mu m$ lines are estimates for the corresponding area scaling factors for the strong and weak inversion mismatch standard deviations, respectively.

CMOS Technology scaling

Device Mismatch

- Mismatch of two matched transistors identical by design can be:

$$\Delta V_T = V_{T1} - V_{T2} \quad \text{with} \quad \sigma_{V_T} = \sigma(\Delta V_T) = A_{V_T} / \sqrt{WL}$$

$$\Delta\beta/\beta = 2(\beta_1 - \beta_2) / (\beta_1 + \beta_2) \quad \text{with} \quad \sigma_\beta = \sigma(\Delta\beta/\beta) = A_\beta / \sqrt{WL}$$

- A_{V_T} and A_β depends on process, layout and more ...

- Same gate voltage

$$\sigma\left(\frac{\Delta I_d}{I_d}\right) = \sqrt{\sigma_\beta^2 + \left(\frac{g_m}{I_d} \sigma_{V_T}\right)^2}$$

- Same drain current

$$\sigma(\Delta V_G) = \sqrt{\sigma_{V_T}^2 + \left(\frac{I_d}{g_m} \sigma_\beta\right)^2}$$

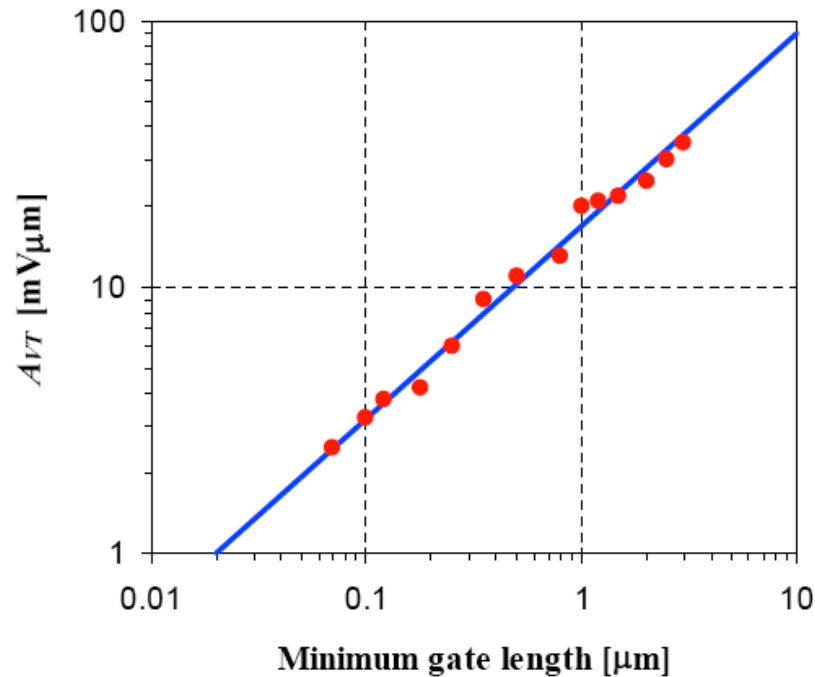
CMOS Technology scaling

Device Mismatch

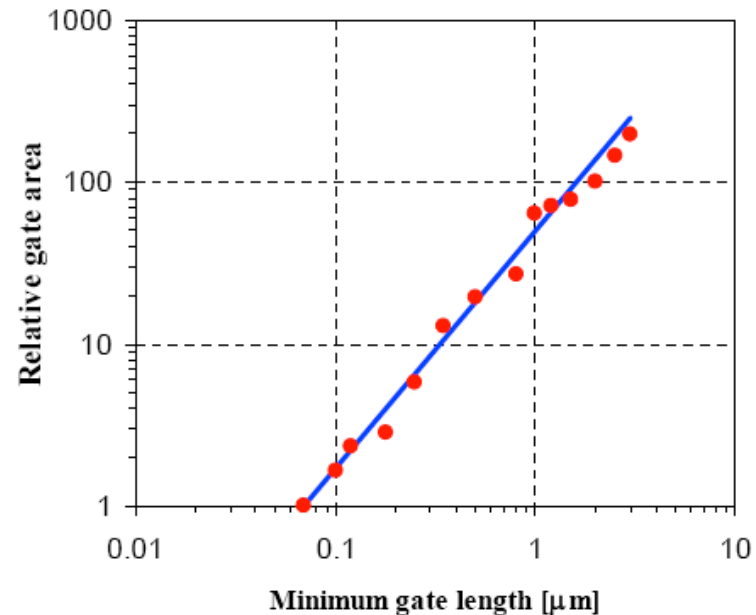
- Mismatch per unit area decreases as technologies are scaled down
- From theory and ideal scaling

$$A_{VT} \propto t_{ox} \propto L_{min}$$

- In reality A_{VT} does not scale as fast as L_{min}

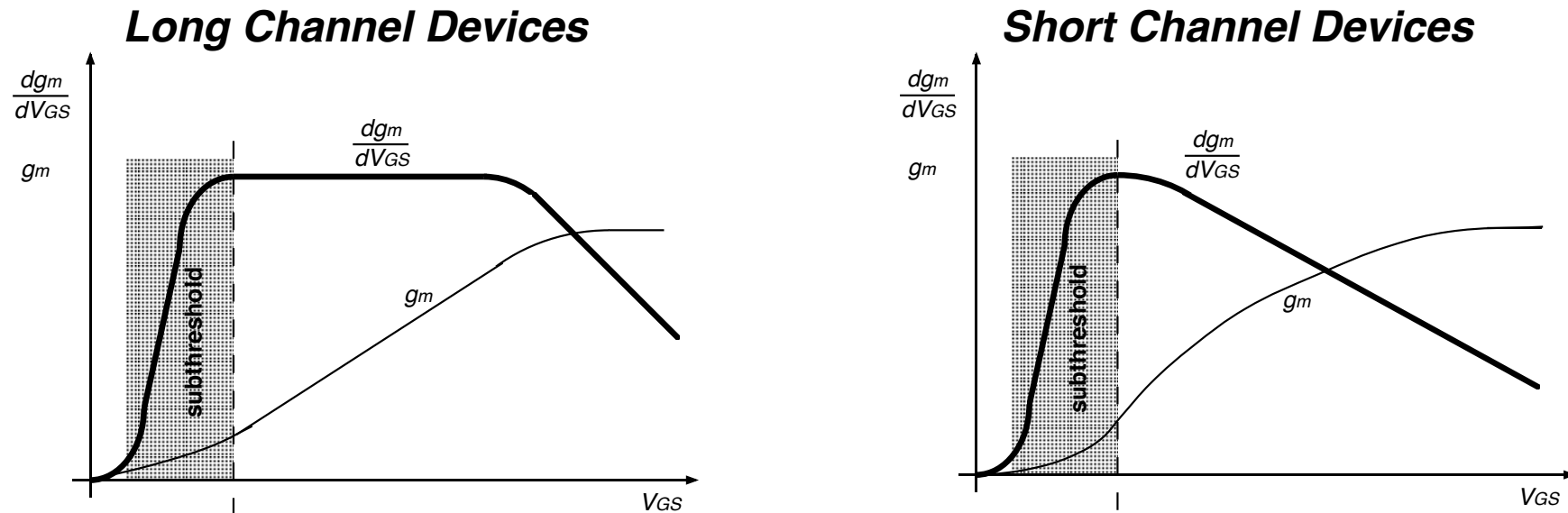


Gate area required for any given $\sigma(\Delta V_T)$ normalized to the $L_{min} = 70$ nm



CMOS Technology scaling

Transconductance in short channel devices



$$g_m \cong \mu_o \cdot C_{ox} \cdot \frac{W}{L} \cdot \frac{V_{GS} - V_{TH}}{1 + 2 \cdot \left(\theta + \frac{1}{\epsilon_c \cdot L} \right) \cdot (V_{GS} - V_{TH})}$$

- It is still valid that: $g_m \cong \frac{2 \cdot I_D}{(V_{GS} - V_{TH})}$
- For very strong electrical field perpendicular to the channel, g_m becomes independent on I_D and becomes also independent of L

$$g_m \cong W \cdot C_{ox} \cdot v_{sat}$$

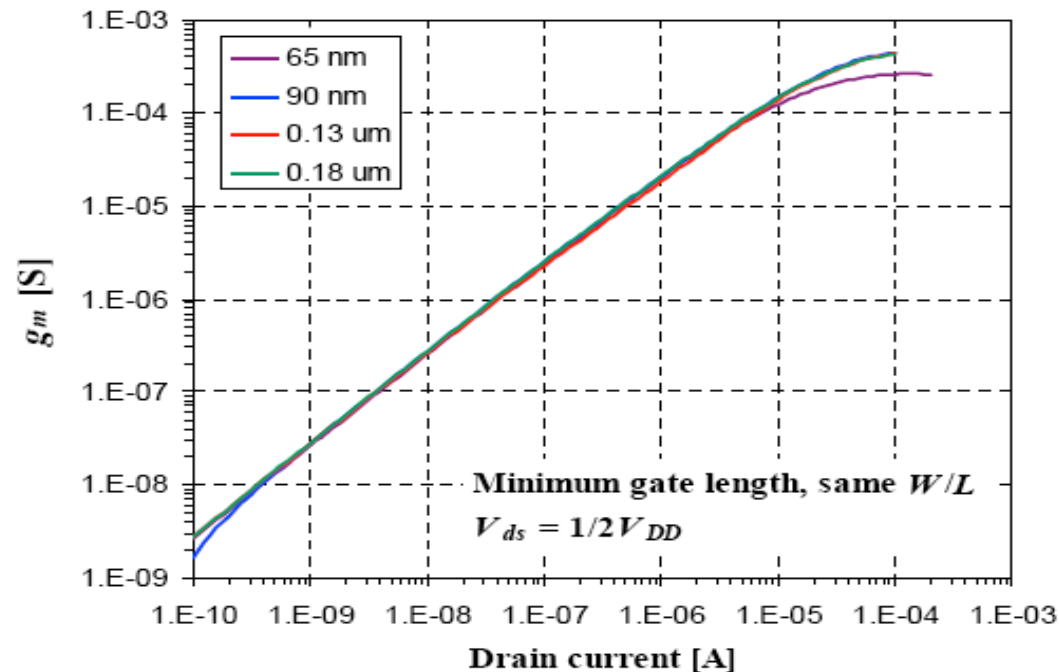
CMOS Technology scaling

Transconductance in Scaled Technologies*

- Transconductance is almost independent of the technology node
- For a velocity saturated channel

$$g_m \cong W \cdot C_{ox} \cdot v_{sat}$$

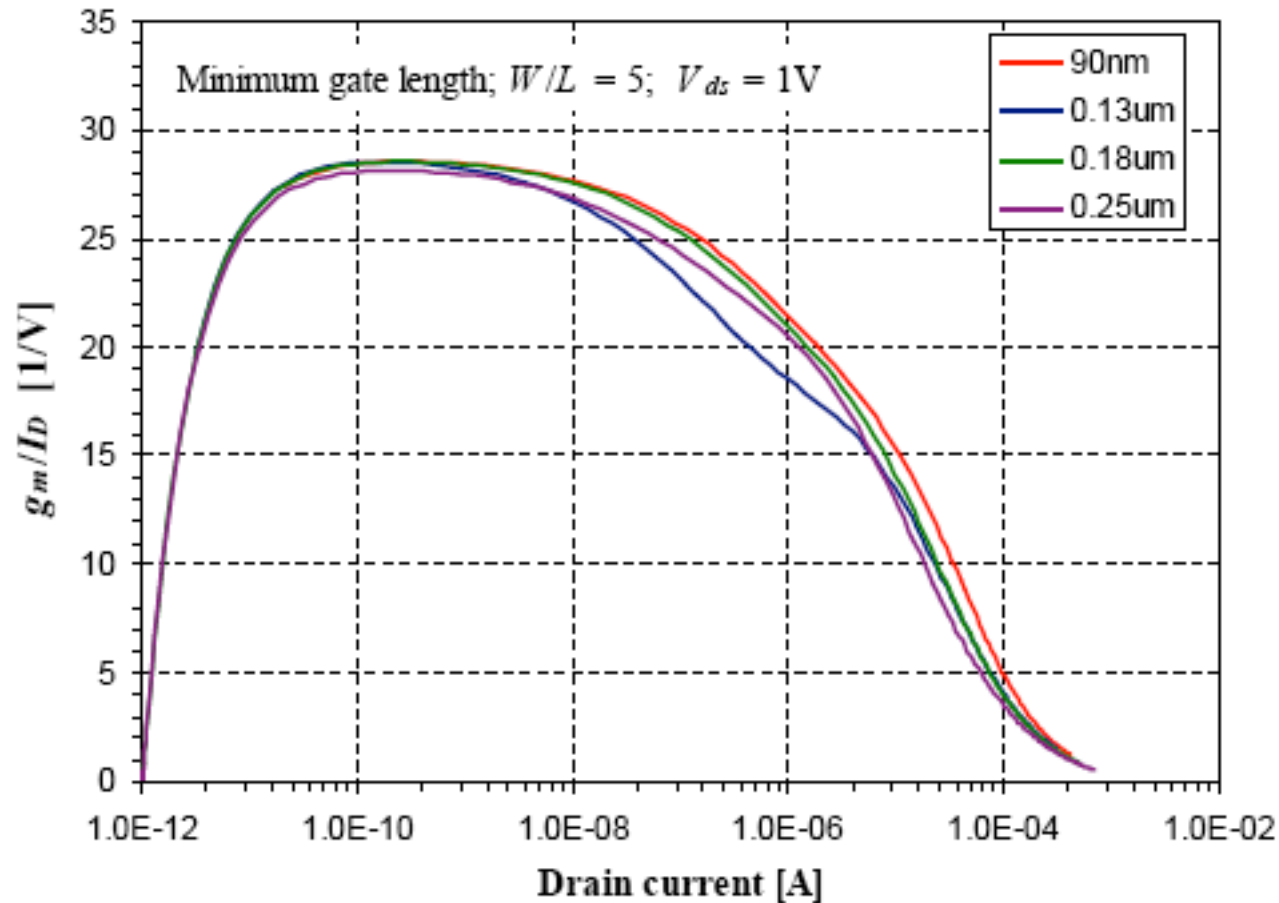
$$W \propto L \quad C_{ox} \propto \frac{1}{L} \quad \Rightarrow \quad g_m \text{ does not scale}$$



■ _____
* Trond Ytterdal , 2006

Technology scaling

Transconductance efficiency

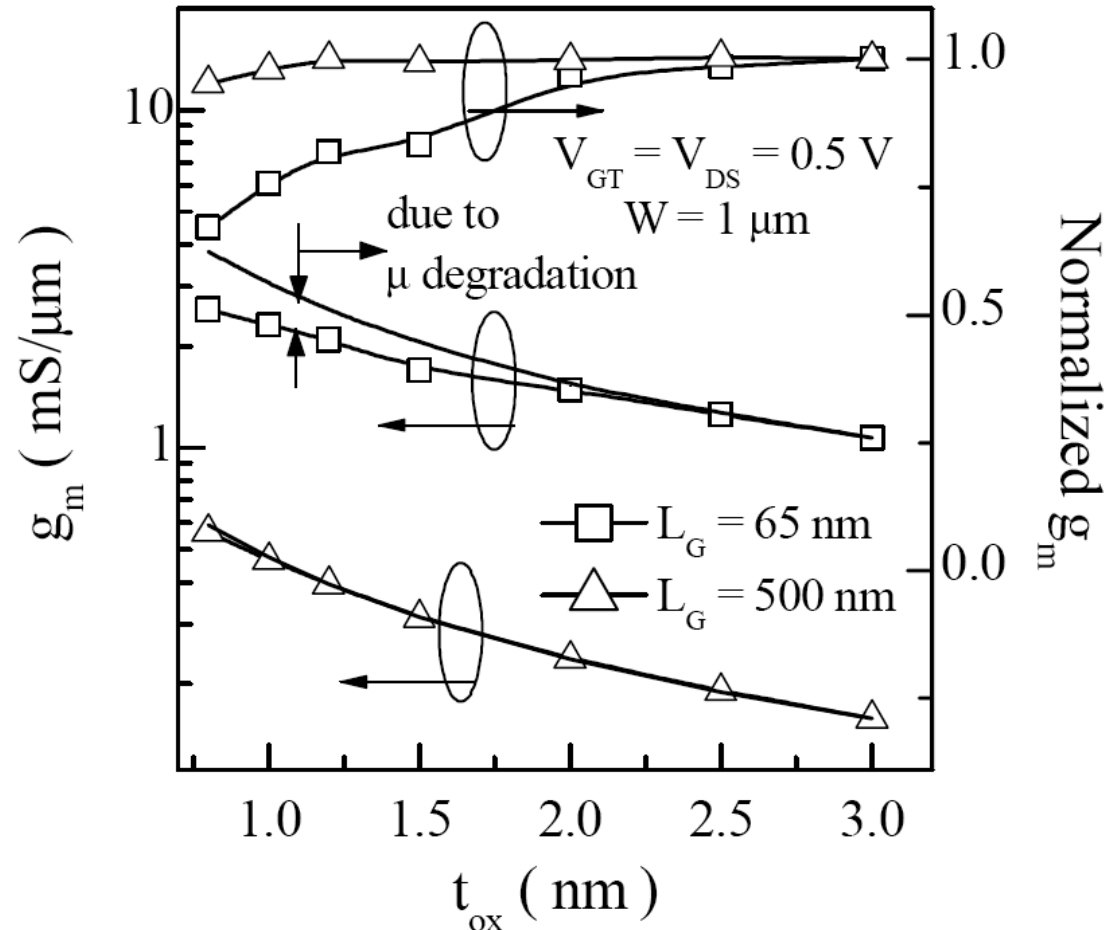


- The transistor is most efficient (maximum bang for the buck) in weak inversion
- Maximum value is nearly independent of technology

CMOS Technology Scaling

Transconductance in short channel devices*

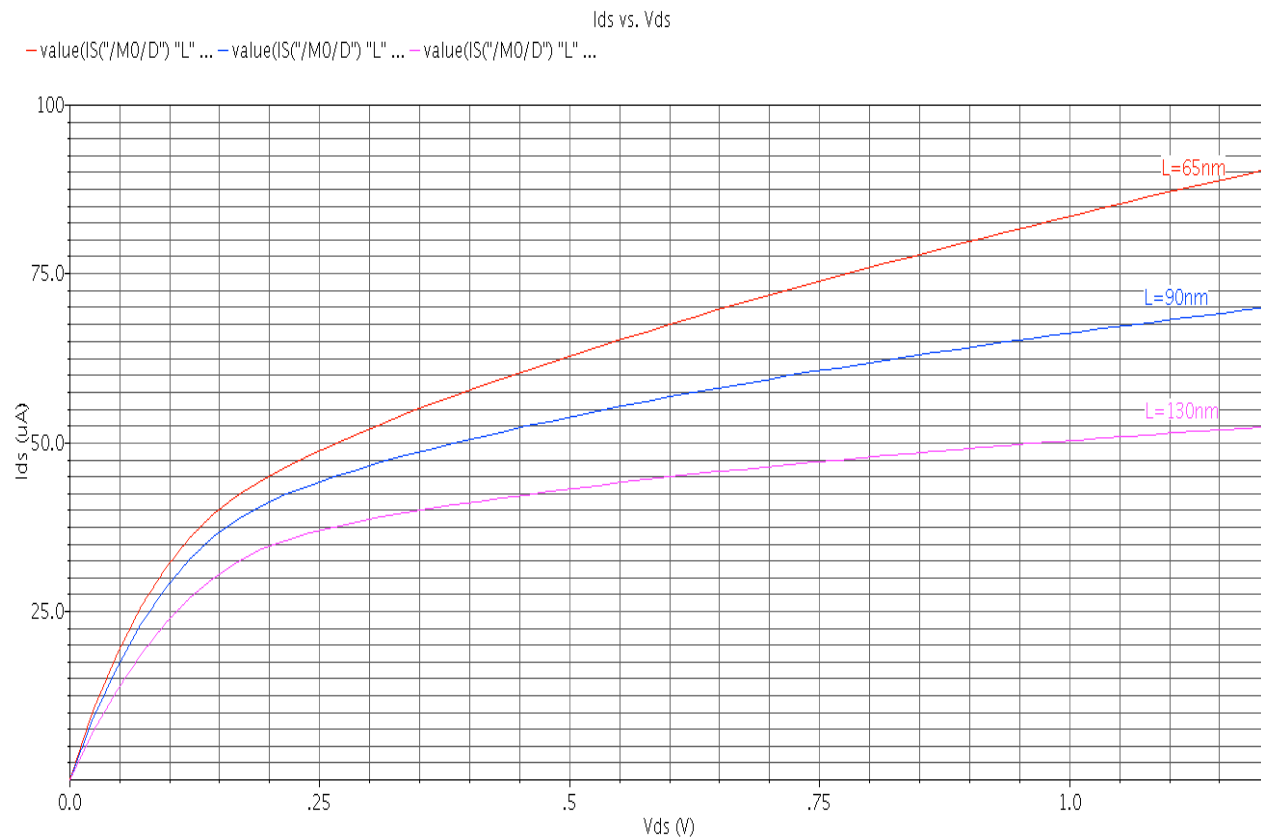
- Device transconductance (g_m) and its normalized value (normalized to g_m observed at $t_{ox} = 3$ nm) as a function of gate oxide thickness



CMOS Technology Scaling

Channel length modulation effects

- The output characteristic ($I_{DS}-V_{DS}$) of the MOS transistor is plotted for different L value, while maintaining the same W/L ratio (=10)



L=65nm

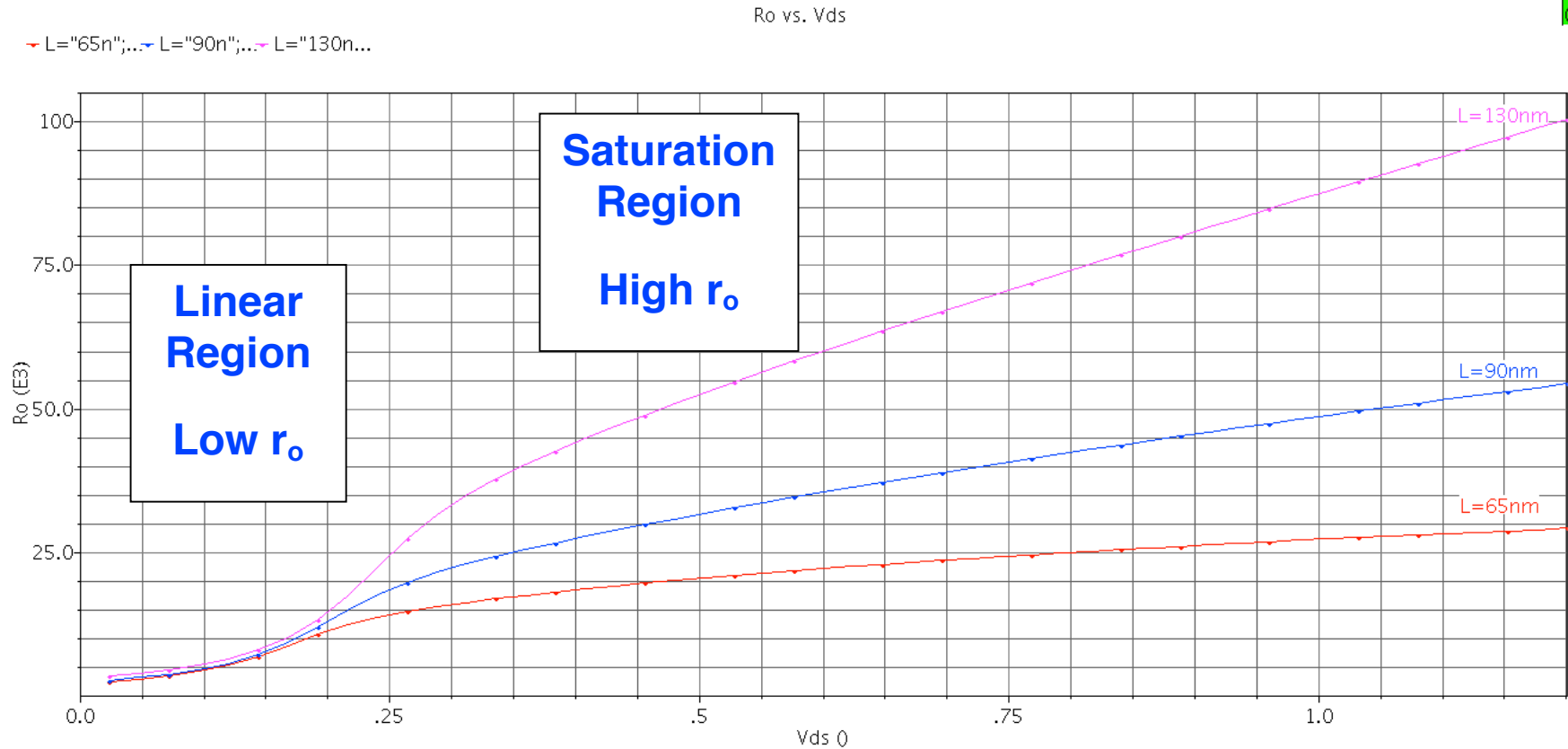
L=90nm

L=130nm

CMOS Technology Scaling

Channel length modulation effects

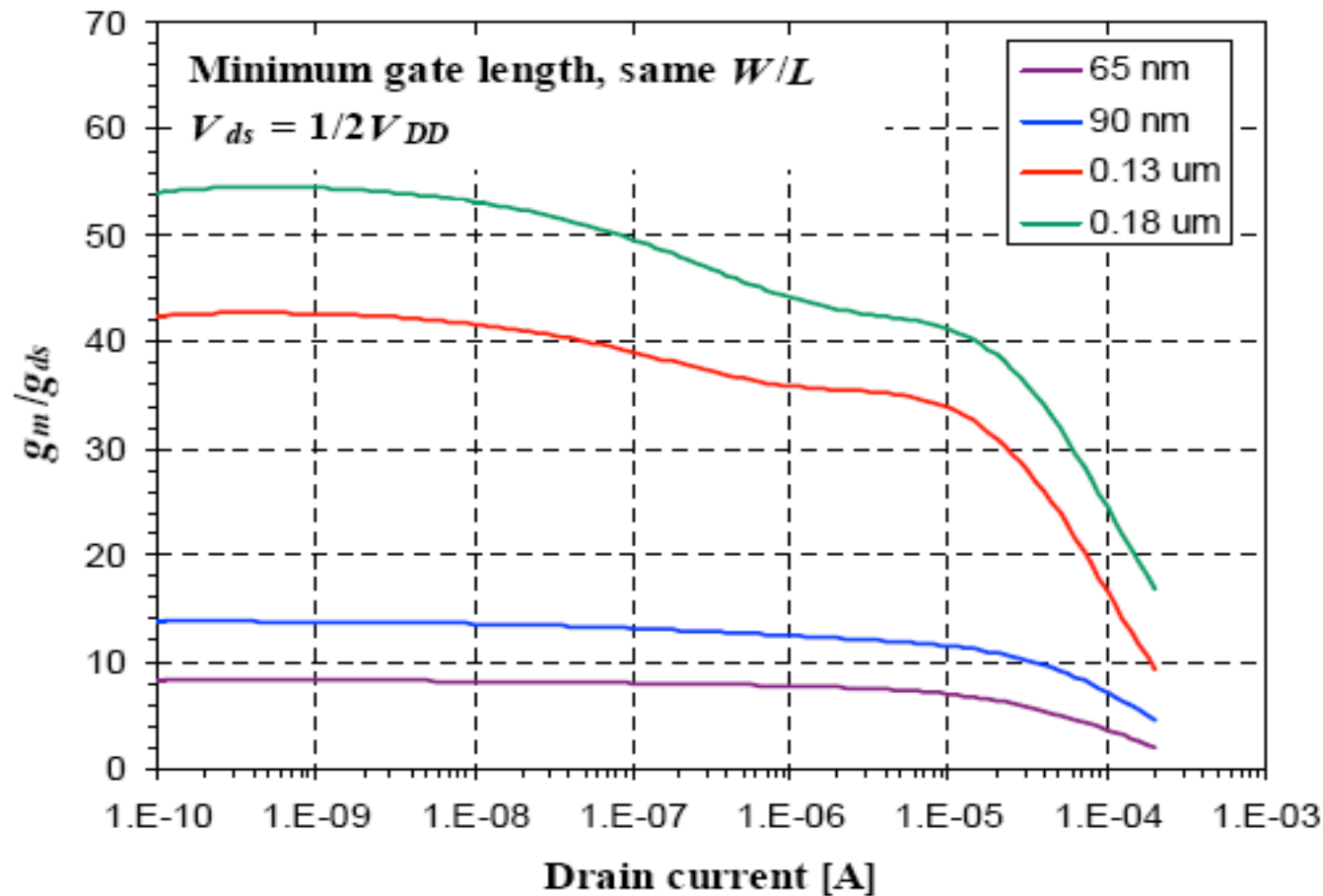
- The inverse of derivative of (I_{DS} -vs.- V_{DS}) is the output impedance ($r_o = (\partial I_{DS} / \partial V_{DS})^{-1}$)



CMOS Technology Scaling

Intrinsic gain

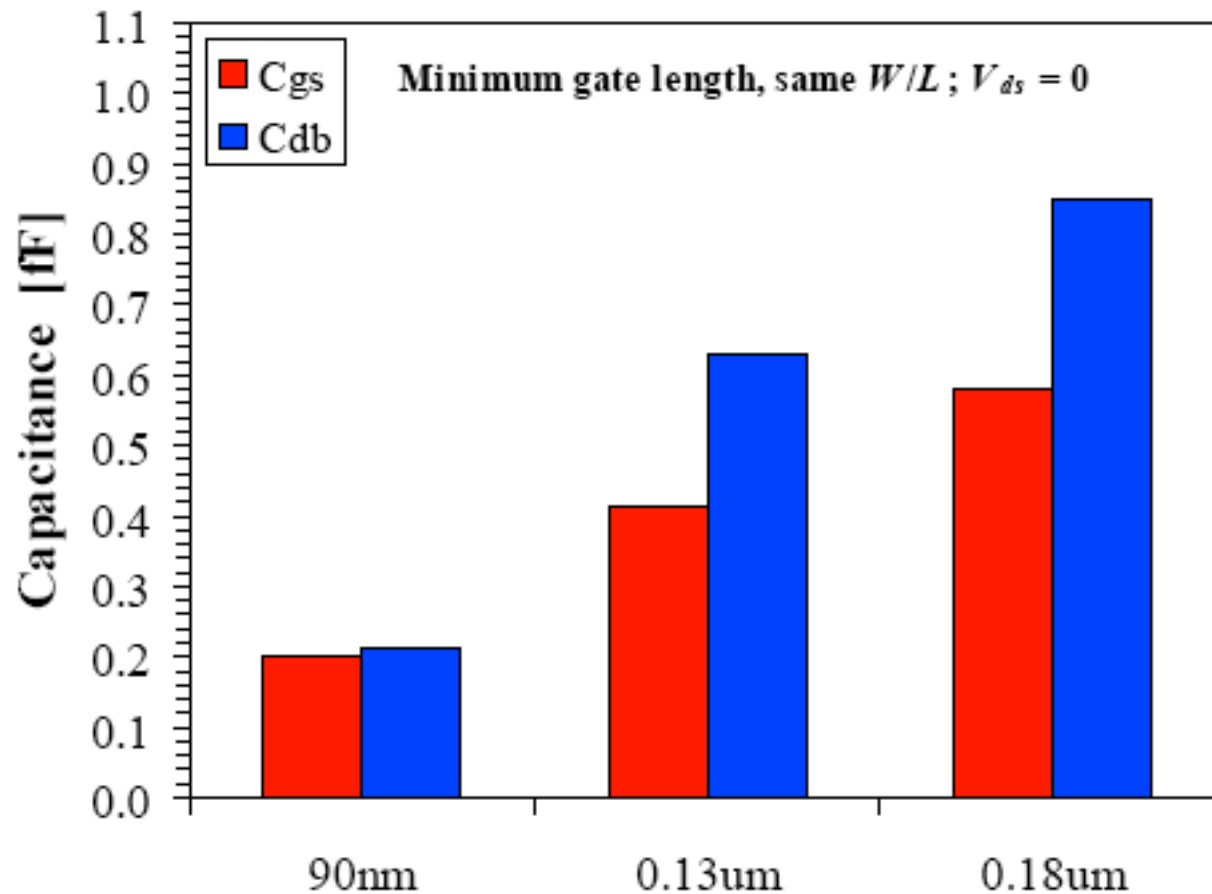
- Intrinsic gain is reduced as technologies are down scaled down.
 - At the 65nm node the maximum intrinsic gain is reduced by more than 80% compared to the gain at the 0.18 μm



CMOS Technology scaling

Capacitor

- Capacitances extracted from NMOS having minimum drain and source areas for the given W/L (~ 3).

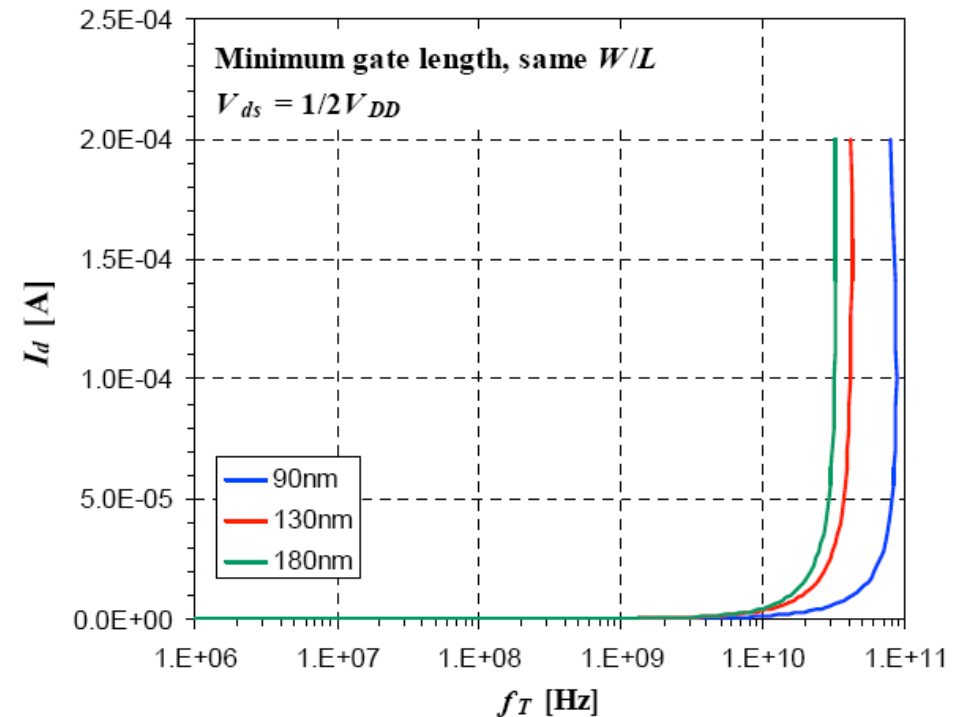
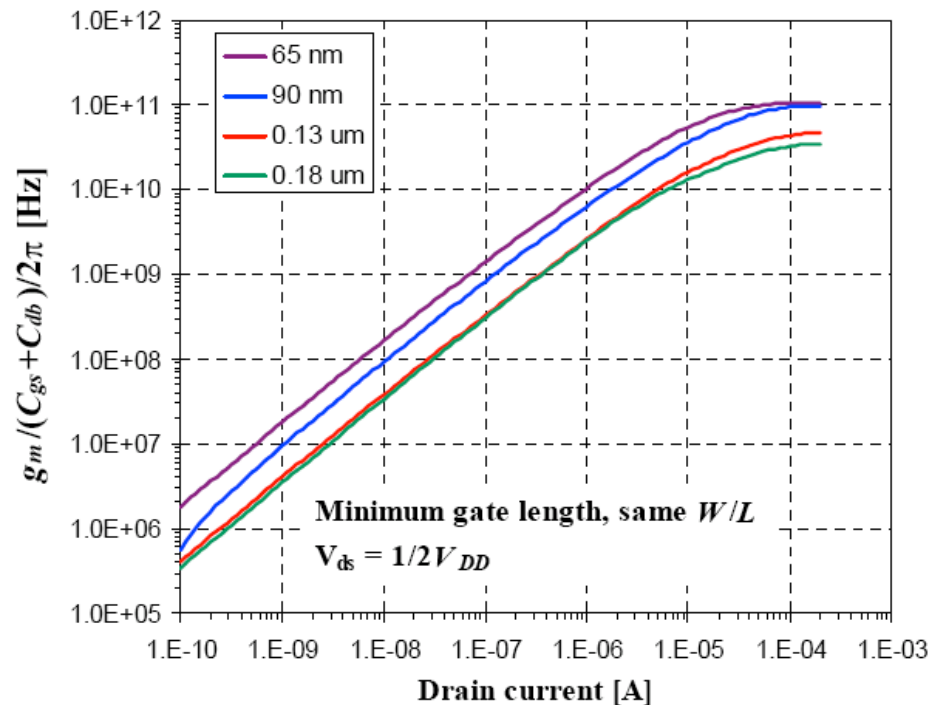


CMOS Technology scaling

Maximum operating frequency (f_T)

- The maximum speed of an amplifier is limited by the ratio of the transconductance and the capacitance of a transistor:

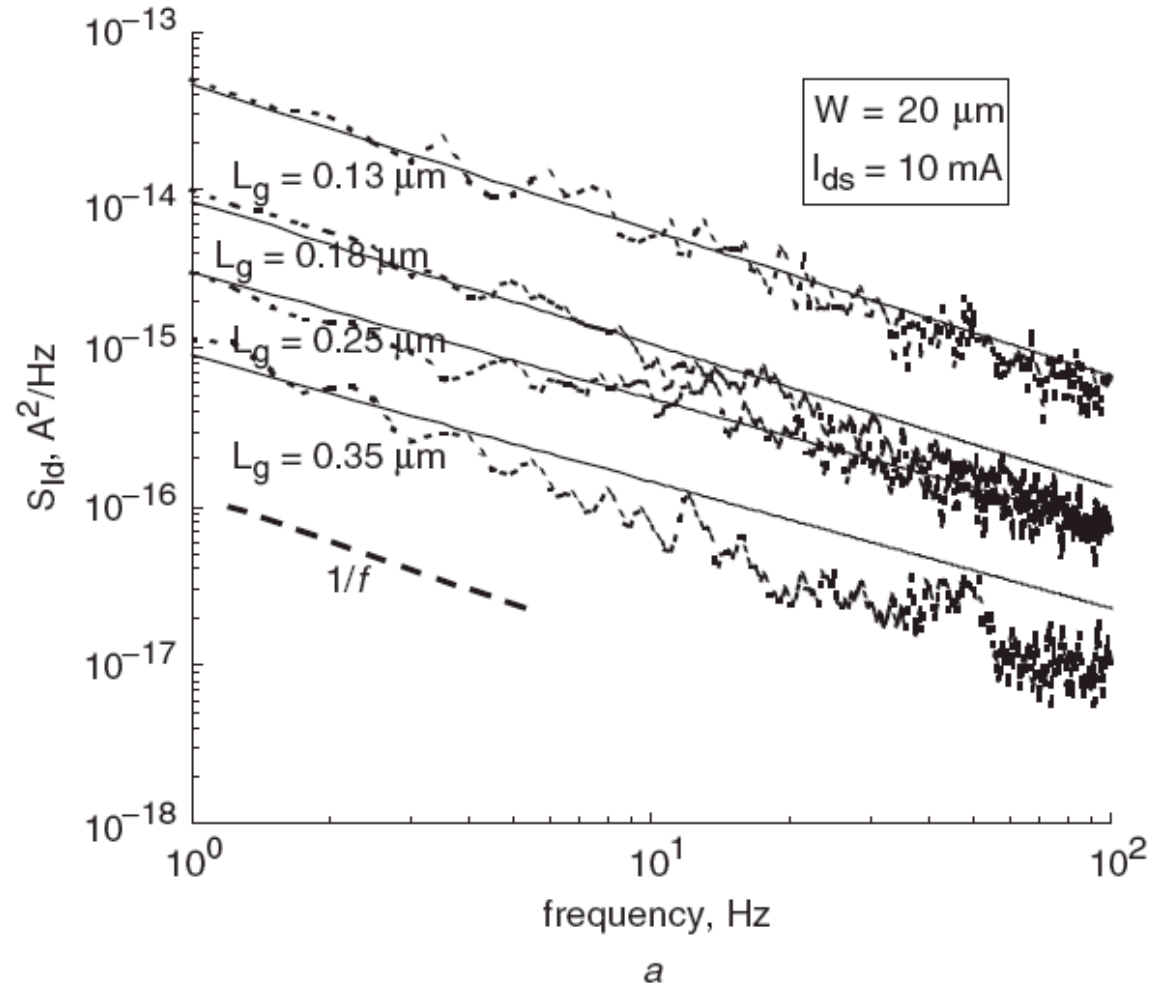
$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd} + C_{db})}$$



CMOS Technology scaling

1/f noise*

- Effect of technology scaling on drain current noise spectra of thin gate oxide, minimum channel length NMOS
- V_{DS} for each technology node corresponds to its respective V_{DD}



■ _____

* K.W. Chew, K.S. Yeo and S.-F. Chu, "Impact of technology scaling on the 1/f noise of thin and thick gate oxide deep submicron NMOS transistors", IEE Proc.-Circuits Devices Syst., Vol. 151, No. 5, October 2004



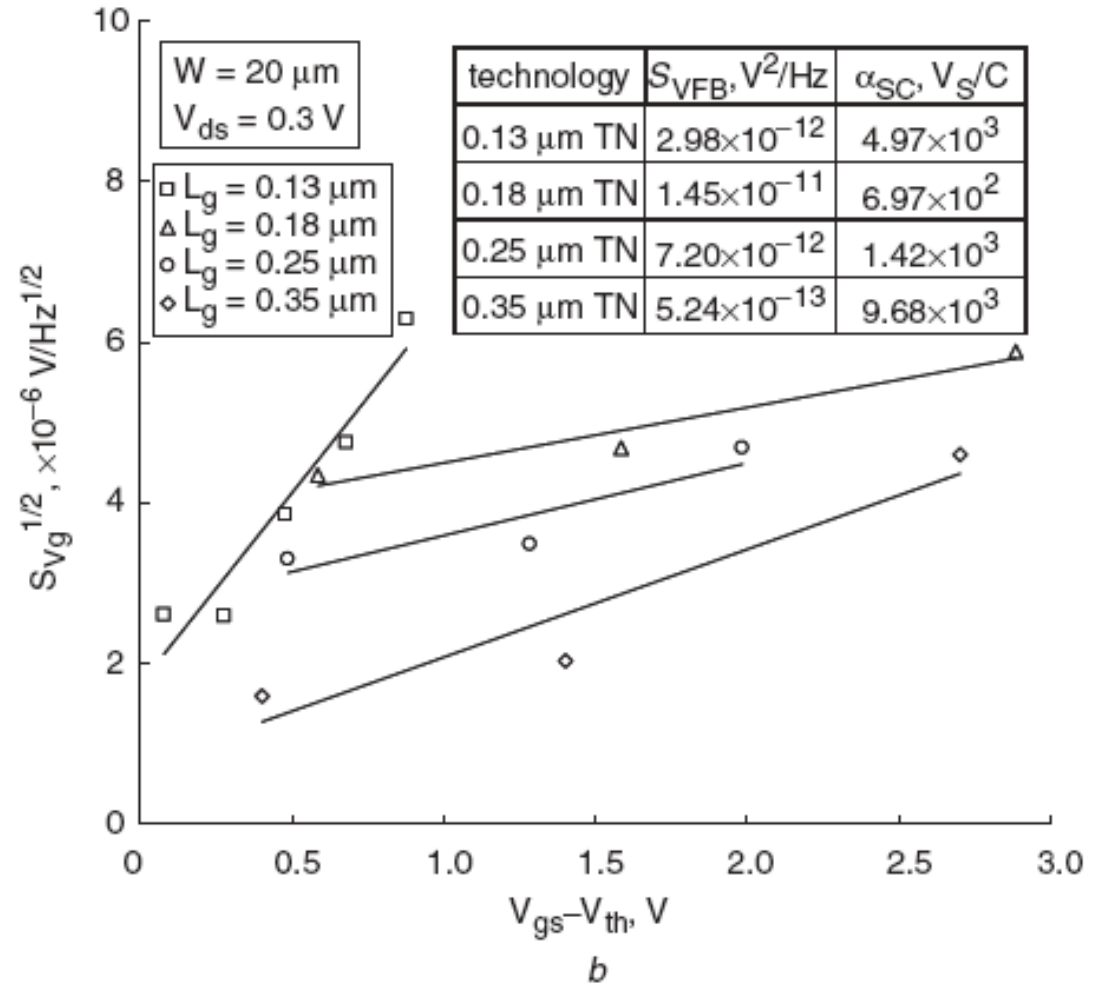
CMOS Technology scaling

1/f noise

Fig. 4 Voltage noise spectral density against gate overdrive voltage ($V_{gs} - V_{th}$) for thin gate oxide, minimum channel length n-MOSFETs in linear operation at 10 Hz

a S_{Vg}
b $S_{Vg}^{1/2}$

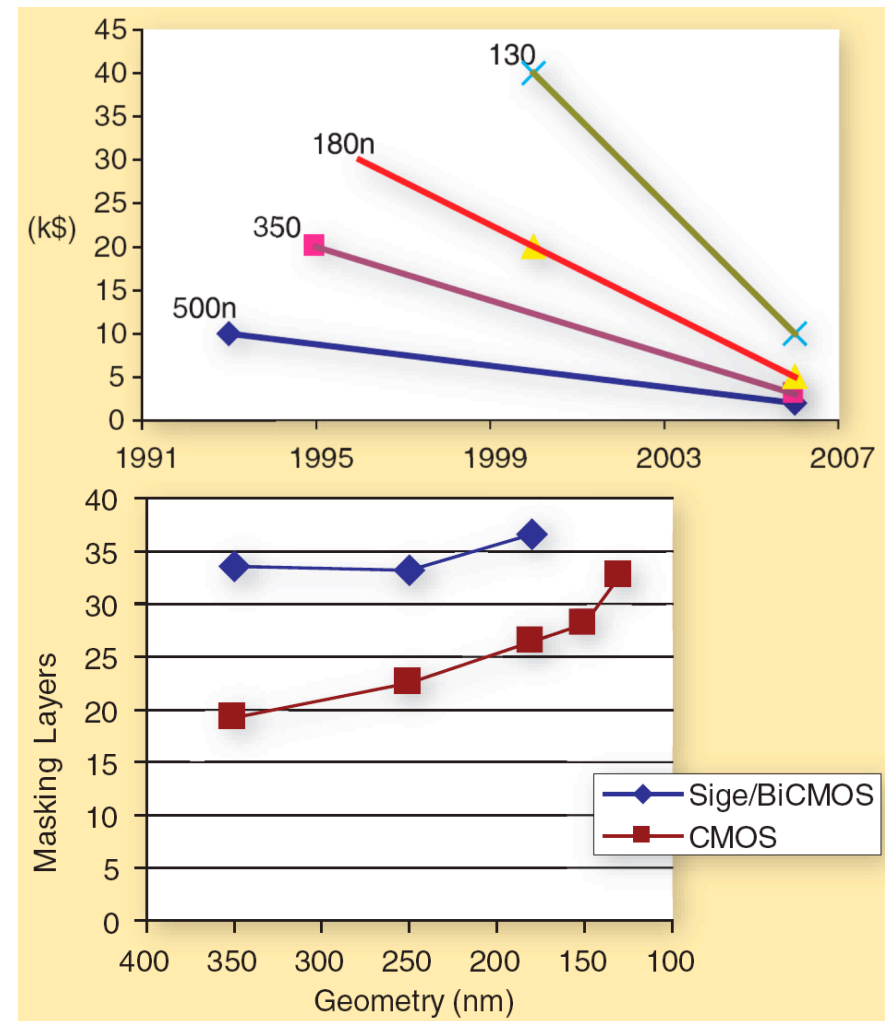
Shown insert is a table listing the extracted flat band spectral density, S_{VFB} and the scattering parameter, α_{sc} for each technology node
— linear fits of the experimental data
□ ○ ◇ △ experimental data



CMOS Technology scaling

Costs

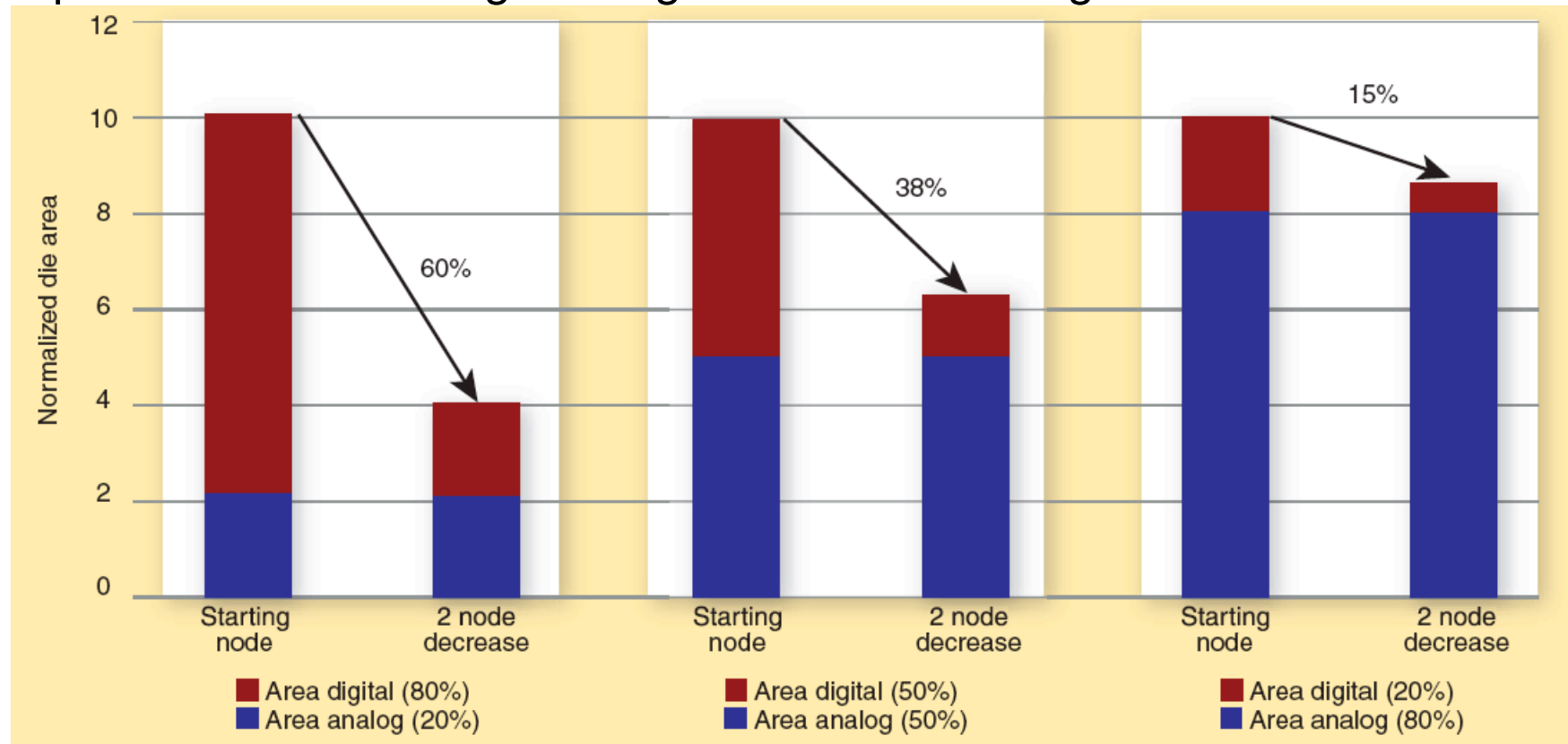
- Mask cost trends by CMOS transistor node
- CMOS typically requires less masking steps than SiGe/BiCMOS.
- Lower wafer costs and faster manufacturing cycle times.
- The number of masking steps increases with CMOS scaling and, given the masking cost increase per node
 - → the cost advantage offered by CMOS begins to erode as geometries decrease.



Technology scaling

Die size

- Die area reduction achieved for a two-node CMOS geometry shrink for various percent mix of analog and digital in an SoC design



- Low-cost digital can be used to fix analog performance loss

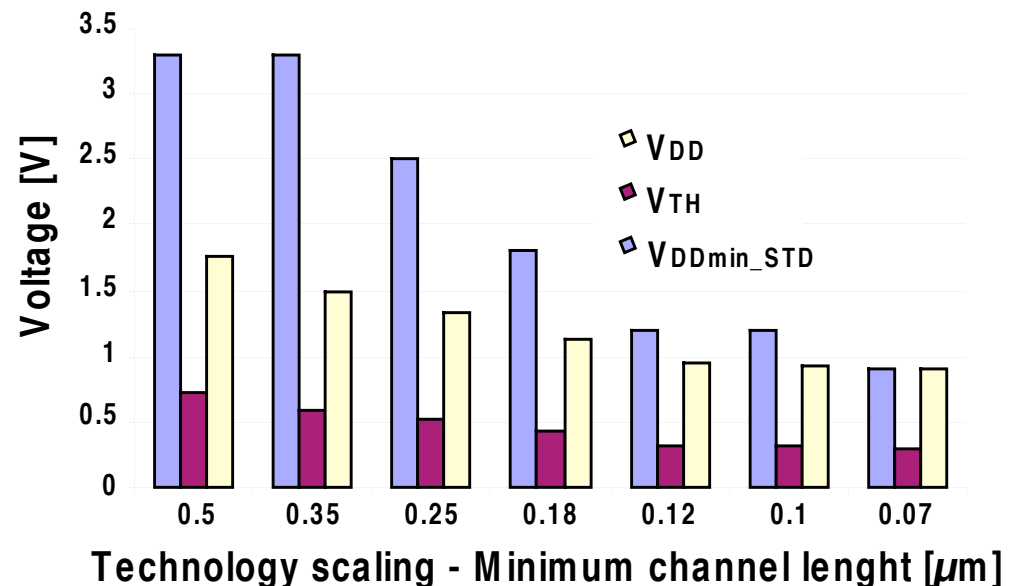
LV Analog Design in scaled CMOS technology

Outline

- Introduction
 - Basic CMOS operation
 - CMOS technology scaling trends
 - What is LV ←←←
 - LV Analog design
 - LV at transistor level
 - LV at circuit level
 - Current Mirror
 - Opamp design
 - Basic bandgap design
 - LV at system level
 - Active-RC filter design
 - Gm-C filter design
 - SC circuit design

Introduction: Why LV ?

- Technology scaling
 - CMOS Mixed (analog-digital) systems popularity is increasing and digital section forces the use of the latest scaled-down CMOS technology (increased number of function for the same die area)
 - Scaled-down CMOS technologies operate from lower and lower V_{DD}
 - The maximum acceptable electric field limits V_D
 - V_{TH} follows V_{DD} scaling



- Application requirements
 - Portable systems require the use of few battery cells (when possible a single one, i.e. $V_{DD}=1.2\text{V}$ with $V_{DD}=0.9\text{V}$ worst case)

Why LV ?

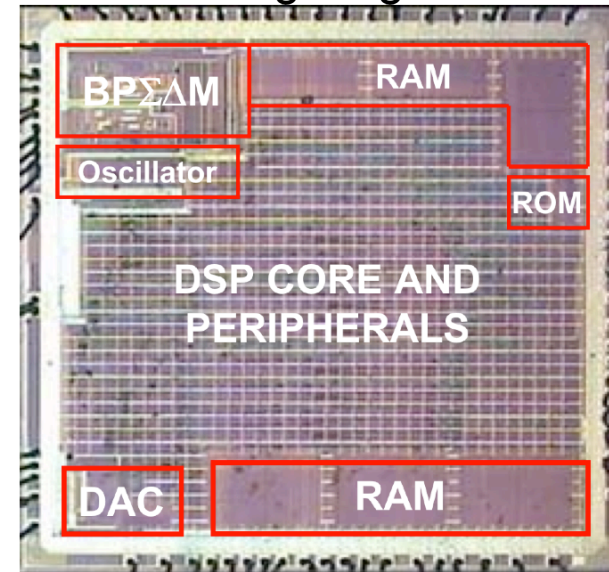
CMOS Technology scaling

- For CMOS SoC's,
 - the larger digital part forces the use of the latest scaled-down CMOS technology
 - increased number of function for the same die area
- They allow an increased number of function for the same die area
- They reduces the digital part power consumption
 - Example: FM receiver (JSSC2004)

BiCMOS Fully Analog Solution



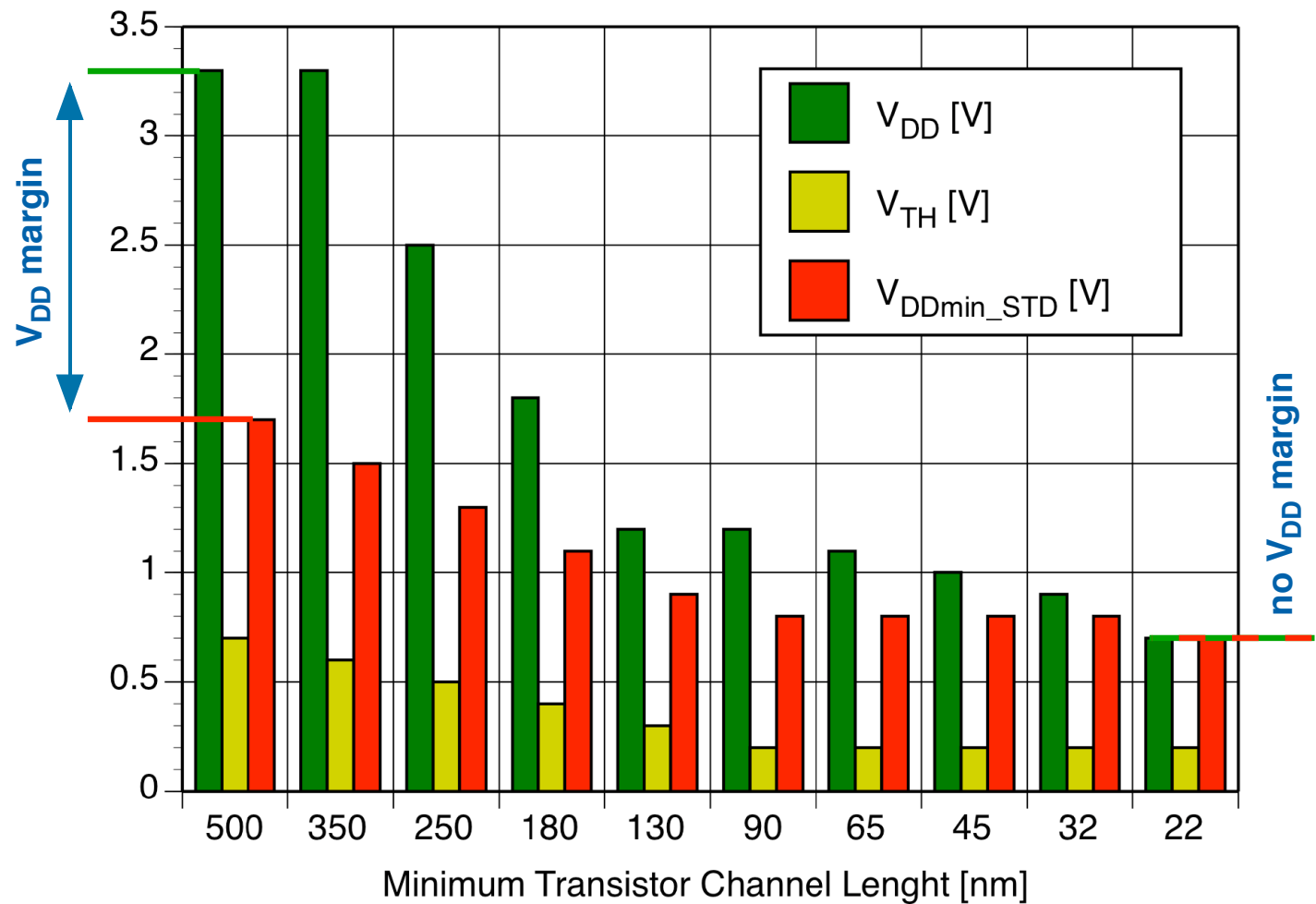
CMOS Analog&Digital Solution



Why LV ?

CMOS Technology scaling

- In scaled-down CMOS technologies the maximum acceptable electric field limits V_{DD}
- V_{TH} follows V_{DD} scaling
- V_{TH} scales faster than V_{DD}



MOS behaviour

Worst case variation – (65nm node)

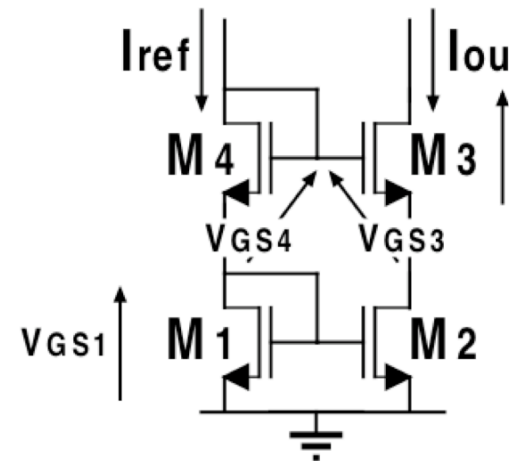
- The following table is composed for:
 - $L=90\text{nm}$; $V_{GS}=730\text{mV}$; $V_{DS}=1.2\text{V}$

	<i>Nominal</i>			<i>Fast</i>			<i>Slow</i>		
	<i>-40°C</i>	<i>27°C</i>	<i>120°C</i>	<i>-40°C</i>	<i>27°C</i>	<i>120°C</i>	<i>-40°C</i>	<i>27°C</i>	<i>120°C</i>
<i>I (μA)</i>	79.69	87.63	95.78	129.5	133.5	137.4	46.38	56.34	66.87
<i>V_{TH} (mV)</i>	581	540	484	527	486	430	631	590	533
<i>g_{ds} (μA/V)</i>	24.2	24.8	25.6	34.7	34.6	34.5	15.6	17.0	18.6
<i>g_m (μA/V)</i>	633	560	492	784	680	580	47V	444	409
<i>g_m/g_{ds}</i>	26.2	22.6	19.2	22.6	19.6	16.8	30.4	26.1	22.0

MOS behaviour

Worst case variation

- About V_{TH}
 - V_{TH} changes in the range [430mV – 630mV] → A very large V_{TH} variation
 - These variations have to be considered in conjunction with the available supply voltage of 1.2V.
 - Even in the same worst case (i.e. for a given technology case – fast, nominal or slow) the variation is in the range of about 100mV
 - A robust design needs to take into account these spreads
 - Example 1: in a basic current-mirror the minimum V_{GS} depends on V_{TH}
 - → it can significantly change
 - Example 2: a cascode current mirror requires for the two cascode diodes at least $2 \cdot V_{GS} > 2 \cdot V_{TH} \geq 1.2V$ in the worst case
 - → A cascode current mirror cannot be used in a safe design



MOS behaviour

Worst case variation – (65nm node)

- The same analysis is carried out for other two transistor L sizes (W/L is constant)

- L=65nm; $V_{GS}=730\text{mV}$; $V_{DS}=1.2\text{V}$

	Nominal			Fast			Slow		
	-40°C	27°C	120°C	-40°C	27°C	120°C	-40°C	27°C	120°C
$V_{TH} [mV]$	584	547	496	510	475	425	646	606	552
$g_{ds} [\mu A/V]$	34.4	34.1	34.1	50.9	49.2	47.4	19.6	21.0	22.5
$g_m [\mu A/V]$	548	486	432	667	583	505	392	370	348
g_m/g_{ds}	15.9	14.3	12.7	13.1	11.8	10.6	20	17.6	15.5

- L=180nm; $V_{GS}=730\text{mV}$; $V_{DS}=1.2\text{V}$

	Nominal			Fast			Slow		
	-40°C	27°C	120°C	-40°C	27°C	120°C	-40°C	27°C	120°C
$V_{TH} [mV]$	565	522	462	523	480	421	605	562	503
$g_{ds} [\mu A/V]$	12.3	12.9	13.4	16.5	16.7	16.9	8.8	9.6	10.6
$g_m [\mu A/V]$	754	660	564	930	786	651	580	533	480
g_m/g_{ds}	61.3	51.2	42.1	56.4	47.1	38.5	65.9	55.5	45.3

- For L = 65nm → the intrinsic gain g_m/g_{ds} is lower
- For L = 180nm → V_{TH} is slightly lower

Why LV ?

Low-Voltage vs. Low-Power

- In **digital circuits**, reducing V_{DD} (in scaled-down CMOS tech.) reduces power:

$$P_{dig} \approx f \cdot C \cdot V_{DD}^2$$

- In **Thermal-noise-limited analog circuits**, it is typically the opposite

- Maximum output swing: $SW = [V_{DD} - 2 \cdot V_{sat}]$

- The analog power consumption $P_{an} = \beta \cdot I \cdot V_{DD}$ $I = P_{an} / (\beta \cdot V_{DD})$

- The noise is kT/C -limited & $\approx 1/I$: $N = \alpha / I$

$$DR = \frac{[V_{DD} - 2 \cdot V_{sat}]^2}{\alpha / I} = [V_{DD} - 2 \cdot V_{sat}]^2 \frac{P_{an}}{\alpha \cdot \beta \cdot V_{DD}}$$

- For a given DR

$$P_{an} = \frac{DR \cdot \alpha \cdot \beta \cdot V_{DD}}{[V_{DD} - 2 \cdot V_{sat}]^2} \propto \frac{DR}{V_{DD}}$$

- $\rightarrow P_{an}$ increases for V_{DD} decreasing

Why LV ?

Low-Voltage vs. Low-Power - V_{DD} reduction: Performance

- V_{DD} scaling affects analog circuit **performance**

$$FoM_P = \frac{4 \cdot k \cdot T \cdot DR^2 \cdot BW}{P}$$

$FoM_P \Leftrightarrow$ the power dissipation

$$FoM_I = \frac{4 \cdot k \cdot T \cdot DR^2 \cdot BW}{I}$$

$FoM_I \Leftrightarrow$ the current consumption ($F_I = F_P \cdot V_{DD}$)

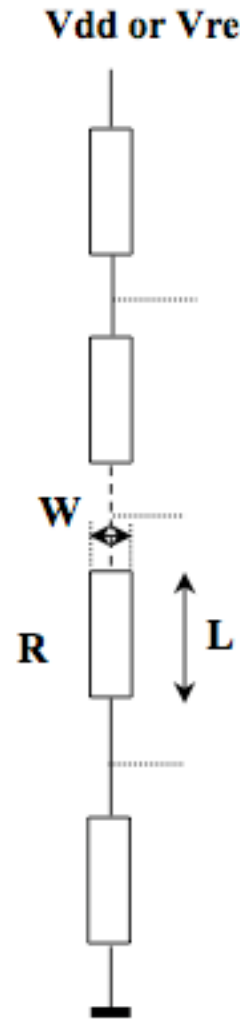
- $\rightarrow F_I$ does not consider P reduction due to the V_{DD} scaling
- $\rightarrow F_I$ considers only the P increase for maintaining the DR

Reference	Year	V_{DD} [V]	DR [dB]	BW [kHz]	P [mW]	$F_P [\times 10^6]$	$F_I [\times 10^6]$
Dessouky	2001	1	88	25	1.00	261	261
Peluso	1998	0.9	77	16	0.04	332	299
Libin	2004	1	88	20	0.14	1493	1493
Rabii	1997	1.8	99	25	2.50	1316	2369
Williams	1994	5	104	50	47.00	443	2214
Nys	1997	5	112	0.4	2.18	483	2415
Wang	2003	5	113	20	115.00	575	2875
YuQing	2003	5	114	20	34.00	2448	12240

Accuracy vs. Low-Power Trade-off

Example: Resistor string

- $I_{DD} = V_{DD}/R_{tot}$
- $R = r_{sq} \cdot L/W$ (1 element)
- High-accuracy requires to keep the spread of R low
 - $\rightarrow W \uparrow$
 - For the same L \rightarrow lower $R_{tot} \rightarrow I_{DD} \uparrow$
 - To reduce $I_{DD} \rightarrow L \uparrow \rightarrow I_{DD} \downarrow$
- Impedance level must be low to minimize noise and influence of the load on the top points, resp. Maximize immunity against perturbations $\rightarrow I_{DD} \uparrow$
- Adding buffers on the tap points solves the problem of loading but has an impact on precision because of the buffer offset
 - \rightarrow precision \downarrow



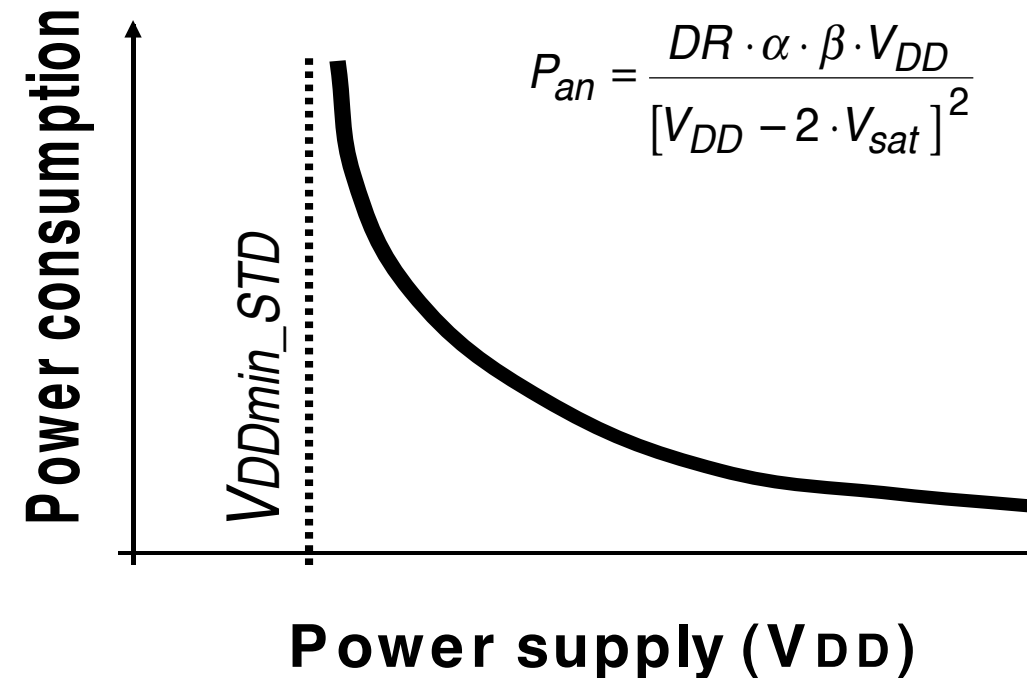
Why LV ?

V_{DD} Reduction: Functionality

- V_{DD} scaling affects analog circuit **functionality**
- For $V_{DD} < V_{DDmin_STD}$ no analog circuit operation

○ → Functionality problem:

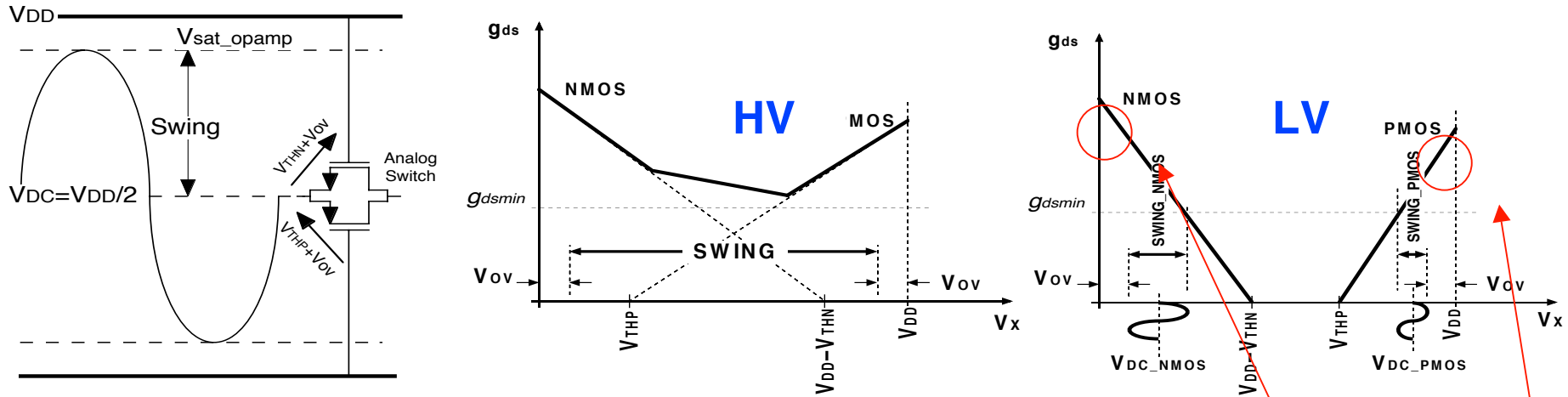
- Which V_{DDmin} is needed to operate ?



Why LV ?

{ $V_{DD} - V_{TH}$ } Reduction: Analog circuit functionality: What is V_{DDmin_STD} ??

- Analog circuit functionality depends on $\{V_{DD} - V_{TH}\}$
- Ex.: Analog switch operation (pass-gate)



- The most critical point @ $V_{DD} / 2$
- Pass-gates functionality is possible for:

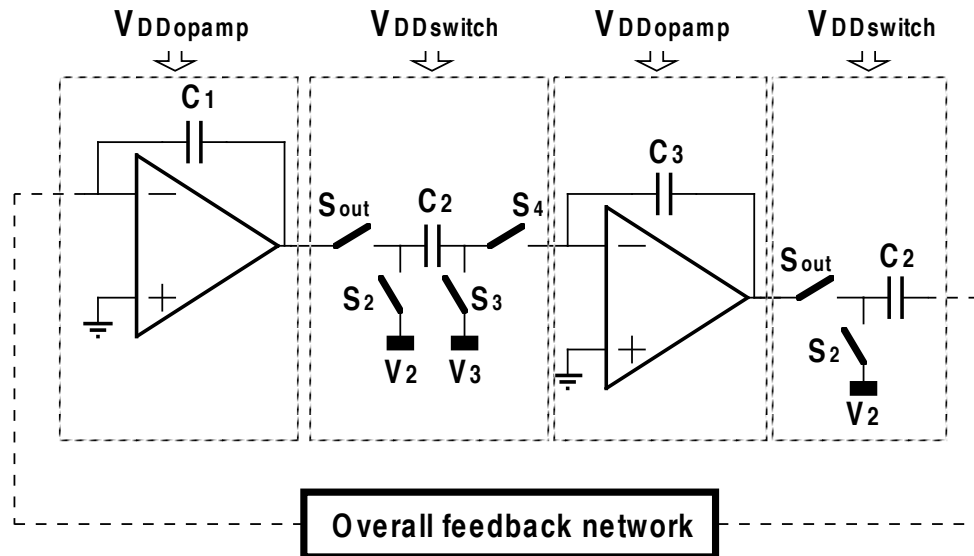
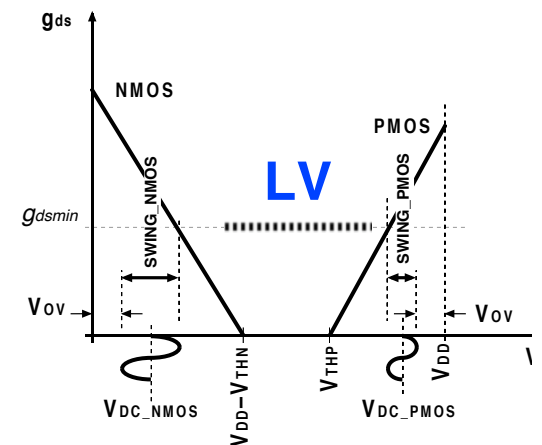
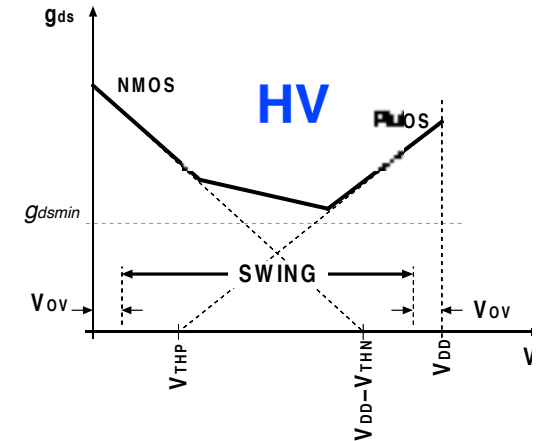
$$V_{DD} > V_{DDmin} = 2 \cdot V_{TH} + 2 \cdot V_{ov}$$

- The best condition is connecting a switch to GND or V_{DD}

Technology scaling: SCN functionality

Switches operation in an SC cell

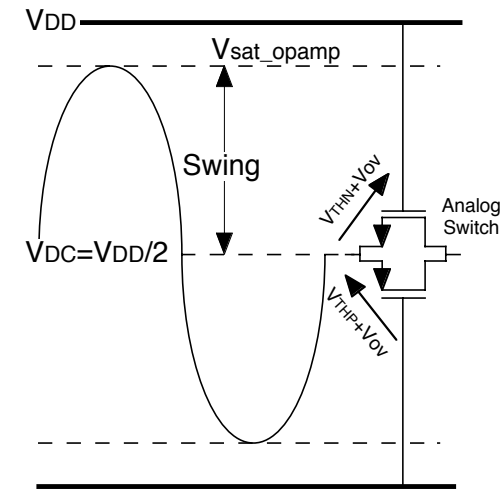
- A critical voltage region centered around $V_{DD}/2$ appears
 - No switch is conducting
 - → Rail-to-rail output swing cannot be achieved
- S_{out} sees the full swing and operates in critical region
- S_2 , S_3 and S_4 are connected to fixed voltage and can be properly designed and operated



Why LV ?

Technology scaling: Switches functionality

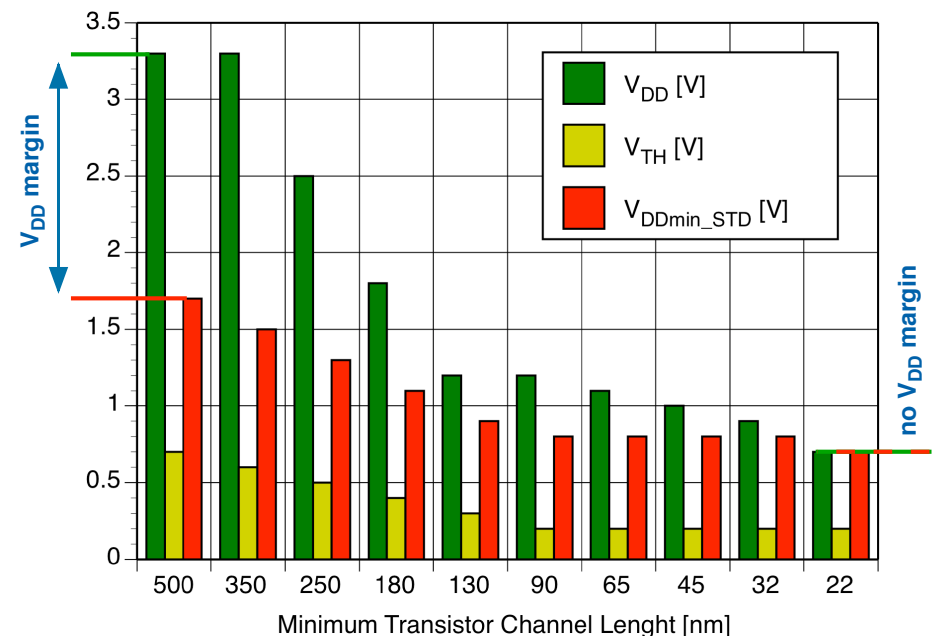
- The passgate is key block for ADC (S&H, etc...)
- The value of V_{DDmin_STD} is extracted from the passgate operation
- Problems at $V_{DD}/2$



$$V_{DDmin_STD} > V_{THN}(V_{DD}/2) + V_{THP}(V_{DD}/2) + 2 \cdot V_{ov}$$

$$V_{DDmin_STD} > 2 \cdot V_{TH} + 2 \cdot V_{ov}$$

- V_{DDmin_STD} is technology dependent
- For the forecast technologies, this condition is going to appear for technologies up to 70nm
 - → standard SC techniques appear to be possible also in a next future

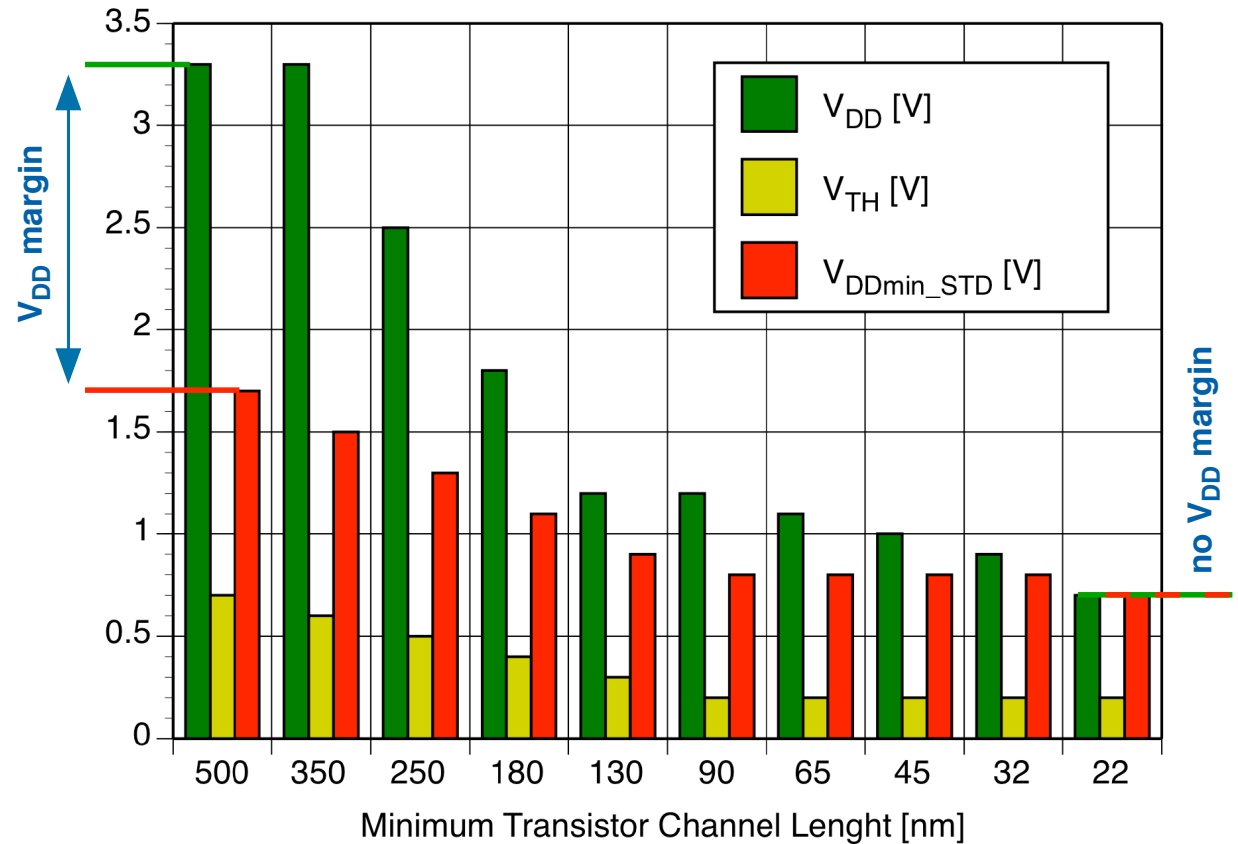


Why LV ?

$\{V_{DD} - V_{TH}\}$ Reduction: Analog switch functionality

$$V_{DDmin} = 2 \cdot V_{TH} + 2 \cdot V_{OV}$$

- Analog switch will be possible until 22nm technology (**functionality**)
- Their linearity is reduced due to the lower and lower overdrive (**performance**)
- The reduced distance $\{V_{DD} - V_{TH}\}$ has impact on analog blocks **functionality**
- Different analog blocks have different limitations



A 1-V 140- μ W 88-dB Audio Sigma-Delta Modulator in 90-nm CMOS

Libin Yao, *Student Member, IEEE*, Michiel S. J. Steyaert, *Fellow, IEEE*, and Willy Sansen, *Fellow, IEEE*

Abstract—A single-loop third-order switched-capacitor Σ - Δ modulator in 90-nm standard digital CMOS technology is presented. The design is intended to minimize the power consumption in a low-voltage environment. A load-compensated OTA with rail-to-rail output swing and gain enhancement is chosen in this design, which provides higher power efficiency than the two-stage OTA. To lower the power consumption further, class-AB operation is also adapted in the OTA design. Due to the relatively low threshold voltage of the advanced technology, no clock bootstrapping circuits are needed to drive the switches and the power consumption of the digital circuits is reduced. All the capacitors are implemented using multilayer metal-wall structure, which can provide high-density capacitance. The modulator achieves 88-dB dynamic range in 20-kHz signal bandwidth with an oversampling ratio of 100. The power consumption is 140 μ W under 1-V supply voltage and the chip core size is 0.18 mm².

accuracy, providing an effective way to implement high-resolution ADCs without stringent matching requirements or calibration in low-voltage environment. By means of oversampling and noise shaping, the Σ - Δ ADC transfers most of the signal processing tasks to the digital domain where the power consumption can be drastically reduced by the technology scaling down and supply voltage decreasing. Meanwhile, the use of an intrinsically linear single-bit quantizer exempts the stringent matching requirement, which is power-hungry. For high-resolution ADCs, the Σ - Δ ADC is more power-effective and robust compared to other architectures.

While moving into ultra-deep-submicron CMOS technologies, for low-voltage low-power designs, certain advantages can be gained. On the other hand, some disadvantages are also

$$V_{DD} = 1V$$

$$V_{TH}=0.3V$$

$$V_{DD} < 2 \cdot (V_{TH} + V_{ov})$$

is not valid !!!!

This is not a LV ADC

Why LV ?

Application requirements

- Portable systems require the use of few battery cells (when possible a single one, i.e. $V_{DD}=1.2V$ with $V_{DD}=0.9V$ worst case)
- Use a technology, that would allow high V_{DD} (and present high V_{TH}) but operate with low V_{DD} (ex.: pacemaker)

$$V_{DD} < V_{DDmin_STD} = V_{THN}(V_{DD}/2) + V_{THP}(V_{DD}/2) + 2 \cdot V_{ov}$$

$$V_{DD} < 2 \cdot (V_{TH} + V_{ov})$$

Functionality problem

- Switch: to be turned on over the entire voltage swing may not be possible

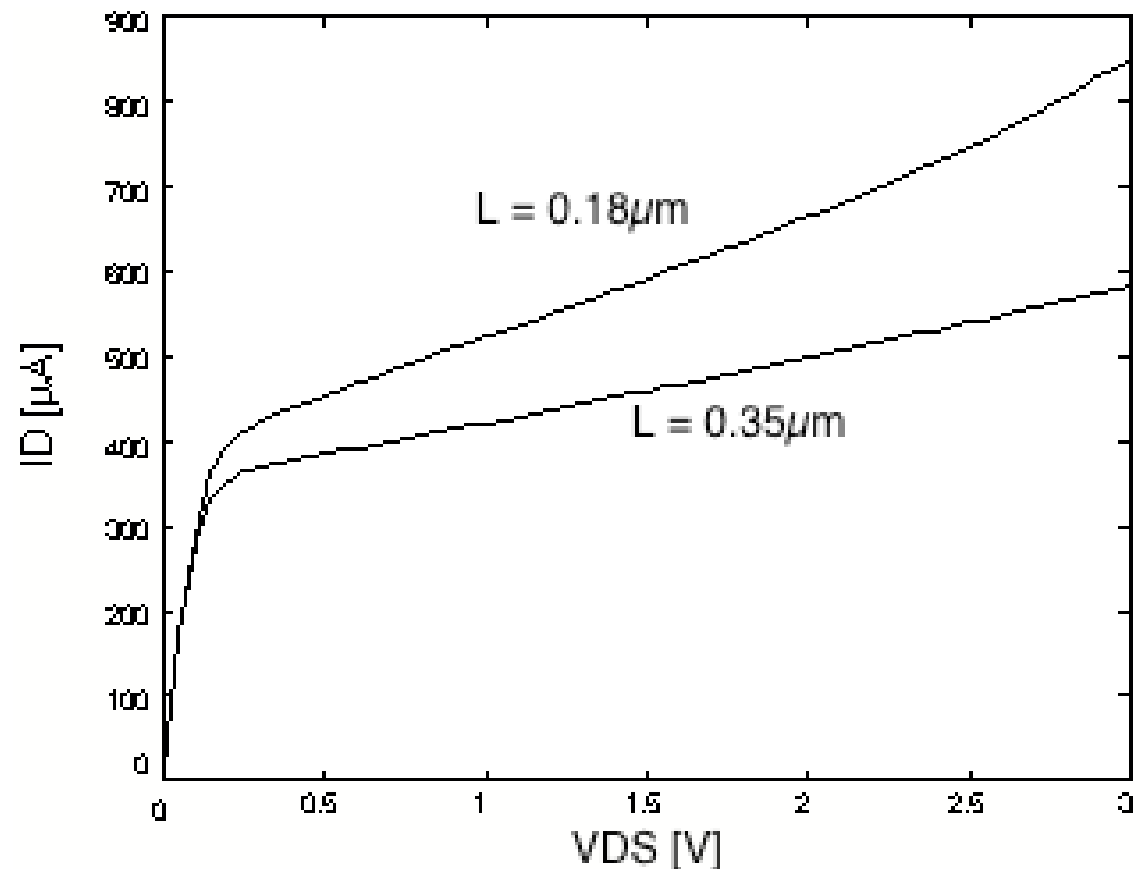
Performance problem

- Opamp design → Limited number of devices between the rails therefore many circuit topologies can not be used (e.g. cascode) => novel solutions are needed
- Dynamic Range → The same DR at lower V_{DD} requires larger power

Why LV ?

Performance problem

- Opamp design
 - Scaled down technologies offer reduced output impedance (i.e. reduce voltage gain-per-stage)
- Switches
 - On resistance variation over swing results is THD
- Dynamic Range
 - The same DR at lower V_{DD}
 - with lower signal swing
 - requires larger power



LV Analog Design in scaled CMOS technology

Outline

- Introduction
 - Basic CMOS operation
 - CMOS technology scaling trends
 - What is LV
 - LV Analog design ←←←
 - LV at transistor level ←←←
 - LV at circuit level
 - Opamp design
 - Basic bandgap design
 - LV at system level
 - Active-RC filter design
 - Gm-C filter design
 - SC circuit design

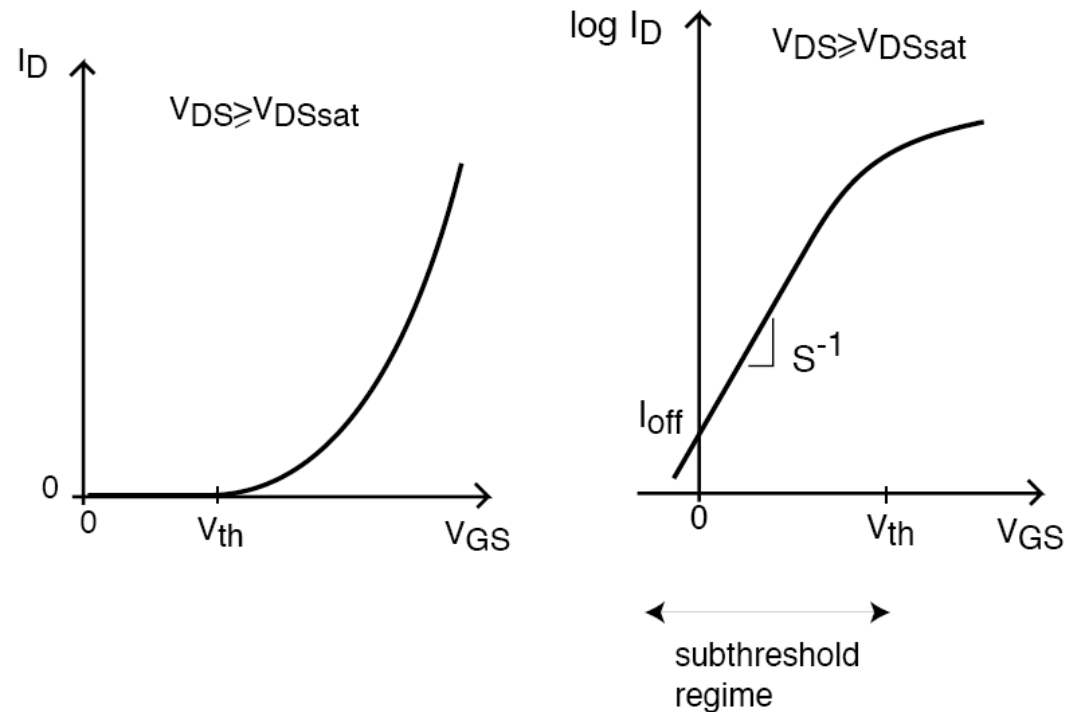
LV MOS Transistors

Weak Inversion

- V_{DDmin} depends on V_{TH} and on V_{OV} ($= V_{GS} - V_{TH}$)
 - Minimizing V_{TH} by the process (technologies with low- V_{TH} have a higher production cost) or by using special circuit techniques
 - Minimizing V_{OV} , the MOS operates in the weak inversion.

- The MOS current in the weak inversion is:

$$I_D = I_S \cdot e^{\frac{V_G - V_{TH}}{n \cdot V_T}} \cdot \left(e^{\frac{-V_S}{n \cdot V_T}} - e^{\frac{-V_D}{n \cdot V_T}} \right)$$



LV MOS Transistors

Weak Inversion

- Low V_{TH} by biasing the MOS with $V_{BS} < 0$

$$V_{TH} = V_{TH0} + \gamma \left(\sqrt{|2 \cdot \phi_F - V_{BS}|} - \sqrt{|2 \cdot \phi_F|} \right)$$

- V_{TH0} is zero bias threshold voltage, γ the bulk effect factor and ϕ_F the Fermi potential.
- Typically $V_{BS} > 0$, $\rightarrow V_{TH} > V_{TH0}$
- Using $V_{BS} < 0$ V, $\rightarrow V_{TH} < V_{TH0}$
- Forward biasing the bulk-source diode turns on the parasitic BJT
- $|V_{BS}|$ is limited by how much current this BJT can tolerate
 - The parasitic BJT introduces additional noise in the MOS and might lead to latch-up

LV MOS Transistors

Weak Inversion Features

- Exponential law
 - translinear circuits & log-domain filters 😊
 - Max I_{on}/I_{off} for a given voltage swing 😊
 - non-linearity (ex. IM in RF front-ends) 😞
- $\min V_{OV}$
 - $\min V_{DSsat}$ 😊
- \min gate capacitance 😊
 - 😊 $\min V_{DSsat}$

LV MOS Transistors

Weak Inversion Features

- Max ratio g_m/I_D
 - Max voltage gain 😊
 - Max bandwidth for a given kT/C & I_D 😊
 - *min* input noise density for a given I_D 😊
 - *min* input offset 😊
 - Max output noise density for a given I_D 😞
 - Max drain current mismatch 😞

- dominated by the V_{TH} mismatch

$$\frac{\Delta I_D}{I_D} \cong \frac{\Delta V_{TH0}}{n \cdot V_T}$$

- $g_m(I_D)$ linear 😊/😞

- Low speed 😞 **(but increased by ScaTech)**

$$f_T \cong \frac{\mu \cdot V_T}{2 \cdot \pi \cdot L^2}$$

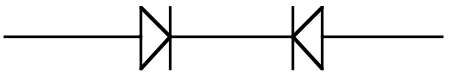
- Good for situation with low offset sensitivity
 - BP

LV MOS Transistors

Weak Inversion Features

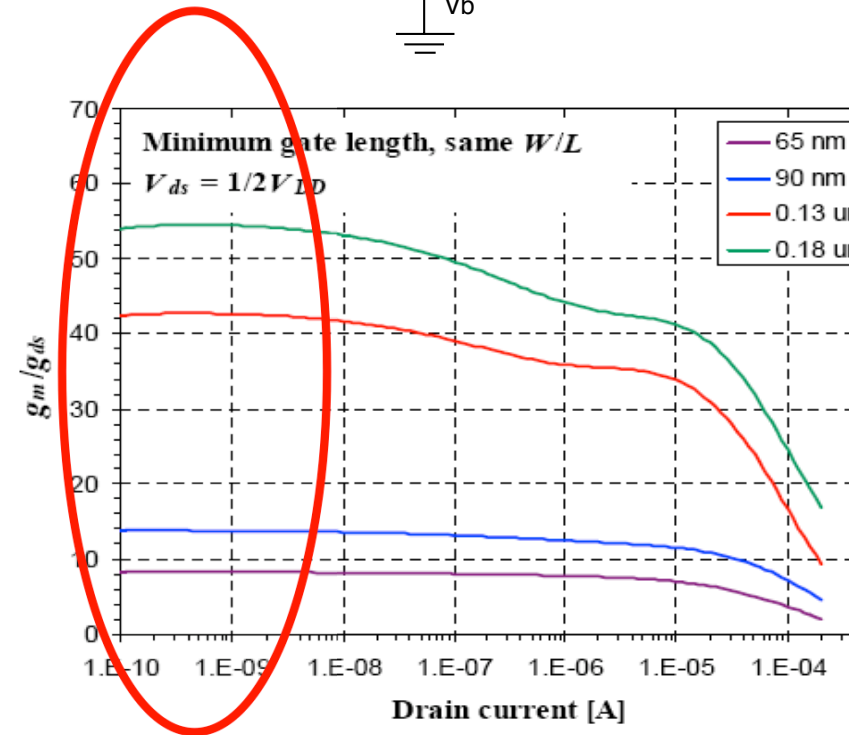
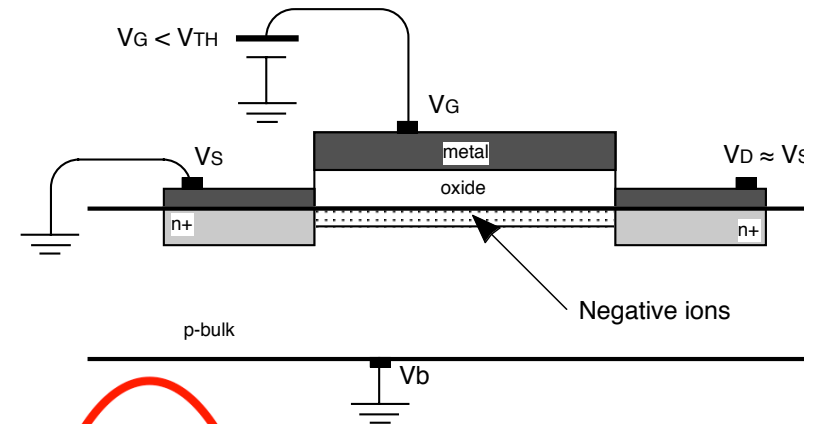
$$V_{GS} \approx V_{TH}$$

- The structure is equivalent to



$$I_D = I_{D0} \cdot e^{q \cdot V_{GS} / n \cdot k \cdot T} \cdot e^{-q \cdot V_{BS} / n \cdot k \cdot T} \cdot \left[1 - e^{-q \cdot V_{BS} / k \cdot T} \right]$$

- ☺ Minimum V_{OV}
- ☺ Small gate capacitance
- ☺ Large g_m/I_D ratio
- ☺ Large voltage gain
 - ☹ Large drain current mismatch
 - ➔ (input offset)
 - ☹ Large output noise current for a given I_D
 - ☹ Low speed, $f_T \cong \frac{\mu \cdot V_T}{2 \cdot \pi \cdot L^2}$



LV MOS Transistors

Weak Inversion Features – (45nm node)

- Diode connected transistor

- $I_D = 60\mu\text{A}$
- $L = 200\text{nm}$

W [μm]	V_{TH} [mV]	V_{GS} [mV]	g_m [mA/V]	g_{ds} [$\mu\text{A/V}$]	r_{ds} [k Ω]	A_o
5	506	556	0,75	27,1	36,9	27,68
10	506	509	0,896	32,5	30,8	27,57
30	506	446	1,12	40,8	24,5	27,45
50	506	421	1,21	44,2	22,6	27,38
70	506	406	1,27	46,2	21,6	27,49
90	506	395	1,31	47,6	21,0	27,52
120	506	382	1,35	49	20,4	27,55
150	506	373	1,39	50	20,0	27,80

- For a given current

- Larger is V_{GS} (closer to V_{TH}) $\leftarrow \rightarrow$ Smaller is W

- Lower is g_m
- Larger is g_{ds}
 - The gain is constant

- \rightarrow For input stage a large device with low V_{GS} is OK \rightarrow Large g_m
- \rightarrow For output stage a small device with large V_{GS} is OK \rightarrow Low g_{ds}

LV MOS Transistors

Weak Inversion Features *

TABLE II

THRESHOLD VOLTAGE MISMATCH STANDARD DEVIATIONS IN STRONG INVERSION ($\sigma_{\Delta V_t}$) AND SUBTHRESHOLD V_{gs} MISMATCH ($\sigma_{\Delta V_{gs}}$ at $I_d = 10 \text{ pA}/(W/L)$) AND THE CORRELATIONS BETWEEN THE MISMATCH OBSERVATIONS FOR A RANGE OF TRANSISTOR DIMENSIONS

drawn_W (μm)	drawn_L (μm)	$\sigma_{\Delta V_t}$ (strong inversion) (mV)	$\sigma_{\Delta V_{gs}}@[I_d=10\text{pA}/(W/L)]$ (mV)	Correlation factor R^2
10	4	0.7	2.1	0.07
2	10	1.1	3.0	0.05
10	1	1.7	4.5	0.03
0.4	10	2.5	5.1	0.01
2	1	5.4	10	
0.32	4	4.0	6.6	
2	0.2	12	27	
0.4	1	8.9	12	
0.4	0.24	23	38	
0.32	0.2	27	44	

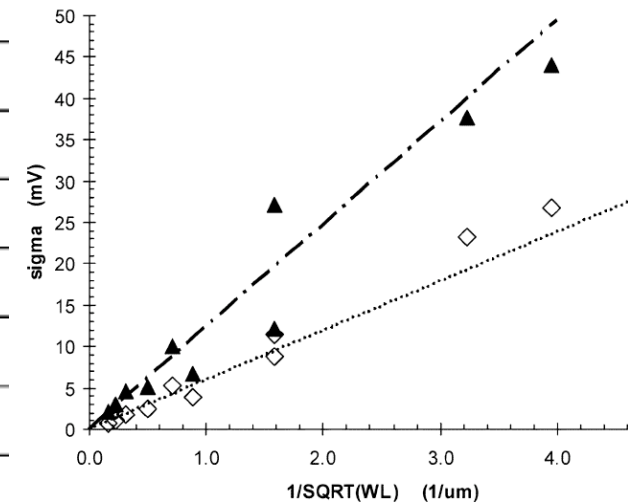


Fig. 12. Mismatch area scaling graph. Diamonds: strong inversion region V_t mismatch. Triangles: subthreshold V_{gs} mismatch (at 10 pA). The 6 mV/um and 12.5 mV/um lines are estimates for the corresponding scaling factors for the strong and weak inversion mismatch standard deviation respectively.



LV Transistor Operation

Saturation region

- Saturation condition requires

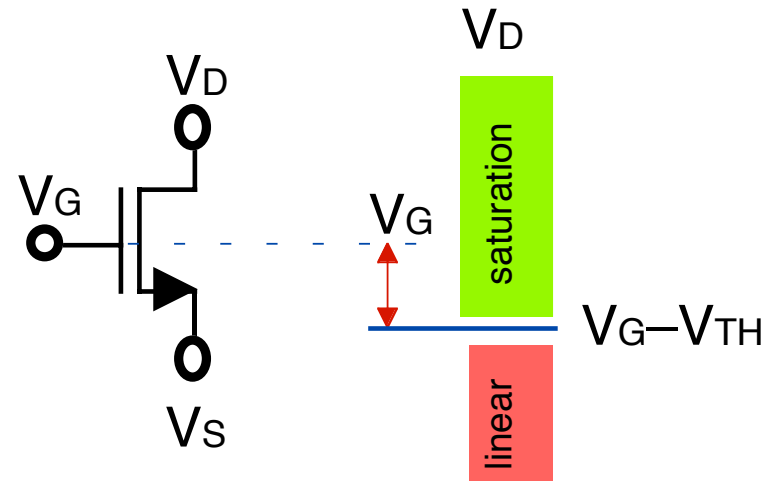
$$V_{DS} > (V_{GS} - V_{TH})$$

- LV operation requires low V_{DS}

$$I_D = \frac{1}{2} \cdot \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})^2$$

- A given I level @ a lower V_{DS}

- → lower $(V_{GS} - V_{TH})$
 - more important ΔV_{TH}
- → larger W/L
 - → larger cap



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 - LV at circuit level ←←←
 - Current Mirrors ←←←
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Basic Current Mirror Function

- A CM is required
 - as bias stage
 - to mirror the reference current accurately
 - as a load stage
 - to have very high output resistance
 - These two parameters trade-off each other in scaled technology
- Two important factors need to be considered:
 - gate current
 - load impedance

Simple Current Mirror

Basic Operation

- M_1 & M_2 operate in saturation

$$I_{out} = I_{ref} \cdot \left(\frac{W}{L}\right)_2 \cdot \frac{(1 + \lambda \cdot V_{DS2})}{\left(\frac{W}{L}\right)_1 \cdot (1 + \lambda \cdot V_{DS1})} = I_{ref} \cdot G_{CM}$$

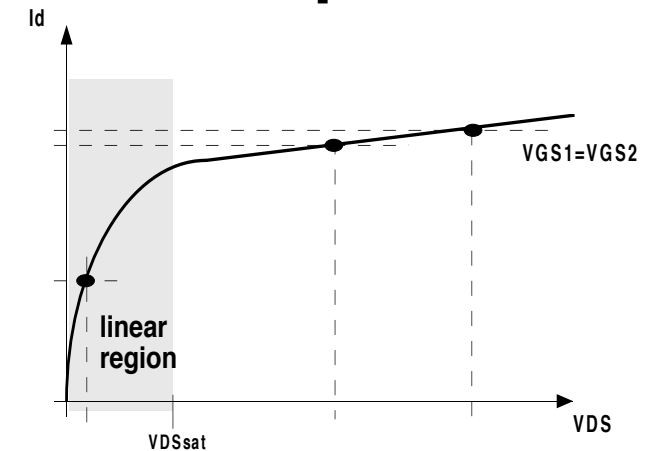
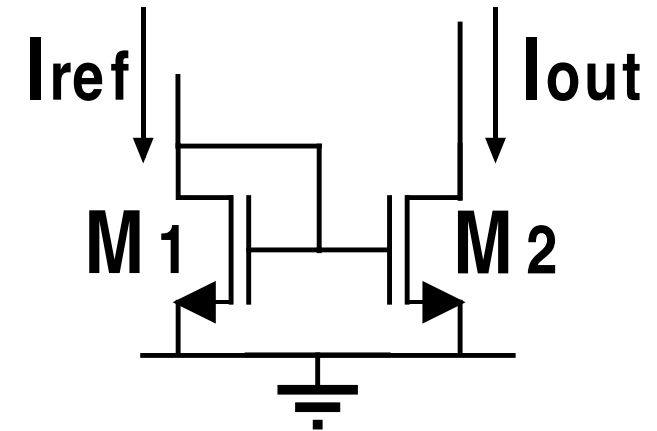
- Output impedance ($r_{out} // C_{out}$)

$$r_{out} = r_{ds2} = \frac{1}{\lambda I_2}$$

- Long L increases r_{out}
 - Use devices with same L (to avoid ΔV_{TH})

$$C_{out} = C_{DB} + C_{DG}$$

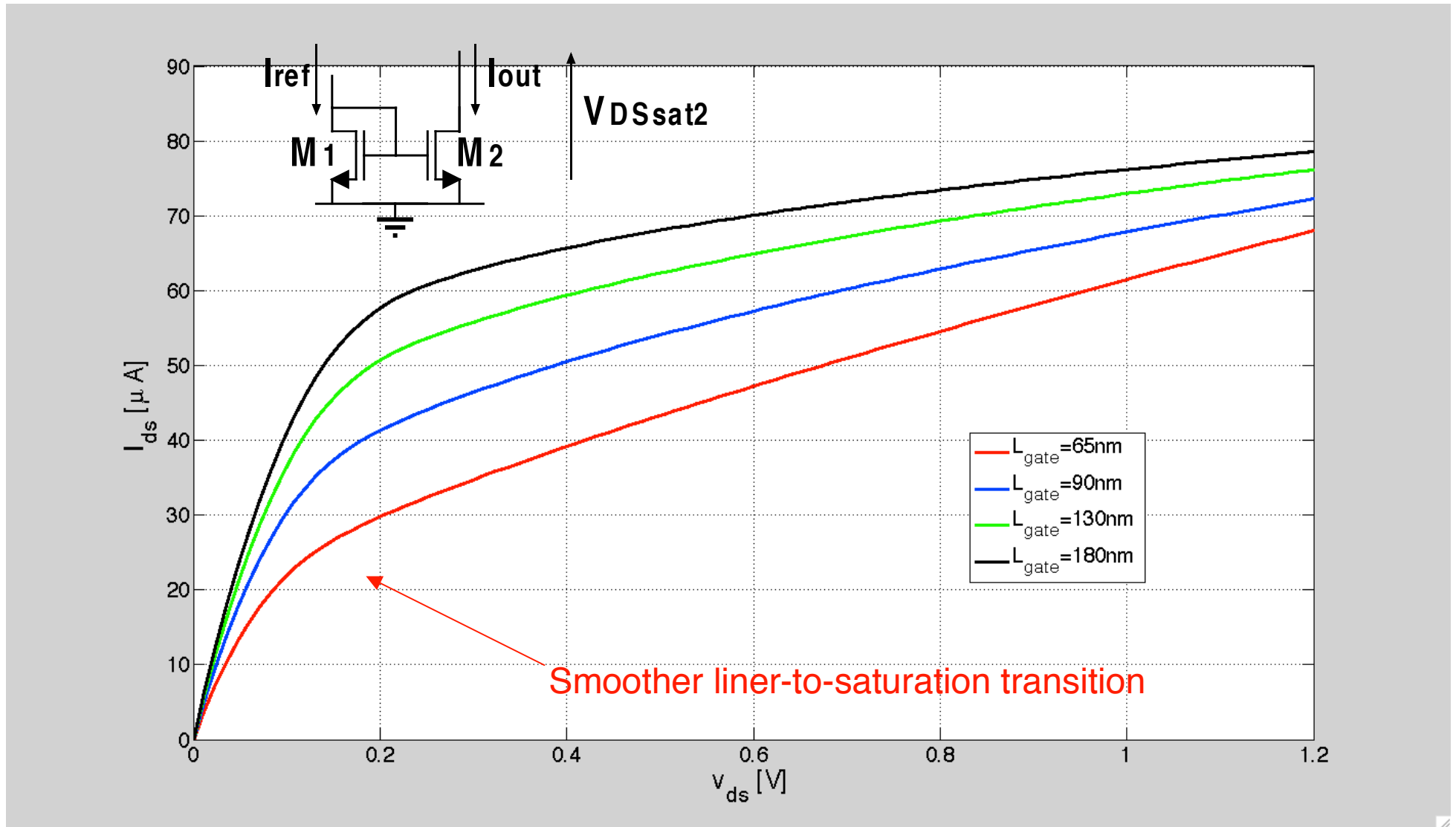
- Proportional to $W \cdot L$



Trade off: Large $r_{out} \Leftrightarrow$ large L \Leftrightarrow large C_{out}

Simple Current Mirror

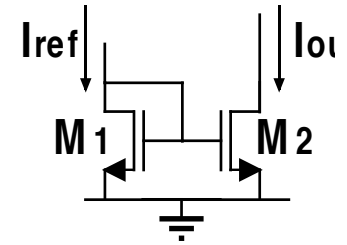
Basic Operation – L dependence (65nm technology)



Simple Current Mirror

G_{CM} variations - Threshold offset deviation

$$I_{out_act} = I_{out_ideal} \cdot \left(1 + 2 \cdot \frac{\Delta V_{TH}}{V_{GS} - V_{TH}} \right)$$



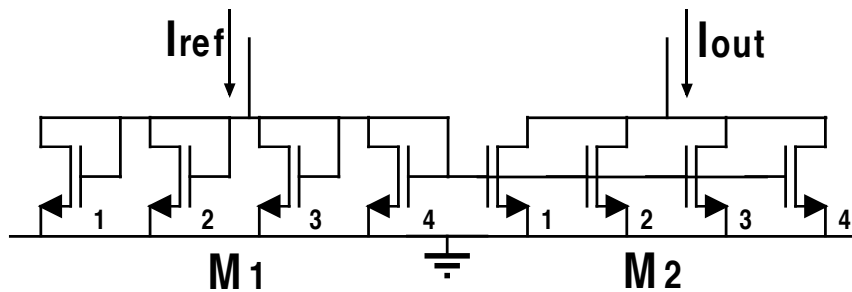
- Use large $(V_{GS} - V_{TH})=V_{SAT}$ to improve matching
- Difficult **At LV !!!**
- → Trade off with output swing
- Threshold offset reasons
 - Design issue
 - Devices with different L and/or W exhibit significant ΔV_{TH}
 - Use same L&W in current mirrors
 - → For large current gain, use multiple units of the same W/L device
 - Layout issue
 - ΔV_{TH} of MOS transistors in close proximity can be a few mV.
 - ΔV_{TH} of transistors hundred of μm apart can be tenths mV
 - → Design current mirror device in close proximity
 - STI effects, if not taken into account

Simple Current Mirror

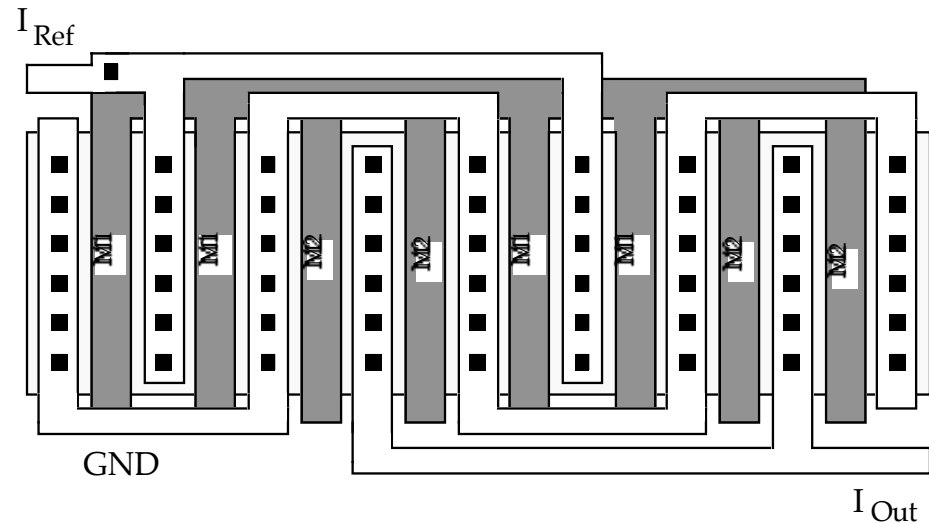
G_{CM} variations – Geometrical mismatch

- Imperfect geometrical matching and current mobility variation
- Example:

Circuit scheme



Layout solution

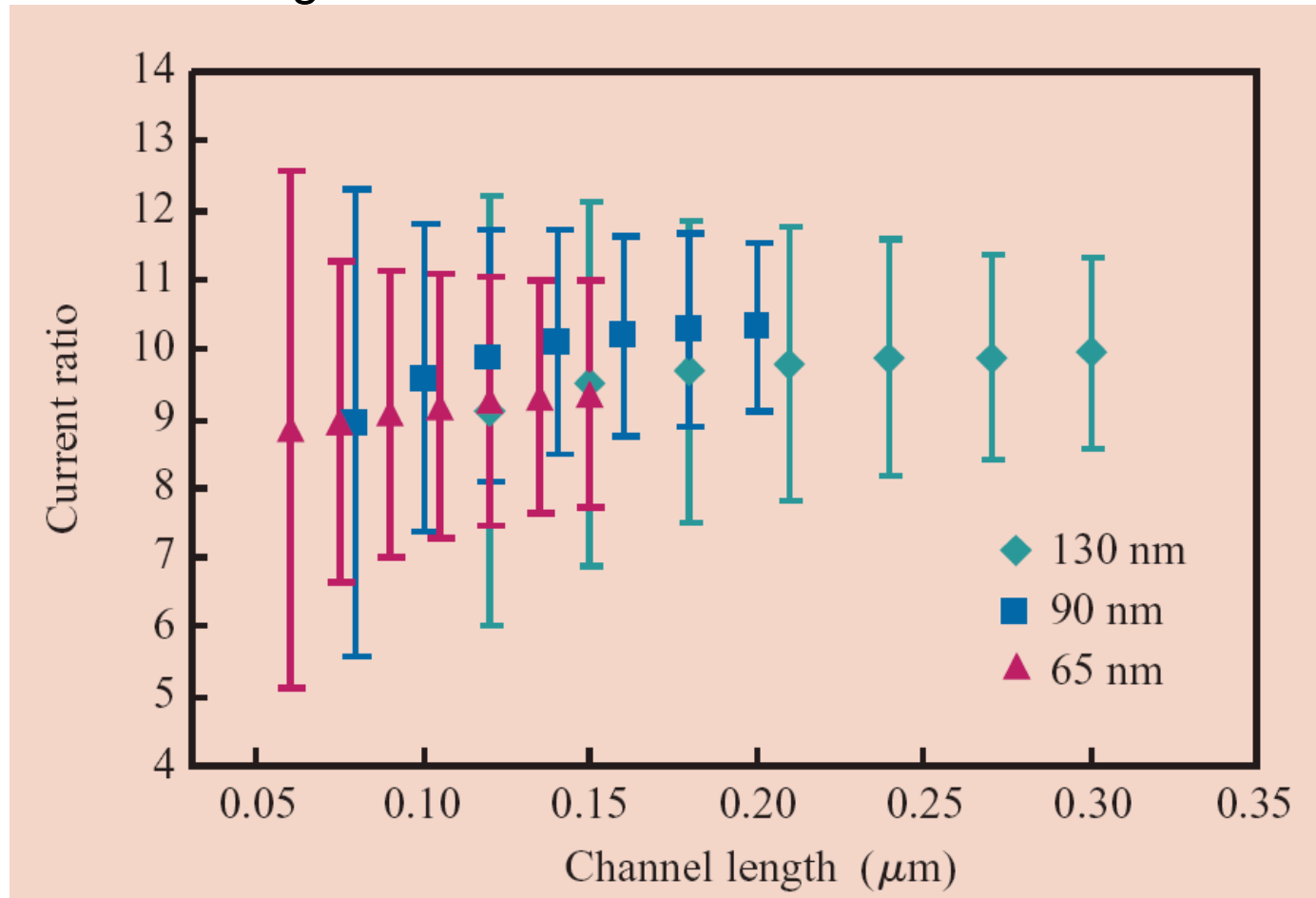


- For a better layout and a better matching use an integer ratio $(W/L)_1/(W/L)_2$
- Border effects & STI mismatch border devices w.r.t. internal ones
 - Add dummy devices at the array edges

Simple Current Mirror

G_{CM} variations – Geometrical mismatch

- Simulated current-ratio variability of 10:1 current mirror for 130-nm, 90-nm, and 65-nm technologies



Cascode Current Mirror

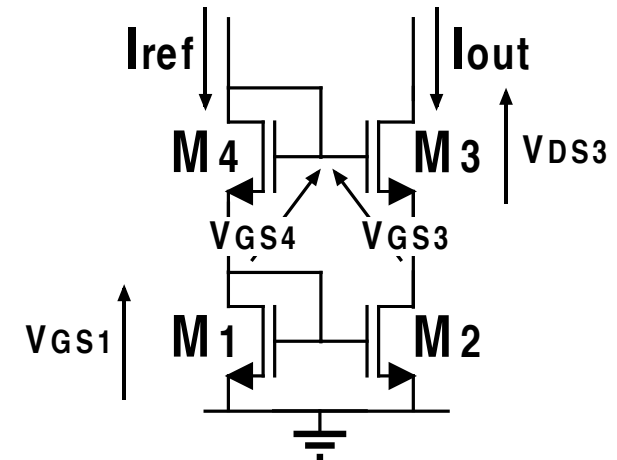
Output swing

$$V_{GS3} = V_{GS4}$$

- The output swing is limited to:

$$V_{out,min} = V_{GS1} + V_{GS4} - V_{GS3} + V_{DSsat,3}$$

$$V_{out,min} = V_{GS2} + V_{DSsat,3}$$



$$V_{out,min} > V_{TH} + 2 \cdot V_{DSsat}$$

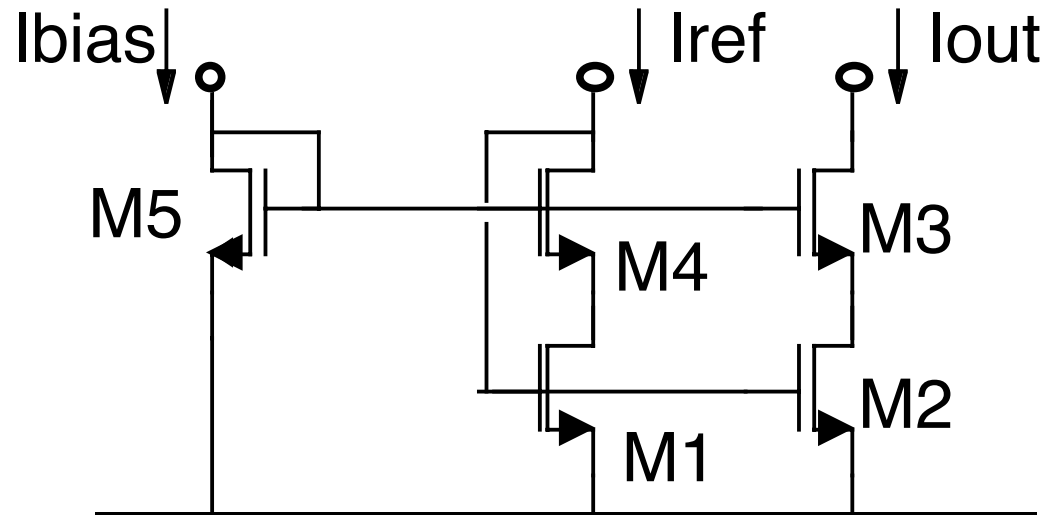
- **At LV** the critical point could be the sensing branch !!!

$$V_{sens,min} > 2 \cdot V_{TH} + 2 \cdot V_{DSsat}$$

- Not possible in ScalTech

High-compliance current mirrors

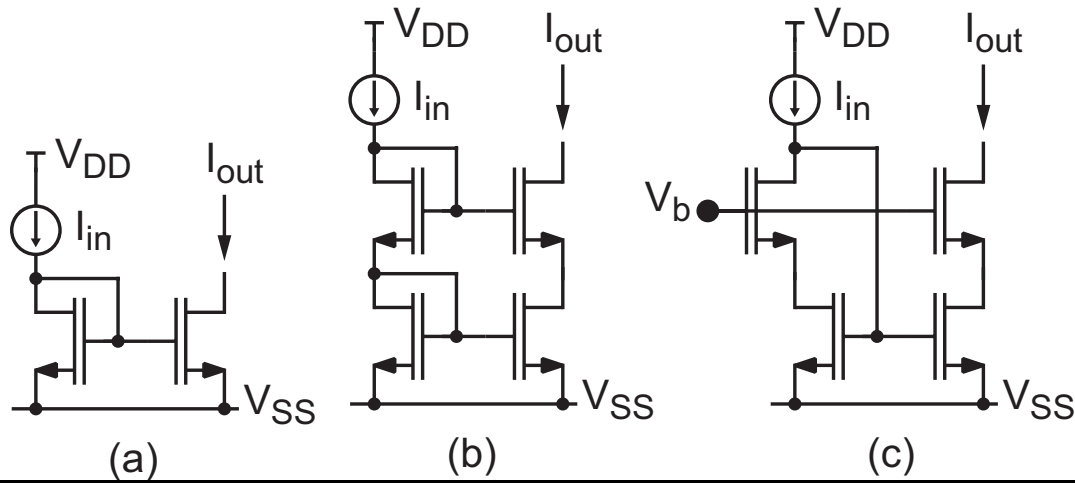
Design issues



$$M1=M2; \quad M3=M4 \quad \Rightarrow \quad I_{out}=I_{Ref}$$

- M_1 operates as M_2
 - Better GCM
- $V_{DSsat4} > V_{TH}$ to properly work
- It is also possible to enter at the drain of $M1$

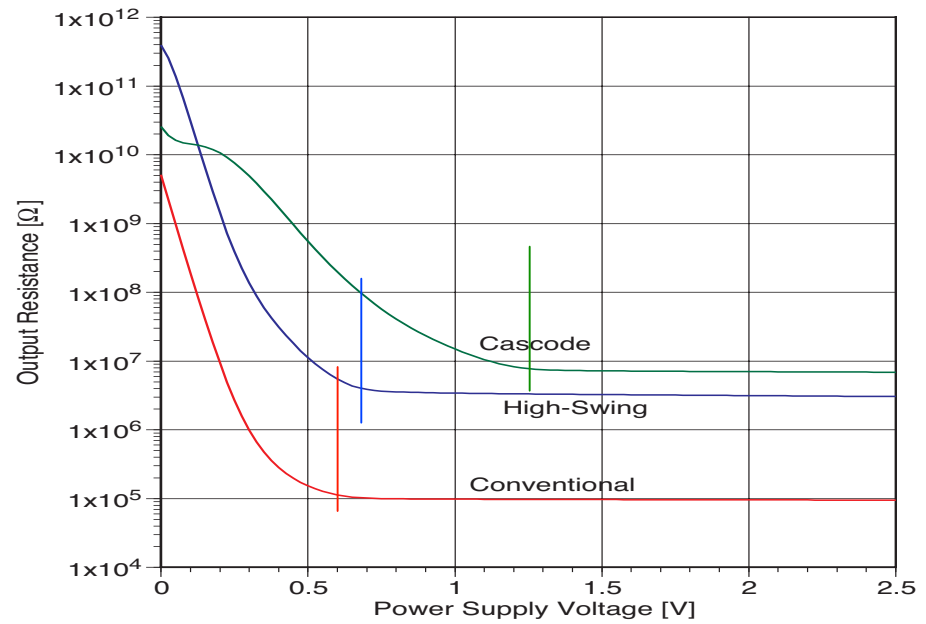
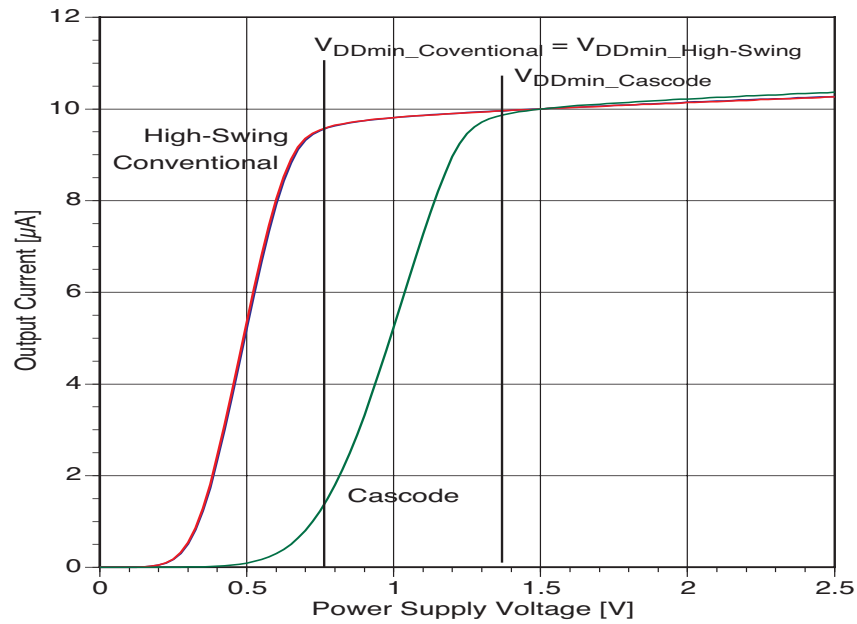
LV Current Mirrors



(a) $V_{DDmin} = V_{TH} + 2 \cdot V_{OV}$

(b) $V_{DDmin} = 2 \cdot V_{TH} + 3 \cdot V_{OV}$

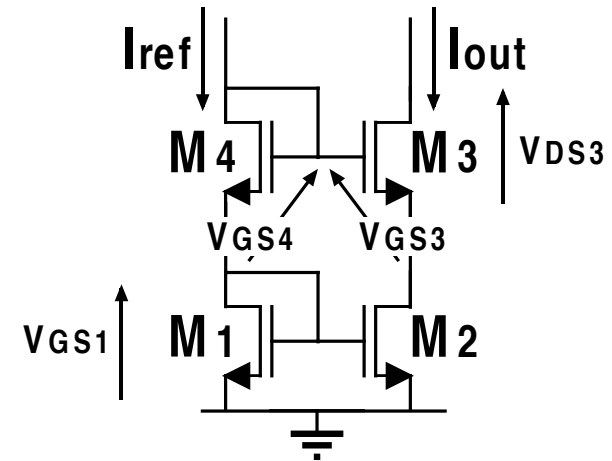
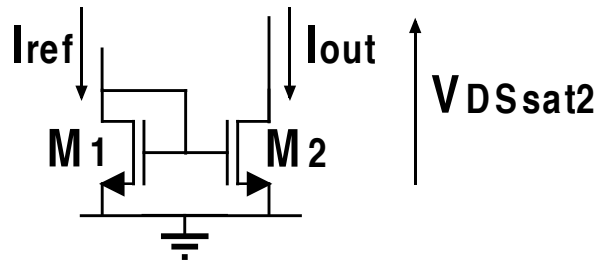
(c) $V_{DDmin} = V_{TH} + 2 \cdot V_{OV}$



CMOS current mirrors

Comparison example

- Same current level $I \rightarrow$ same output impedance



$$r_{o_s} = \frac{L_s}{\lambda' \cdot I}$$

$$r_{o_c} = (r_{o3} \cdot g_{m3}) \cdot r_{o2} = \left(2 \cdot \frac{V_A}{V_{ov}} \right) \cdot \frac{L_{\min}}{\lambda' \cdot I}$$

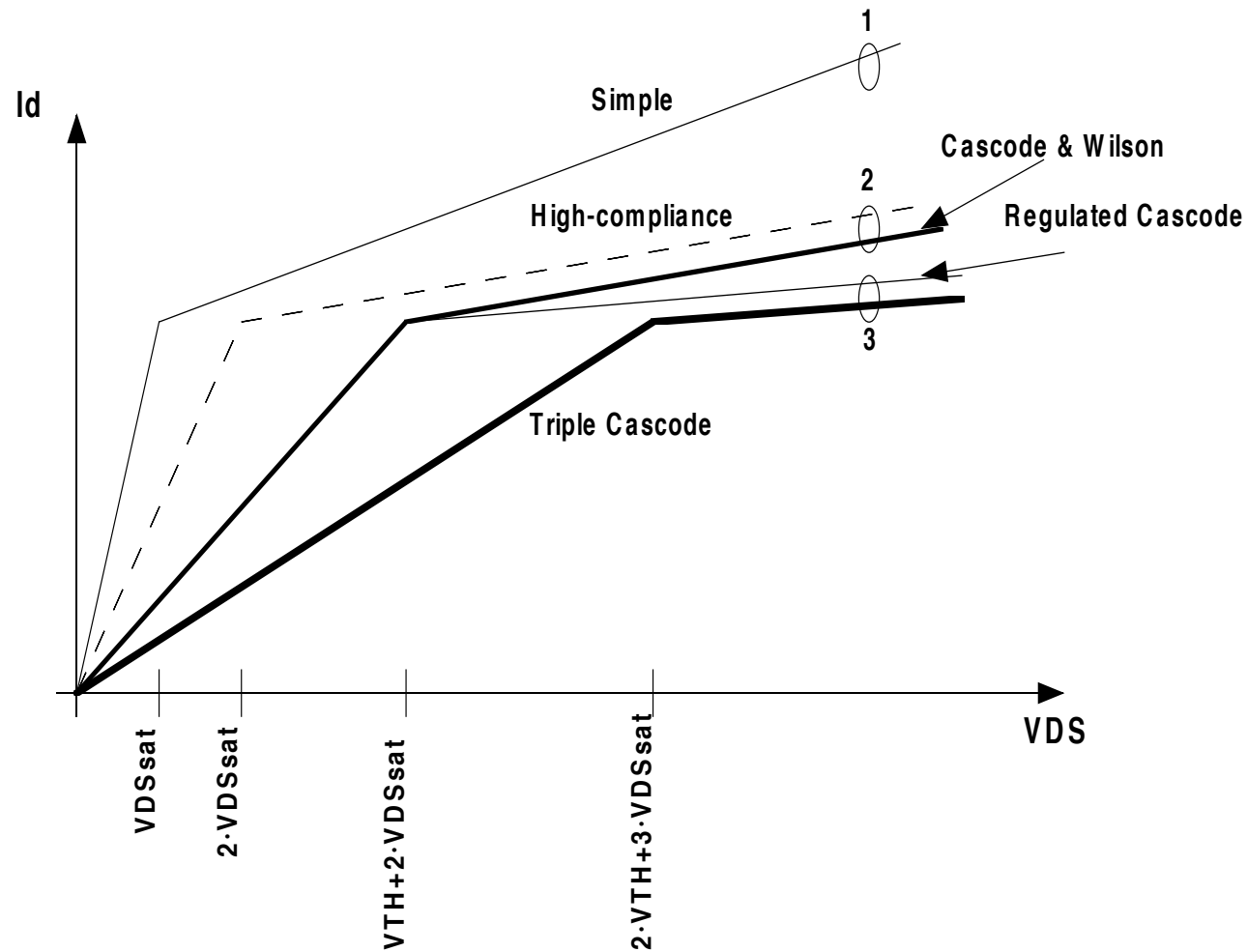
$$r_{o_s} = r_{o_c}$$

\Rightarrow

$$L_s = L_{\min} \cdot \left(2 \cdot \frac{V_A}{V_{ov}} \right)$$

Current mirrors

Output swing comparison



- The slope (1, 2, or 3) indicates the output impedance (r_{out})

Basic Current Mirror

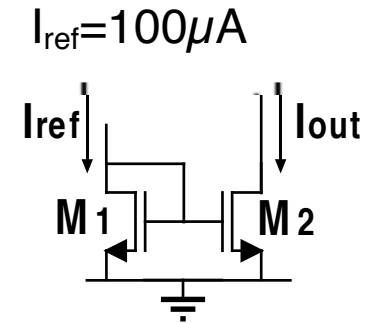
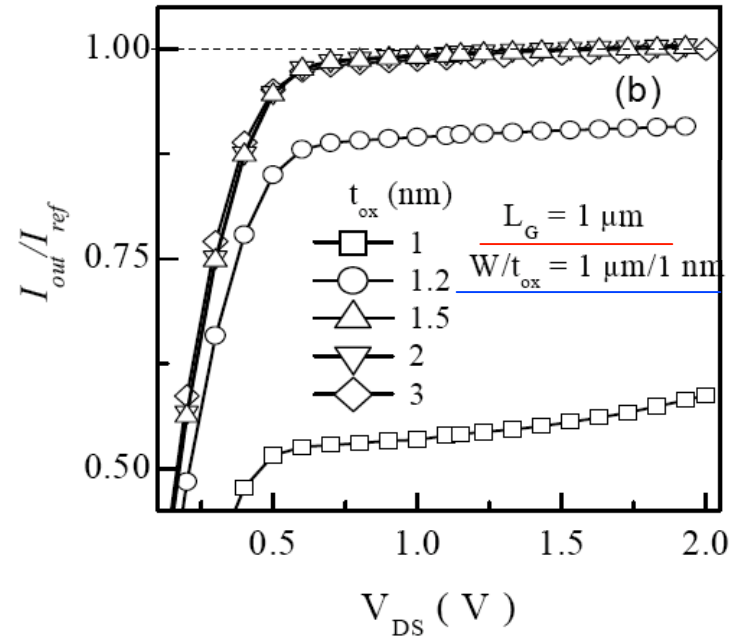
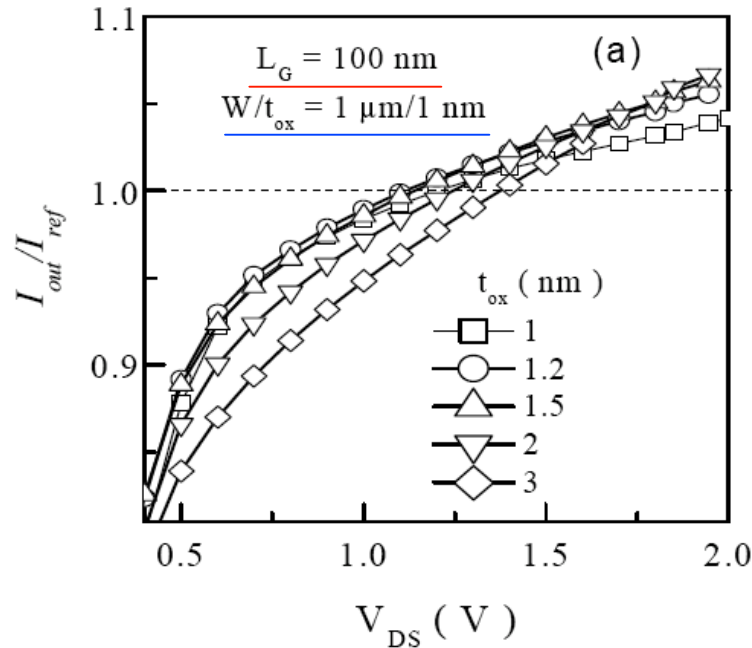
- Two important factors need to be considered:
 - gate current
 - load impedance

- A CM is required
 - as bias stage
 - to mirror the reference current accurately
 - as a load stage
 - to have very high output resistance

- These two parameters trade-off each other in scaled technology

Basic Current Mirror*

$G_{CM} (I_{out}/I_{ref})$ vs. V_{DS}

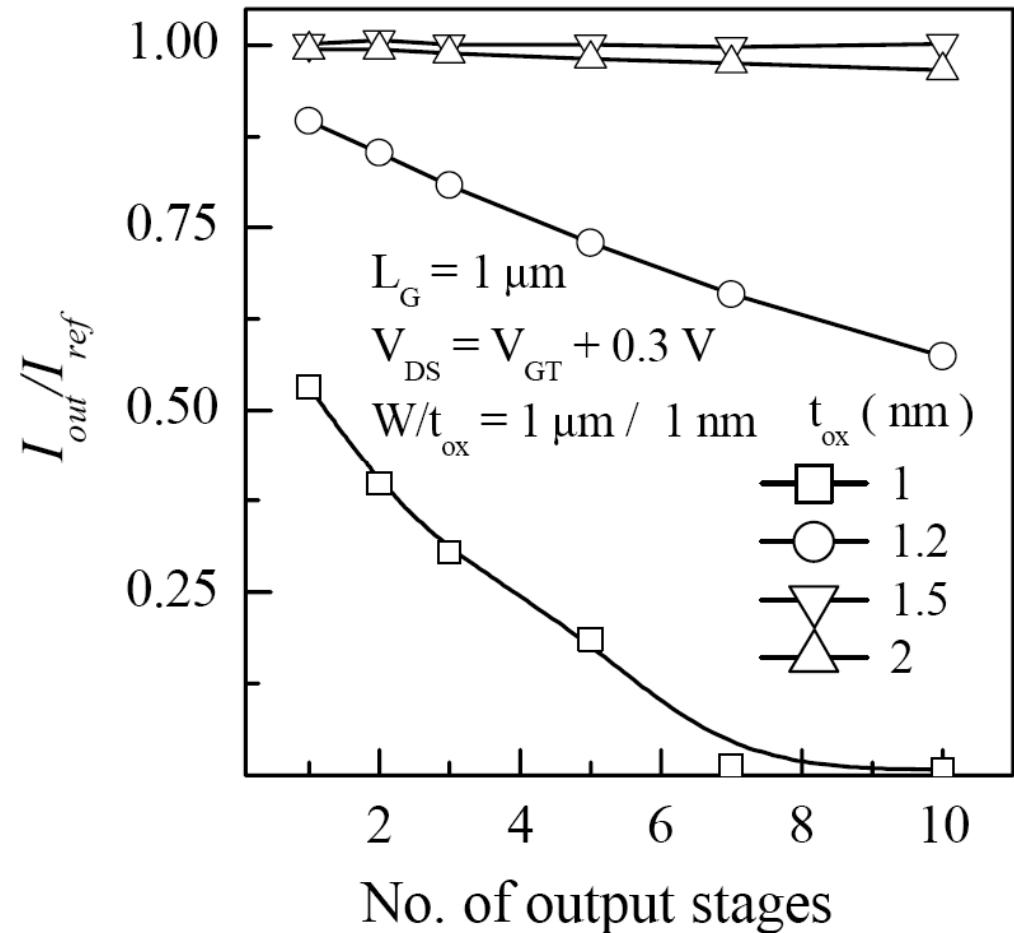


- For $L_G=100$ nm,
 - G_{CM} degrades over the range for all the oxide thicknesses due to:
 - short channel effects (such as DIBL)
 - channel length modulation.
 - the output resistance degrades due to short channel effects

Basic Current Mirror

G_{CM} (I_{out}/I_{ref}) vs. Gate current

- Output resistance is improved with thin oxides
- Long L for r_o increase
- Large W for small V_{ov} (al LV)
 - → large $W \times L$
 - → large I_G
 - → G_{CM} error
 - Similar to base current in BJTs
 - Novel circuit design techniques to reduce the gate leakage effects are needed

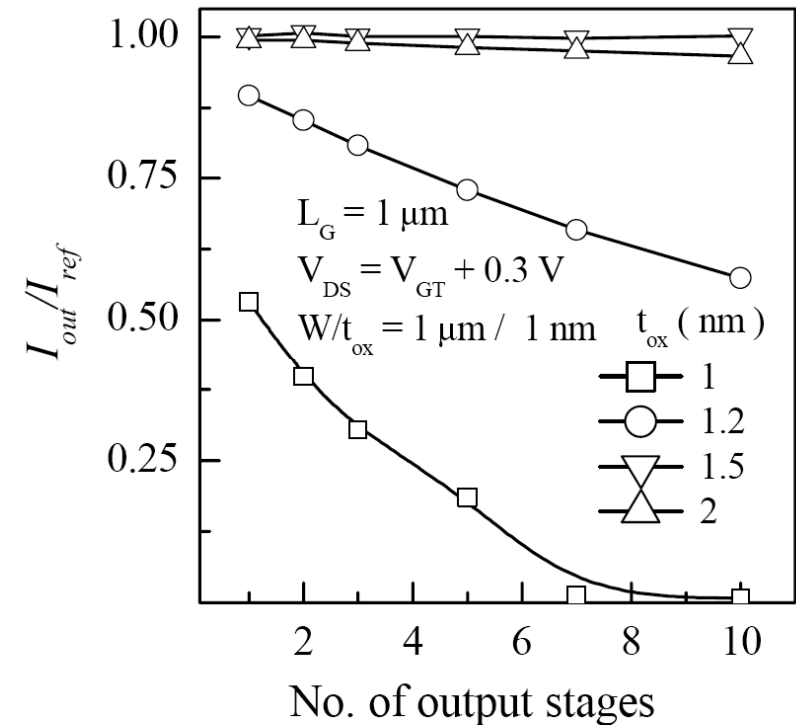


- Ex.: at 1nm oxide → 45% error !!!!

Basic Current Mirror

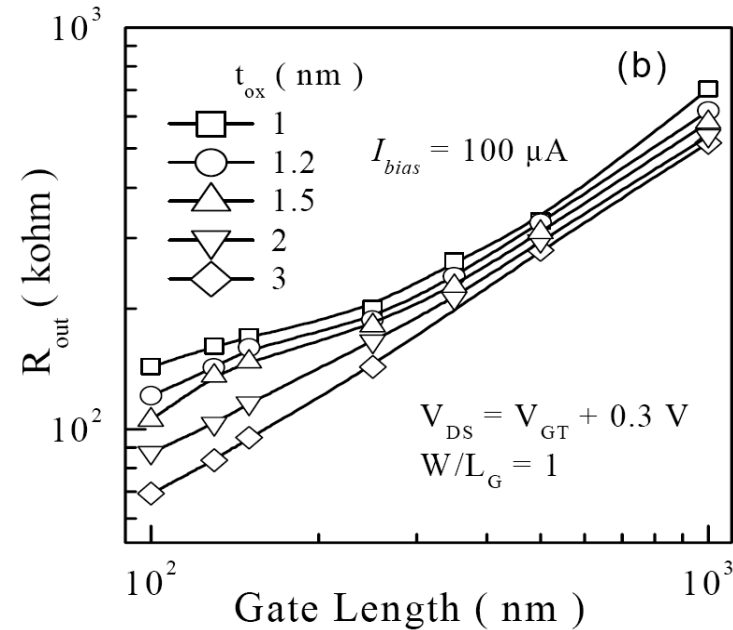
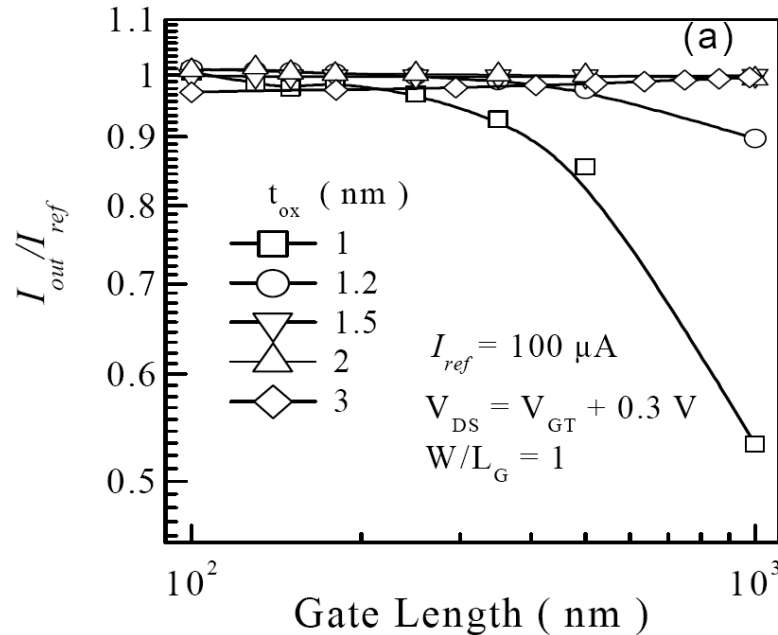
G_{CM} (I_{out}/I_{ref}) vs. Gate current

- G_{CM} error degrades with the number of mirroring output stages
 - The number of stages indicates the number of parallel transistors mirroring I_{ref}
- A drastic G_{CM} degradation with more than 5 stages and $t_{ox}=1\text{nm}$
- Even with 1.2 and 1.5 nm gate oxides, there is considerable degradation in the transfer ratio with increasing number of output stages.
- G_{CM} degrades
 - in **short** channel transistors \leftrightarrow short channel effects
 - in **long** channel transistors \leftrightarrow gate leakage
 - \rightarrow An optimum channel length at which the current mirror results in a transfer ratio of nearly 1



Basic Current Mirror

$G_{CM} (I_{out}/I_{ref})$ vs. Channel length

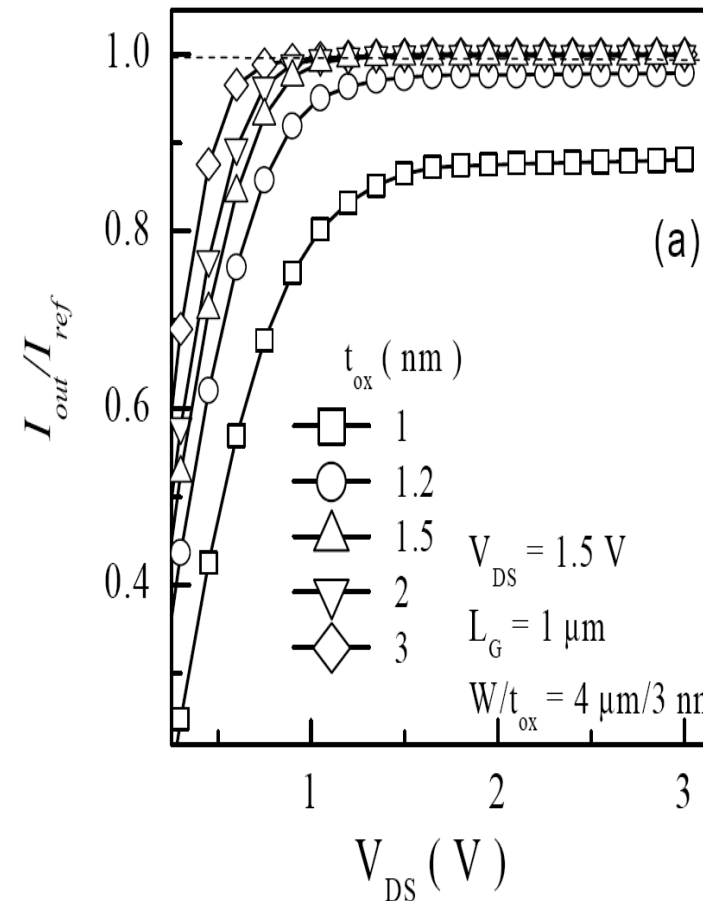
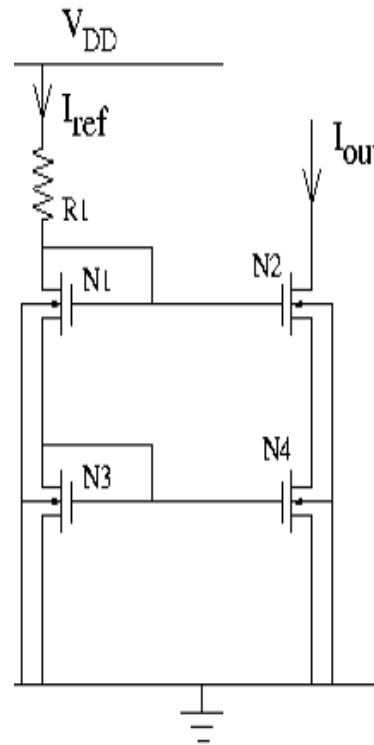


- An optimum value of the channel length for the best current mirroring is about 150nm but at this channel length, the output impedance reduces.
- Output impedance improvement is achieved with scaled oxides for short channel devices
 - This improvement is not substantial for long channel cases.

Cascode Current Mirror

$G_{CM} (I_{out}/I_{ref})$ vs. Gate current

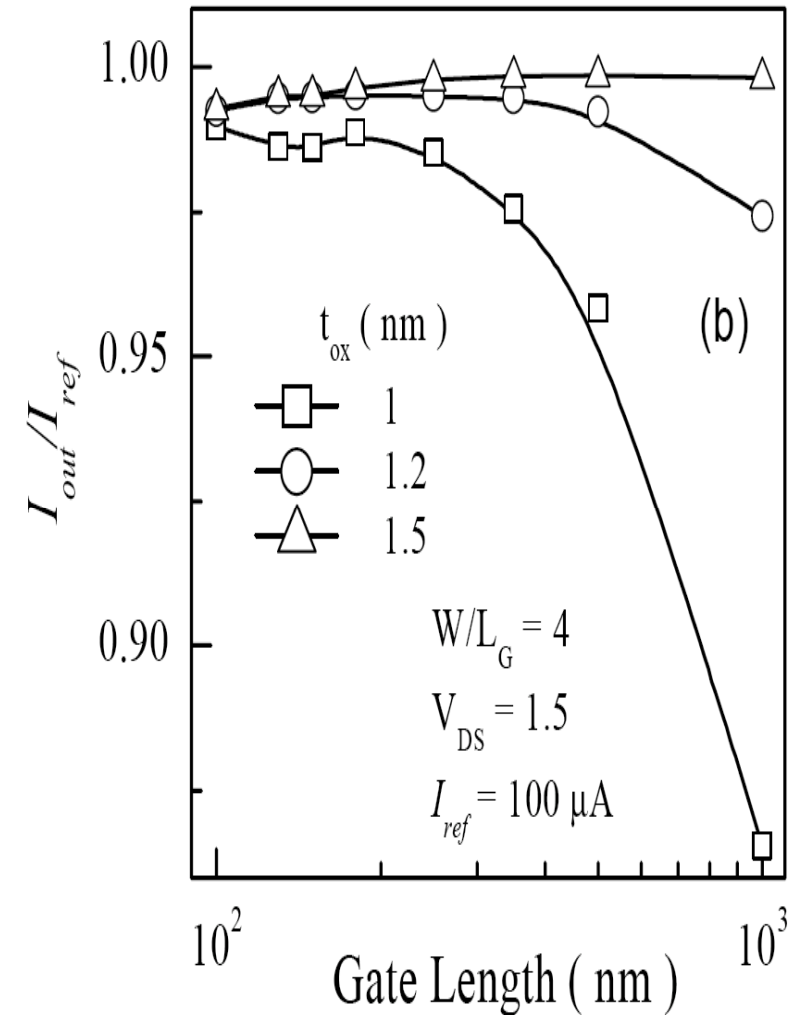
- @ $t_{ox}=1\text{nm}$,
 - the cascode mirror $G_{CM}=0.85$
 - basic mirror $G_{CM}=0.55$
- This higher tolerance to gate current is due to
 - transistor stack
 - inherent reverse body bias reducing the effective gate over drive on the device M2



Cascode Current Mirror

G_{CM} (I_{out}/I_{ref}) vs. Gate current

- Effect of NMOS device scaling on G_{CM} for various gate oxide thicknesses.
- → G_{CM} Degradation @ long L
 - G_{CM} degradation is lesser than that of short channel devices
 - → This shows the potential suitability of cascode mirror circuits for the deeply scaled gate oxide CMOS regime with increased gate leakages



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Scaltech Opamp design

65nm Opamp Design

- Two main design trends:
 - Design an opamp at the lowest supply voltage
 - → LV Opamp Design
 - Design an opamp with maximum performance (gain & bandwidth)
 - → ScalTech Opamp Design

LV opamp design

General issue

- It is not possible to stack many devices between rails
 - → No cascode
 - → Sufficient gain → Multistage structures
 - → Stability → Limited bandwidth
- Input stage
 - No swing → Optimum bias
 - For supply minimization & optimum switch operation

$$V_{in_DC} = 0$$

- Output stage
 - Maximum output swing
 - → Rail-to-Rail output swing is mandatory

$$V_{out_DC} = V_{DD}/2$$

- Minimum supply as close as possible to minimum switch supply

$$V_{DDswitch} = V_{TH} + V_{ov}$$

- Reduced turn-on time for switched-opamp solutions

LV opamp design

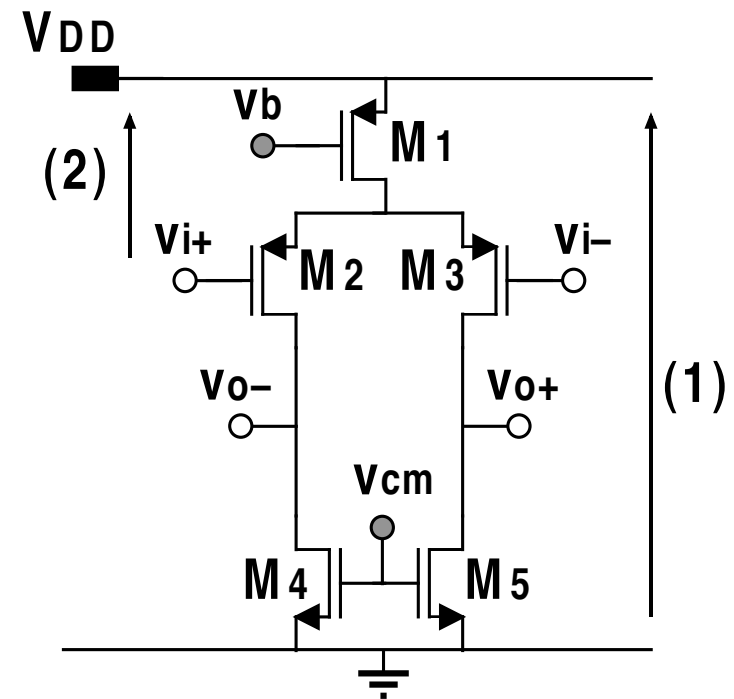
Differential Input stage - Supply minimization*

- Differential input stage

$$V_{DDmin} = \max \begin{cases} 3 V_{ov} + V_{outpp} \\ V_{in_DC} + V_{TH_P} + 2 V_{ov} \end{cases}$$

- V_{outpp} is minimum
- V_o bias point fixed by 2nd-stage
- → V_{DDmin} is achieved using

$$V_{in_DC} = 0$$



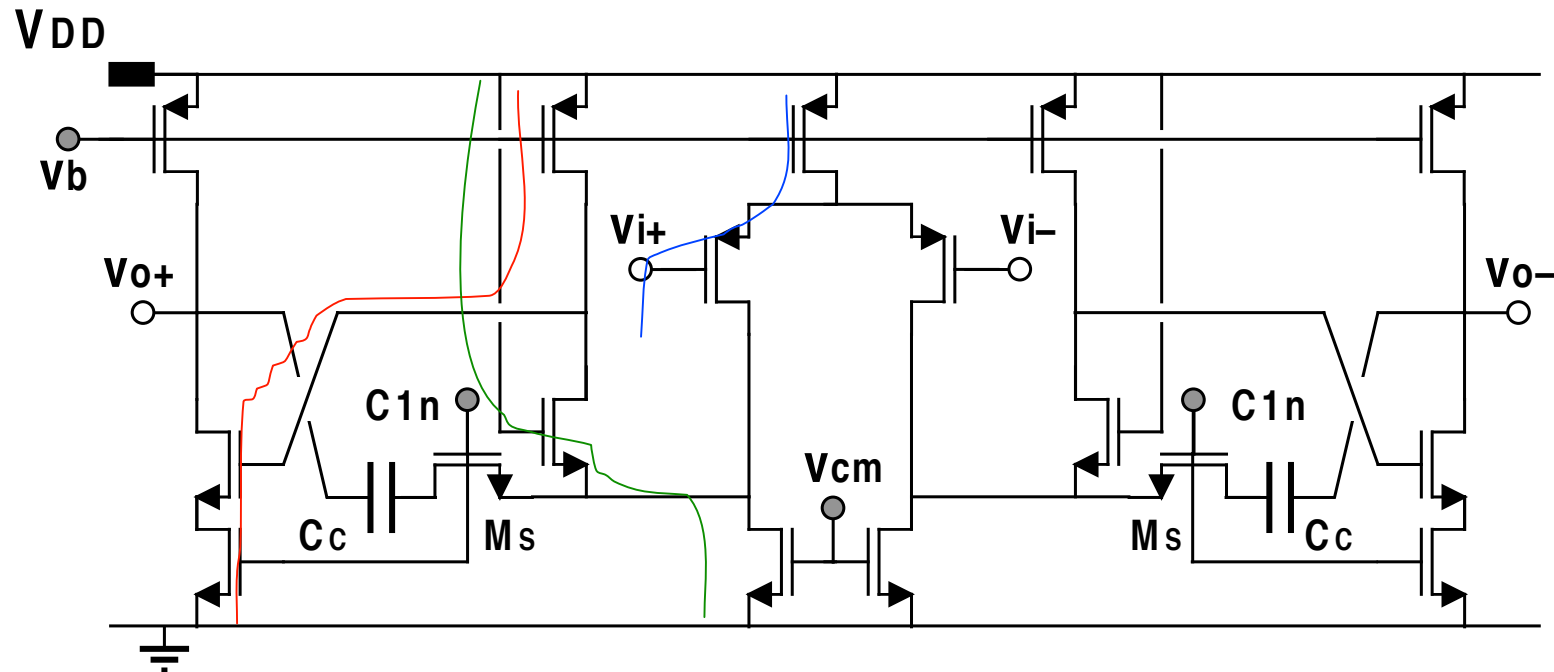
- Optimum operation for a switch connected at the input node

$$\Rightarrow V_{DDmin} = V_{TH_P} + 2 V_{ov}$$

*R. Castello, F. Montecchi, F. Rezzi, and A. Baschirotto, "Low-voltage analog filter", IEEE Transaction on Circuits and Systems - II - Nov. 1995 - pp. 827-840

LV opamp design

Two-stage Miller-compensated Structure



- Assuming $V_{in_DC}=0$
- Any branch requires:

$$V_{DDmin} = V_{TH} + 2 \cdot V_{ov}$$

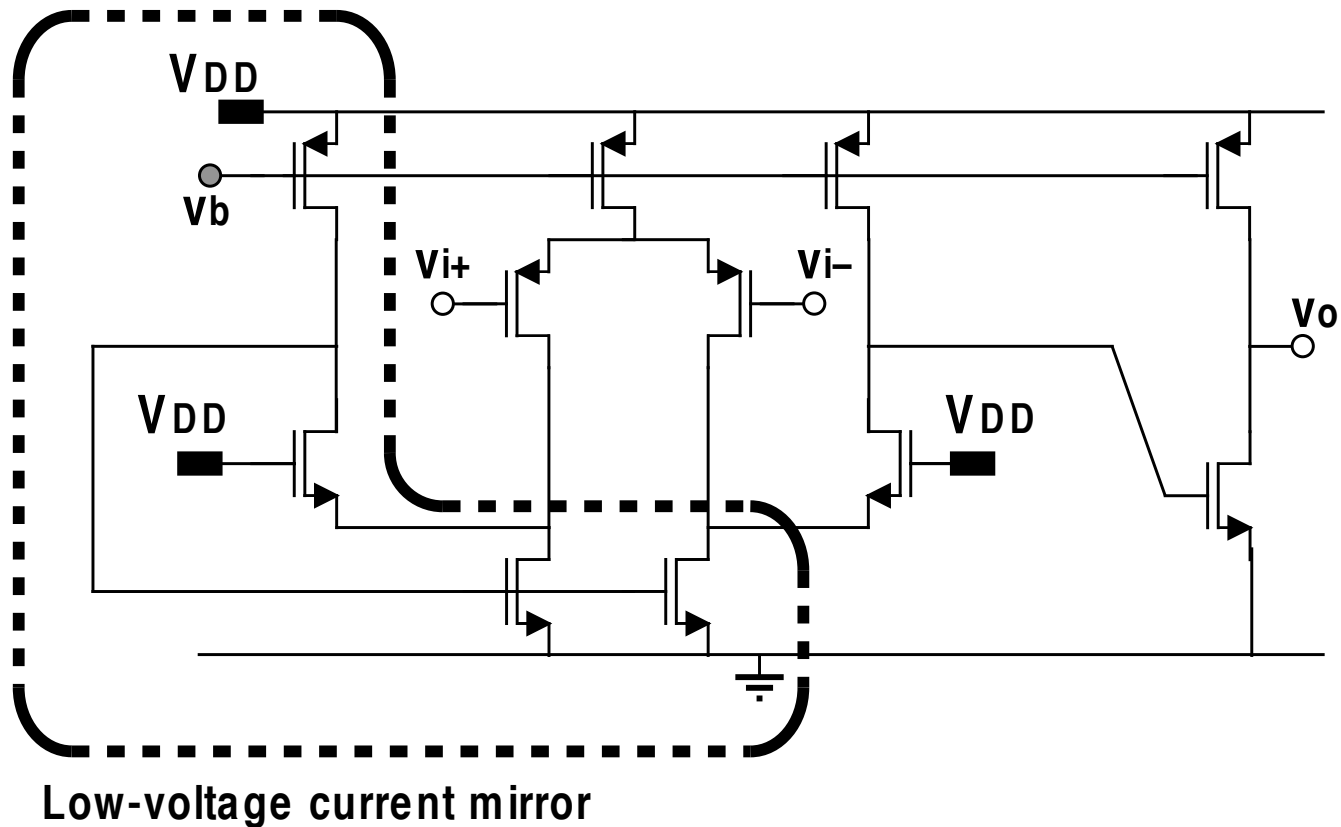
- V_{DDmin} is limited by:
 - Stage coupling
 - Cascode
 - Input diff pair

- Fully-differential
 - → A low-voltage CMFB is needed

LV opamp design

Single-ended two-stage structure

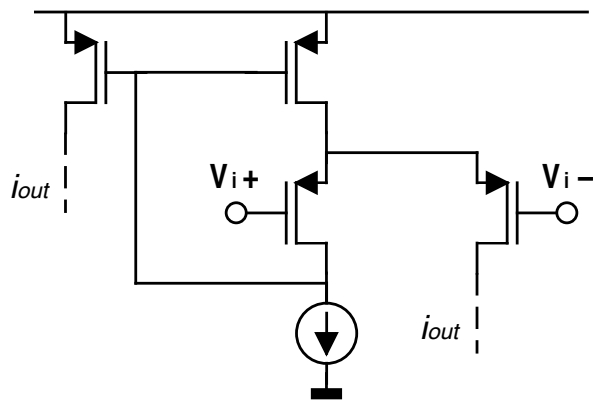
- Two-stage single-ended opamp
 - → Use of low-voltage current mirror



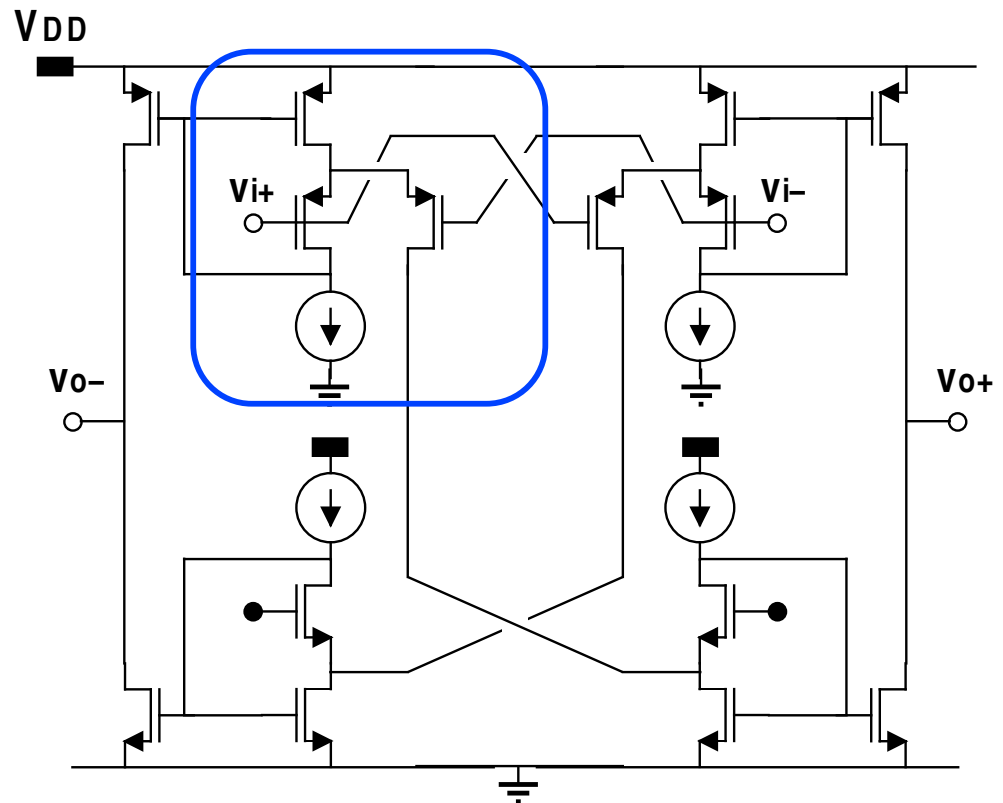
$$V_{DDmin} = V_{TH_P} + 2 V_{ov}$$

LV opamp design

Class-AB input pair*



Input differential pair



complete AB opamp

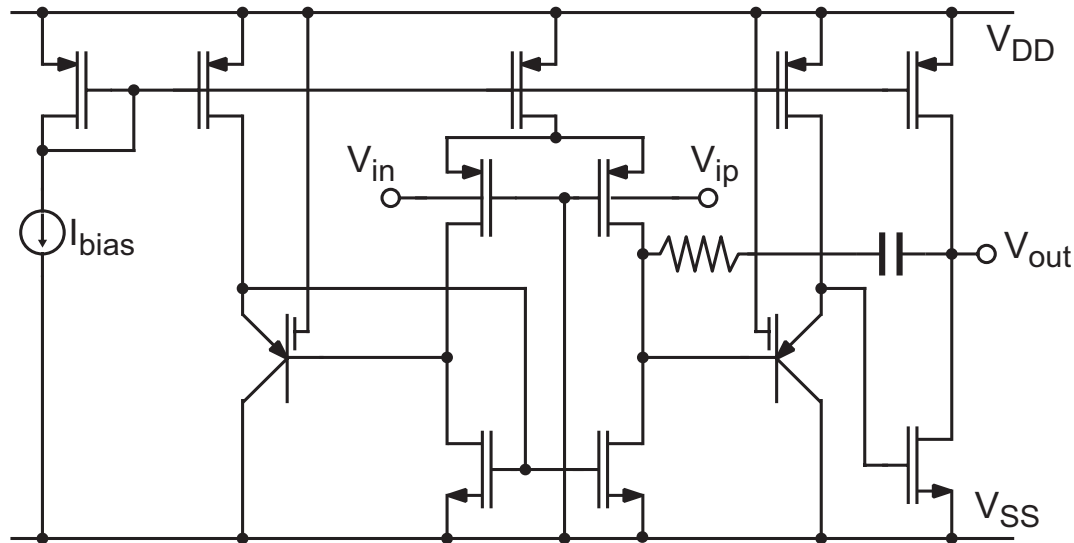
$$V_{DDmin} = V_{TH} + 2 \cdot V_{ov}$$

* M. Peluso, P. Vancorenland, A. Marques, M. Steyaert, W. Sansen, "A 900mV 40 μ W Switched Opamp $\Delta\Sigma$ Modulator with 77dB Dynamic Range", ISSCC '98

LV opamp design

Bulk-driven Opamp

- The input signal is applied to MOS transistors bulk
 - → Rail-to-rail input common-mode swing



$$V_{DDmin} = V_{TH} + 2 \cdot V_{ov}$$

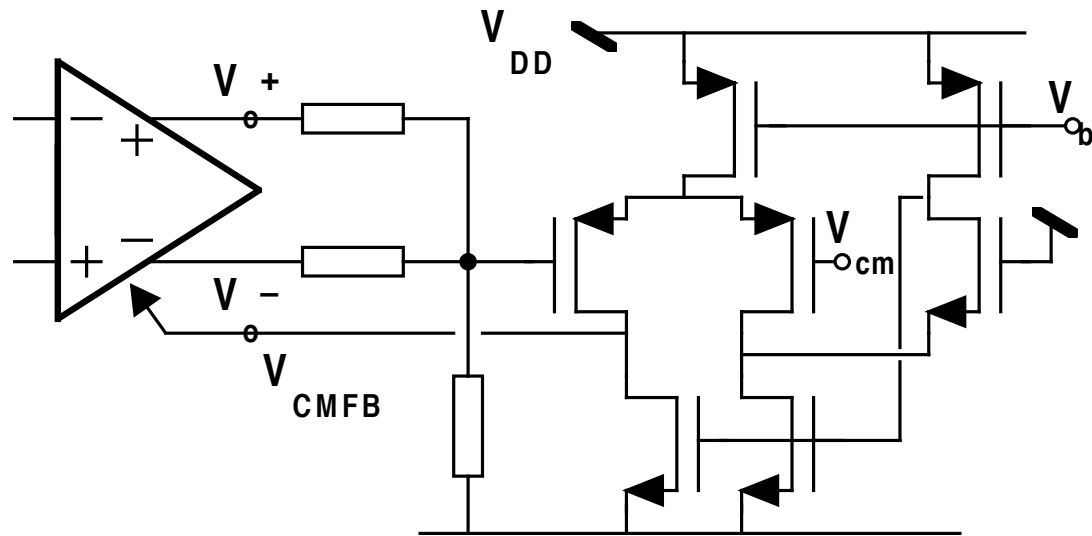
- Input transistors transconductance g_m
 - Large variation ($\approx x2$) with the CM input voltage
 - Small value
 - Small gain
 - Small bandwidth
 - High input referred noise

LV opamp design

LV Common-Mode Feedback

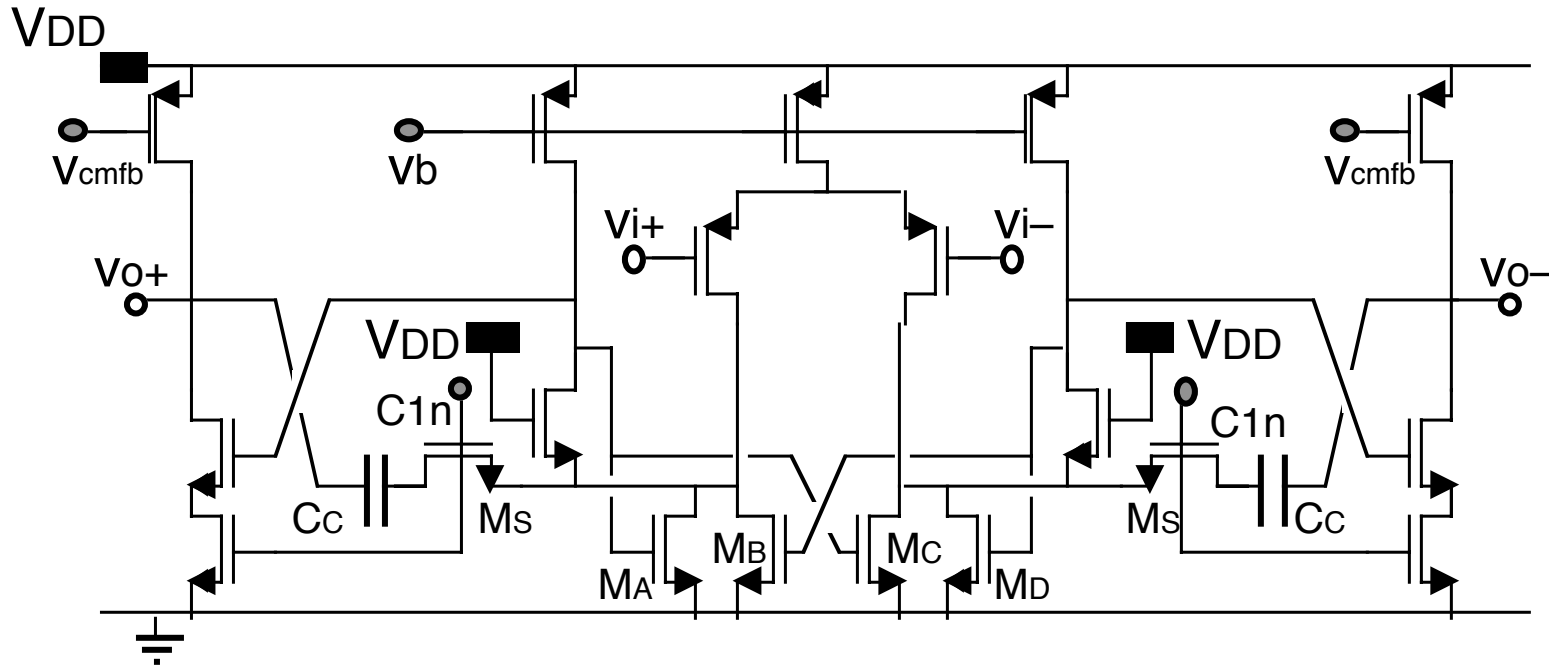
- For a CT solution
 - → the CMFB inputs are connected to the opamp output ($\approx V_{DD}/2$)
 - For LV, $V_{DD}/2 < V_{TH}$
- Solution: Passive (resistive / capacitive) level shift
 - ☹️ CM loop gain loss
 - ☹️ 3/4 poles → Stability ?

$$V_{DD\min} = V_{TH} + 3 \cdot V_{OV}$$



LV opamp design

Efficient CMFB *



- The MA-MB-MC-MD → a low common-mode impedance at the 1st stage
 - → A SC CMFB only to the 2nd stage
 - Larger CMFB bandwidth

■ _____
* M. Dessouky, and A. Kaiser, "Very Low-Voltage Digital-Audio SD Modulator with 88-dB Dynamic Range Using Local Switch Bootstrapping", IEEE JSSC, Mar. 2001

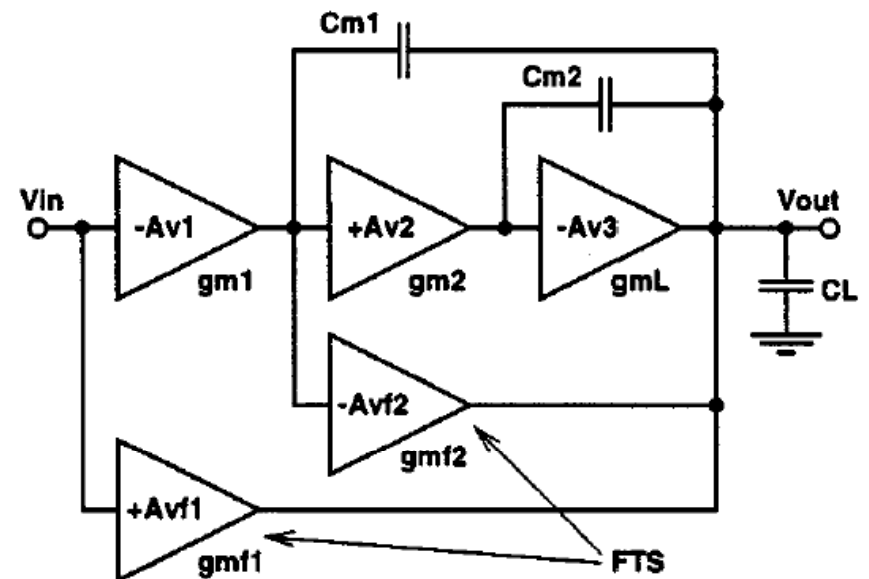
M. Swartari and K. Halonen, "Fully differential switched opamp with enhanced common-mode feedback," *Electron. Lett.*, vol. 34, no. 23, Nov. 1998.

LV Opamp

Future trends

- CMOS gain-per-stage is dropping with technology scaling
- LV design disable cascode
 - → Multistage structure are needed
 - Compensation scheme are becoming crucial

- FD structures are mandatory for achieving a sufficient DR
 - LV CMFB is critical
 - Feedforward paths are not seen by the CMFB !!!



ScalTech Opamp Design

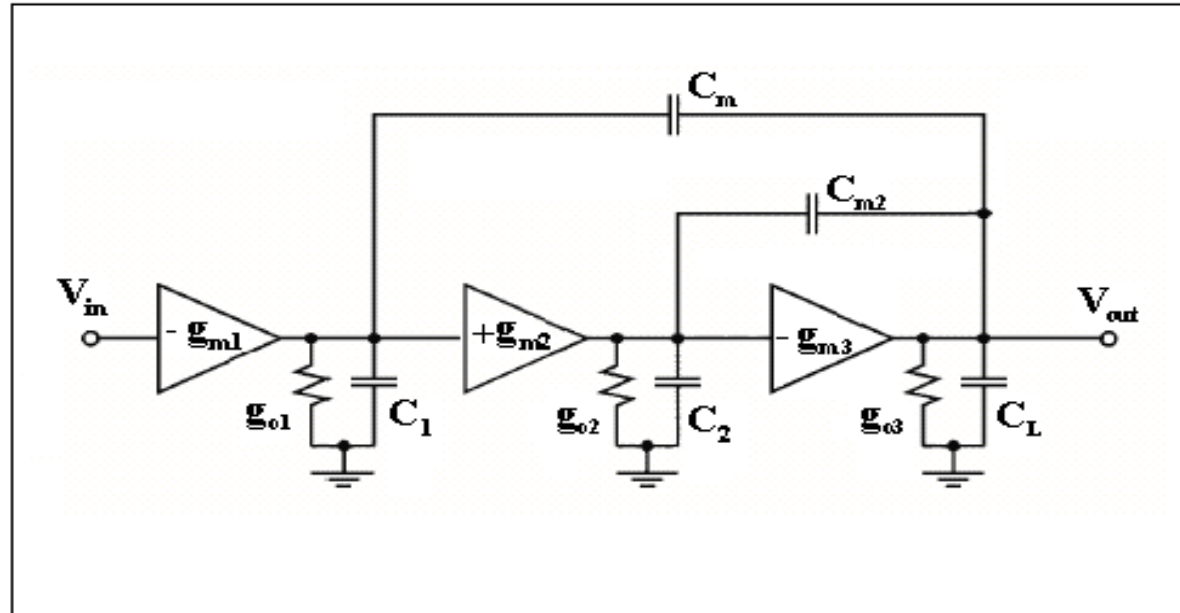
Multistage structures

- Several solutions are available for multistage compensation topology
 - Nested Miller Compensation (NMC)
 - Damping-Factor-Control Frequency Compensation (DFCFC)
 - Positive Feedback Compensation (PFC)
 - Active Feedback Frequency Compensation (AFFC)
 - Single Miller capacitor Compensation (SMC)
 - Single Miller capacitor FeedForward Compensation (SMFFC)
 - Transconductance with Capacitance Feedback Compensation (TCFC)
 - Nested Gm-C Compensation (NGCC)
 - Dual-Loop Parallel Compensation (DLPC)
- They have to be compared in terms of:
 - Performance (Gain, bandwidth, phase margin)
 - Load driving capability
 - Power consumption
 - Area

 - Compensation cap is not scaling with technology

ScalTech Opamp Design

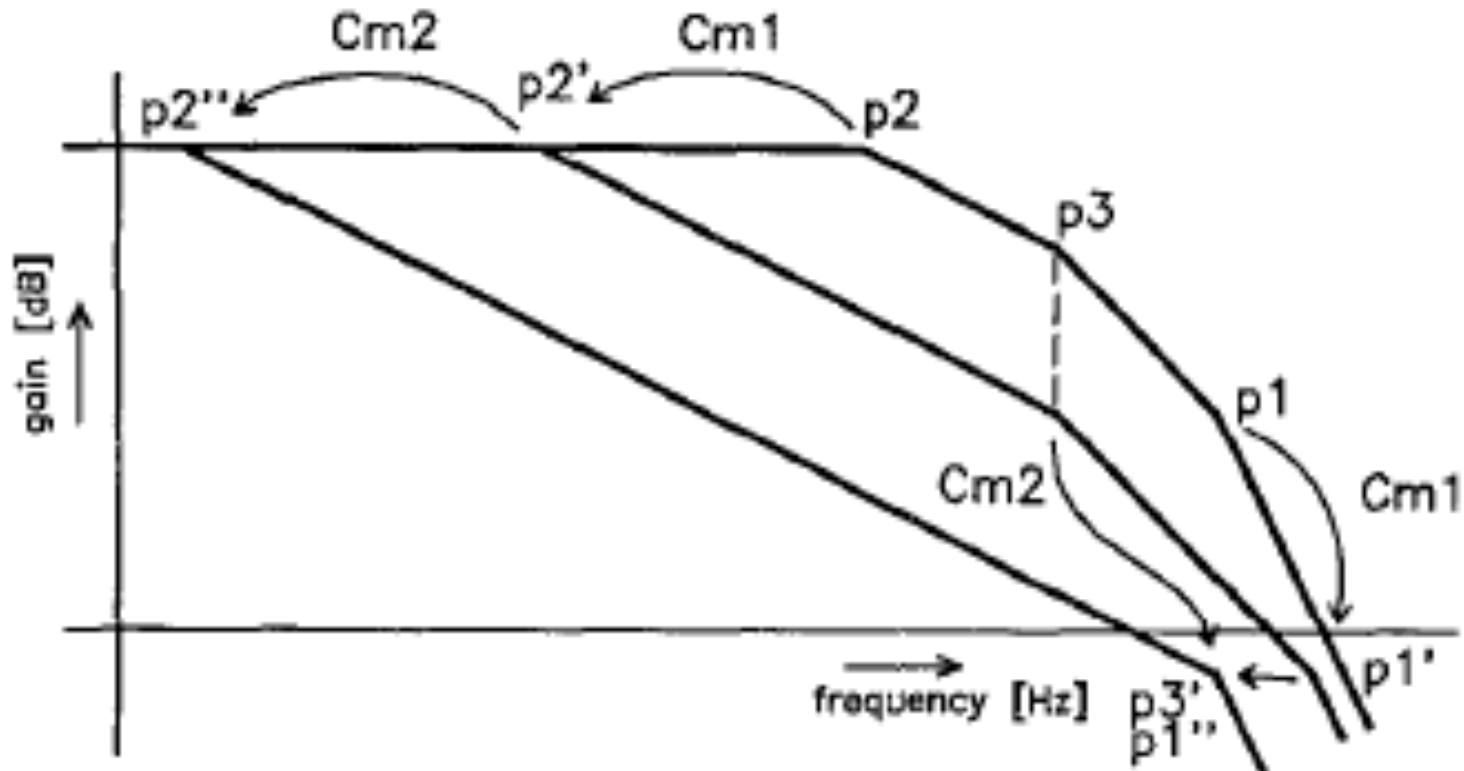
3-stage-opamp: Nested Miller Compensation (NMC)*



- For any additional stage,
 - Larger gain
 - Addit comp cap from the output to close the external feedback loop
 - Smaller bandwidth
 - Smaller compensation capacitors \leftrightarrow Larger g_{m3}

ScalTech Opamp Design

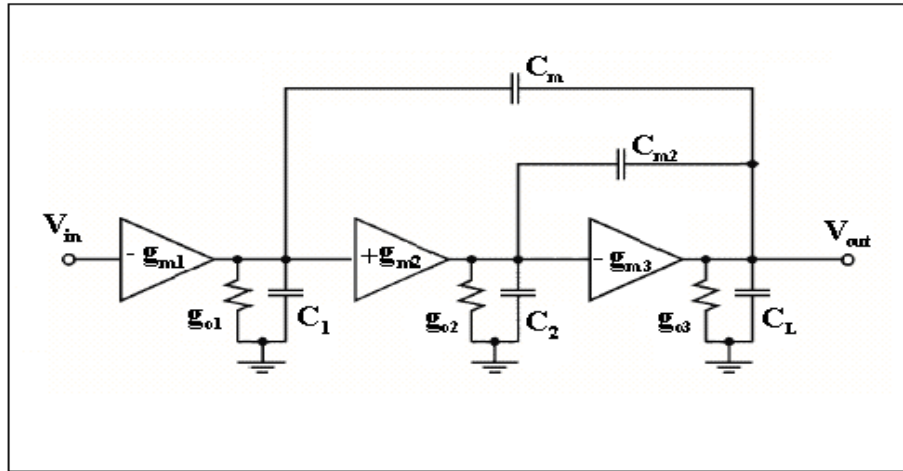
3-stage-opamp: Nested Miller Compensation (NMC)



- Every additional stage
 - Additional gain
 - Lower bandwidth

ScalTech Opamp Design

3-stage-opamp: Nested Miller Compensation (NMC) - Transfer function



$$A_{v(NMC)}(s) = \left(\frac{A_{dc}}{\left(1 + \frac{s}{P_{-3dB}}\right) \left(1 + s \frac{C_{m2}}{g_{m2}} + s^2 \frac{C_L C_{m2}}{g_{m2} g_{m3}}\right)} \right)$$

$$\approx \frac{1}{s \frac{C_m}{g_{m1}} \left(1 + s \frac{C_{m2}}{g_{m2}} + s^2 \frac{C_L C_{m2}}{g_{m2} g_{m3}}\right)}$$

$$PM_{(NMC)} \approx 60^\circ \quad \leftarrow \rightarrow \text{Damping factor} \approx 1/\sqrt{2}$$

$$C_m = 4 \left(\frac{g_{m1}}{g_{m3}} \right) C_L \quad C_{m2} = 2 \left(\frac{g_{m2}}{g_{m3}} \right) C_L$$

$$GBW_{(NMC)} = \frac{1}{4} \left(\frac{g_{m3}}{C_L} \right) \approx \frac{1}{C_L}$$

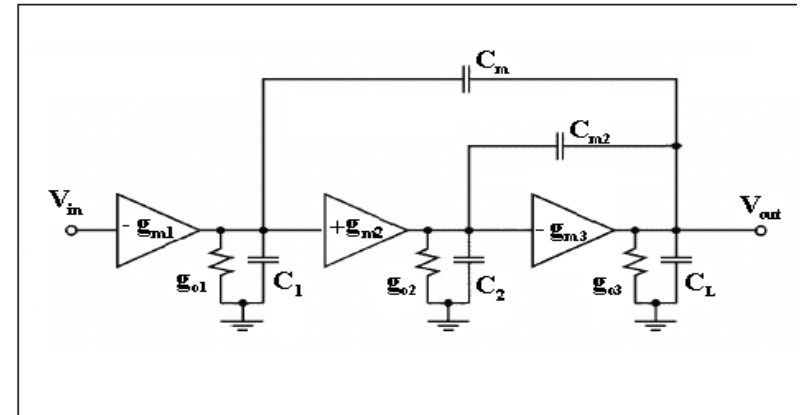
- The two non-dominant poles form a complex pole
 - Their damping factor is very small
 - \rightarrow a frequency 'peak' could appear close to UGB

ScalTech Opamp

3-stage-opamp: Nested Miller Compensation (NMC)

Stability considerations

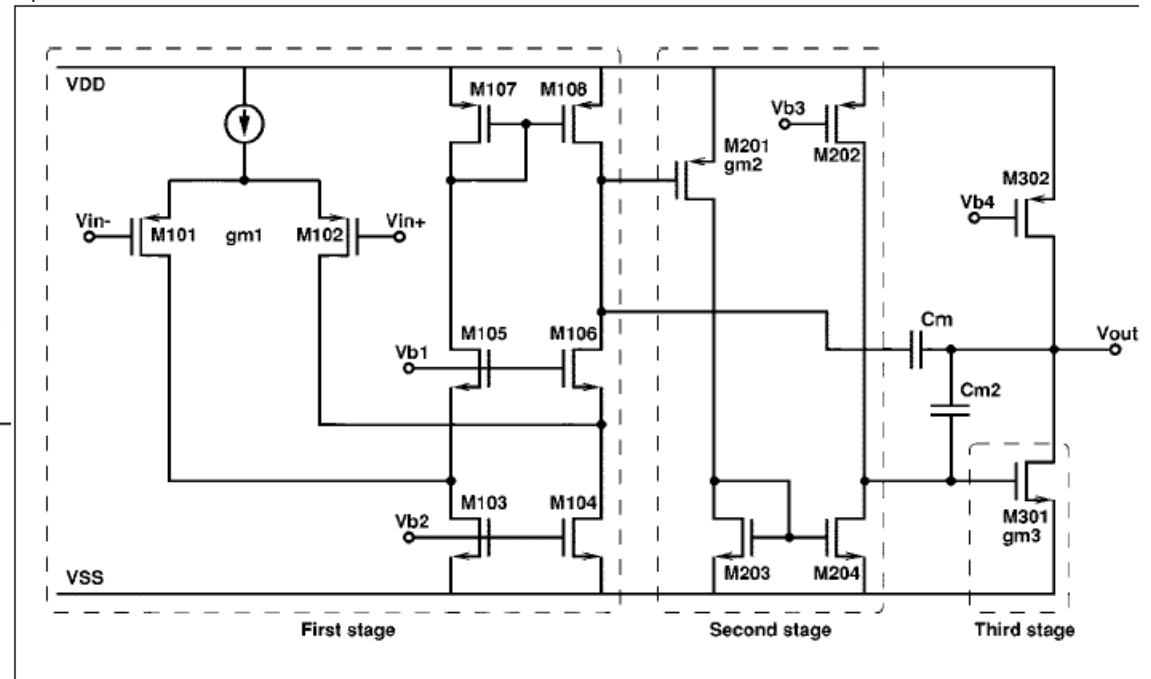
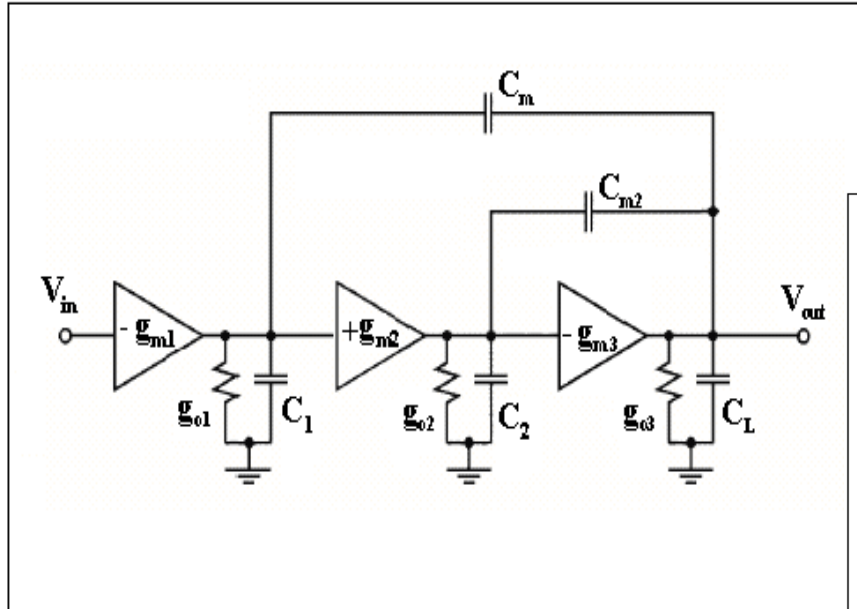
- Key point is the loading cap (C_L)
 - ☹️ C_L affects the non-dominant poles location
 - → affects the opamp stability
 - ☹️ C_L increases → UGB decreases
 - Miller capacitor $\approx C_L$ size
 - Large C_L
 - → Large Miller cap
 - → Large area → smaller bandwidth
- To increase the bandwidth
 - → increase g_{m3}
 - increase output gain stage bias current and transistors size
- Also C_{m2} (part of opamp cap load) reduces NMC UGB bandwidth
 - Eliminating C_{m2} , the capacitive load at the output is reduced.
 - The non-dominant poles are pushed at higher frequencies
 - The NMC UGB is extended



ScalTech Opamp Design

3-stage-opamp: Nested Miller Compensation (NMC)

Circuit implementation

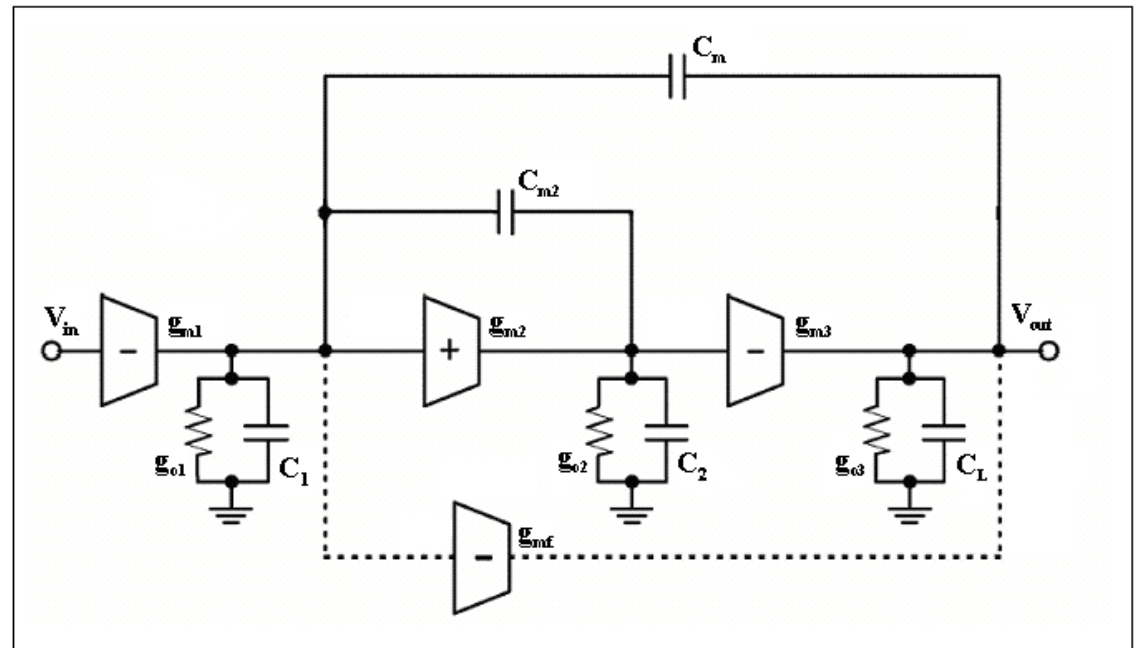


ScalTech Opamp

3-stage-opamp: Positive Feedback Compensation (PFC)*

General features

- The inner comp. cap is removed
 - the output load is reduced
 - the UGB is enhanced
- Positive feedback with cap C_{m2} around the 2nd-stage
 - → a LHP zero to cancel out one of the non-dominant poles



- A single feedforward stage is used to turn the output stage into a class AB stage
 - → The slew rate will be limited by the DC current in the first stage

* J. Ramos and M. Steyaert, "Three-stage amplifier with positive feedback compensation scheme," in *Proc. IEEE Custom Integrated Circuits Conference*, Orlando, FL, pp. 333-336, May 2002

ScalTech Opamp

3-stage-opamp: Positive Feedback Compensation (PFC)

The small-signal transfer function

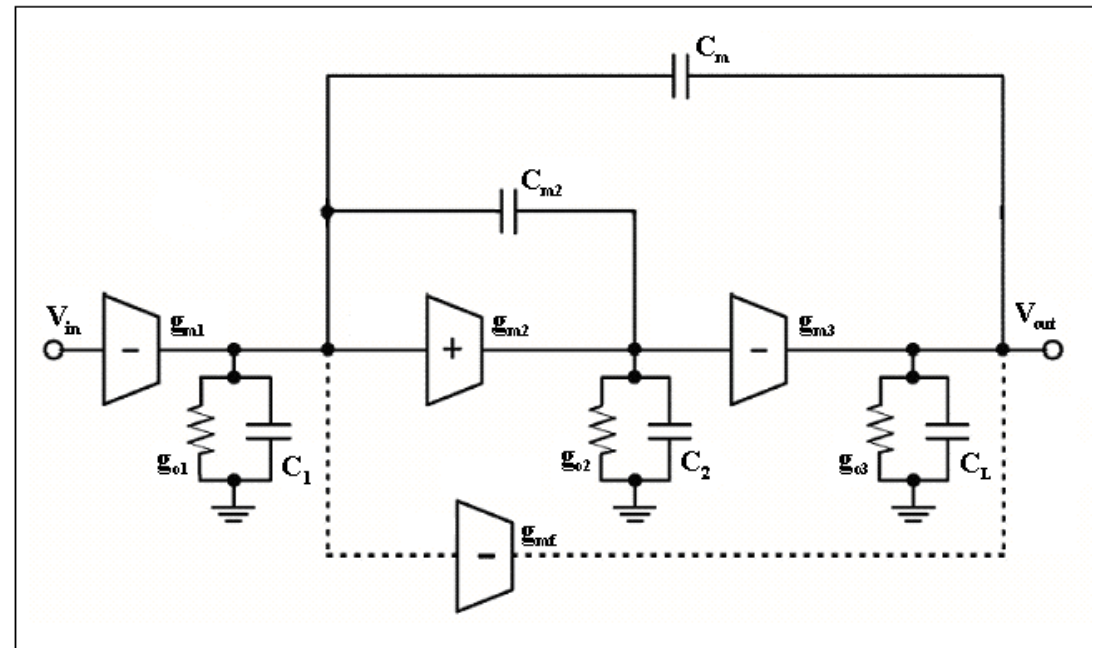
$$A_{V(PFC)}(s) = \frac{A_{dc} \left(1 + s \frac{2C_{m2}}{g_{m2}} - s^2 \frac{C_m C_{m2}}{g_{m2} g_{m3}} \right)}{\left(1 + \frac{s}{p_{-3dB}} \right) \left(1 + s \frac{C_{m2} (2g_{m3} C_m - g_{m2} C_L)}{g_{m2} g_{m3} C_m} + s^2 \frac{C_L (C_{m2} - C_2)}{g_{m2} g_{m3}} \right)}$$

$$PM_{(PFC)} \approx 60^\circ$$

$$GBW_{(PFC)} = \frac{1}{4} \cdot \left(\frac{g_{m3}}{C_L} \right) \cdot \beta \approx \frac{1}{\sqrt{C_L}}$$

with

$$\beta = \frac{7}{2} \cdot \sqrt{\left(\frac{g_{m2}}{g_{m3}} \right) \cdot \left(\frac{C_L}{C_{m2} + C_2} \right)}$$



ScalTech Opamp

3-stage-opamp: Positive Feedback Compensation (PFC)

Stability considerations

- g_{m3} or C_m must be sufficiently large (C_m avoids excessive power consumption)
- C_{m2} realizes a positive feedback around g_{m2}
 - C_{m2} controls of the damping factor of the complex poles
 - $C_{m2} \ll C_m \rightarrow$ no 1st-stage slew rate limitation

- C_{m2} creates a LHP zero
 - to cancel out one of the non-dominant poles
 - \rightarrow phase margin improvement

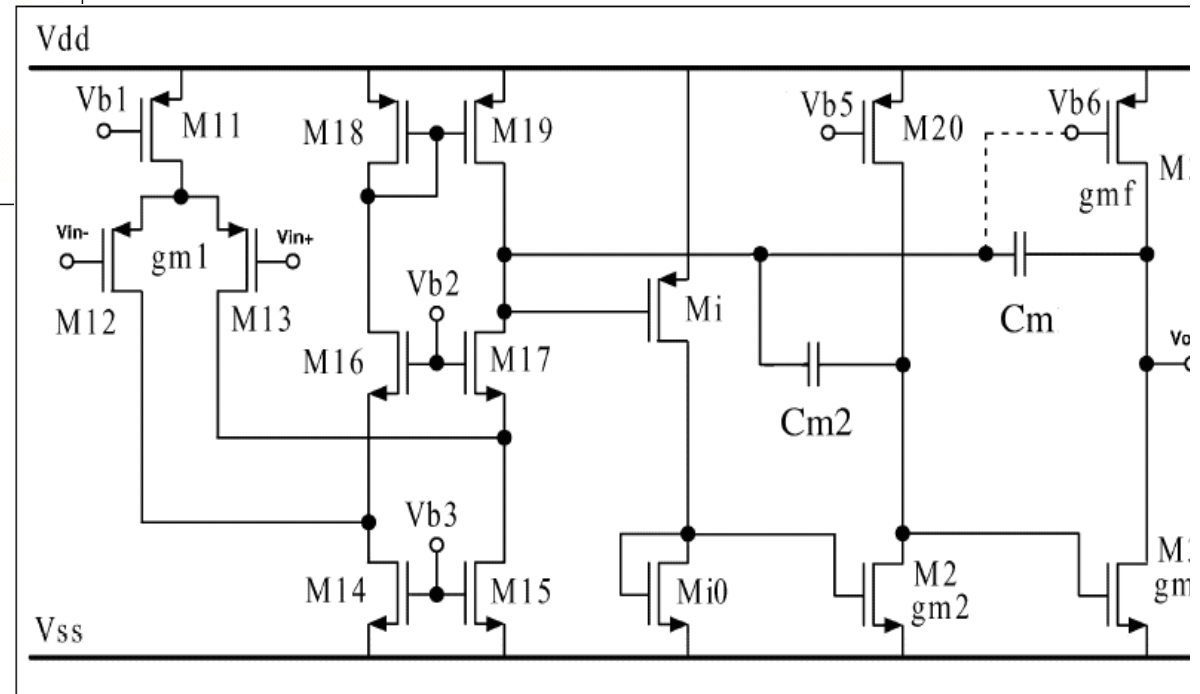
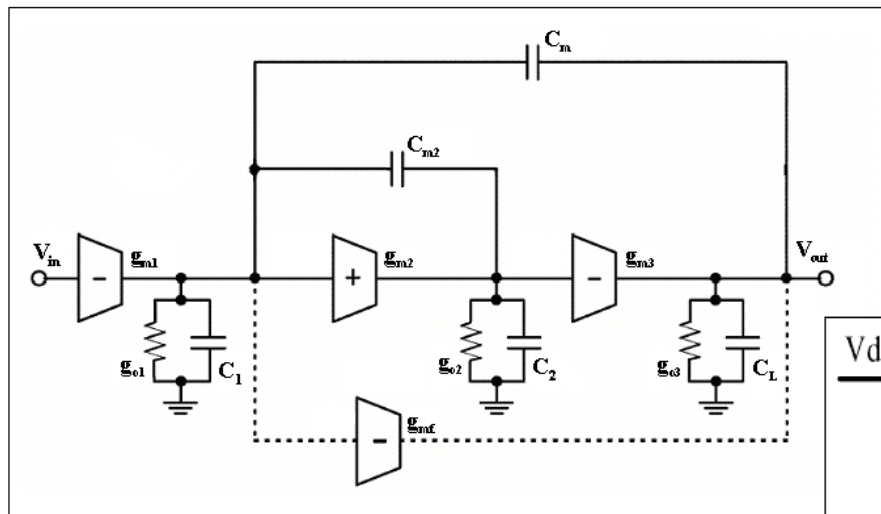
$$A_{V(PFC)}(s) = \frac{A_{dc} \left(1 + s \frac{2C_{m2}}{g_{m2}} - s^2 \frac{C_m C_{m2}}{g_{m2} g_{m3}} \right)}{\left(1 + \frac{s}{p_{-3dB}} \right) \left(1 + s \frac{C_{m2} (2g_{m3} C_m - g_{m2} C_L)}{g_{m2} g_{m3} C_m} + s^2 \frac{C_L (C_{m2} - C_m)}{g_{m2} g_{m3}} \right)}$$

- The GBW equations of both the NMC and PFC are similar, unless a β factor
- To drive large cap. loads
 - The PFC ($\approx 1/\sqrt{C_L}$) is more efficient than the NMC ($\approx 1/C_L$)
 - Ex.: PFC gives a $\approx 6x$ GBW larger than NMC (for the same C_L and power)

ScaTech Opamp

3-stage-opamp: Positive Feedback Compensation (PFC) Circuit implementation

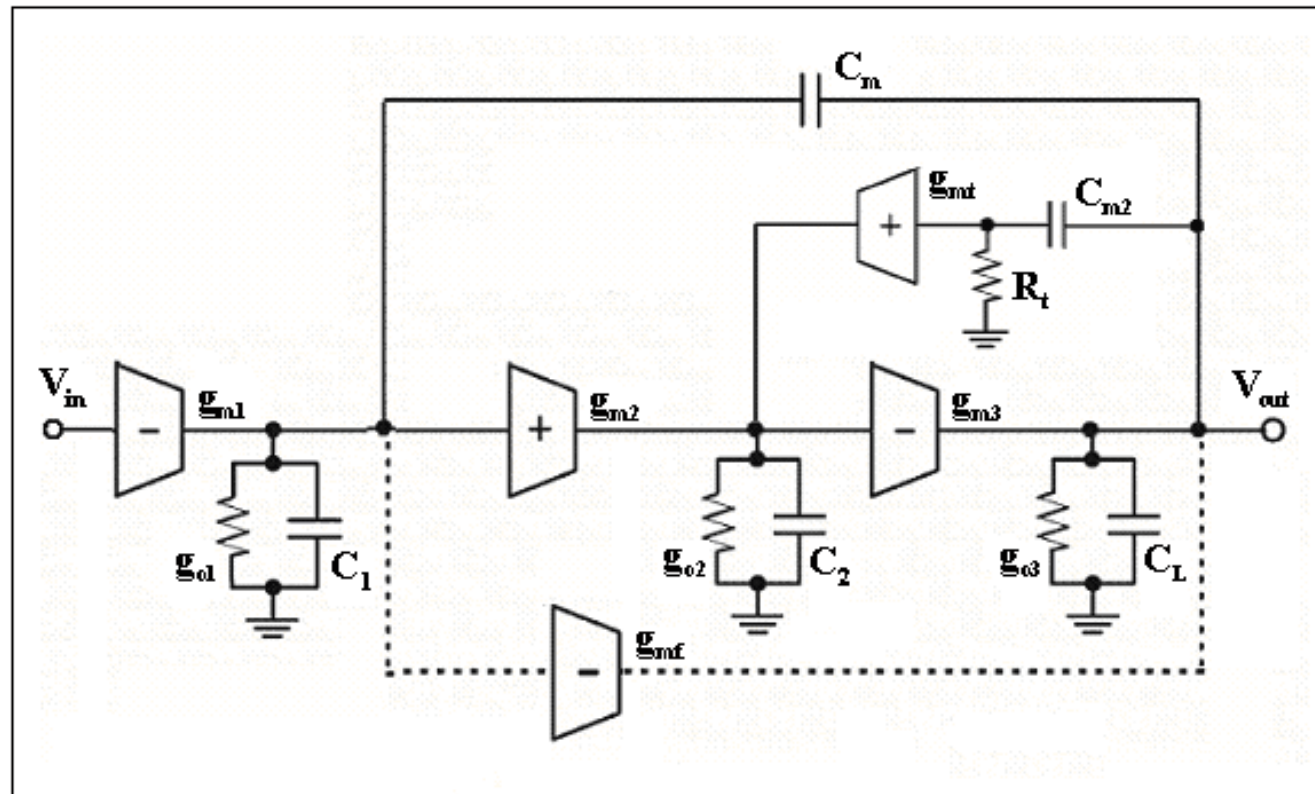
Circuit implementation



ScalTech Opamp

3-stage-opamp: Transconductance with cap. feedback compenss. (TCFC)*

- General features
 - The compensation cap C_{m2} & g_{mf} makes up the internal feedback loop



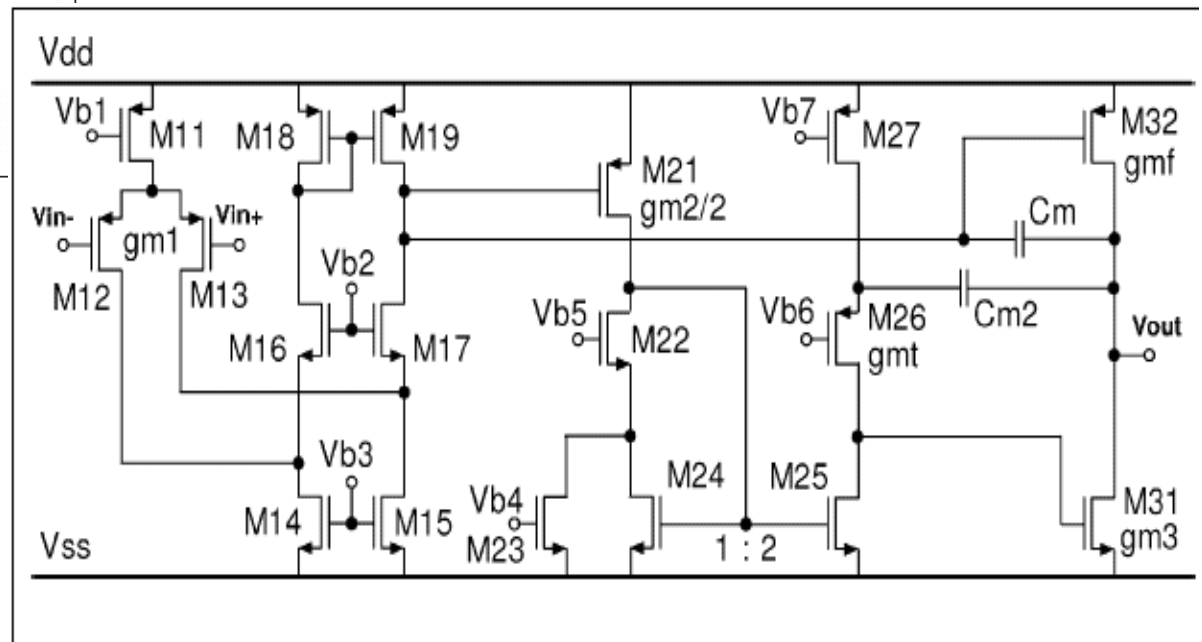
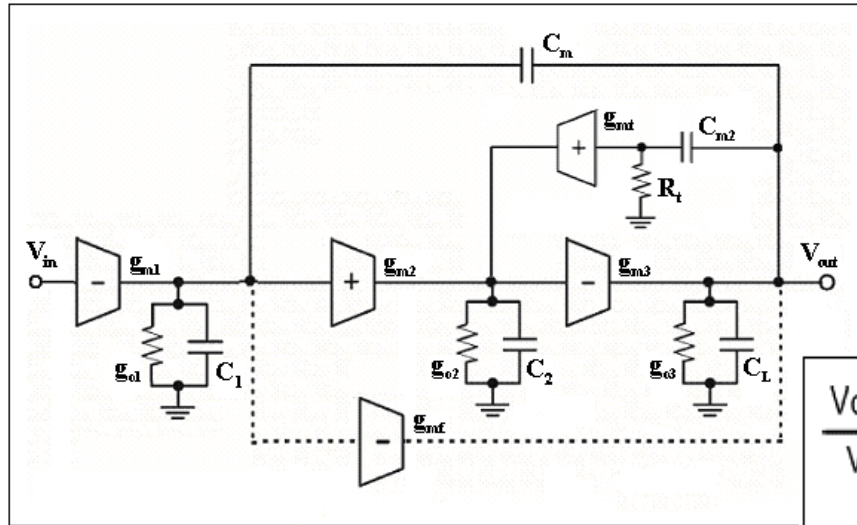
■ _____

* H. Lee, K. N. Leung, and P. K. T. Mok, "A dual-path bandwidth extension amplifier topology with dual-loop parallel compensation", *IEEE Journal of Solid State Circuits*, vol. 38, pp. 1739-1744, Oct. 2003

ScalTech Opamp

3-stage-opamp: Transconductance with cap. feedback comp. (TCFC)*

- Circuit implementation



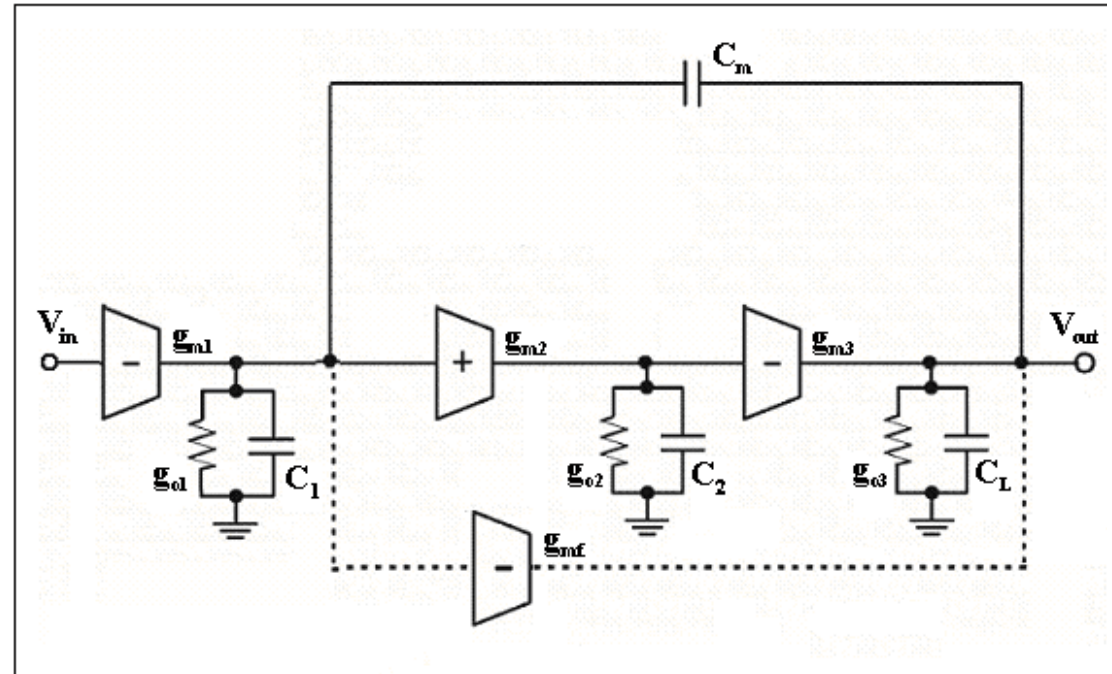
* H. Lee, K. N. Leung, and P. K. T. Mok, "A dual-path bandwidth extension amplifier topology with dual-loop parallel compensation", *IEEE Journal of Solid State Circuits*, vol. 38, pp. 1739-1744, Oct. 2003

ScalTech Opamp

3-stage-opamp: Single Miller Cap compensation (SMC) *

General features

- three gain stages
- only one comp. capacitor
- an additional g_{mf} from the 1st-stage output to the final output,
 - → a push-pull stage at the output
 - improving the opamp transient response



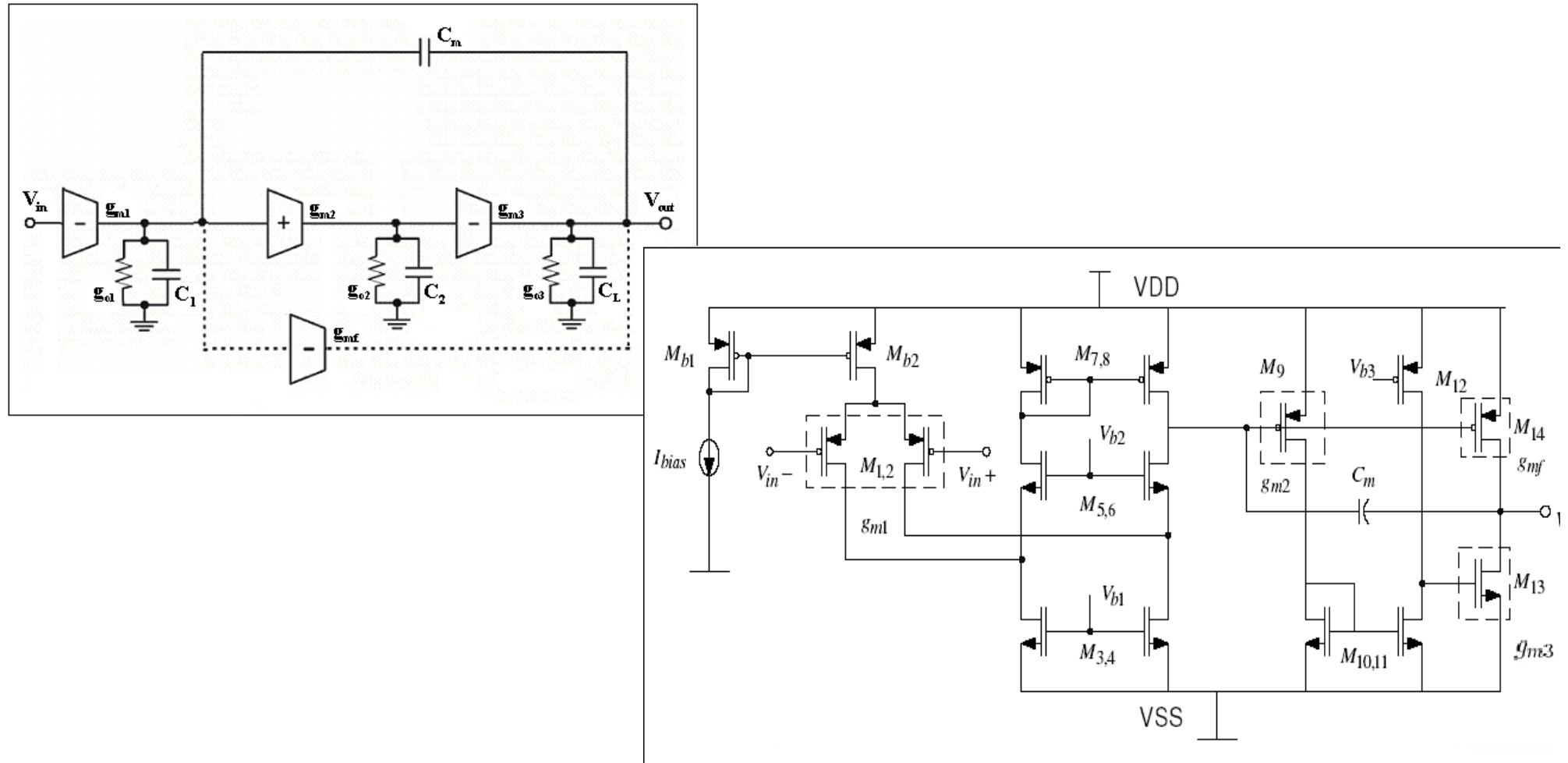
■ _____

* X. Fan, C. Mishra, and E. Sánchez-Sinencio, "Single Miller capacitor compensated multistage amplifiers for large capacitive load applications", in *Proc. IEEE International Symposium on Circuits and Systems*, Vancouver, Canada, pp. 493-496, May 2004

ScaTech Opamp

3-stage-opamp: Single Miller Cap Compensation (SMC)

Circuit implementation

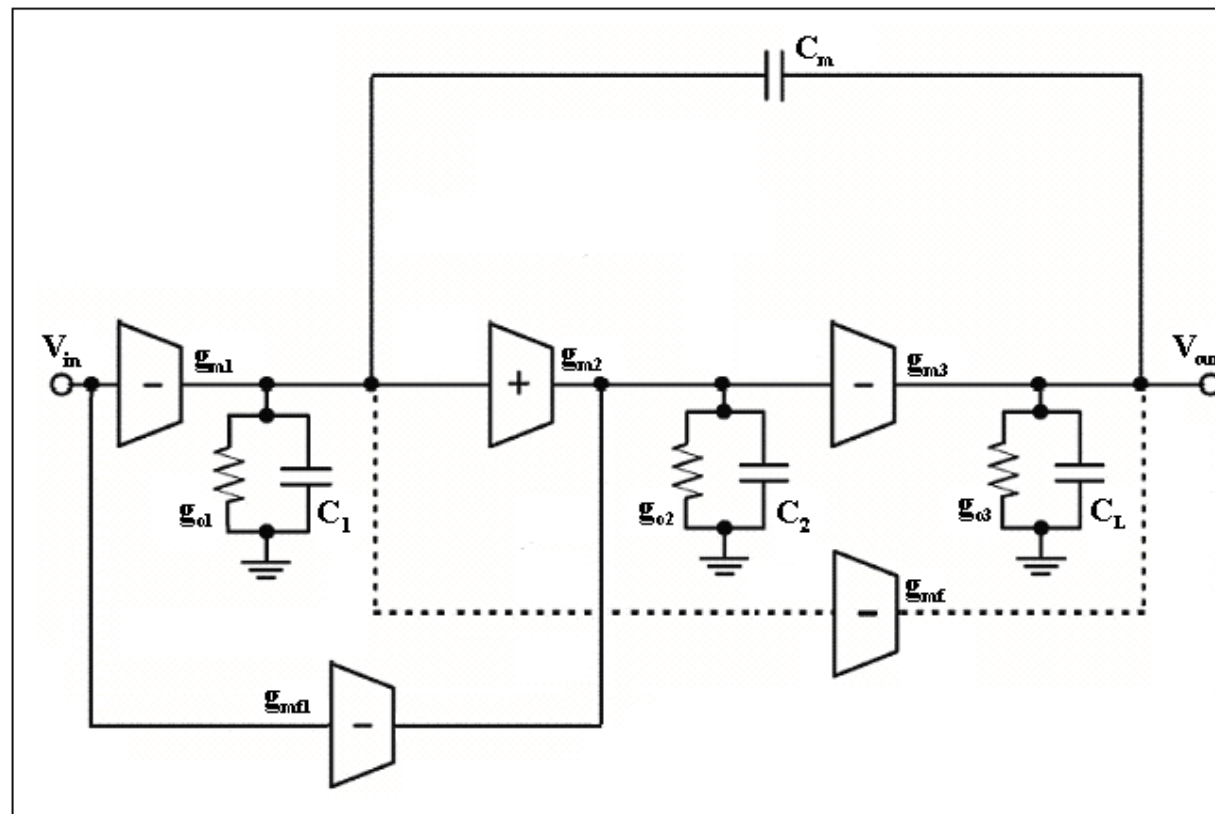


ScalTech Opamp

3-stage-opamp: Single Miller Cap FeedForward Compensation (SMFFC)

General features

- A feedforward path
 - → LHP zero to compensate the second pole (first non-dominant pole).
 - The FF path adds current at the 2nd-stage output pushing the second non-dominant pole to higher frequencies.

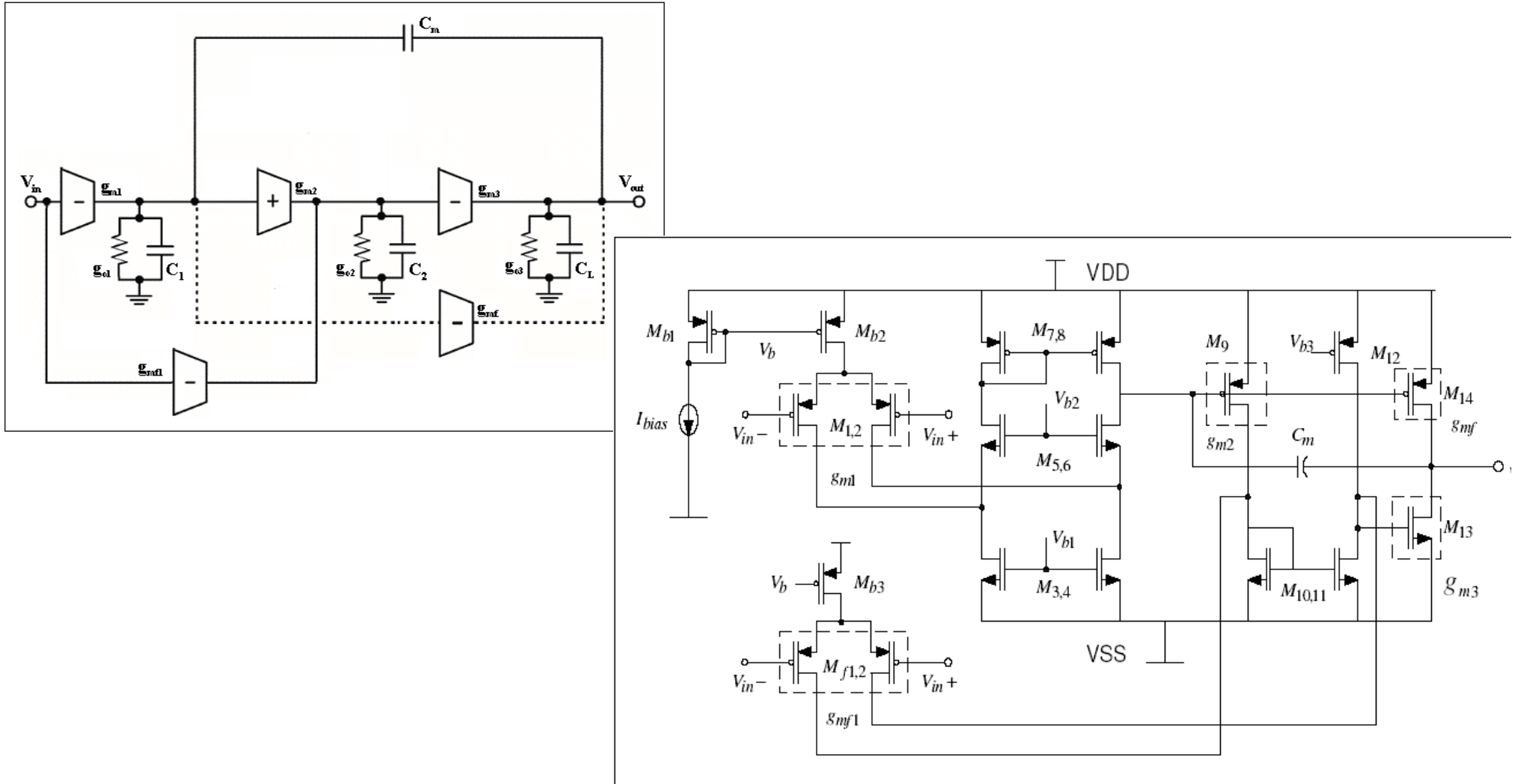


- The LHP zero is placed near the 2nd-pole
 - → a positive phase shift and compensates for the negative phase shift due to the non-dominant poles

ScaTech Opamp

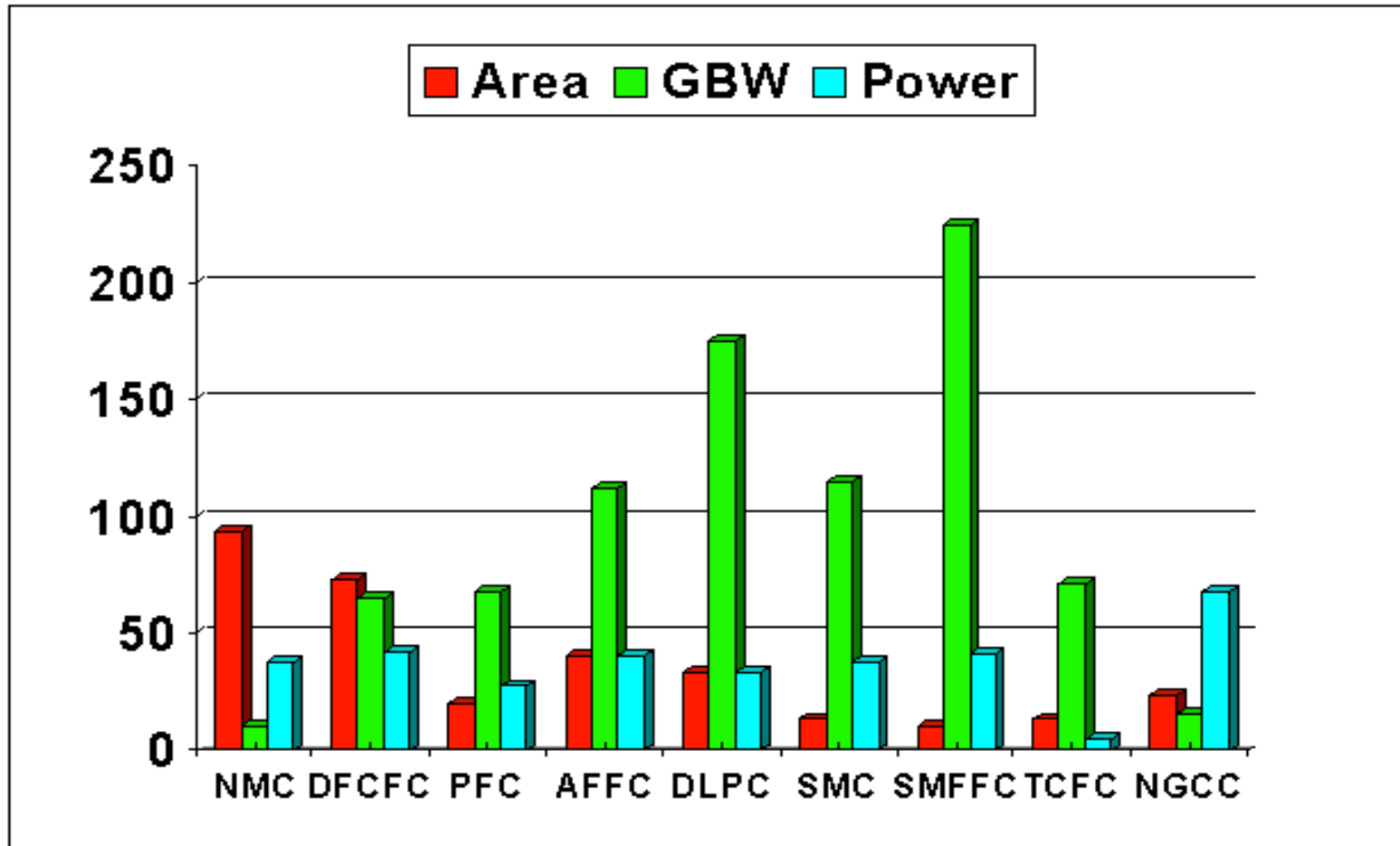
3-stage-opamp: Single Miller Cap FeedForward Compensation (SMFFC)

- Circuit implementation



ScalTech Opamp

3-stage-opamp: Final comparison



ScalTech Opamp

3-stage-opamp: Final comparison

<i>Parameter</i>	<i>NMC</i>	<i>DFCFC</i>	<i>PFC</i>	<i>AFFC</i>	<i>DLPC</i>	<i>SMC</i>	<i>SMFFC</i>	<i>TCFC</i>	<i>NGCC</i>
Load (pF/k Ω)	120/25	100/25	130/24	120/25	120/25	120/25	120/25	150/25	20/10
DC-gain (dB)	>100	>100	>100	>100	100	>100	>100	>100	>100
GBW (MHz)	0.4	2.6	2.7	4.5	7	4.6	9	2.85	0.61
Phase Margin	61°	43°	52°	65°	46°	57°	57°	58°	60°
Power (mW@Vdd)	0.38 @ 2	0.42 @ 2	0.275 @ 1.5	0.4 @ 2	0.33 @ 1.5	0.38 @ 2	0.41 @ 2	0.045 @ 1.5	0.68 @ 2
Cap (pF)	$C_m=88$ $C_{m2}=11$	$C_m=18$ $C_{m2}=3$	$C_m=15$ $C_{m2}=3$	$C_{m2}=3$ $C_a=7$	$C_a=4.8$ $C_b=2.5$	$C_m=7$	$C_m=4$	$C_m=1.1$ $C_{m2}=0.9$	-
Technology	0.8 μ m CMOS	0.8 μ m CMOS	0.35 μ m CMOS	0.8 μ m CMOS	0.6 μ m CMOS	0.5 μ m CMOS	0.5 μ m CMOS	0.35 μ m CMOS	0.8 μ m CMOS

ScalTech Opamp

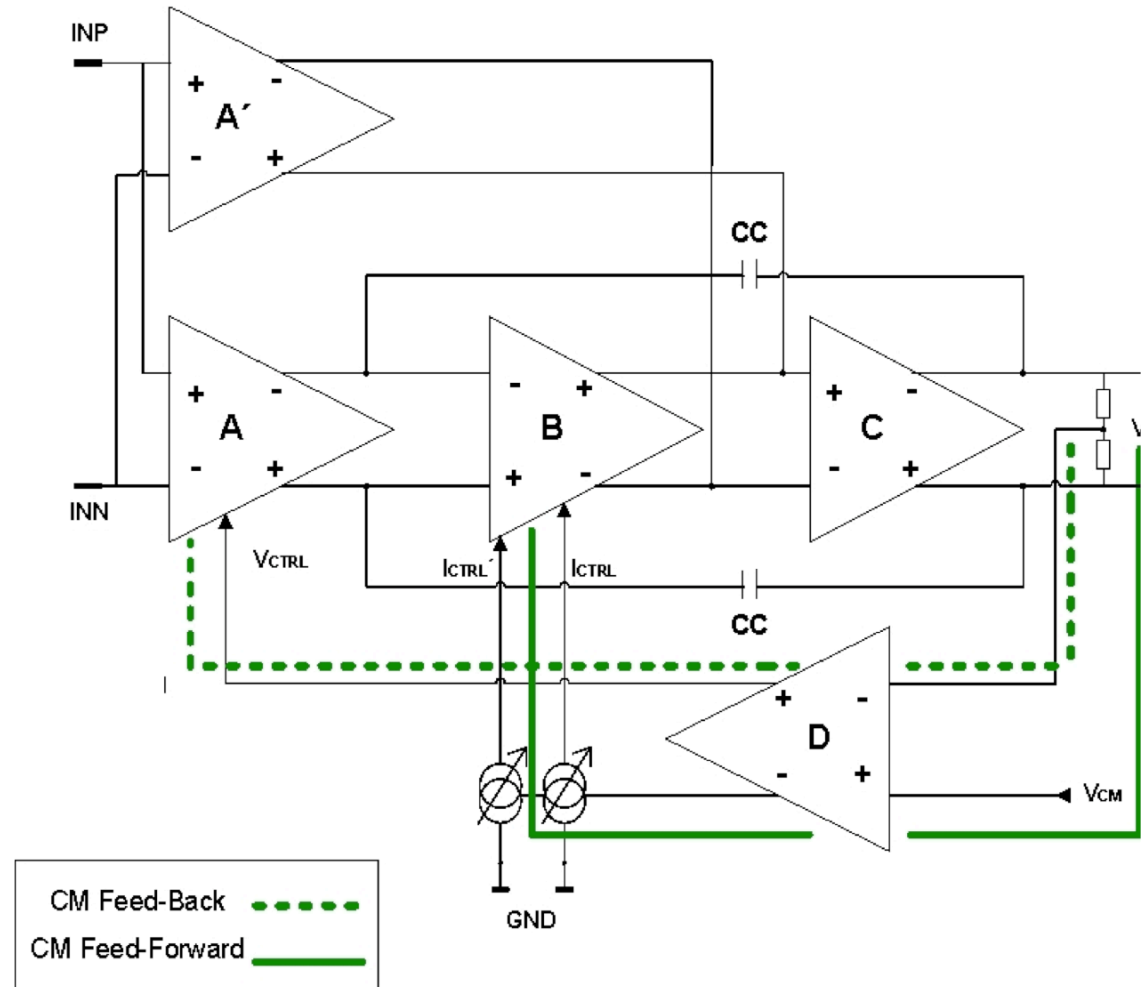
3-Stage-Opamp: Comparison in 65nm

	DC-gain (dB)	Gain Bandwidth (MHz)	Phase Margin (degree)	Power (no bias) (mW)	Area (gates+caps) (μm^2)	GBW/power (MHz/mW)
PFC	82	100	51	1.6	5577	62.5
TCFC	87	86	53	1.9	5543	45.3
SMFFC	91	179	72	2.3	3388	77.8

ScalTech Opamp Design

3-stage SMFFC opamp 65nm -prototype - Common-Mode Feedback Circuit *

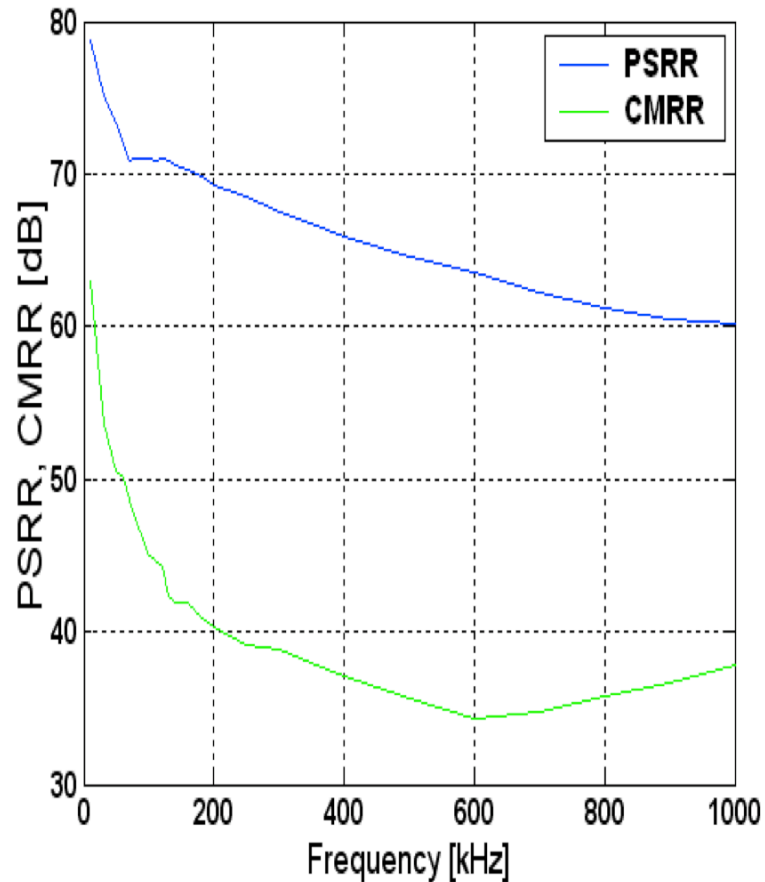
- The key point for compensation of the **fully-differential** mode is the use of a feedforward path through A'
- This path is not available for the **common-mode**-feedback circuits
 - → insufficient CM control circuit stability
- → A feed-forward path to a conventional Common-Mode Feed-Back (CMFB) amplifier
 - → to improve its stability and increase its bandwidth.



ScalTech Opamp Design

3-stage SMFFC opamp prototype

Experimental results



<i>Parameter</i>	<i>Performance</i>
Technology CMOS	65nm
Differential Gain/UGB	84dB / 200MHz
Common Mode Gain/UGB	85dB / 136MHz
PSRR@1MHz	60dB
CMRR@1MHz	38dB
HD3@5MHz	-82dBc
Output Noise@1MHz	27nV/ $\sqrt{\text{Hz}}$
Power Consumption	10mW

LV Analog Design in scaled CMOS technology

Outline

- Introduction
 - Basic CMOS operation
 - CMOS technology scaling trends
 - What is LV
 - LV Analog design
 - LV at transistor level
 - LV at circuit level
 - Current Mirror
 - Opamp design
 - Basic bandgap design ←←←
 - LV at system level
 - Active-RC filter design
 - Gm-C filter design
 - SC circuit design

LV Bandgap Reference Voltage

“Natural” Bandgap voltage

- Basic principle: a weighted combination can be temperature-independent

$$V_{BG} = V_{BE} + m \cdot V_T \cong 1.2V$$

- V_{BE} : temperature dependence $\cong -2.2 \text{ mV}/^\circ\text{C}$
- V_T : temperature dependence $\cong +0.086 \text{ mV}/^\circ\text{C}$.
- If $m \cong 25.6$
- $\rightarrow \text{TC} \cong 0$ for V_{REF} @ $T = 300 \text{ K}$

$$V_{BG} = V_{BE} + 25.6 \cdot V_T \cong 1.26 \text{ V}$$

(silicon band-gap)

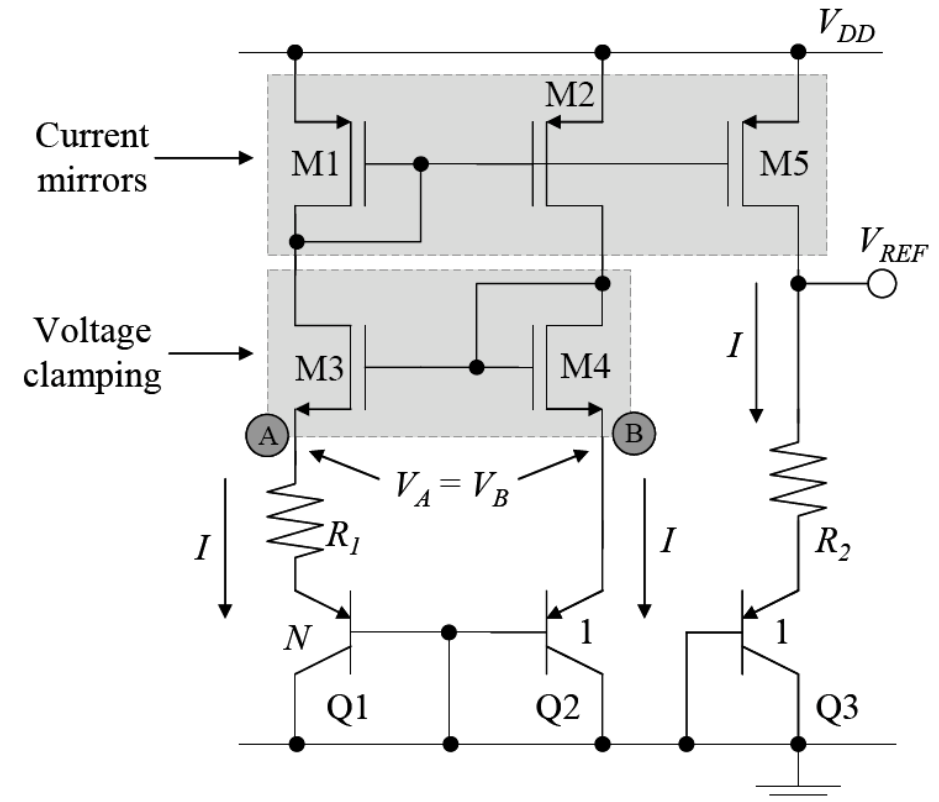
- \rightarrow cannot be used in scaled technology with $V_{DD} < 1.2V$
- A V_{BG} fraction is obtained (sustainable in low-voltage devices)

LV Bandgap Reference Voltage *

Basic implementation

- Use of parasitic vertical BJTs
- A voltage-clamping circuit composed of M4 and M5 forces $V_A = V_B$
- A proportional-to-absolute temperature (PTAT) current I is generated by Q1, Q2 and R_1
- Current mirrors (M1, M2, & M3) enforce branch currents equal

$$\rightarrow V_{REF} = V_{EB3} + (R_2 / R_1) \cdot \ln(N) \cdot V_T$$

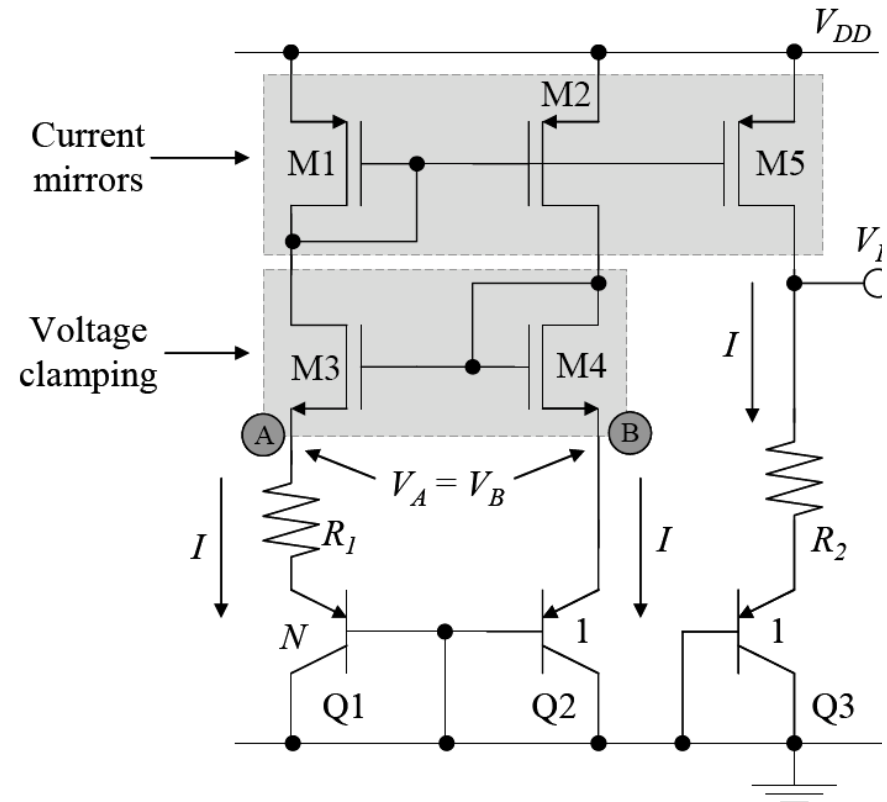


- A V_{REF} with low temperature coefficient (tempco) is obtained by optimizing temperature-independent circuit parameters R_2/R_1 and N

LV Bandgap Reference Voltage

LV limitation

- V_{DS1} is generated in an additional branch
- The current mirror and voltage-clamping circuit are not effective @ LV
- Long L reduces the channel-modulation effect
- If $V_{DS1} \neq V_{DS2}$ & $V_{GS3} \neq V_{GS4}$
 - $\rightarrow I_{D1} \neq I_{D2} \rightarrow$ error in the PTAT loop to generate an error contained V_{REF}
- Cascode current mirror reduces error,
 - but a higher V_{DD} is needed



LV Bandgap Reference Voltage

LV limitation

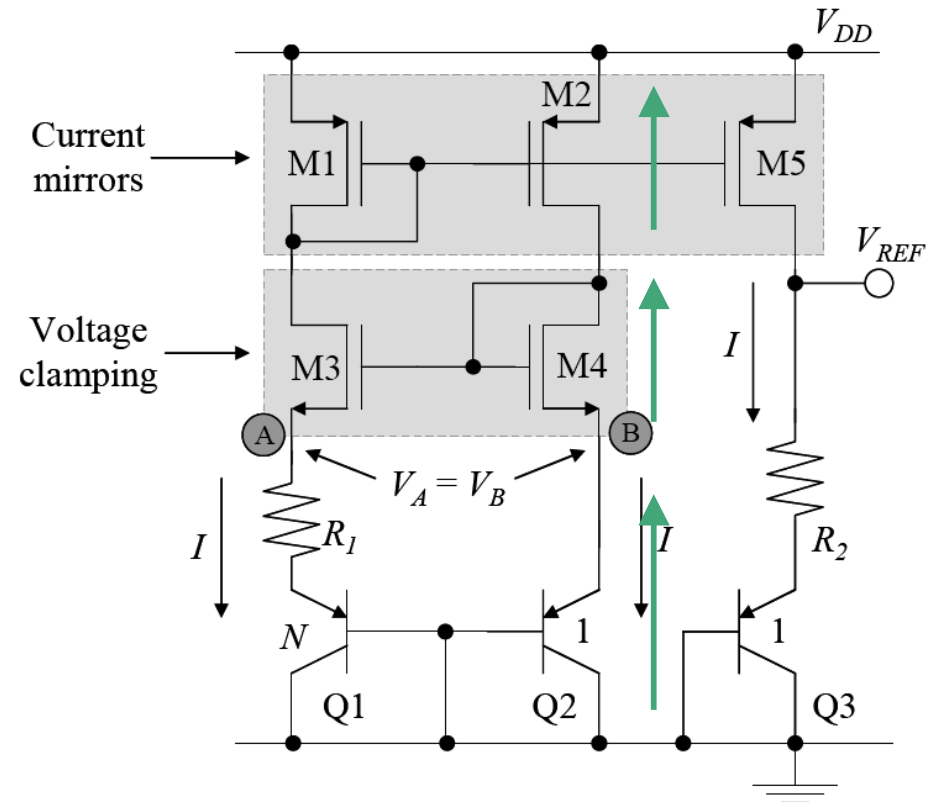
- V_{DDmin}

- For good CM gain

$$V_{DS1} = V_{DS2} = V_{TH} + V_{ov}$$

$$V_{DDmin} = V_{DS2} + V_{DS4} + V_{EB}$$

$$V_{DDmin} = 2 \cdot (V_{TH} + V_{ov}) + V_{EB}$$

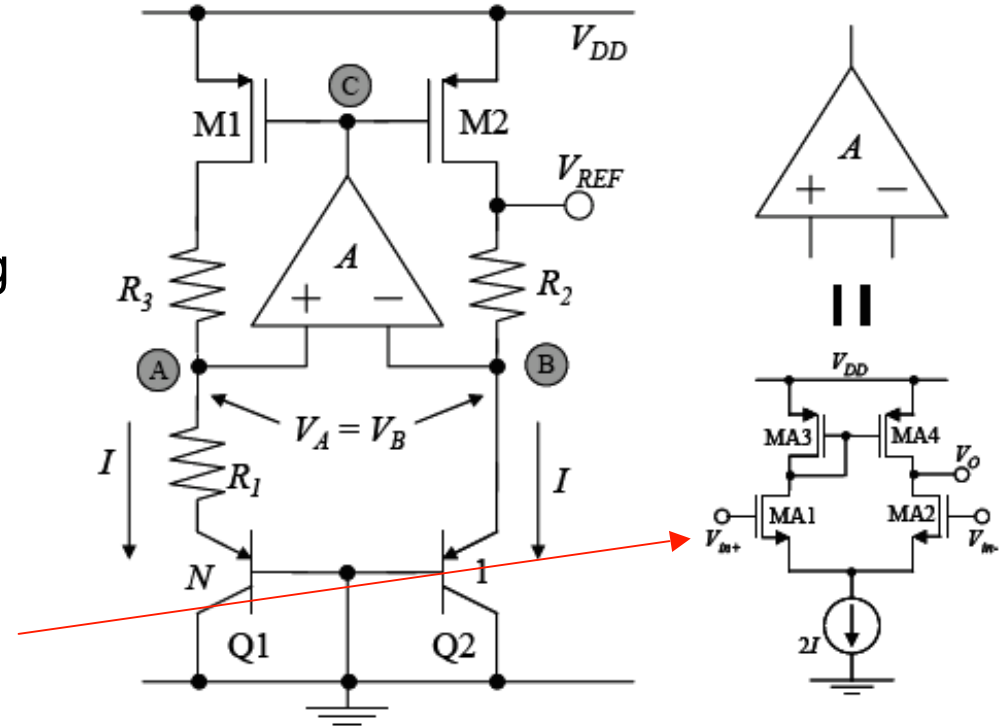


- Not used @ LV

LV Bandgap Reference Voltage

Error-Based current mirror

- Large error amplifier voltage gain A
 - $\rightarrow V_A = V_B$
- With $R_2 = R_3 \rightarrow V_{DS1} = V_{DS2}$
 - \rightarrow a very good current matching
- V_{REF} is generated by this structure without an extra current branch
- Power consumption (no extra branch) and CM errors can be reduced
- The error amplifier should be simple



- Only two pairs of matched devices to consider on the random offset voltage (V_{OFFR})
- With long-L devices, the bias current could be the generated PTAT current

LV Bandgap Reference Voltage

Error-Amplifier-Based current mirror

- Same size for MA3 and MA4 as M1 and M2.
 - → V_{DS} of MA3 and MA4 match to reduce the systematic offset voltage (V_{offS}) at different T

- A high-gain error amplifier difficult @ LV !
- A low gain gives $V_A \neq V_B$

$$V_{ERR} = V_A - V_B$$

$$V_{ERR} = V_{offR} + V_{offS} + V_{DD} / A$$

- It must be

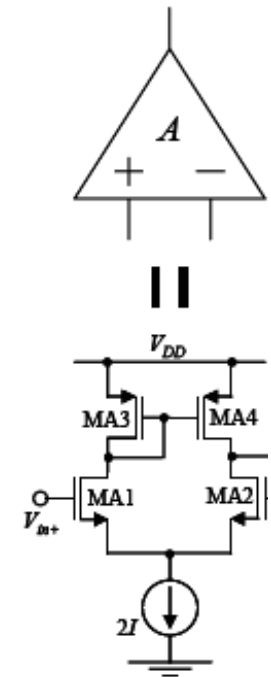
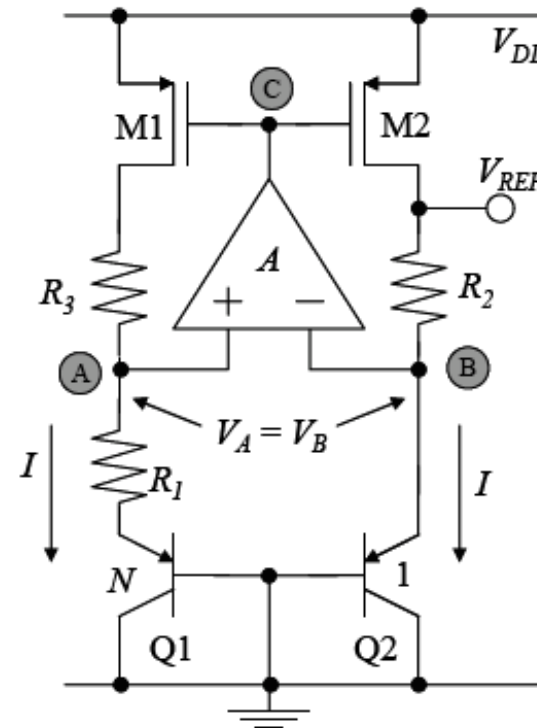
$$V_{ERR} \ll V_{EB2} - V_{EB1} = V_T \cdot \ln(N)$$

- → a large N is used

- The required A should be done at the lowest T to have the smallest $V_T \cdot \ln(N)$.

- V_{offR} & V_{offS} significant, ΔV_{REF} cannot be reduced by using a large A

- → Error-amplifier is designed for simplicity (good @ LV)



LV Bandgap Reference Voltage

Error-Amplifier-Based current mirror

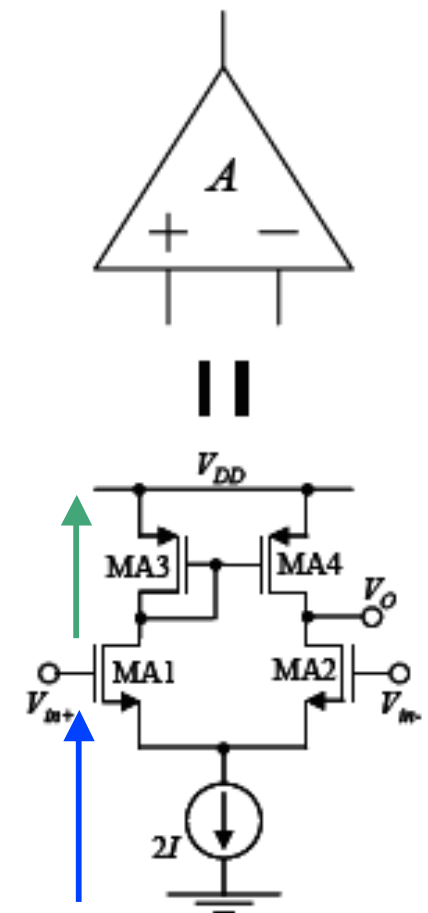
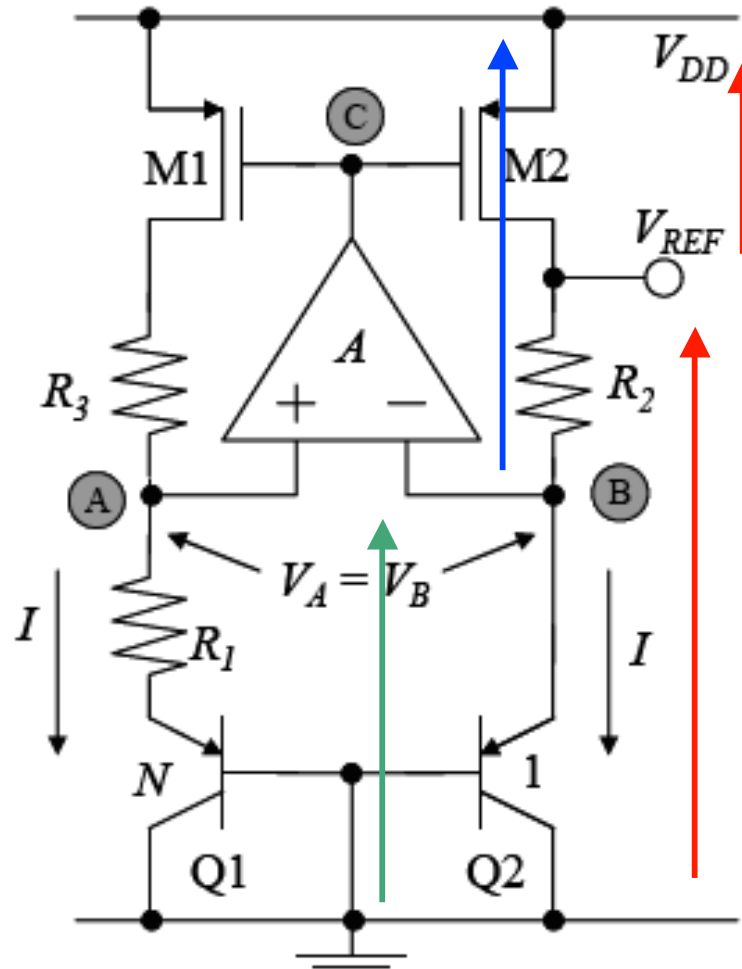
V_{DDmin}

$$V_{REF} + V_{DSsat} = V_{BG} + V_{ov}$$

$$V_{ov} + V_{TH} + V_{ov} + V_T \cdot \ln(N) \cdot (R_2/R_1) + V_{DSsat}$$

$$3 \cdot V_{ov} + V_{TH} + V_T \cdot \ln(N) \cdot (R_2/R_1)$$

$$V_{BE} + V_{ov}$$



LV Bandgap Reference Voltage

A CMOS Bandgap Reference with Sub-1-V Operation*

- The reference voltage is formed by two currents I_1 and I_2
- I_1 is a PTAT current

$$I_1 = V_T \cdot \ln(N) / R_1$$

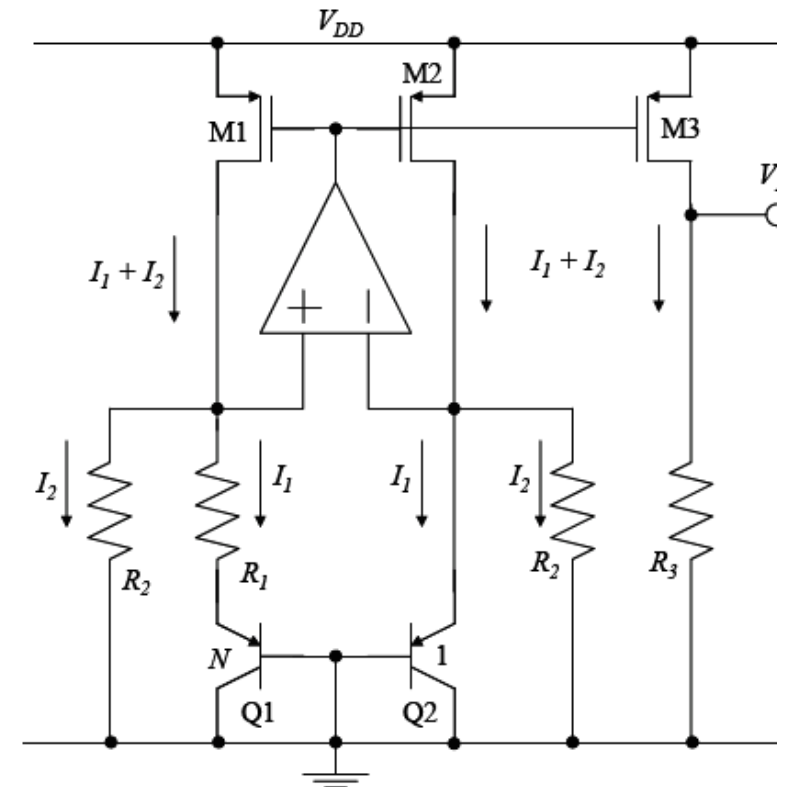
$$I_2 = V_{EB2} / R_2$$

$$V_{REF} = (I_1 + I_2) \cdot R_3$$

$$V_{REF} = \left(\frac{R_3}{R_2} \right) \cdot \left[V_{EB2} + \left(\frac{R_2}{R_1} \right) \cdot \ln(N) \cdot V_T \right]$$

- (R_2/R_1) & N reduces temperature dependence
- $R_3/R_2 < 1 \rightarrow V_{REF} < 1.2V$
 - $\rightarrow V_{REF}$ adjusted for different applications
- Ex.: $V_{REF} \approx 550mV$
 - $\rightarrow V_{DS1} = V_{DS2} \approx V_{DS3}$ for good current matching at different temperatures

ΣI



■ _____

* H. Banba, H. Shiga, A. Umezawa, T. Tanzawa, S. Atsumi and K. Sakui, "A CMOS Bandgap Reference Circuit with Sub-1-V Operation," *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 670-674, May 1999



LV Bandgap Reference Voltage

A CMOS Bandgap Reference with native device

- The bandgap uses native NMOSTs for the NMOS opamp input stage

- $V_{TH_nativeNMOS} < V_{EB}$ in the full operational temperature

- $\rightarrow V_{EB}$, (@ highest T i.e. lowest V_{EB}) is sufficiently high to turn on the opamp input stage

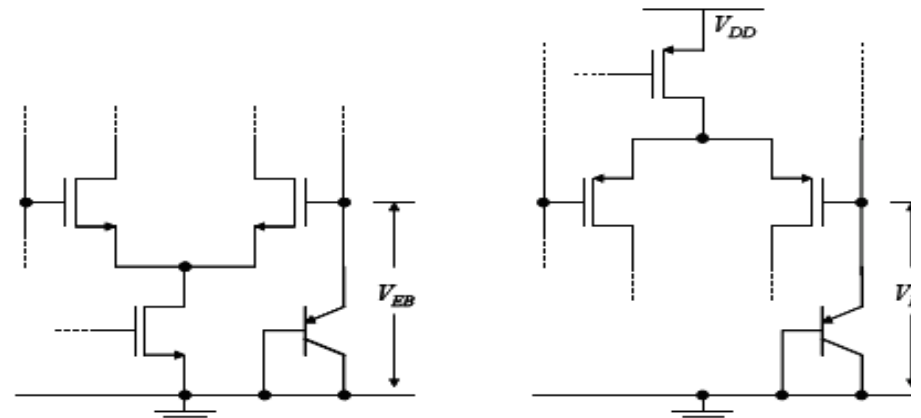
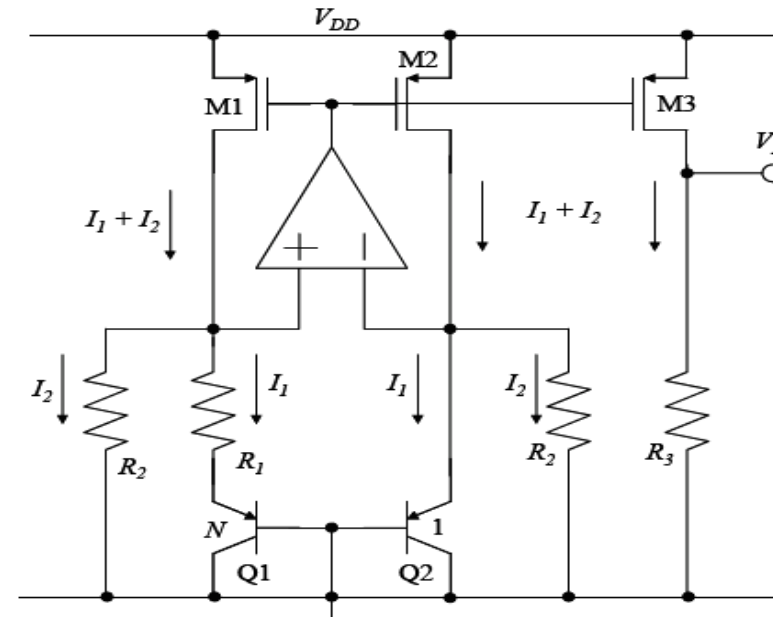
$$V_{EB} > V_{THN} + 2 \cdot V_{DS(sat)}$$

$$V_{DDmin} = V_{EB} + V_{DS(sat)} = V_{THN} + 3 \cdot V_{DS(sat)}$$

- A PMOS input stage

$$V_{DD(min)} = V_{EB} + |V_{THP}| + 2V_{SD(sat)}$$

- \rightarrow Low $|V_{THP}|$ is needed



LV Bandgap Reference Voltage

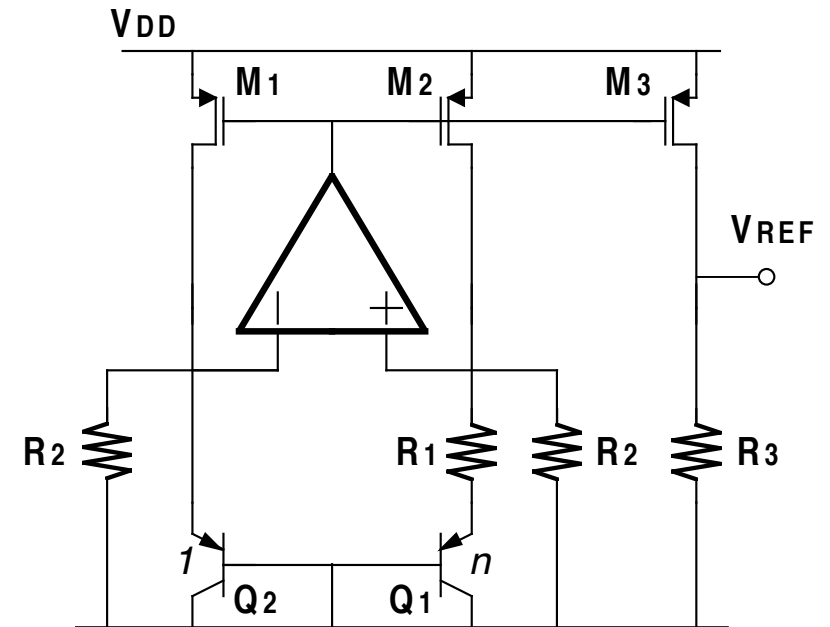
V_{DDmin}

$$I_1 = \frac{V_T \cdot \ln(N)}{R_1} + \frac{V_{BE}}{R_2}$$

- The output voltage is:

$$V_{ref} = I_1 \cdot R_3 = \frac{R_3}{R_1} \cdot \left[V_T \cdot \ln(N) + \frac{R_1}{R_2} \cdot V_{BE} \right]$$

- V_{DDmin} is limited by opamp operation



PMOS opamp input pair
 $V_{DDmin} = V_{BE} + V_{TH} + 2 \cdot V_{ov}$

NMOS opamp input pair
 $V_{DDmin} = \max\{V_{BE} + V_{ov}, V_{TH} + 3 \cdot V_{ov}\}$

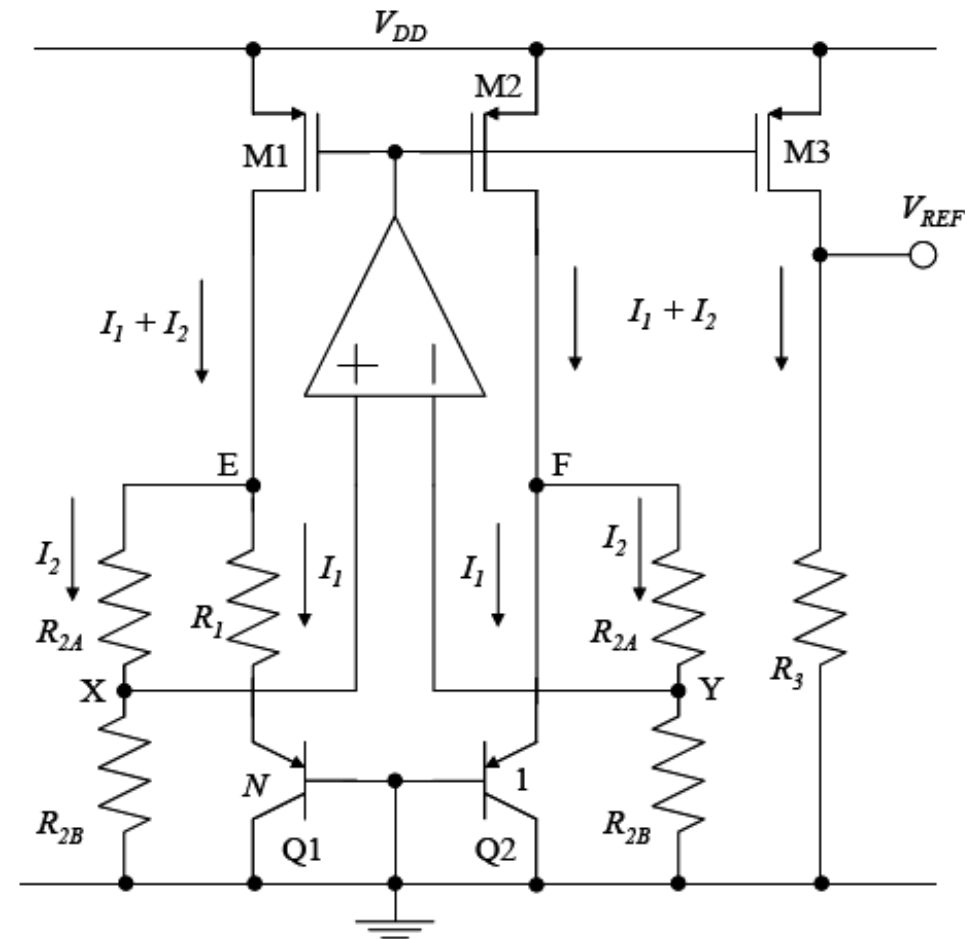
LV Bandgap Reference Voltage

A Sub-1-V CMOS Bandgap w/out Low V_{TH} Devices*

$\Sigma I + \text{Reduced } \Delta V$

- Resistive voltage divider
- Voltages at E and F are not enforced directly
- Voltages at X and Y are enforced to be equal.
- The resistances at the two current branches are set to be equal
 - → the voltages at E and F are equal

$$V_X = V_Y = \left(\frac{R_{2B}}{R_{2A} + R_{2B}} \right) \cdot V_{EB2}$$



■ _____

* K.N. Leung and P.K.T. Mok, "A Sub-1-V 15-ppm/°C CMOS Bandgap Voltage Reference without Requiring Low Threshold Voltage Device," *IEEE Journal of Solid-State Circuits*, vol.37, pp.526-530, Apr.

LV Bandgap Reference Voltage

A Sub-1-V CMOS Bandgap w/out Low V_{TH} Devices

$$V_X = V_Y = \left(\frac{R_{2B}}{R_{2A} + R_{2B}} \right) \cdot V_{EB2}$$

- → A PMOS error amplifier input stage
- 😊 V_{DDmin} lowers (limited by the input stage of the voltage-mode error amplifier)

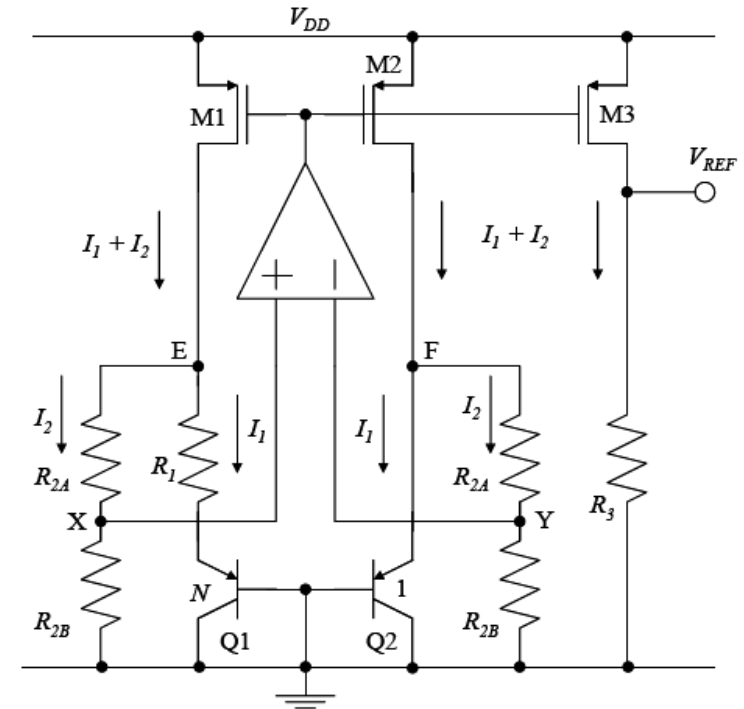
$$V_{REF} = \left(\frac{R_3}{R_2} \right) \cdot \left[V_{EB2} + \left(\frac{R_2}{R_1} \right) \ln(N) \cdot V_T \right]$$

- ☹️ The amplified effect of the offset voltage (V_{OFF}) due to the error amplifier.

$$V_{REF} = \left(\frac{R_3}{R_2} \right) \cdot \left\{ V_{EB2} + \left(\frac{R_2}{R_1} \right) \cdot [\ln(N) \cdot V_T + V_{ERR1}] \right\}$$

$$V_{ERR1} = [(R_{2A} + R_{2B})/R_{2A}] \cdot V_{OFF} > V_{OFF}$$

- This is reduced by using a large value of N ($N=64$)



LV Bandgap Reference Voltage

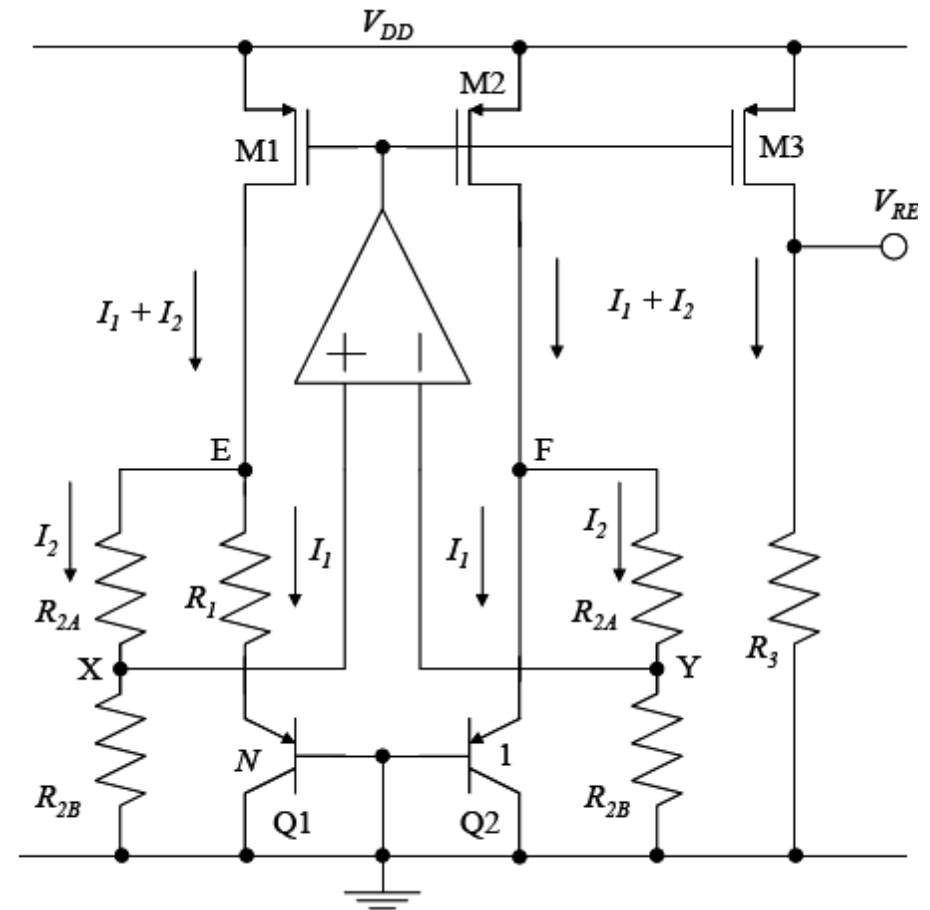
A Sub-1-V CMOS Bandgap w/out Low V_{TH} Devices

- The bulk-source junctions of M_1 - M_3 are forward-biased

- $\rightarrow |V_{THP}|$ is reduced

- The forward bias voltage is set to about 0.3V at the highest operational temperature

- \rightarrow the p-n junction of the p-substrate and N-well will not be turned on.
- \rightarrow the error amplifier can operate in its high-gain output region to enforce voltages at nodes X and F more closely



LV Analog Design in scaled CMOS technology

Outline

- Introduction
 - Basic CMOS operation
 - CMOS technology scaling trends
 - What is LV
 - LV Analog design
 - LV at transistor level
 - LV at circuit level
 - Current mirror
 - Opamp design
 - Basic bandgap design
 - LV at system level
 - Active-RC filter design ←←←
 - Gm-C filter design
 - SC circuit design

Analog filter in ScalTech

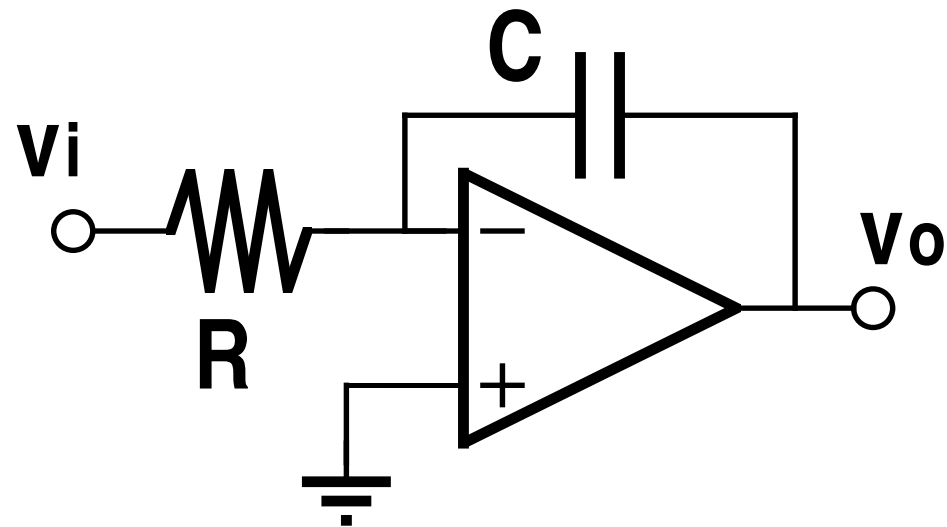
Introduction

- Scal tech device performance
 - Lower $V_{DD}-V_{TH}$ distance
 - Difficult bias point
 - Lower Finite gain
 - Lower frequency response accuracy
 - Lower linear range (in closed loop structures)
 - Higher device f_T
 - Larger filter bandwidth

LV Active-RC filter

Introduction

- Active-RC filters are widely used in several applications (like telecom systems)
- Closed loop structure
- Advantages
 - High-linearity
 - No opamp input swing
 - Rail-to-rail output swing
 - Parasitic insensitivity
- Disadvantages
 - Large bandwidth opamp



LV Active-RC filter

LV for Closed Loop Structure

- To maximize output swing, $V_{out} = V_{DD}/2$
Without any level shift (I_o & R_B), for cell coupling

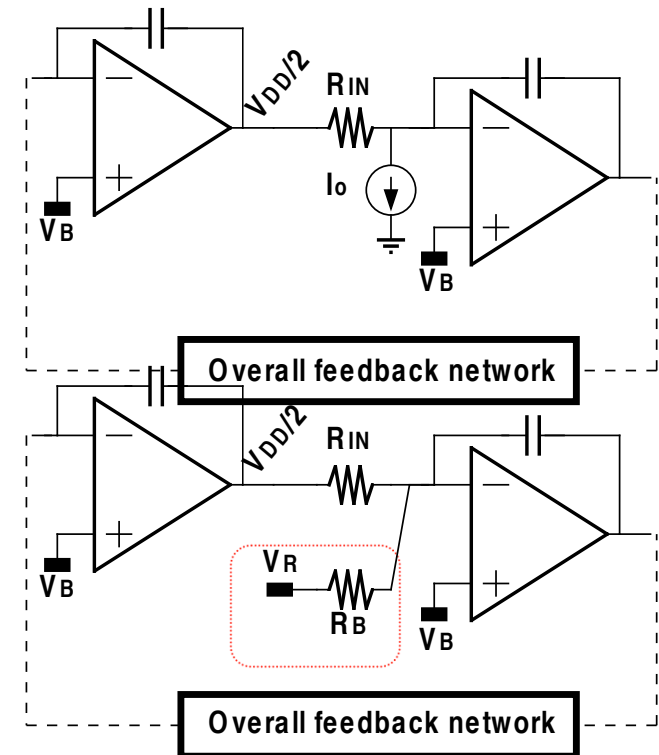
$$V_i = V_o = V_{DD}/2$$

$$V_{DDmin} = V_{sw} + V_{TH} + 3 \cdot V_{ov}$$

- A V_{DDmin} reduction is obtained with a level shift from the output to the input
- the input stage is optimized by biasing $V_b = V_{ov}$ (required by the I_o)
- the optimum value for the current I_o to set $V_{out_DC} = V_{DD}/2$ is given by:

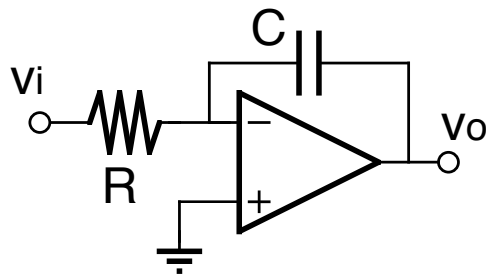
$$I_o = \frac{V_{DD}/2 - V_b}{R_i}$$

$$V_{DDmin} = (V_{TH} + 2 \cdot V_{ov}) + V_b = (V_{TH} + 2 \cdot V_{ov}) + V_{ov} = V_{TH} + 3 \cdot V_{ov}$$

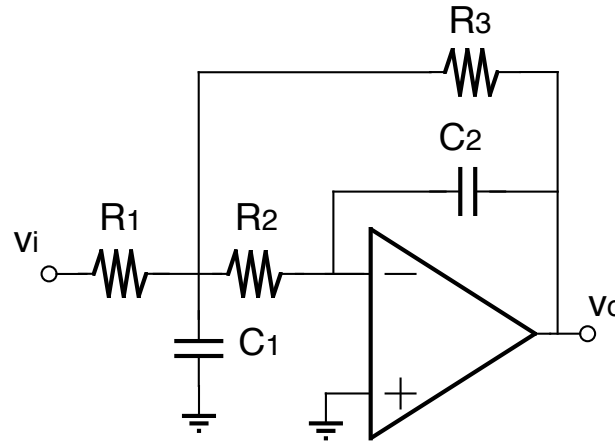


LV Active-RC filter

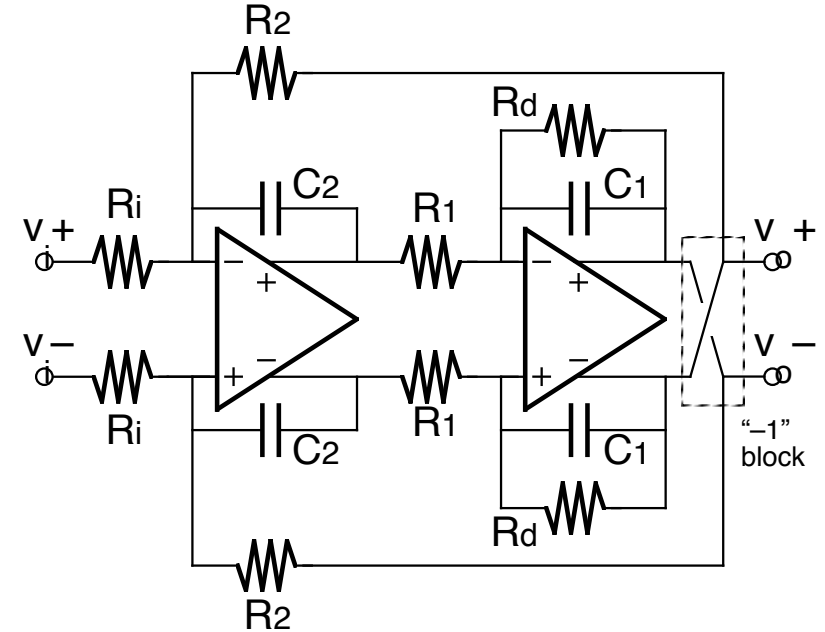
Typical Active-RC structures



1st order



2nd order – Rauch cell
One opamp for two poles



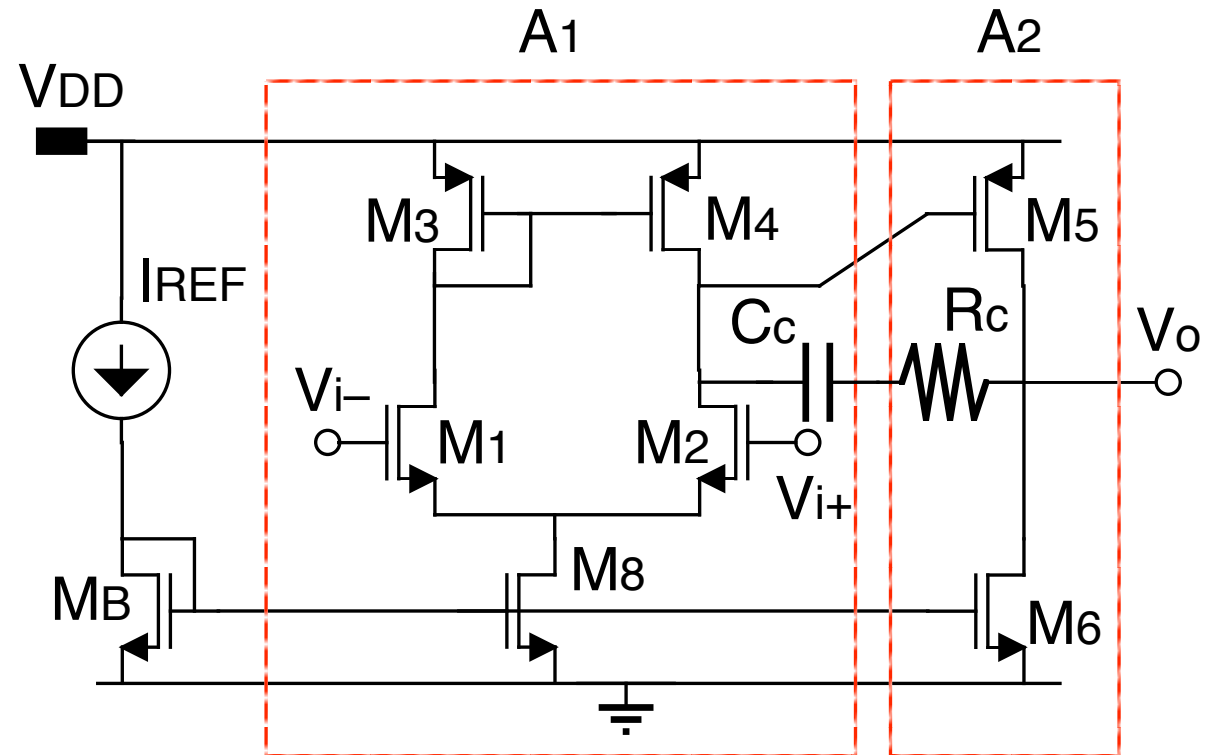
2nd order – Two-opamp biquad cell

- Opamp design is a critical issue
- Trade-off power-performance @ LV

LV Active-RC filter

Two-Stage Opamp Design

- The 1st (input) stage is designed to fit bandwidth and noise performance
- The 2nd (output) stage is designed to drive the output resistive and capacitive load



- A LV class-AB output stage could be eventually used to reduce distortion due to class-A current limitation

LV Active-RC filter

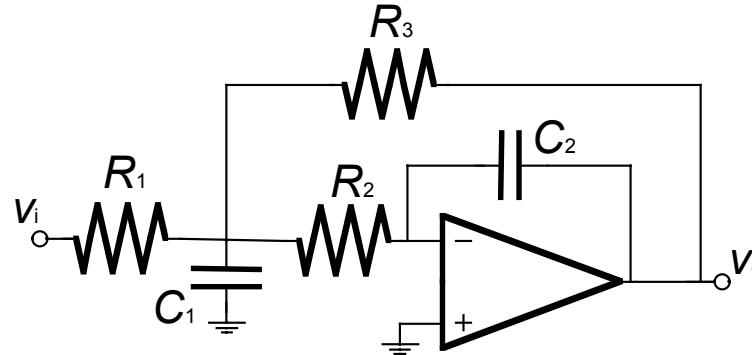
Low-voltage issues

- Technology scaling gives
 - V_{DD} reduction
 - Reduced $V_{DD} - V_{TH}$ distance
- In the opamp design V_{DD} scaling gives:
 - No cascode → Lower gain-per-stage
 - Cascade → Stability issue vs. area (caps do not scale with technology)
 - New solutions for large bandwidth (in small area)
 - Multi-stage opamp stability
 - Increased power consumption
 - → Power reduction techniques
 - Noise optimization
 - Using low-UGB Opamp (Active-Gm-RC)

LV Active-RC filter

Rauch Biquadratic cell: Lowpass Frequency Response

- Rauch cell is used as benchmark



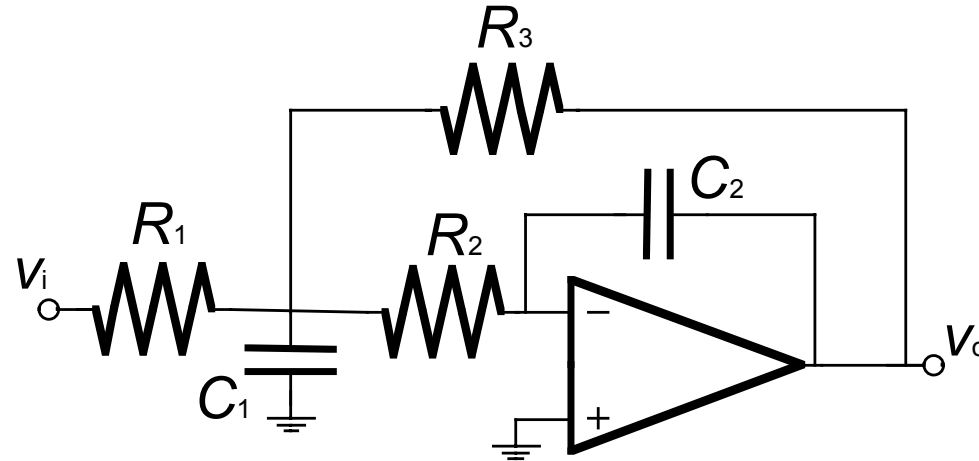
$$H(s) = - \frac{1}{s^2 \cdot R_1 \cdot R_2 \cdot C_1 \cdot C_2 + s \cdot C_2 \cdot \left(R_1 + R_2 + \frac{R_1 \cdot R_2}{R_3} \right) + \frac{R_1}{R_3}}$$

$$Q = \sqrt{\frac{C_1}{C_2}} \cdot \frac{R_1 \cdot \sqrt{R_2 \cdot R_3}}{R_1 \cdot (R_2 + R_3) + R_2 \cdot R_3} \quad G = \frac{R_3}{R_1} \quad f_0 = \frac{1}{2 \cdot \pi} \cdot \frac{1}{\sqrt{R_2 \cdot R_3 \cdot C_1 \cdot C_2}}$$

- The transfer function is sensitive to any parasitic capacitance in parallel at C_1

LV Active-RC filter

Rauch Biquadratic cell: Lowpass Frequency Response



- Noise performance

$$\overline{V_{n_out}^2} = 4 \cdot k \cdot T \cdot R_1 \cdot \left(\frac{R_3}{R_1}\right)^2 + 4 \cdot k \cdot T \cdot R_2 \cdot \left(1 + \frac{R_3}{R_1}\right)^2 + 4 \cdot k \cdot T \cdot R_3 + \overline{V_{n_opamp}^2} \cdot \left(1 + \frac{R_3}{R_1}\right)^2$$

- Linearity performance
 - Good linearity for closed loop configuration
 - For out-of-band signals (blockers) a R_1 - C_1 prefilter increases out-of-band linearity

LV Active-RC filter

Low-Voltage Opamp points

- Bias circuits
 - → Active-RC filters are dc-coupled

Question 1 → What is V_{DDmin} ?

- Signal processing
 - Frequency response synthesis and accuracy

Question 2 → Which specs for the opamp ?

- Power reduction
 - → Noise optimization design approach

Question 3 → Noise-oriented design approach ?

- → Limited opamp bandwidth structure

Question 4 → Novel filter structure ?

LV Active-RC filter

Question 1 → What is V_{DDmin} ? - Bias Point Design

- To maximize output swing (rail-to-rail)

$$V_{o_DC} = V_{DD}/2$$

- To have a dc-coupling between cells

$$V_{i_DC} = V_{o_DC} = V_{DD}/2$$

- To balance dc-currents

$$V_{ioa_DC} = V_{i_DC} = V_{o_DC} = V_{DD}/2$$

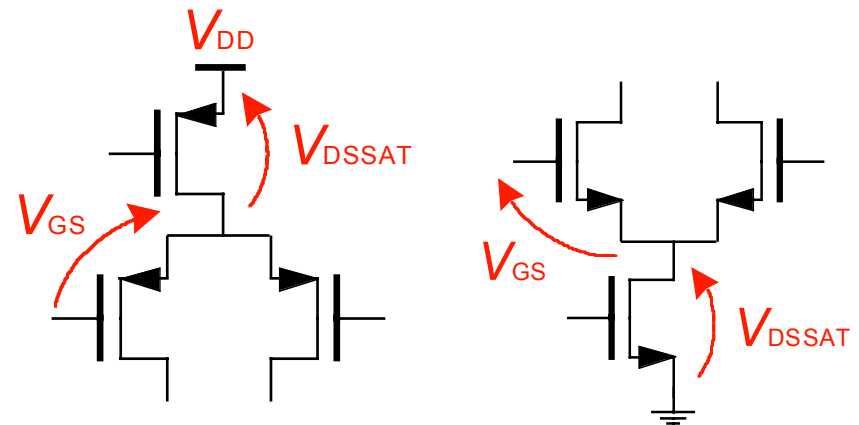
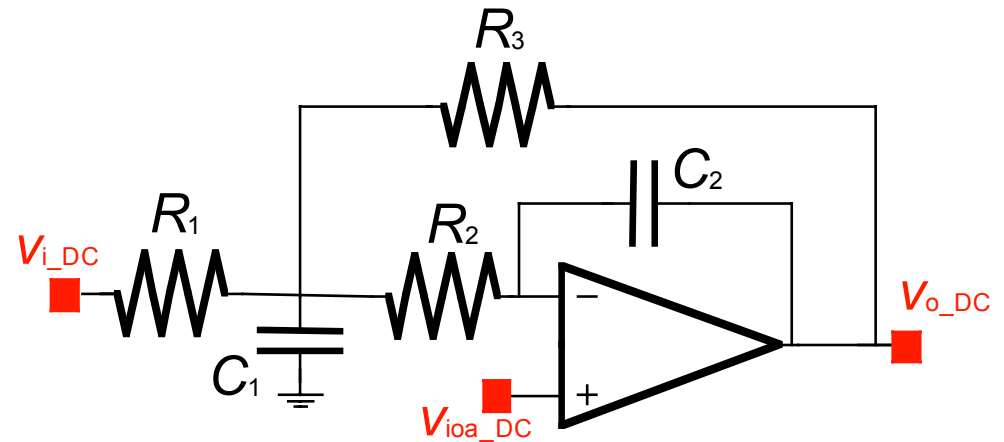
- To bias PMOS input pair

$$V_{ioa_DC} = V_{DD} - (V_{GS_inputpair} + V_{DSsat}) = V_{DD}/2$$

- The minimum V_{DDmin} results

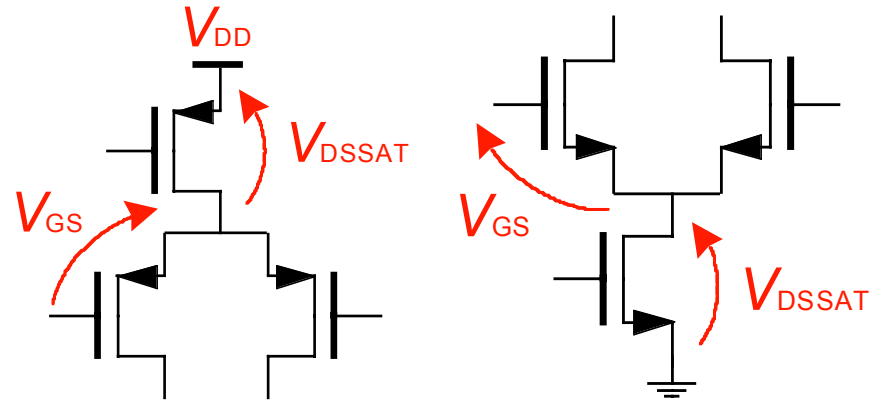
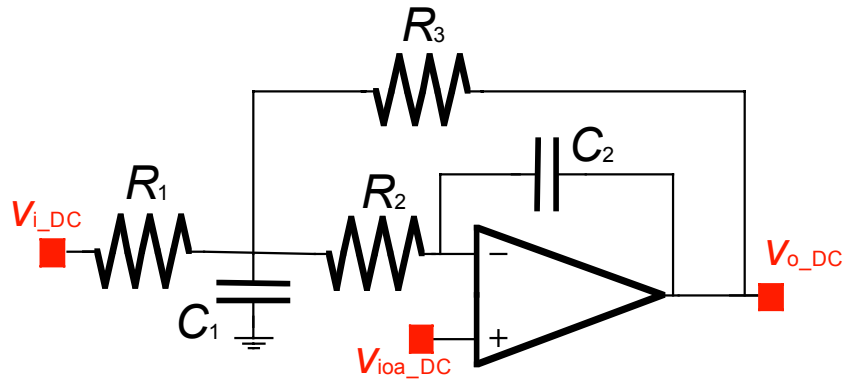
$$V_{DDmin} = 2 \cdot V_{ioa_DC} = 2 \cdot (V_{GS_inputpair} + V_{DSsat})$$

- Valid also for NMOS input pair



LV Active-RC filter

Question 1 → What is V_{DDmin} ? - Bias Point Design



- The minimum V_{DDmin} results

$$V_{DDmin} = 2 \cdot V_{ioa_DC} = 2 \cdot (V_{GS_inputpair} + V_{DSsat})$$

$$V_{DDmin} = 2 \cdot V_{TH} + 4 \cdot V_{ov}$$

- Example:
- $V_{TH} = 0.35V$
- $V_{ov} = 0.1 V$
- → $V_{DDmin} = 1.1V$

$$V_{DSsat} \approx V_{ov}$$

LV Active-RC filter

Question 1 → What is V_{DDmin} ? - Bias Point Design

- I_1 reduces V_{DDmin}

$$I_1 = \frac{V_{i_DC} - V_{ioa_DC}}{R_1} + \frac{V_{o_DC} - V_{ioa_DC}}{R_3}$$

$$I_1 = \frac{V_{DD}/2 - V_{ov}}{R_1} + \frac{V_{DD}/2 - V_{ov}}{R_3}$$

$$I_1 = (V_{DD}/2 - V_{ov}) \cdot \left(\frac{1}{R_1} + \frac{1}{R_3} \right)$$

- → $V_{DDmin} = V_{ov} + V_{GS_inputpair} + V_{DSSat}$

$$V_{DDmin} = V_{TH} + 3 \cdot V_{ov} \ll 2 \cdot V_{TH} + 4 \cdot V_{ov}$$

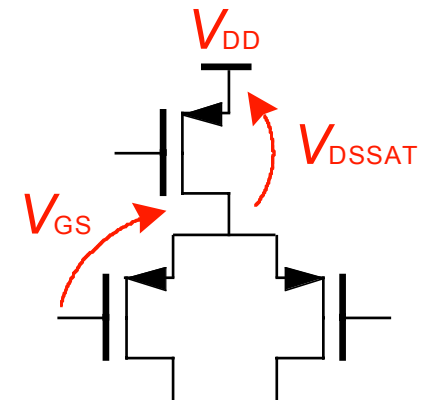
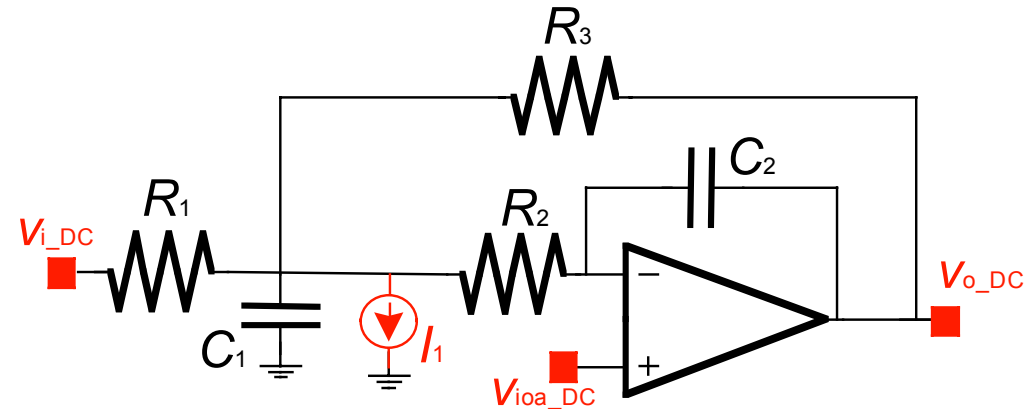
- Example:

- $V_{TH} = 0.35V$

- $V_{ov} = 0.1V$

- → $V_{DDmin} = 0.65V \ll 1.1V$

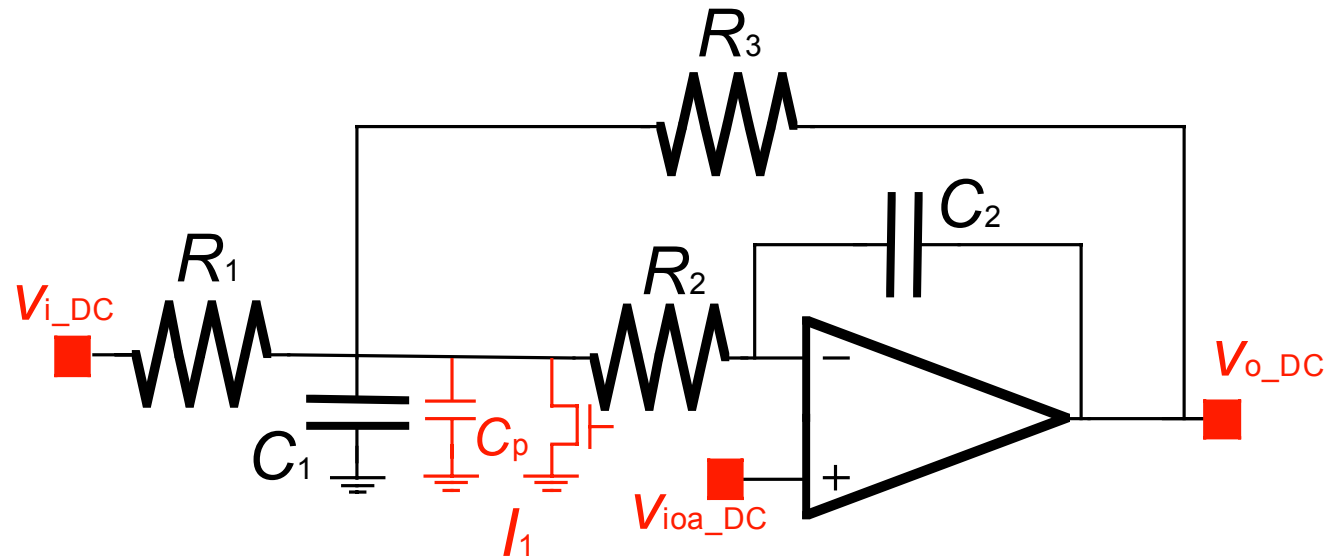
- → A 600mV xDSL filter



LV Active-RC filter

Question 1 → What is V_{DDmin} ? - Bias Point Design

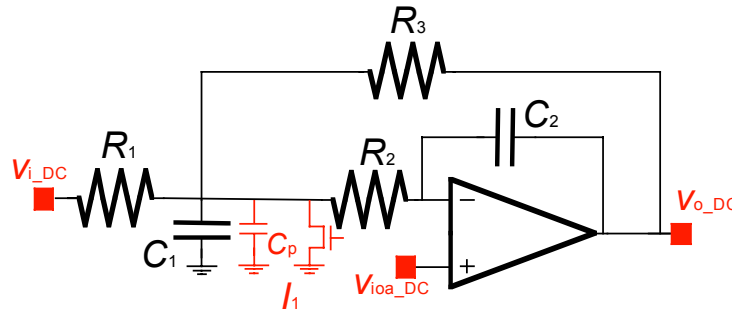
$$V_{DDmin} = V_{TH} + 3 \cdot V_{ov}$$



- Inserting I_1
 - reduces V_{DDmin}
- BUT
 - Increases noises
 - Reduces DR !!
 - Increases parasitic capacitance sensitivity

LV Active-RC filter

Question 1 → What is V_{DDmin} ? - Bias Point Design



- Noise performance

$$\overline{i_{n1}^2} = \frac{2}{3} \cdot 4 \cdot k \cdot T \cdot g_m = \frac{2}{3} \cdot 4 \cdot k \cdot T \cdot \frac{2 \cdot I_1}{V_{ov}}$$

$$\boxed{V_{n_I1_out}^2} = \overline{i_{n1}^2} \cdot R_3^2 = \left(\frac{2}{3} \cdot 4 \cdot k \cdot T \cdot \frac{2 \cdot I_1}{V_{ov}} \right) \cdot R_3^2 < \boxed{V_{nR_out}^2}$$

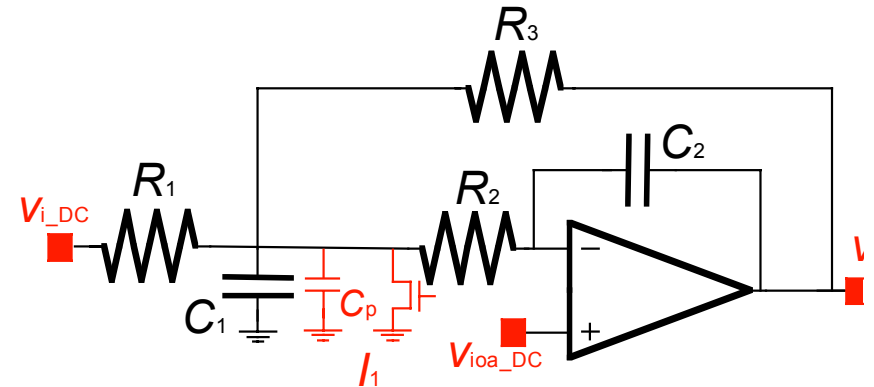
$$V_{ov} > \frac{4}{3} \cdot \frac{V_{DD}/2}{\frac{7}{3} + \frac{R_2}{R_3} \cdot \frac{1+G^2}{1+G}}$$

- Ex.: $V_{DD} = 1.2V$, $G=1$, $R_2=R_3$, → $V_{ov} > 0.185V$

LV Active-RC filter

Question 1 → What is V_{DDmin} ? - Bias Point Design

- Reducing V_{ov} requires to reduce $V_{nR_out}^2 \rightarrow$ reducing R's
- Larger power consumption to drive R's
- Larger I_1 to perform the same ($V_{DD}/2 - V_{ioa}$)
- Larger I_1 device
- Larger parasitic capacitance in parallel to C_1



$$H(s) = - \frac{1}{s^2 \cdot R_1 \cdot R_2 \cdot (C_1 + C_p) \cdot C_2 + s \cdot C_2 \cdot \left(R_1 + R_2 + \frac{R_1 \cdot R_2}{R_3} \right) + \frac{R_1}{R_3}}$$

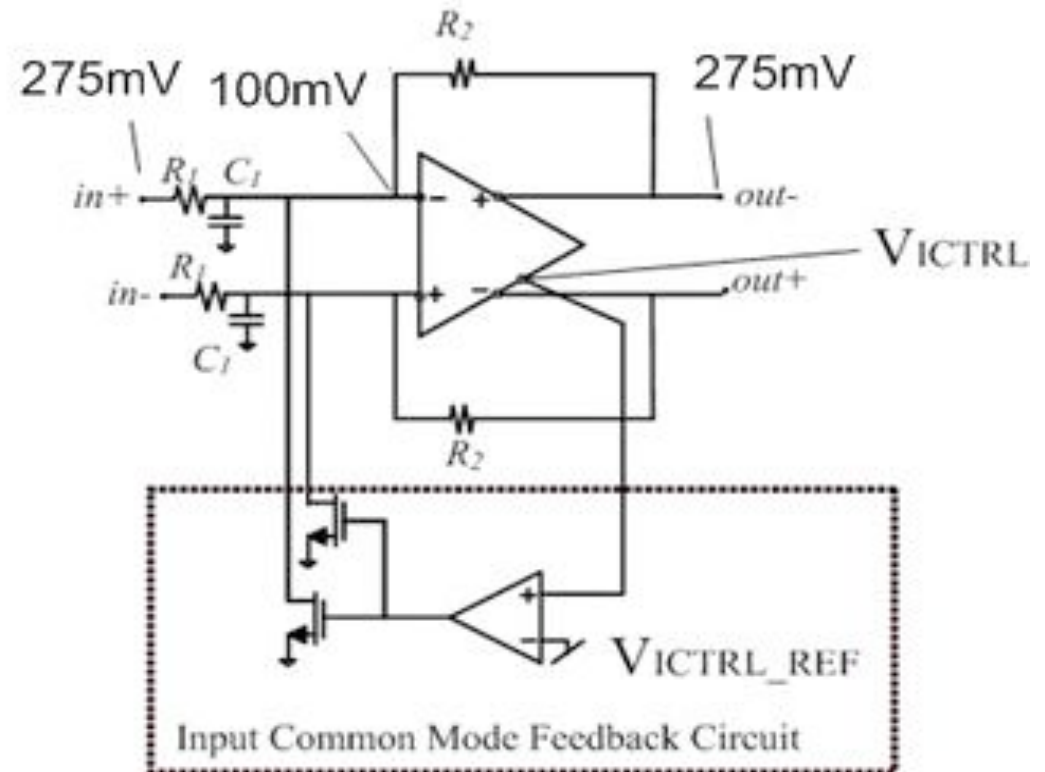
- Frequency response inaccuracy

LV Active-RC filter

Question 1 → What is V_{DDmin} ? - Low-voltage Design: Experimental results*

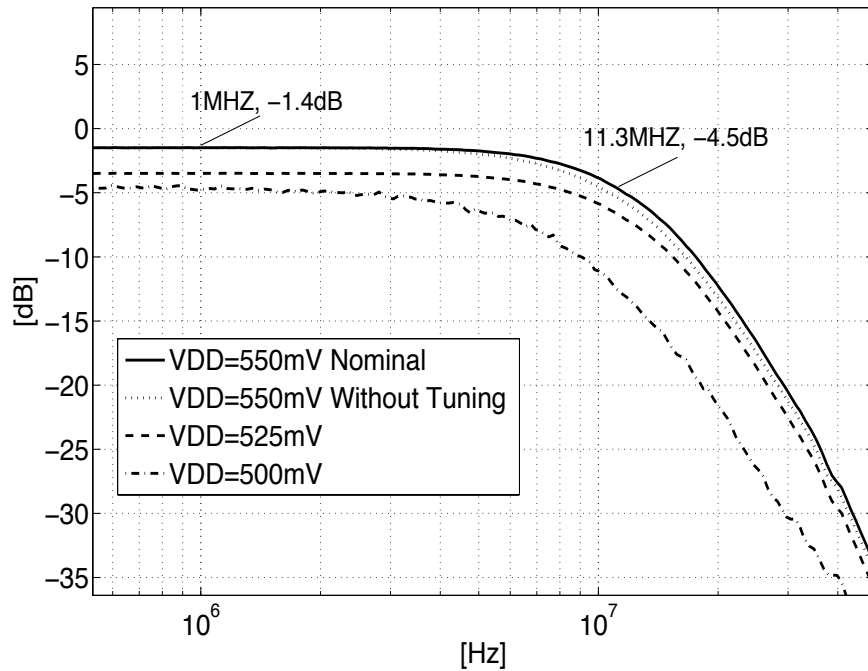
- WLAN Receivers baseband filter design

	Cell 1	Cell2
Ω_o [Mrad/s]	$2\pi \cdot 12$	$2\pi \cdot 12$
G [dB]	0	0
$R_1 = R_2$ [k Ω]	2.3	2.3
C_1 [pF]	15.5	3
C_c [pF]	14.1	15.5

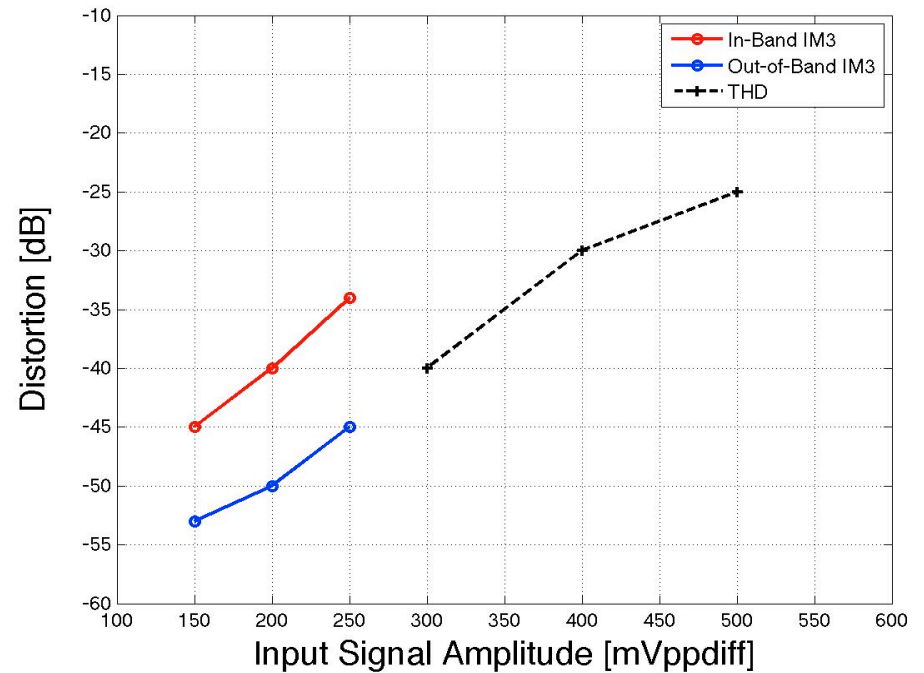


LV Active-RC filter

Question 1 → What is V_{DDmin} ? - Low-voltage Design: Experimental results



Filter transfer function vs. V_{DD}



Linearity (THD&IM3) vs. Input signal amplitude

LV Active-RC filter

Question 1 → What is V_{DDmin} ? - Low-voltage Design: Experimental results

Filter Performance Summary

	This design	D'Amico
V_{DD}	0.55 V	1.2
CMOS Technology	0.13 μm	0.13 μm
V_{TH}	300 mV	300mV
Current Cons.	5.8 mA	-
Power Consumption	3.5 mW	14.2 mW
Filter Order	4 th	4 th
G	0 dB	4 dB
f_{-3dB}	11.3 MHz	10 MHz
In-band IIP3	8 dBm	21dBm
Out-of-Band IIP3	13.3dBm	-
Noise	110 μV_{rms}	36 μV_{rms}
DR (THD=-40dB)	60 dB	81 dB

LV Active-RC filter

Question 2 → Which specs for the opamp ? - Transfer function Sensitivity

- Ideal opamp: zero output impedance

$$H(s) = -\frac{1}{s^2 \cdot \left[R_1 \cdot R_2 \cdot C_1 \cdot C_2 \cdot \left(1 + \frac{1}{A} \right) \right] + s \cdot \left[C_2 \cdot \left(R_1 + R_2 + \frac{R_1 \cdot R_2}{R_3} \right) + \frac{1}{A} \cdot \left((C_1 + C_2) \cdot R_1 + C_2 \cdot R_2 + C_2 \cdot \frac{R_1 \cdot R_2}{R_3} \right) \right] + \left[\frac{R_1}{R_3} + \frac{1}{A} \cdot \left(1 + \frac{R_1}{R_3} \right) \right]}$$

- Opamp specs (“Rule-of-Thumbs”)
- Opamp Finite Gain

$$A_o \approx (50 \approx 100) \cdot Q$$

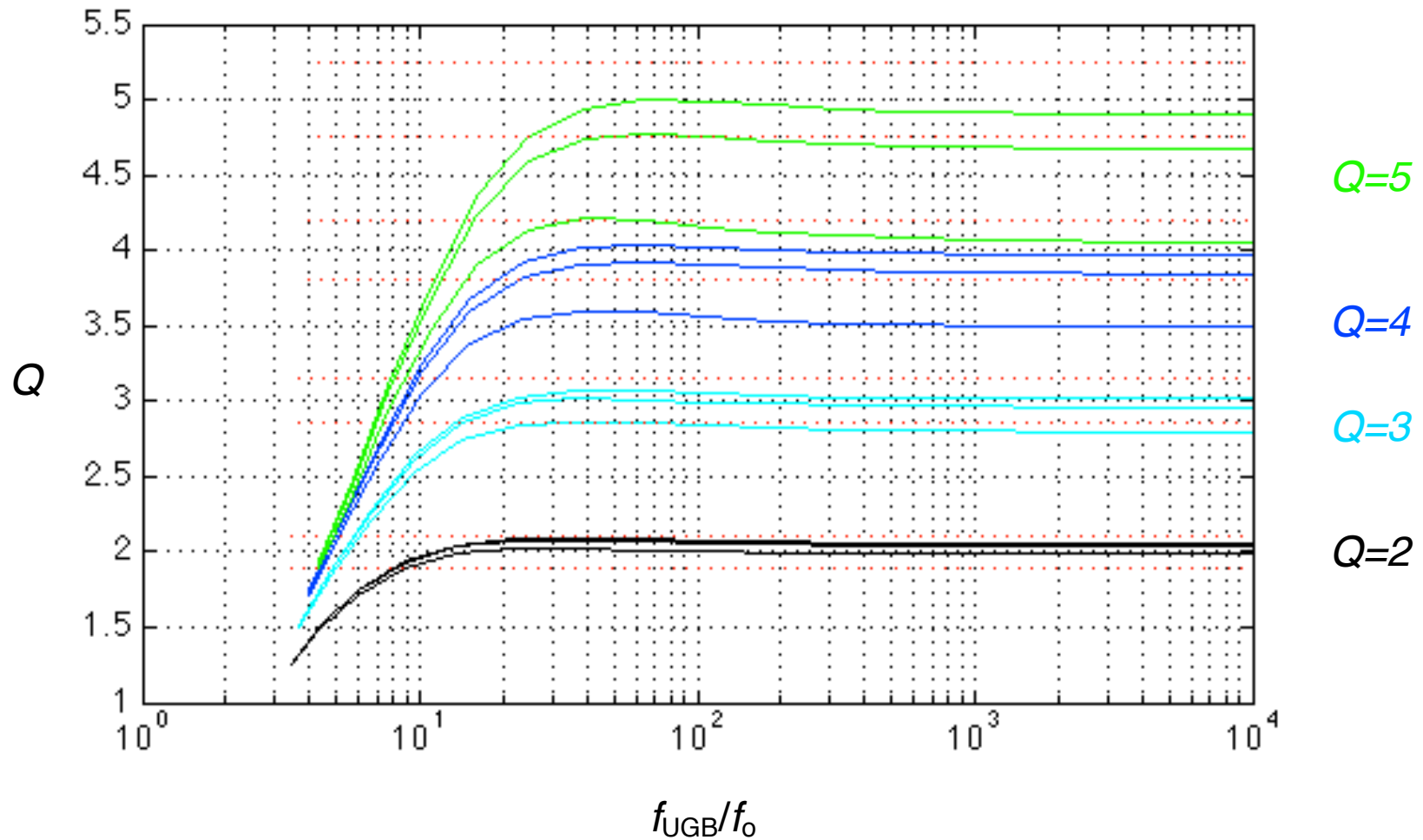
- Opamp Finite UGBW (f_{UGB})

$$f_{UGB} \approx (50 \approx 100) \cdot Gain_{peak} \cdot f_o \approx (50 \approx 100) \cdot Q \cdot f_o$$

LV Active-RC filter

Question 2 → Which specs for the opamp ? - Transfer Function Robustness

$A_o = 50\text{dB}, 60\text{dB}, 70\text{dB}$



LV Active-RC filter

Question 2 → Which specs for the opamp ? - Design example

- WLAN specs:
 - $f_o = 2 \cdot \pi \cdot 10\text{MHz}$
 - $G_o = 1$
 - $Q=3$

$$A_o \approx 100 \cdot Q = 300 = 50\text{dB}$$

$$f_{UGB} \approx 100 \cdot \text{Gain}_{peak} \cdot f_o \cong 100 \cdot Q \cdot f_o \cong 100 \cdot 3 \cdot 10\text{MHz} = 3\text{GHz}$$

- Difficult to achieve @ LV

LV Active-RC filter

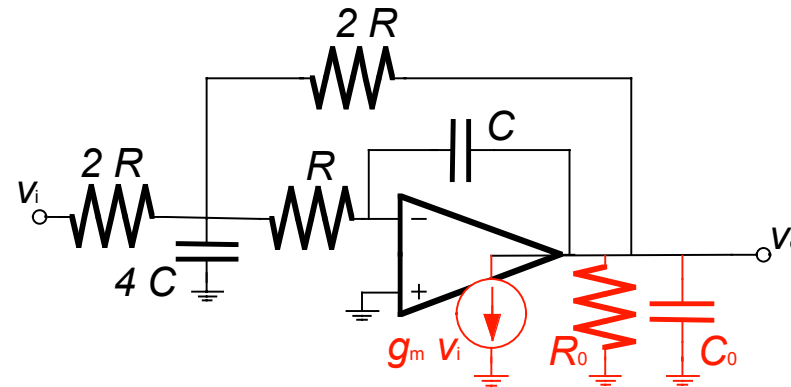
Question 2 → Which specs for the opamp ?

Real op-amp effects: Opamp finite output impedance

- Opamp Single-pole approximation in the frequency band of interest
- Benchmark: For an in-band maximally flat frequency response ($Q = \sqrt{2} / 2$)

$$R_1 = R_3 = 2 \cdot R_2 = 2R \quad C_1 = 4 \cdot C_2 = 4C \quad f_o = 1 / (4 \cdot \pi \cdot \sqrt{2} \cdot R \cdot C)$$

$$H(s) = \frac{-1 + s \cdot \frac{(R + R_o) \cdot C}{A_o + 1}}{\delta \cdot s^3 + \gamma \cdot s^2 + \beta \cdot s + \alpha}$$



$$\alpha = 1 + \frac{4}{A_o - 1} \quad \beta = 4 \cdot R \cdot C + \frac{2 \cdot R_o \cdot C_o + R_o \cdot C + 13 \cdot R \cdot C}{A_o - 1} \quad \gamma = 8 \cdot R^2 \cdot C^2 + \frac{6 \cdot R \cdot R_o \cdot C \cdot C_o + 2 \cdot R \cdot R_o \cdot C^2 + 18 \cdot C^2 \cdot R^2}{A_o - 1}$$

$$\delta = 8 \cdot \frac{R^2 \cdot R_o \cdot C_o \cdot C^2}{A_o - 1} \cdot g_m \quad A_o = g_m \cdot R_o$$

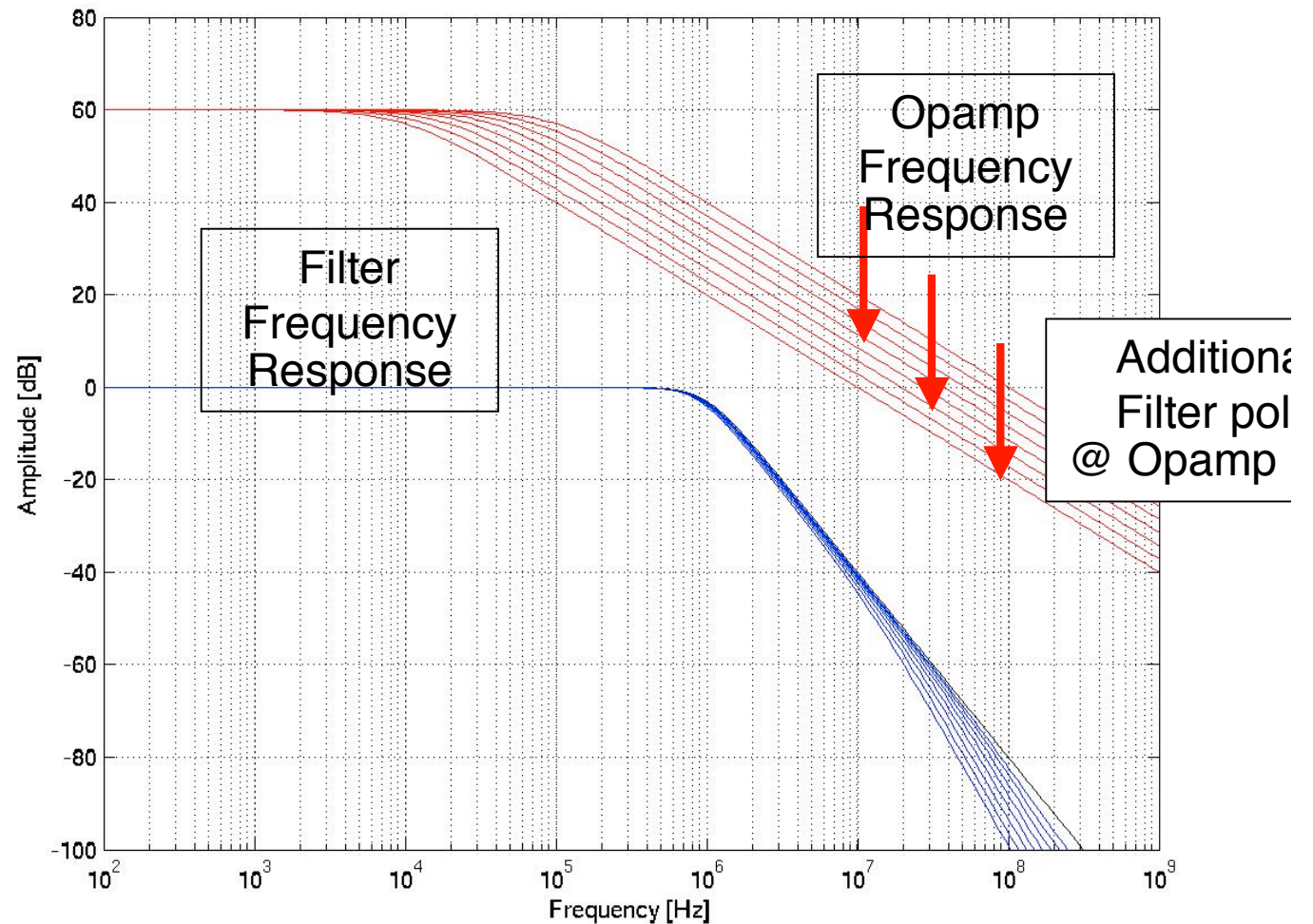
- The transfer function has one zero and three poles
- The **additional zero** is far away from f_p if $A_o \gg 1$
- The **additional pole** is $\approx f_{UGB}$

→ A_o & f_{UGB} to be maximized

LV Active-RC filter

Question 2 → Which specs for the opamp ? - Real opamp effects

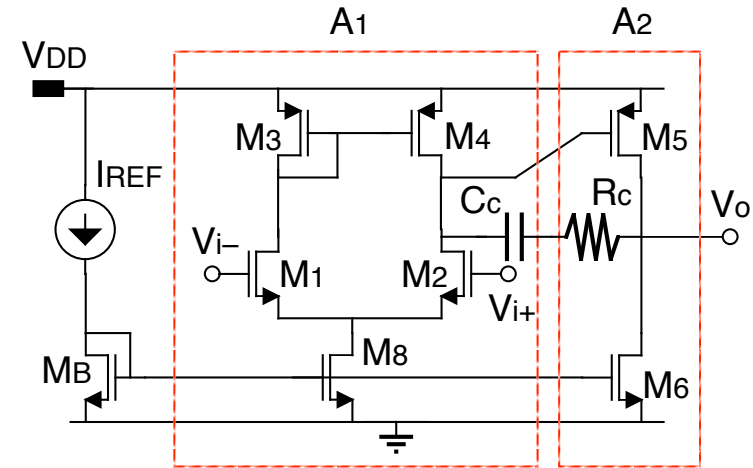
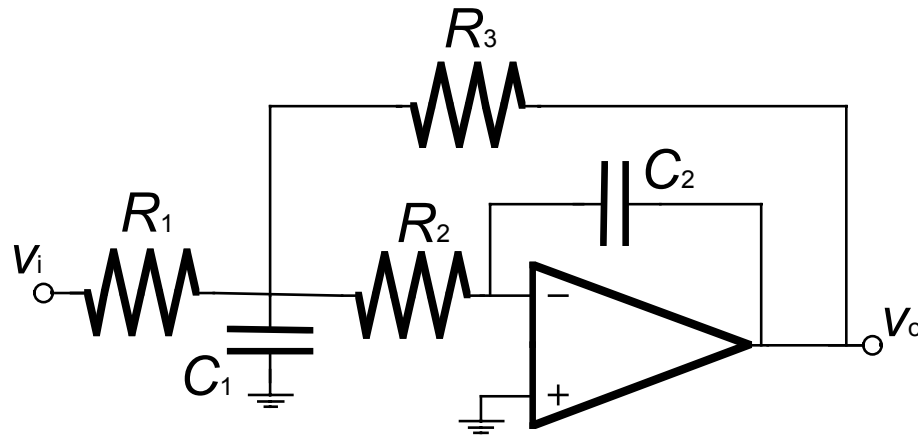
- Frequency pole deviation arises



LV Active-RC filter

Question 3 → Noise-oriented design approach ?

Rauch Biquadratic Cell Noise Performance



$$\overline{V_{n_out}^2} = 4 \cdot k \cdot T \cdot R_1 \cdot \left(\frac{R_3}{R_1} \right)^2 + 4 \cdot k \cdot T \cdot R_2 \cdot \left(1 + \frac{R_3}{R_1} \right)^2 + 4 \cdot k \cdot T \cdot R_3 + \overline{V_{n_opamp}^2} \cdot \left(1 + \frac{R_3}{R_1} \right)^2$$

LV Active-RC filter

Question 3 → Noise-oriented design approach ?

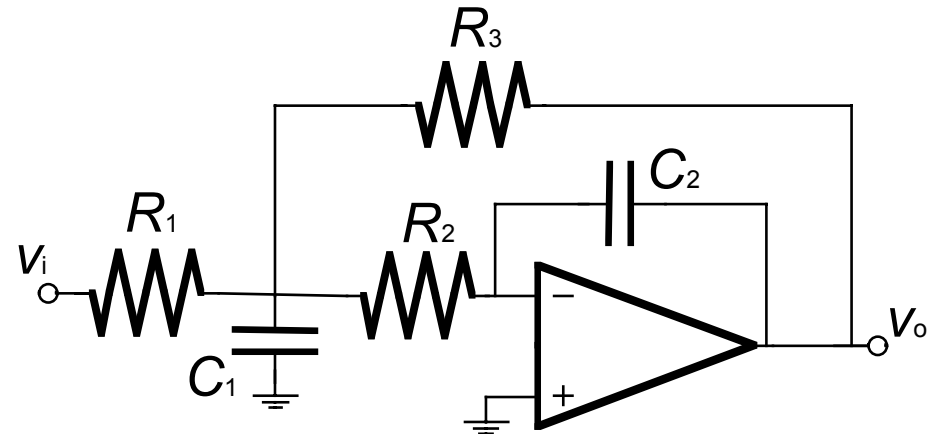
Design procedure

- Input data
- System level specifications:

- f_o , k_{dc} , Q , IRN_{cell} .

- Output data

- R, C values
- $I_{tot}(IRN_{opamp})$ curve
- the opamp A_o and f_{UGB}
- the MOS transistor sizes (W/L)



- Typically opamp noise (IRN_{opamp}) is made negligible w.r.t. resistor noise
 - This increases power consumption
 - → Trade-Off between the IRN_{opamp} and IRN_{cell} to minimize the power consumption

LV Active-RC filter

Question 3 → Noise-oriented design approach ? - Design procedure*

- Start Point: Rauch Cell Specifications

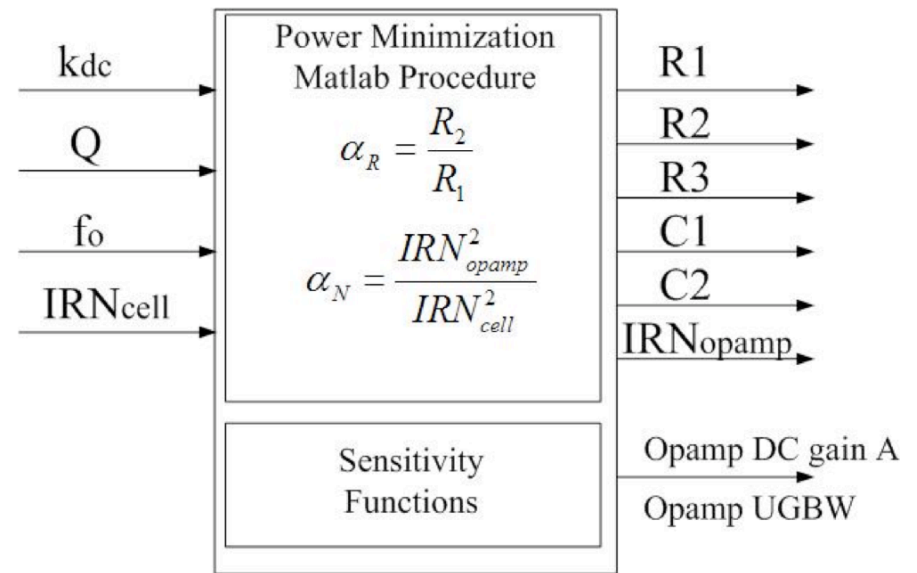
$$Q = \sqrt{\frac{C_1}{C_2}} \cdot \frac{R_1 \cdot \sqrt{R_2 \cdot R_3}}{R_1 \cdot (R_2 + R_3) + R_2 \cdot R_3} \quad G = k_{dc} = \frac{R_3}{R_1} \quad \omega_o = \frac{1}{\sqrt{R_2 R_3 C_1 C_2}}$$

$$IRN_{cell}^2 = 4kTR_1 + 4kTR_3(1/k_{dc})^2 + \left(4kTR_2 + IRN_{opamp}^2\right) \cdot (1 + 1/k_{dc})^2$$

- Parameters to be calculated: $R_1, R_2, R_3, C_1, C_2, IRN_{opamp}$

$$\alpha_N = \frac{IRN_{opamp}^2}{IRN_{cell}^2} \quad \alpha_R = \frac{R_2}{R_1}$$

- α_N, α_R are not fixed by the specifications



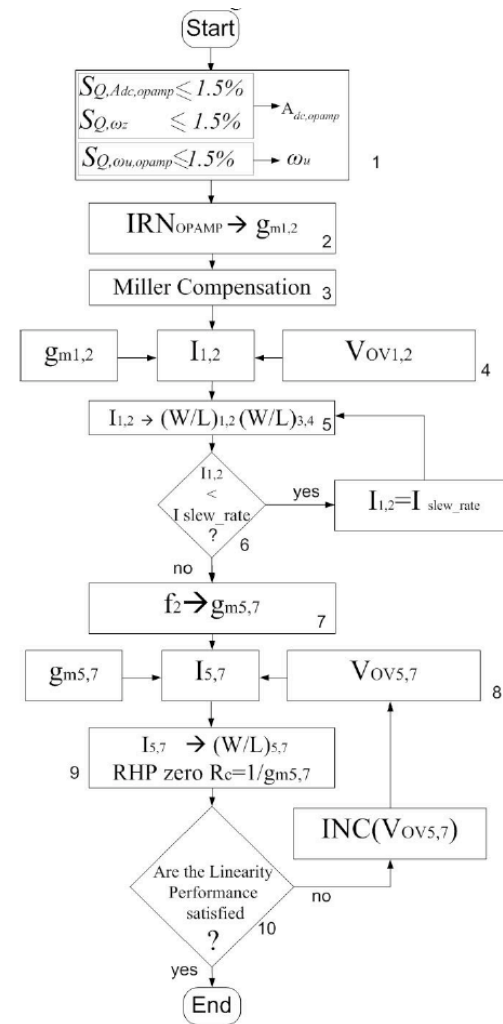
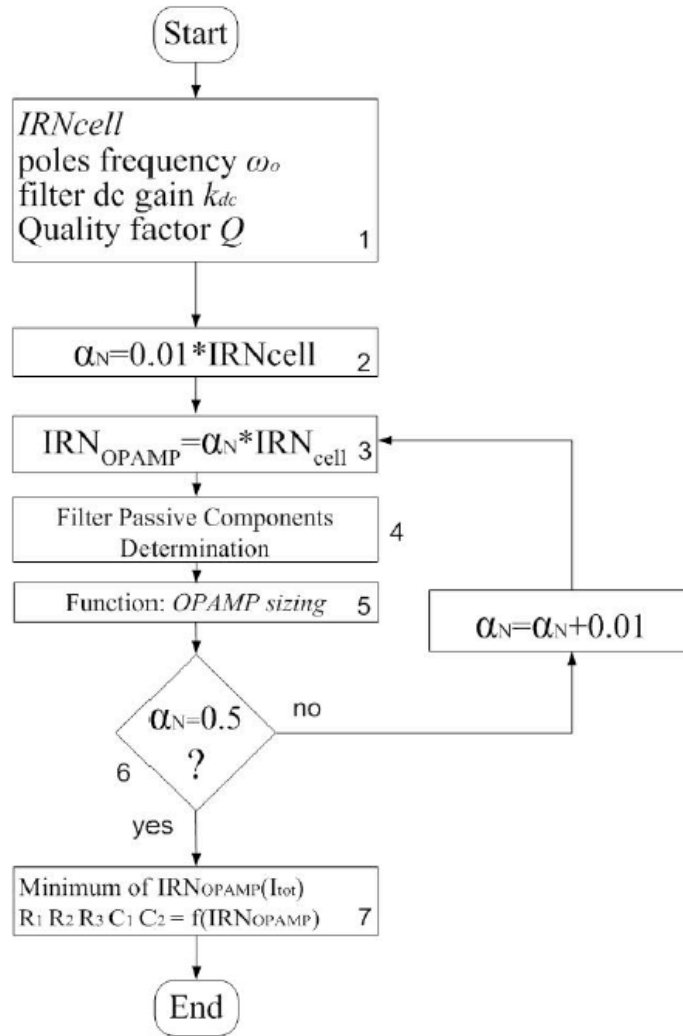
- The Design Procedure optimizes α_N to minimize the opamp power consumption.

- _____

LV Active-RC filter

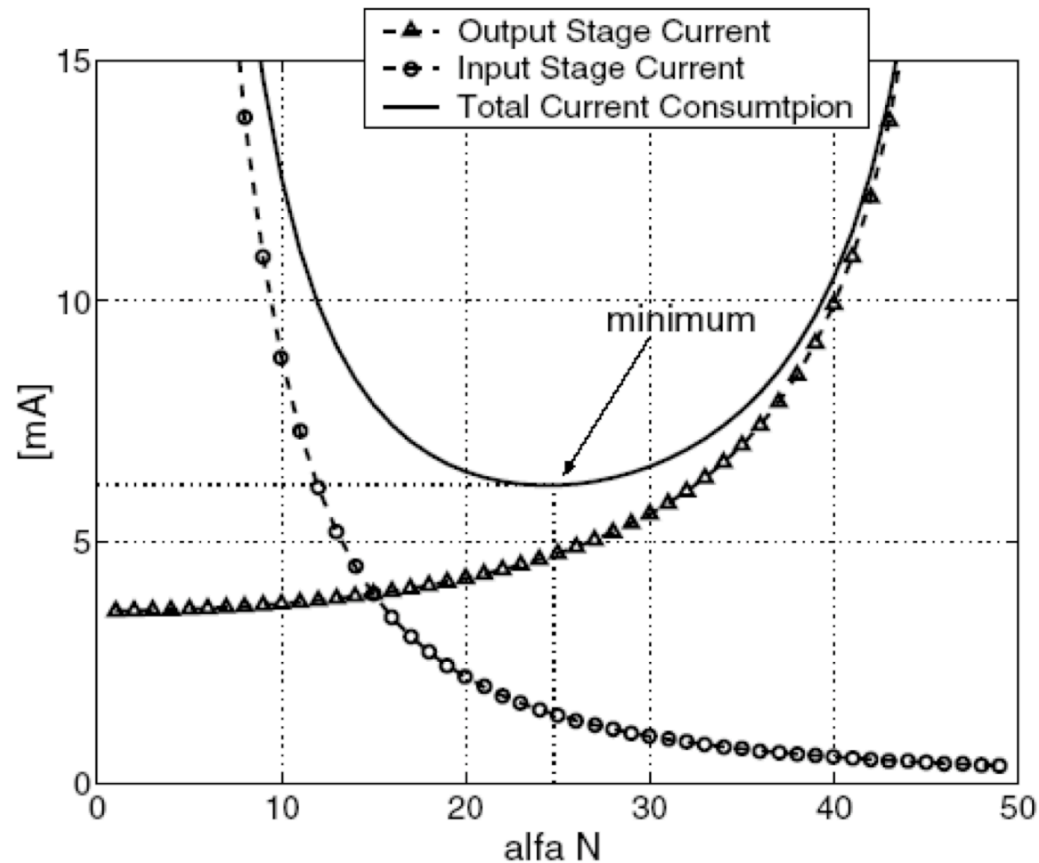
Question 3 → Noise-oriented design approach ?

Design procedure algorithm: Design flow



LV Active-RC filter

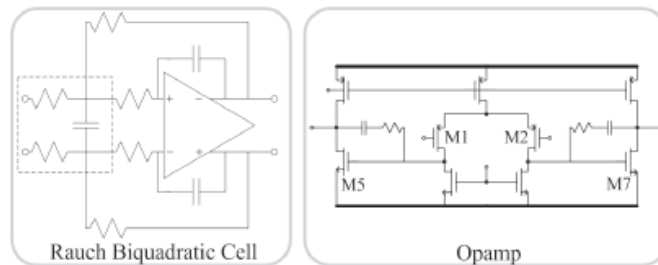
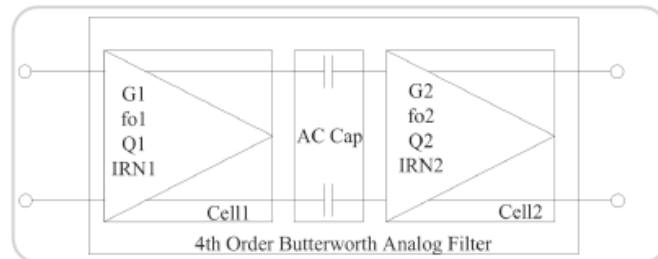
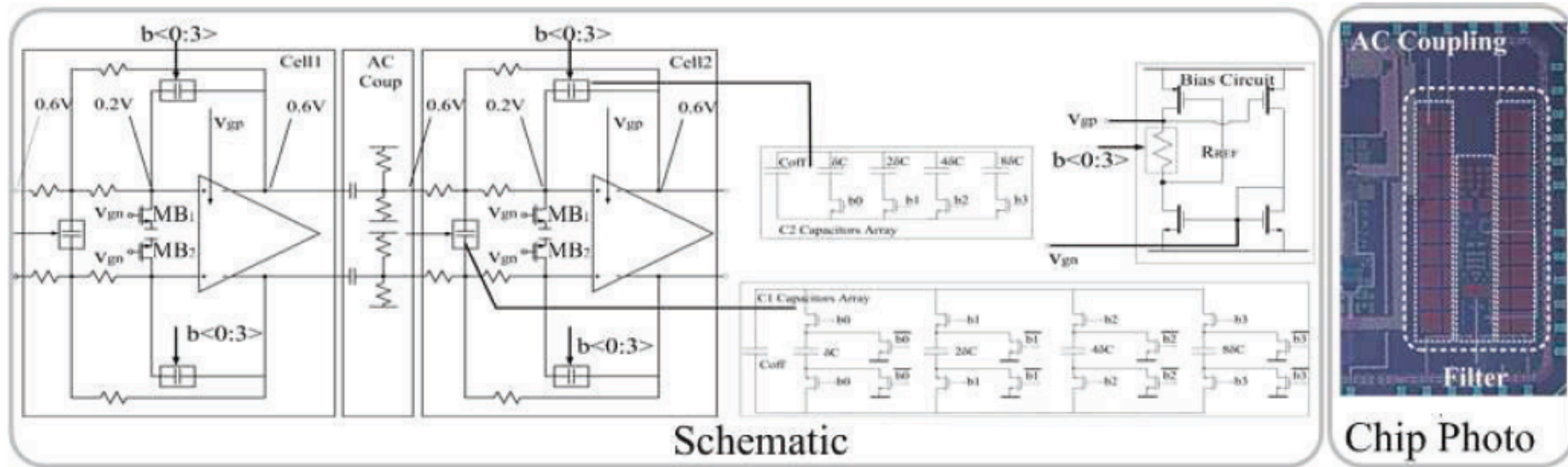
Question 3 → Noise-oriented design approach ? - Power minimization



- There is an optimum design for power minimization

LV Active-RC filter

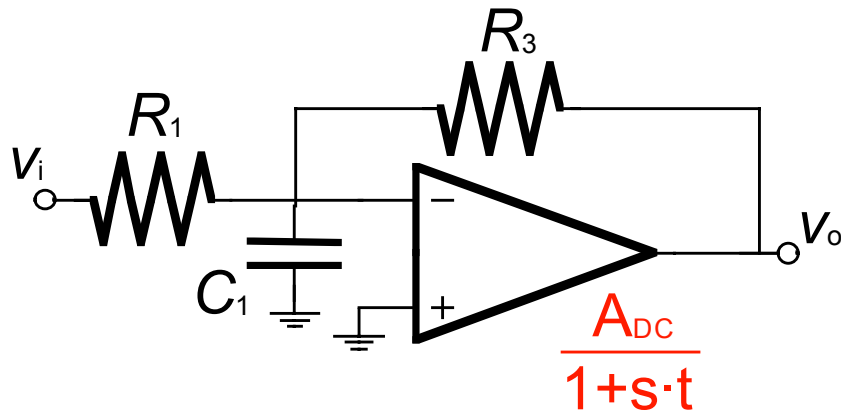
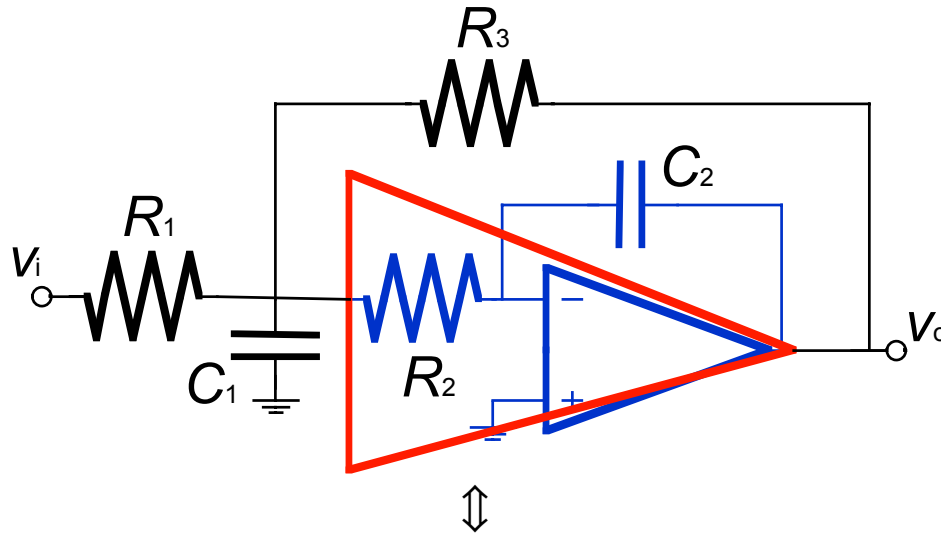
65nm design example*



Parameter	Value
G[dB]	31
$f_{@-3dB}$ [MHz]	8.2
V_{DD} [V]	1.2
CMOS Technology	65nm
Power Consumption[mW]	1.3
Output Integrated Noise[mV _{rms}] - (100kHz÷10MHz)	1.63
IRN Spectral Density@7MHz [nV/√Hz]	18
Output 1dBcP - [V _{zero-peak}]	0.9
THD[dBc] - $v_{out}=1.05V_{zero-peak}$ @3MHz	40
DR@THD=40dBc - [dB]	52
IIP3 [dBm]	-10
OIP3 [dBm]	21.3
$v_{in}=v_{in1}+v_{in2} - v_{in1}@2MHz, v_{in2}@3MHz$	
$v_{in}=v_{in1}+v_{in2} - v_{in1}@2MHz, v_{in2}@3MHz$	

LV Active-RC filter

Question 4 → Novel filter structure (Active Gm-RC) ? - The Low-Pass Cell



- R_2 - C_2 is an integrator in the frequency range of interest
- It is replaced by a bandwidth controlled opamp

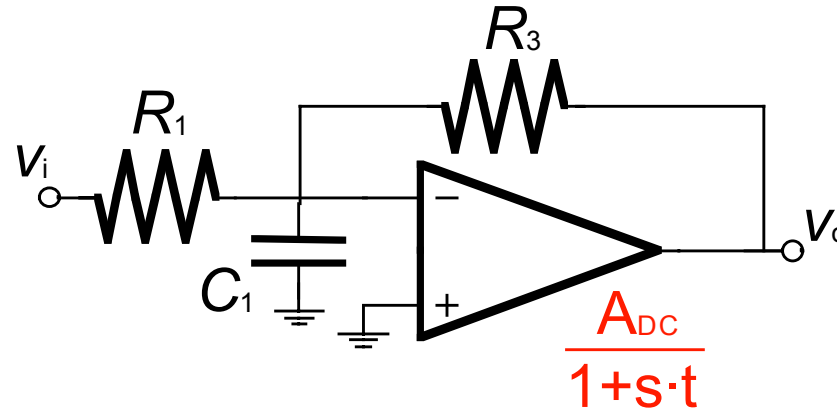
$$A(s) = \frac{A_{DC}}{1 + s \cdot \tau} = \frac{\omega_U \cdot \tau}{1 + s \cdot \tau}$$

- $1/\tau$ is the 1st-pole angular frequency
- A_{DC} is the DC-gain
- The unity gain angular frequency is:

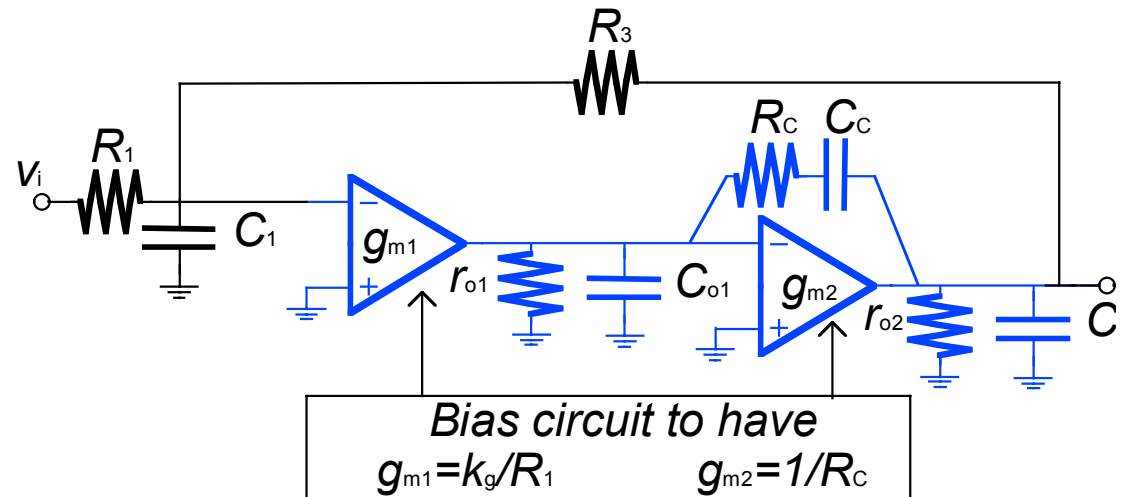
$$\omega_U = \frac{A_{DC}}{\tau}$$

LV Active-RC filter

Question 4 → Novel filter structure (Active Gm-RC) ? - The Low-Pass Cell

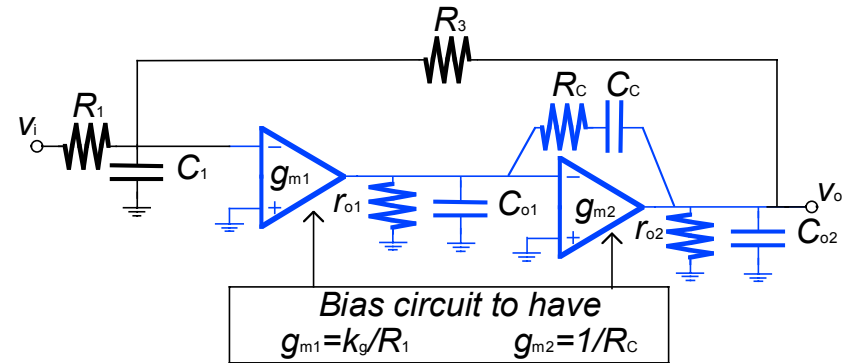
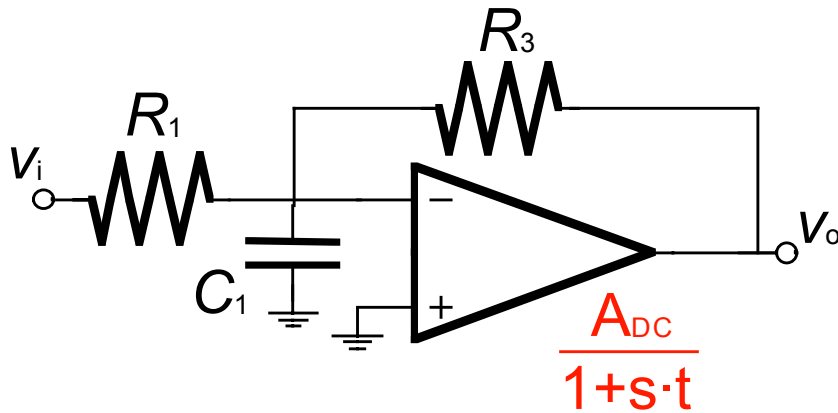


- A possible two-stage opamp implementation
- An input stage (g_{m1} & r_{o1})
- An output stage (g_{m2} & r_{o2})
- A Miller compensation network (R_C & C_C)



LV Active-RC filter

Question 4 → Novel filter structure (Active Gm-RC) ? - The Low-Pass Cell



$$A_{DC} = g_{m1} \cdot R_{o1} \cdot g_{m2} \cdot R_{o2}$$

- The adjusting circuit sets

$$g_{m1} = 1/(k_g \cdot R_1)$$

- For the filter frequency response (H_{LP}), the adjusting circuit transfers

dependence on the opamp frequency response parameters (g_{m1} , & C_C)



dependence on parasitic component values (R_1 , R_2 , & C_1)

$$H(s) = - \frac{\frac{g_{m1}}{C_1 \cdot R_1 \cdot C_C}}{s^2 + s \cdot \left(\frac{R_1 + R_3}{C_1 \cdot R_1 \cdot R_3} \right) + \frac{g_{m1}}{C_1 \cdot R_3 \cdot C_C}} = - \frac{1}{k_g \cdot R_1^2 \cdot C_1 \cdot C_C} \frac{1}{s^2 + s \cdot \left(\frac{R_1 + R_3}{C_1 \cdot R_1 \cdot R_3} \right) + \frac{1}{k_g \cdot R_1 \cdot R_3 \cdot C_1 \cdot C_C}}$$

$$\omega_u = \frac{g_{m1}}{C_C}$$

$$A_{DC} \gg R_1 \cdot C_1 \omega_u$$

$$A_{DC} \gg R_3 \cdot C_1 \omega_u$$

$$A_{DC} \gg 1 + \frac{R_3}{R_1}$$

LV Active-RC filter

Question 4 → Novel filter structure (Active Gm-RC) ?

Numerical design example

- 4th order UMTS&WLAN reconfigurable filter

	UMTS		WLAN	
	1 st cell	2 nd cell	1 st cell	2 nd cell
f_o [MHz]	3.39	3.02	19.27	17.19
Q	0.806	0.522	0.806	0.522
$G=k_{LP}$	1.26	1.26	1.26	1.26
f_{UGB} [MHz]	6.17	3.56	35.08	20.27
f_{UGB}/f_o	1.82	1.18	1.82	1.18

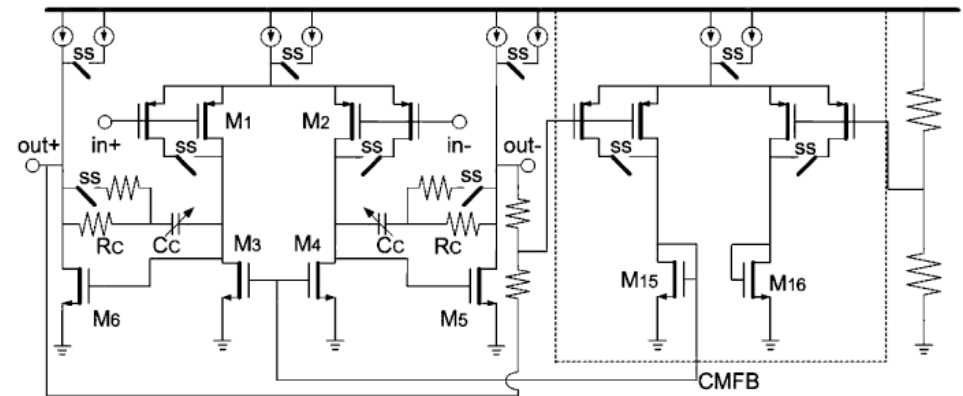
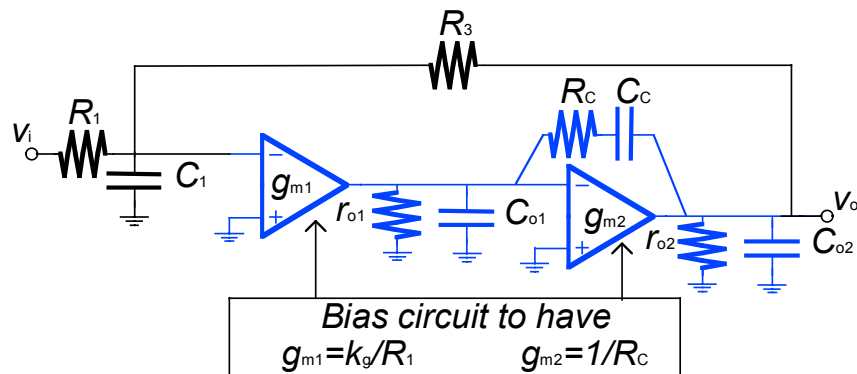
- The opamp unity-gain-frequency (f_{UGB}) is comparable to the filter cut-off frequency (f_o)
- A standard closed loop structure (Active-RC/MOSFET-C) needs $f_{UGB}/f_o > 50 \div 100$ and requires a larger power consumption

LV Active-RC filter

Question 4 → Novel filter structure (Active Gm-RC) ?

Second order singularities

- The influence of the op-amp 2nd pole on the overall cell structure frequency response



- The opamp frequency response 2nd-pole angular frequency is:

$$\omega_{p2} = \frac{g_{m2}}{C_{load}} = \frac{g_{m_M5}}{C_{load}}$$

LV Active-RC filter

Question 4 → Novel filter structure (Active Gm-RC) ?

- The output stage bias circuit

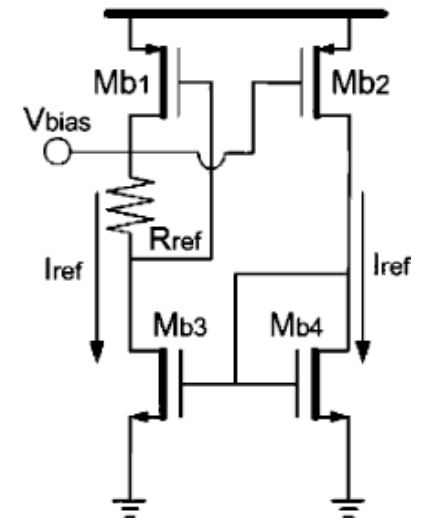
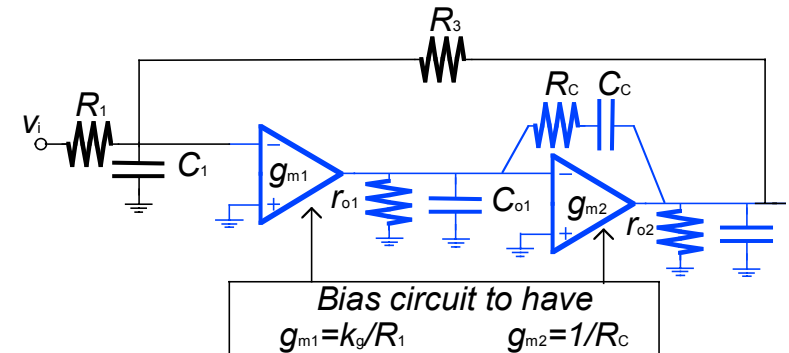
$$\omega_{p2} = \frac{g_{m2}}{C_{load}} = \frac{g_{m_M5}}{C_{load}}$$

- Impedance R_C & C_C introduce a zero:

$$\omega_z = \frac{1}{C_C \cdot \left(\frac{1}{g_{m2}} - R_C \right)}$$

- g_{m2} must be equal to $1/R_C$
- The output stage bias circuit correlates
 $g_{m2} = 1/R_C$

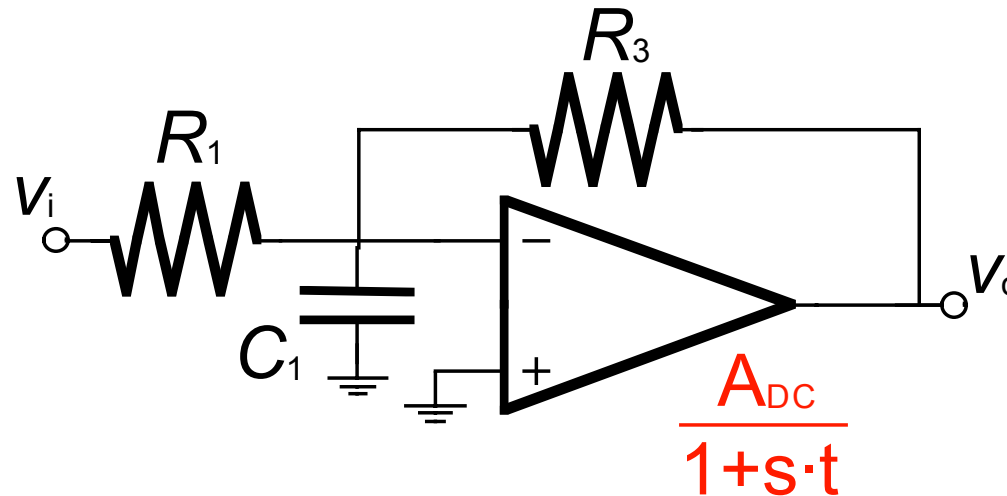
→ The op-amp behaves like a single pole circuit



LV Active-RC filter

Question 4 → Novel filter structure (Active Gm-RC) ? Linearity performance

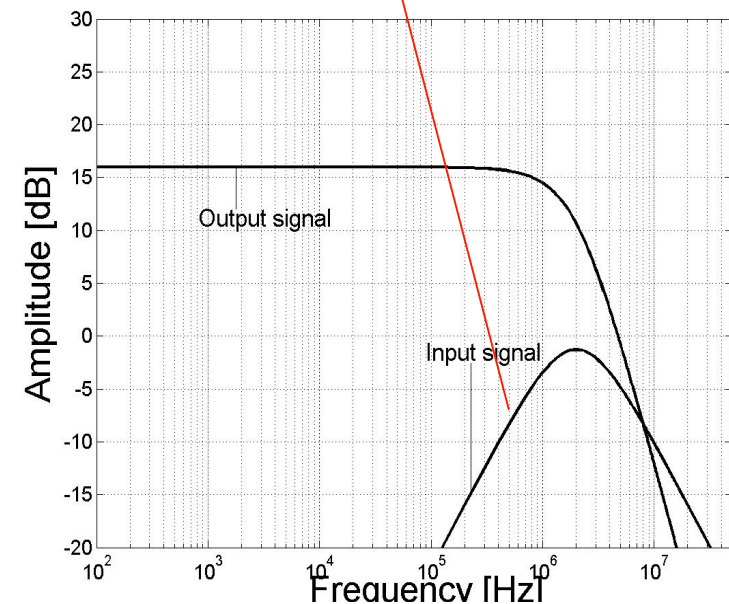
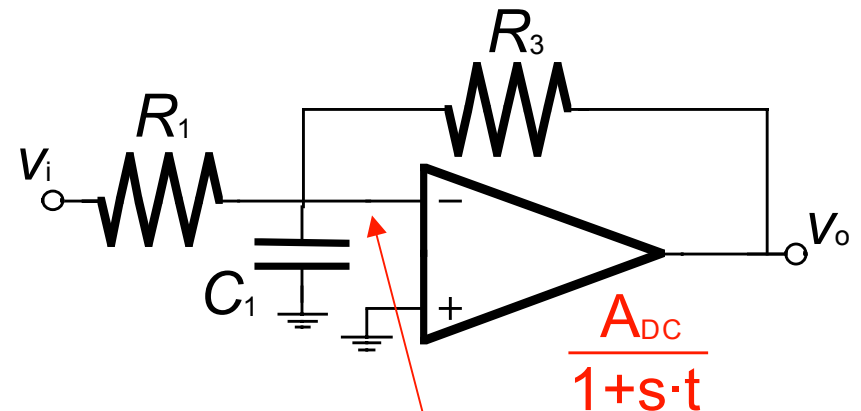
- The main source of non-linearity can be found in the op-amp performance
 - the input stage transconductance non-linearity
 - the output stage current swing limitation



LV Active-RC filter

Question 4 → Novel filter structure (Active Gm-RC) ? Linearity performance

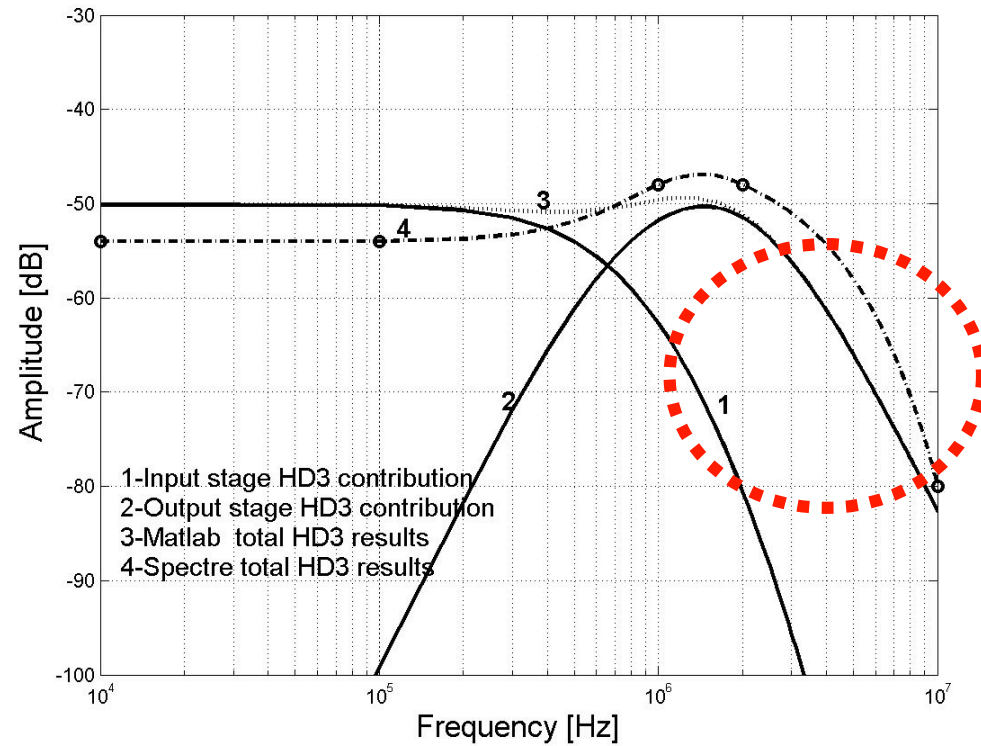
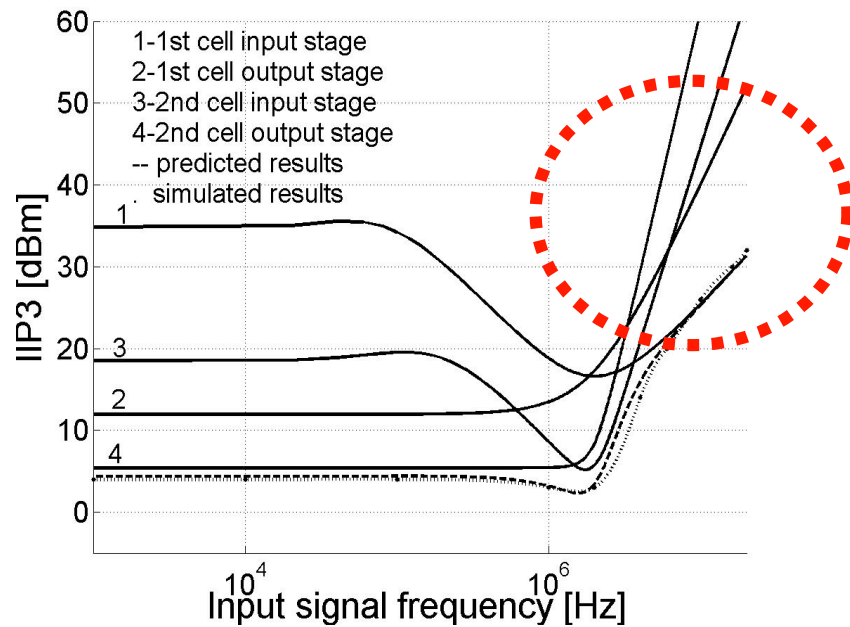
- Large linear range
- In-band Signals
 - The closed loop operation guarantees large linearity
- Out-of-band Signals (Blockers)
 - The larger signal part is processed by passive linear elements (R_1 , R_2 and C_1)
 - The smaller part is processed by the non-linear opamp stages



LV Active-RC filter

Question 4 → Novel filter structure (Active Gm-RC) ?

Linearity performance

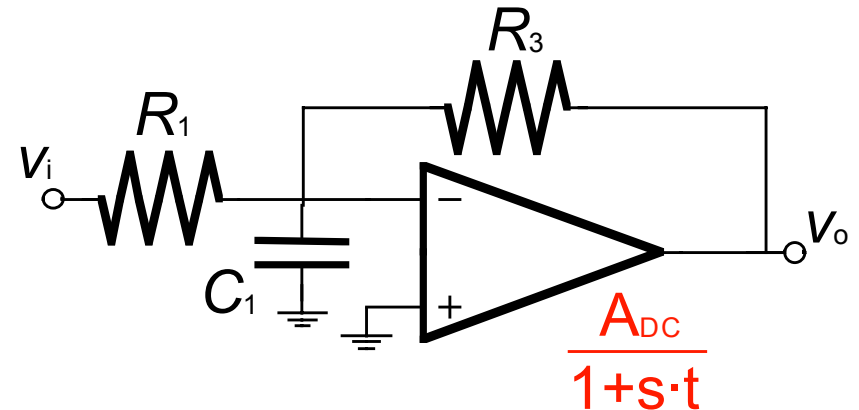


LV Active-RC filter

Question 4 → Novel filter structure (Active Gm-RC) ?

Noise performance

- The total op-amp input referred noise is due to the input transistors noise (g_{m1})



- The total Input Referred Noise is:

$$IRN = \sqrt{8 \cdot kT \cdot \left(R_1 + \frac{R_2}{K_{LP}^2} + \frac{8}{3g_{m1}} \left(1 + \frac{R_1}{R_2} \right)^2 \left(1 + \frac{Q_{LP}^2}{3} \right) \right)}$$

- With $K_G = 1/(g_{m1}R_1)$, the input referred noise calculation can be simplified:

$$IRN = \sqrt{8 \cdot kT \cdot R_1 \cdot \left(1 + \frac{1}{K_{LP}} + \frac{8 \cdot K_G}{3} \left(\frac{K_{LP} + 1}{K_{LP}} \right)^2 \left(1 + \frac{Q^2}{3} \right) \right)}$$

LV Active-RC filter

Question 4 → Novel filter structure (Active Gm-RC) ?

Design Methodology

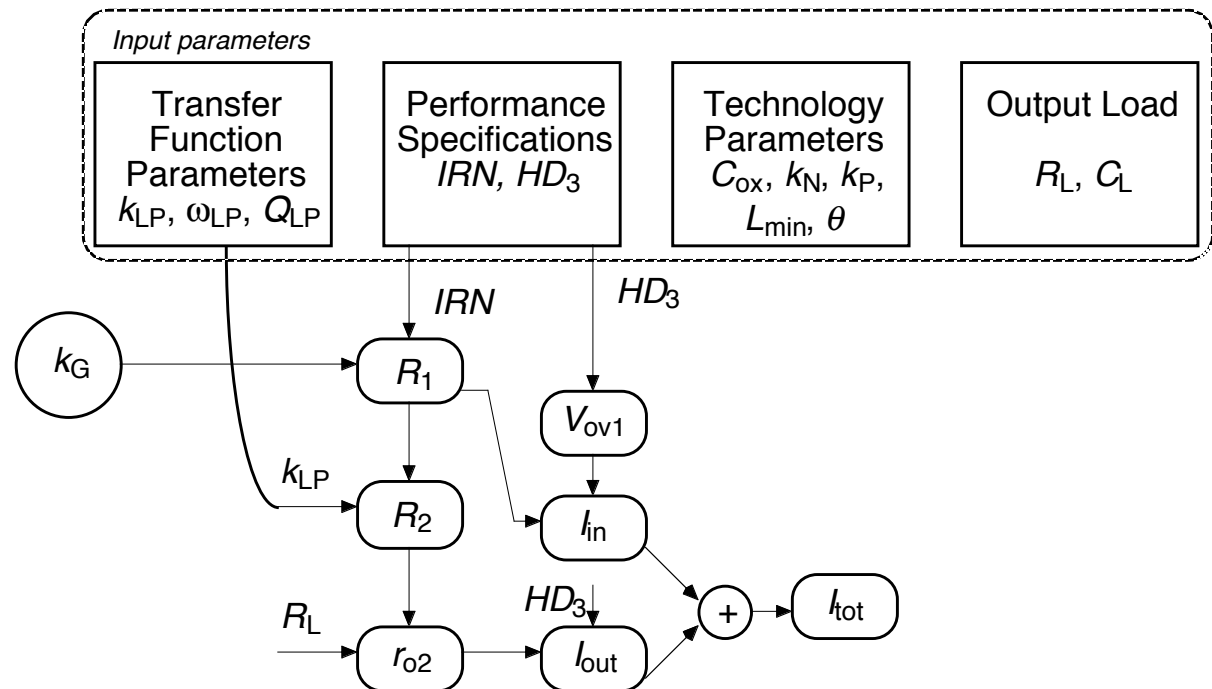
A design methodology is possible

for speed-up the design
for preliminary system evaluation

The methodology is divided in two steps:

Step 1: Among all the possible designs, the lowest power consumption one is selected.

Step 2: The Component values (R's, C0's, W/L's) are calculated



LV Active-RC filter

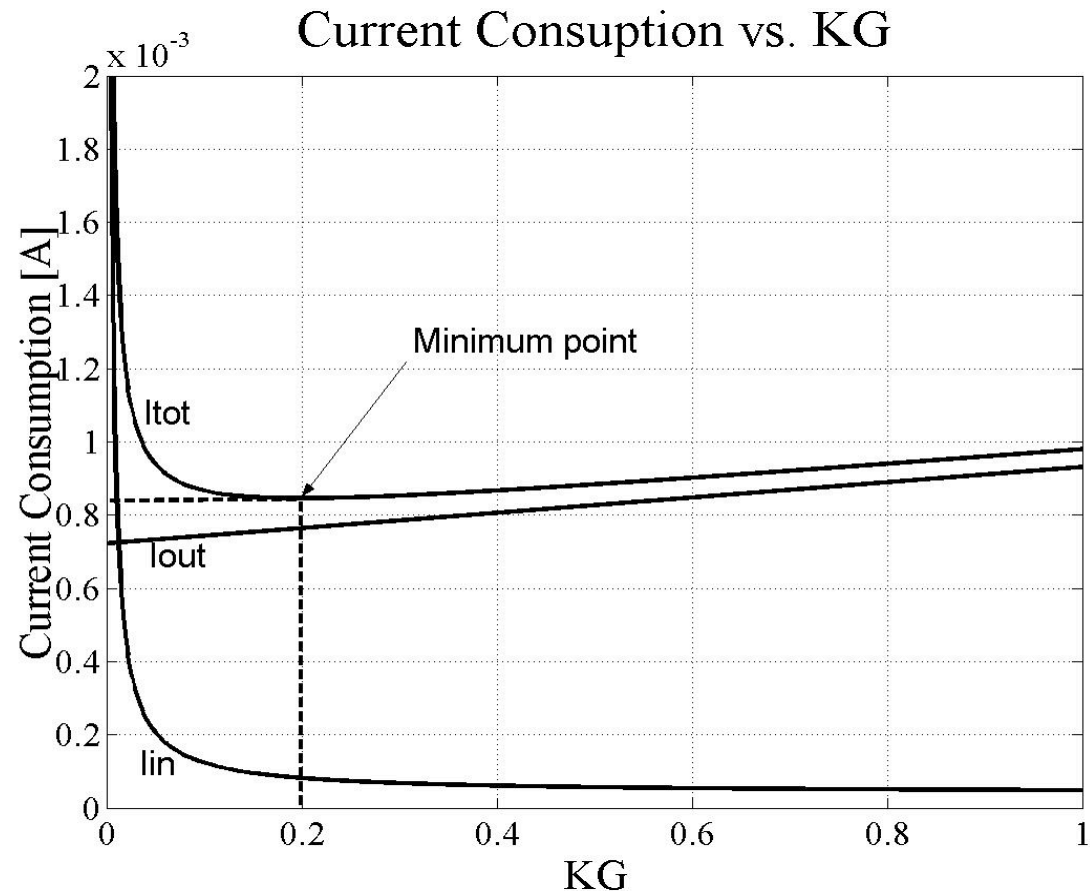
Question 4 → Novel filter structure (Active Gm-RC) ?

Methodology Description

- The total current I_{tot} is a function of k_G :

$$I_{tot} = I_{in}(k_G) + I_{out}(k_G) = f(k_G)$$

- There is a set of values of k_G for which the current remains very close to the minimum value
- k_G is selected in this set of values in order to optimize other design parameters (e.g. matching and layout)

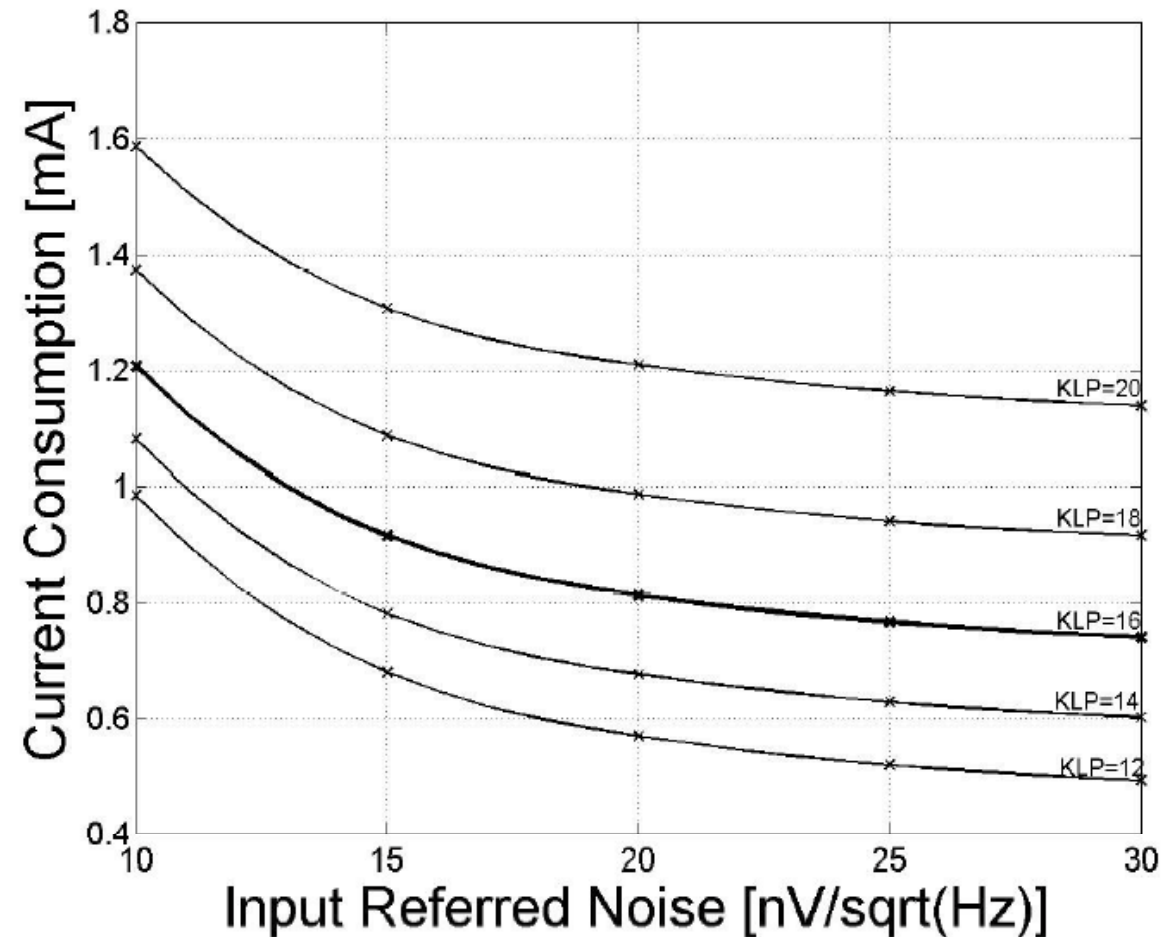


LV Active-RC filter

Question 4 → Novel filter structure (Active Gm-RC) ?

System evaluation

- The tool-box allows to make parametrical current consumption evaluation
- Example I
I (IRN & DC-Gain)



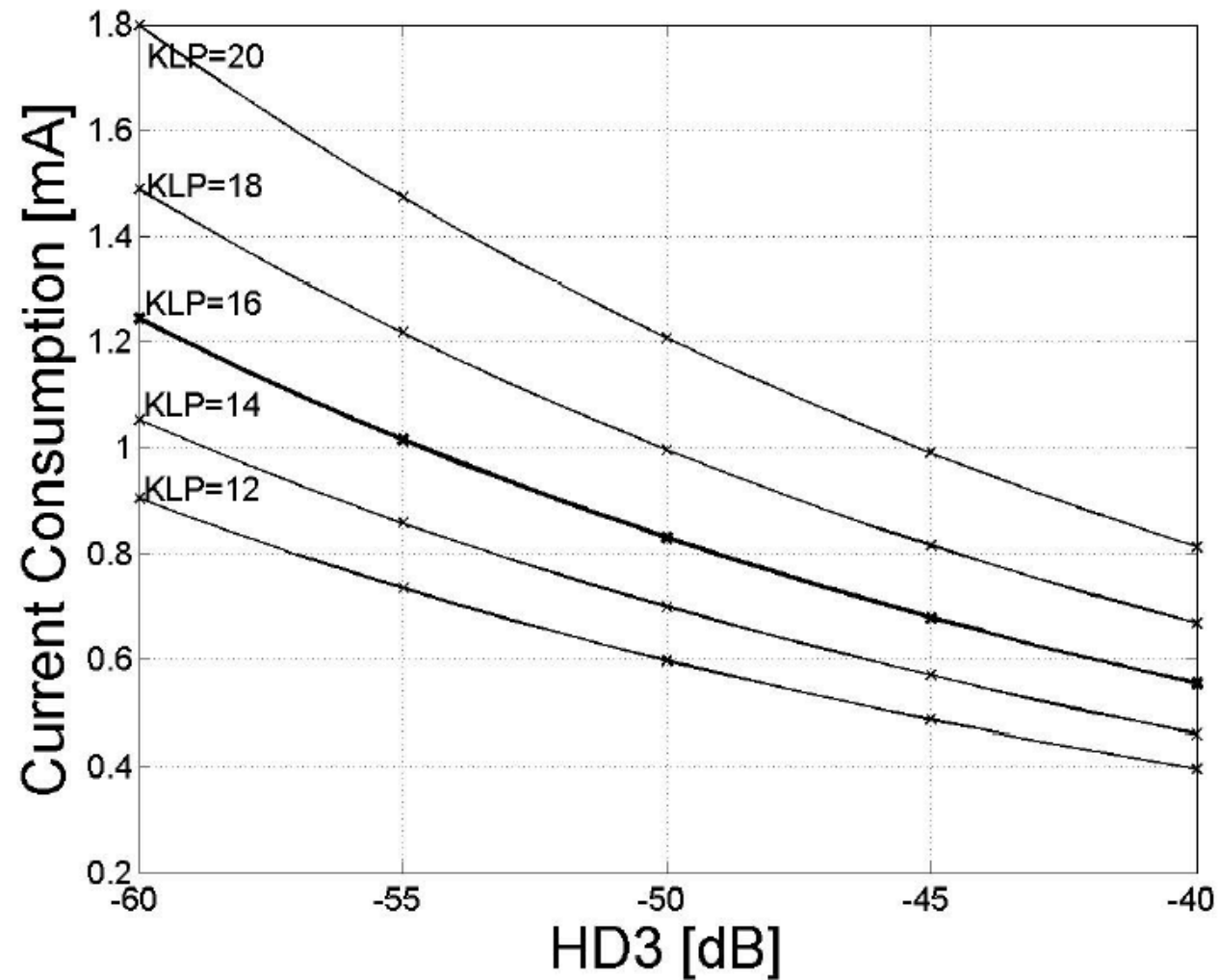
LV Active-RC filter

Question 4 → Novel filter structure (Active Gm-RC) ?

System evaluation

Example II

I (HD3 & DC-Gain)

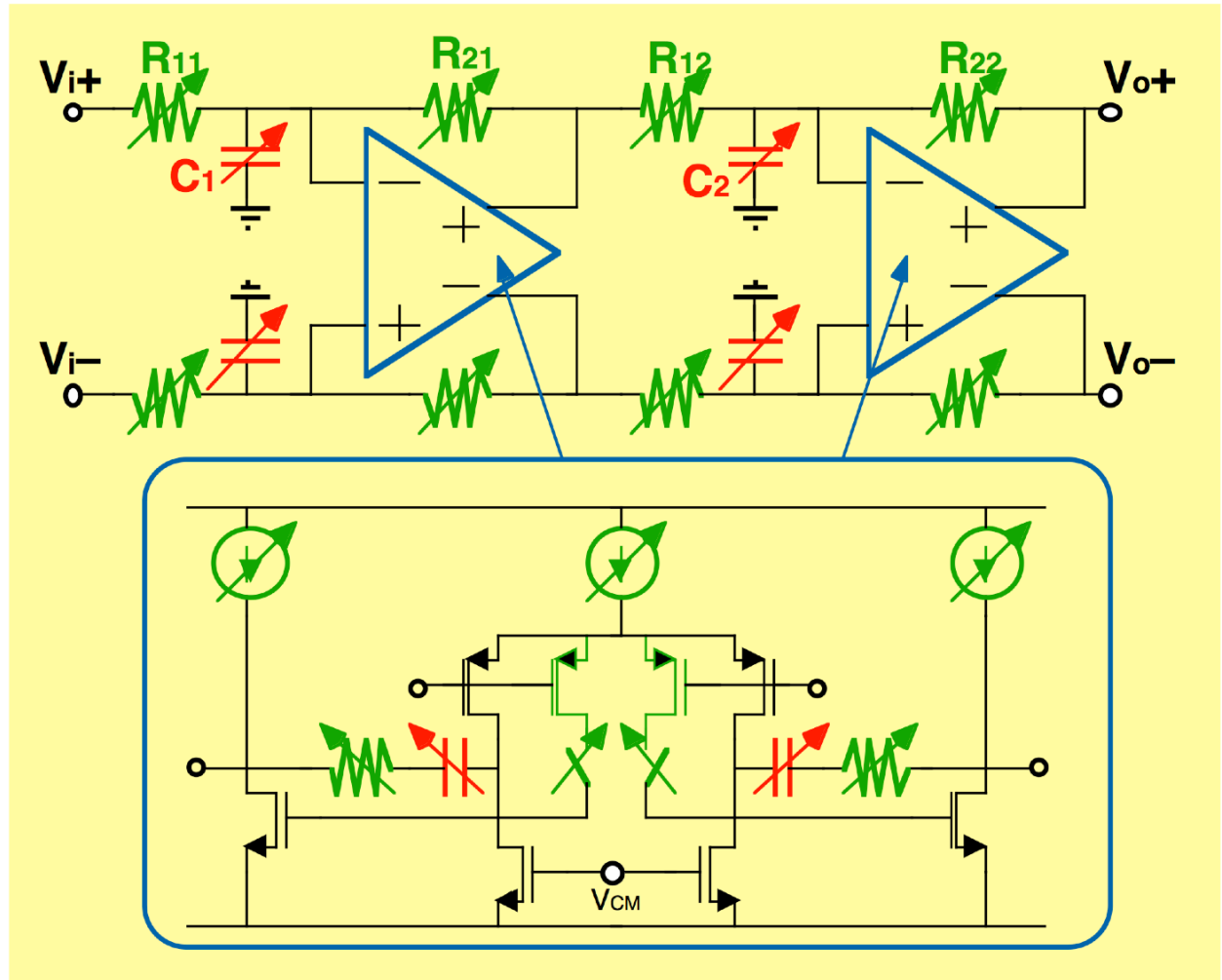


LV Active-RC filter

Question 4 → Novel filter structure (Active Gm-RC) ?

Design example (D'Amico, JSSC2006) : 4th order Bessel Filter

- Reconfigurable filter
- Red control
- 4-bit for Technology spread compensation
- Green control
- 1-bit for UMTS/WLAN selection



LV Active-RC filter

Question 4 → Novel filter structure (Active Gm-RC) ?

Design example: 4th order Bessel Filter*

	UMTS	WLAN
Technology	0.13 μ m CMOS @ 1.2V	
Die area occupation	2.8mm ²	
f _{-3dB}	2.11MHz	11MHz
f _{-3dB} Programmable Range	[1.45-3.6] MHz	[5.87-19.44] MHz
Programmable Δ f _{-3dB} step	135kHz	850kHz
DC-gain	4dB	4dB
Input-referred noise	36 μ V _{rms}	36 μ V _{rms}
In-band IIP3	21dBm	21dBm
Out-of-band IIP3	31dBm	n.a.
1dbCP (f _i =f _o /3)	11dBm	10.6dBm
THD=-40dB (f _i =f _o /3)	1.8V _{pp}	1.8V _{pp}
Power consumption	3.4mW	14.2mW

*Large in-band lineari
(1dB_{CP} @ $\pm 1.1V_p$ out
voltage) w.r.t. the sup,
voltage (1.2V)*

Large out-of-band lineari

LV Analog Design in scaled CMOS technology

Outline

- Introduction
 - Basic CMOS operation
 - CMOS technology scaling trends
 - What is LV
 - LV Analog design
 - LV at transistor level
 - LV at circuit level
 - Current mirror
 - Opamp design
 - Basic bandgap design
 - LV at system level
 - Active-RC filter design
 - Gm-C filter design ←←←
 - SC circuit design

Gm-C Filter Design

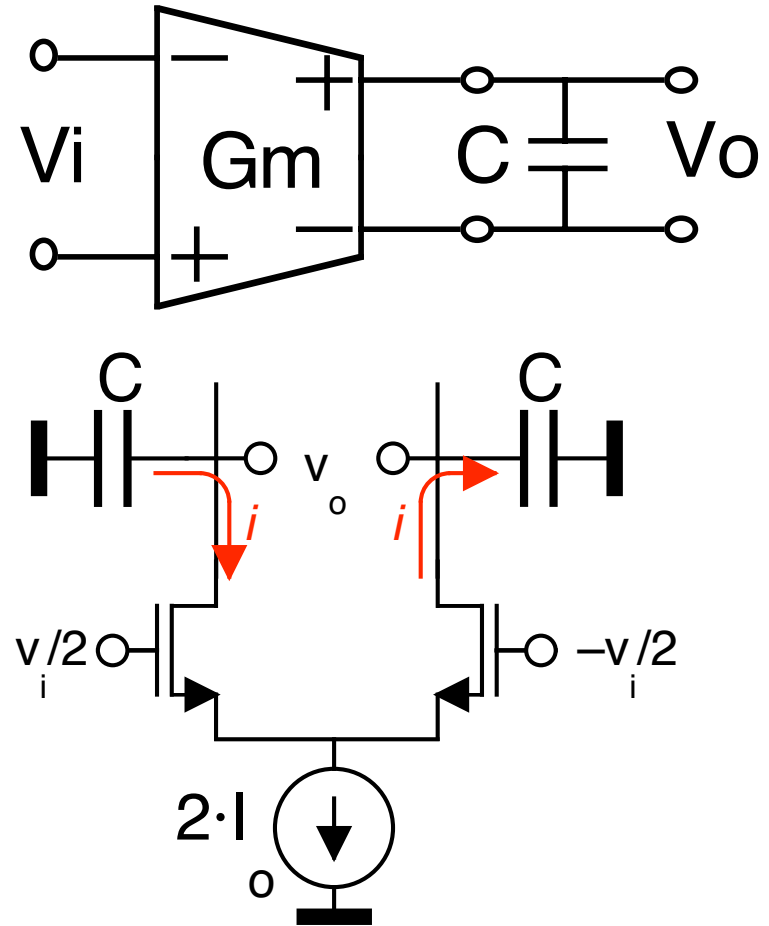
MOS in saturation region

$$H(s) = \frac{V_o}{V_i} = \pm \frac{G_m}{s \cdot C}$$

$$I_D = \frac{1}{2} \cdot \mu \cdot C_{ox} \cdot \left(\frac{W}{L}\right) \cdot (V_{GS} - V_{TH})^2$$

$$G_m = \mu \cdot C_{ox} \cdot \left(\frac{W}{L}\right) \cdot (V_{GS} - V_{TH})$$

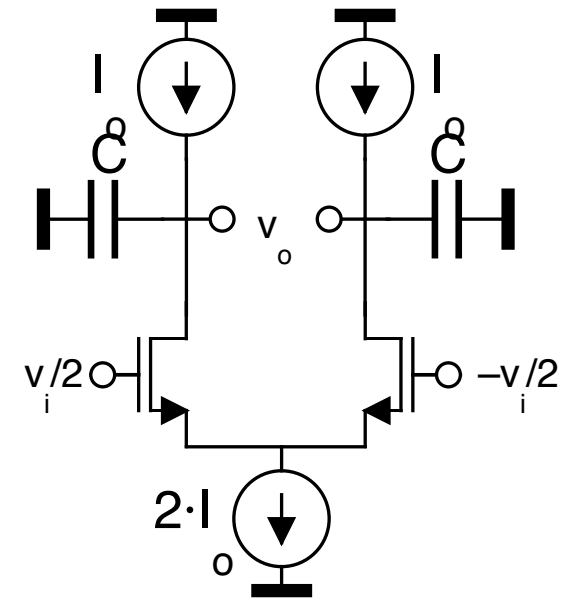
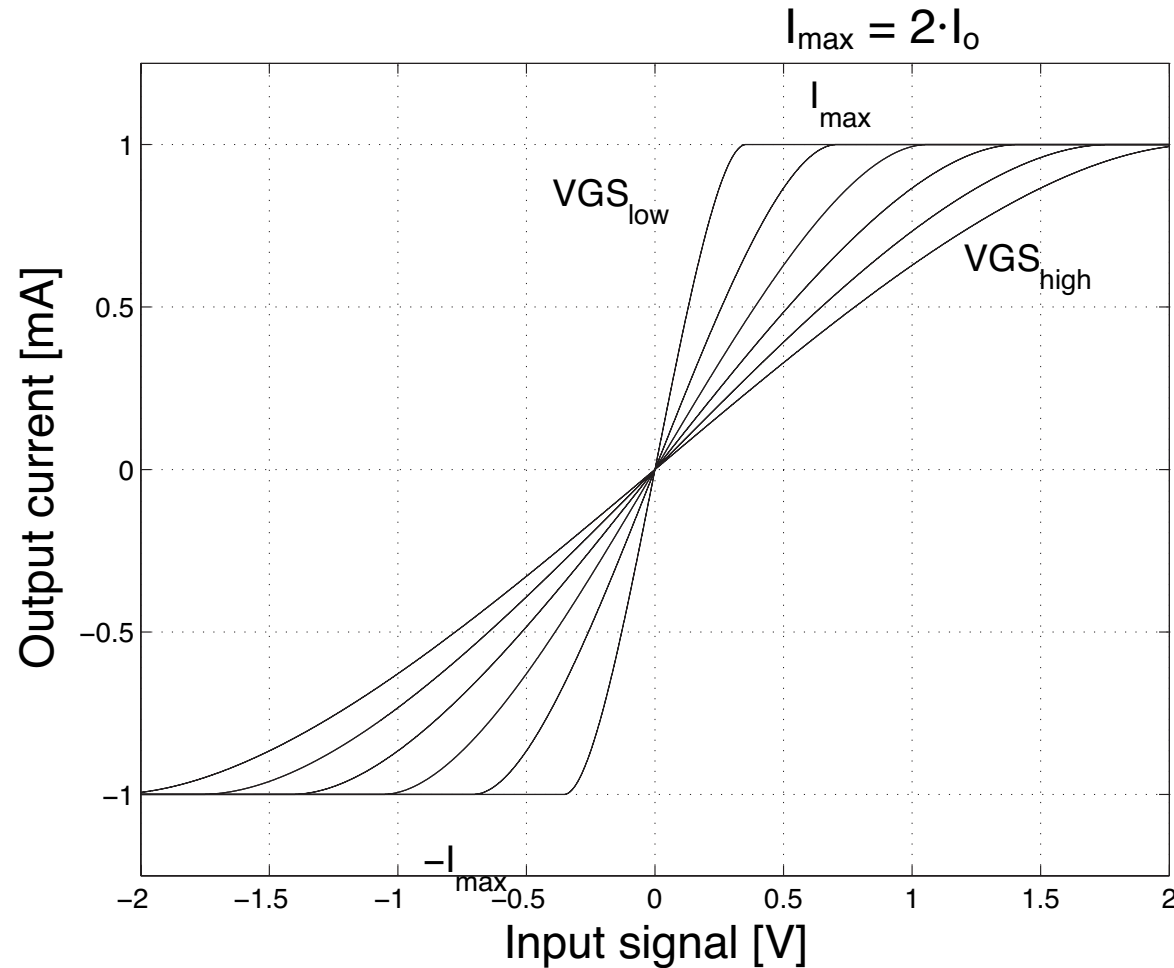
$$G_m = \frac{2 \cdot I}{V_{GS} - V_{TH}}$$



Gm-C Filter Design

MOS in saturation region – Input linear range

- For a constant bias current $2 \cdot I_o$



Gm-C Filter Design

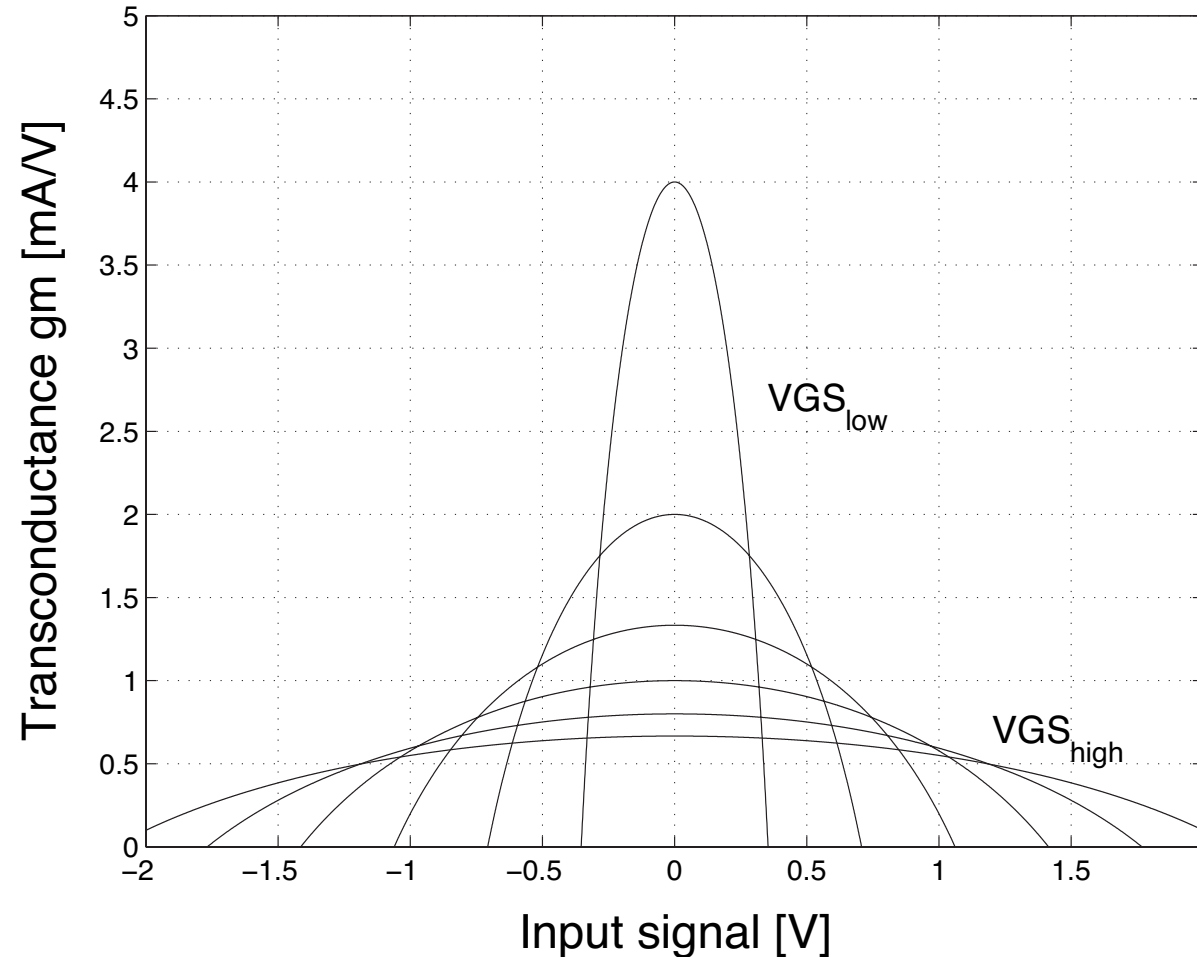
MOS in saturation region – Input linear range

- For a constant bias current $2 \cdot I_D$

$$g_{mo} = \mu \cdot C_{ox} \cdot (V_{GS} - V_{TH})$$

$$g_{mo} = \frac{2 \cdot I_D}{V_{GS} - V_{TH}}$$

- A higher g_m value corresponds to a smaller linear range



Gm-C Filter Design

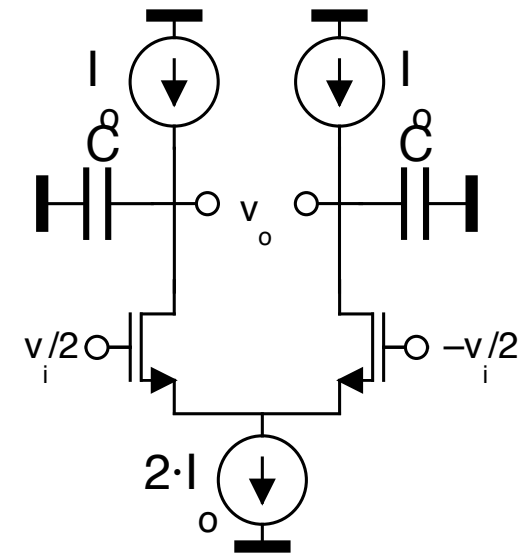
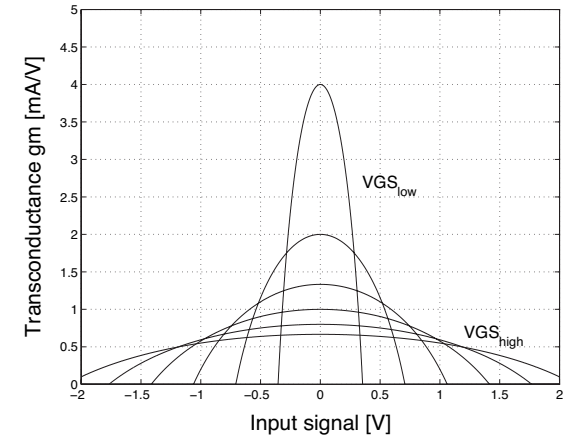
MOS in saturation region – Input linear range

- The THD for an input voltage sinewave of the input voltage-to-current transconductor is given by:

$$THD = \frac{1}{32} \cdot \frac{V_i^2}{V_{OV}^2}$$

$$IM3 = \frac{3}{32} \cdot \frac{V_i^2}{V_{OV}^2}$$

- The sinewave stays only for a small part on the non linear region



LV Gm-C Filters

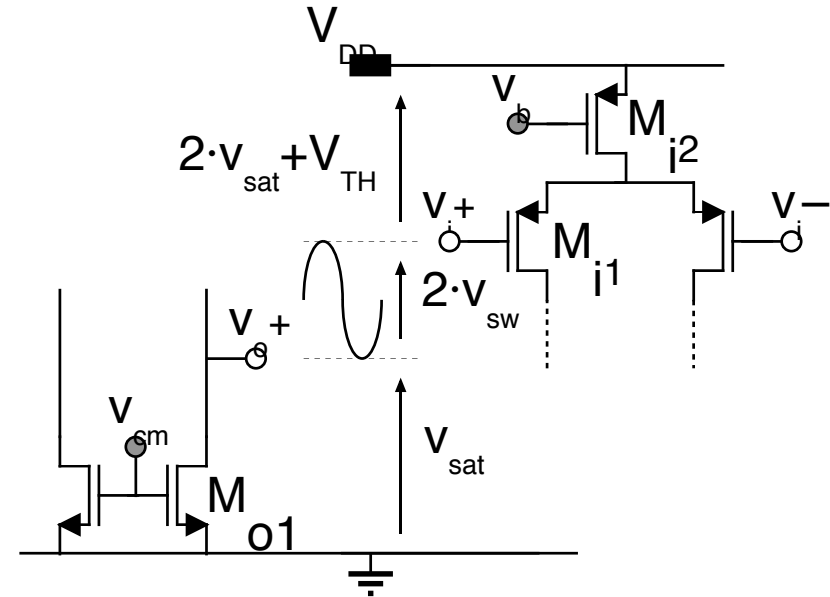
CT Systems

- Open-loop (like gm-C filters):
 - output-to-input connection of two similar stages
- V_{DDmin} depends both on input and output stage limitation, and it is given by:

$$V_{DDmin} = (V_{GSdiff} + V_{sat_top}) + 2 \cdot V_{sw} + V_{sat_bottom}$$

$$V_{DDmin} = V_{TH} + 3 \cdot V_{ov} + 2 \cdot V_{sw}$$

- V_{GSdiff} is correlated with the maximum signal amplitude i.e. with V_{sw}
- A V_{DDmin} reduction by using a pseudo-differential structures
- A PD structure exhibits a worse CM-signal rejection and a worse CM-signal control is needed



Pseudo-Differential LV Gm-C Filters

Low-voltage solutions

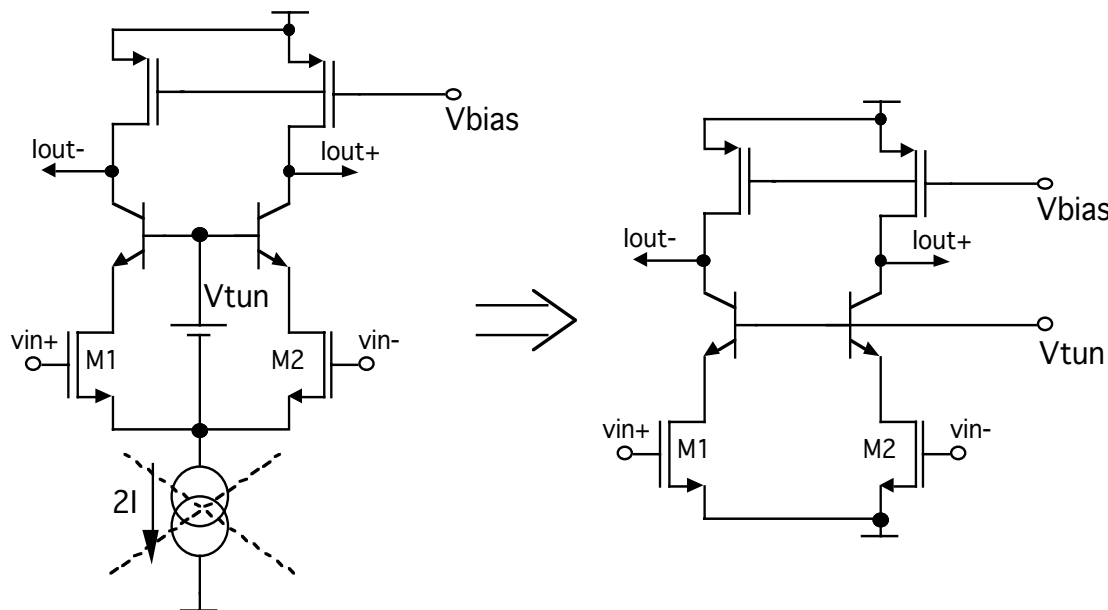
- Eliminate the voltage drop of the current source by using pseudo-differential structures
- two single-ended structures in parallel and operated with complementary signals)
 - ☺ Avoid the voltage drop of current source

Open problems

- ☹ 1 Input CM rejection
- ☹ 2 Linearity at low power
- ☹ 3 Output CM feedback
- ☹ 4 Dc-gain

Solutions

- ☺ 1 Feedforward technique
- ☺ 2 Proper current summing
- ☺ 3+4 Use of damped integrator (Precise gain concept)



Pseudo-Differential LV Gm-C Filters

Pseudo-Differential Low-Voltage Transconductors [Rezzi-TCAS95]

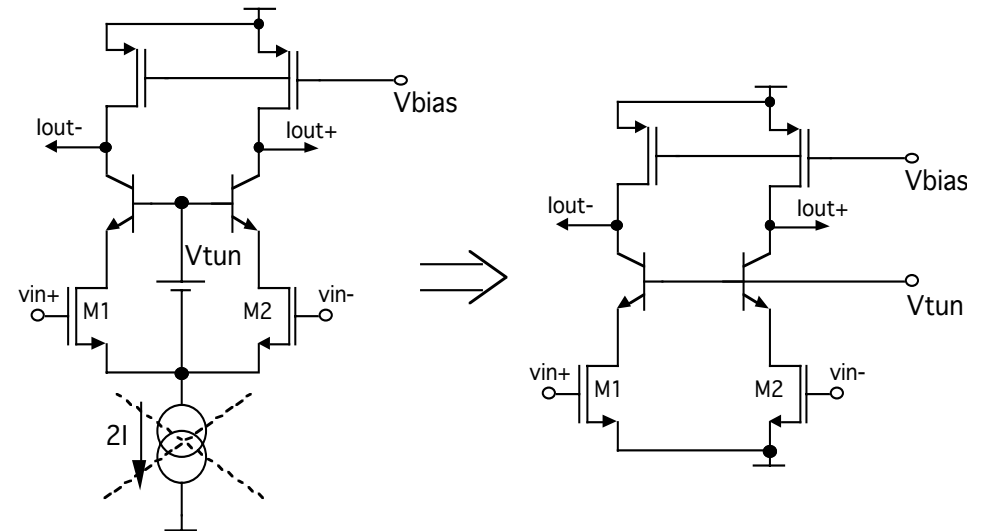
- Fully-differential structure
- 😊 A single V_{tun} for each transconductor
- 😞 Minimum CM voltage $V_{CMmin} \approx 1.5V$

$$V_{CMmin} = V_{dsmax} + V_{cesat} + V_{gen} + V_{signal}$$

- 😊 Intrinsic rejection of the CM input signals

- Pseudo-Differential

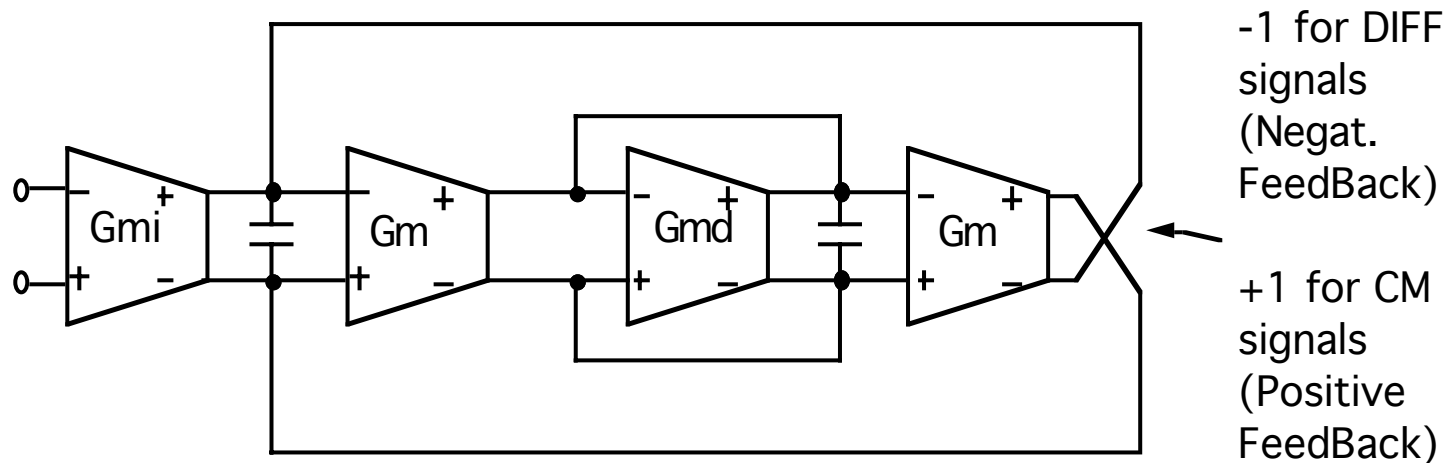
- 😊 Easy to bias and easy to tune (V_{tun} can be shared among different transconductors)
- 😊 Minimum CM voltage $V_{CMmin} = V_{dsmax} + V_{cesat} + V_{signal} \approx 1V$
- 😞 **No rejection of CM input signals** (CMRR=1)



Pseudo-Differential LV Gm-C Filters

Effect of non-zero input CM signals

- A cancellation of the common-mode signal is mandatory to avoid positive feedback
- Example of CM positive feedback: Differential biquadratic cell

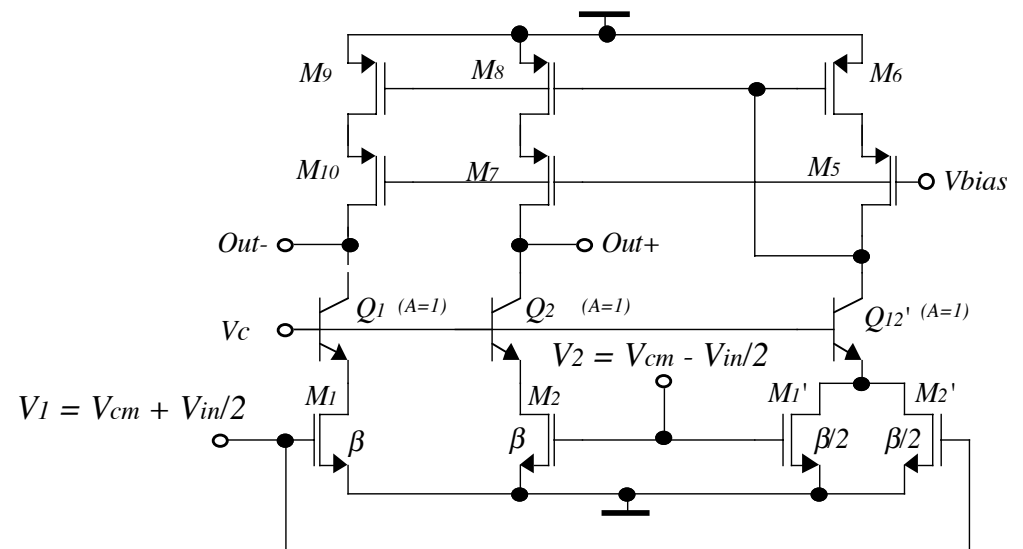
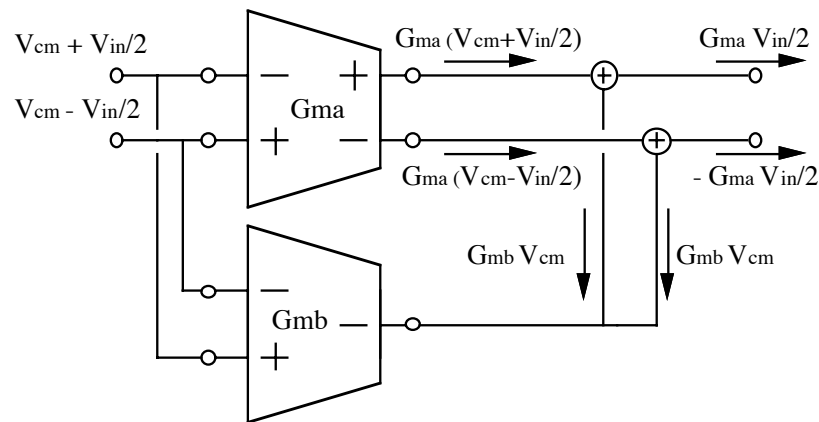


- The feedback is negative for the differential signal while it is positive for CM
- Fully differential $\Rightarrow G_{loop} \ll 1 \Rightarrow \text{😊}$ The system is stable
- Pseudo-differential $\Rightarrow G_{loop} > 1 \Rightarrow \text{😞}$ The system is not stable

Pseudo-Differential LV Gm-C Filters

☺ 1 - Input CM signals Feed-forward cancellation

- The input CM signal is sensed and subtracted at the output node



- Auto-biasing circuit

Pseudo-Differential LV Gm-C Filters

Common Mode Rejection Ratio Performance

- Low frequency

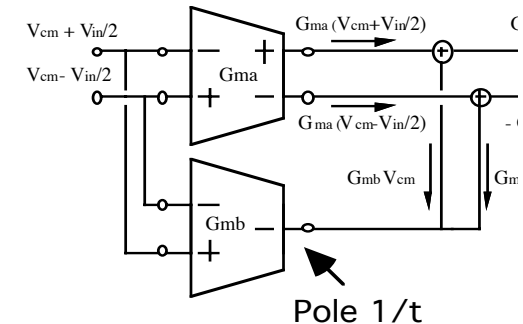
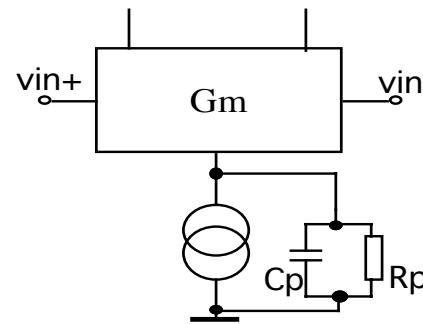
$$CMRR_{LF} \approx G_m \cdot R_p \gg 1 \quad f(\text{offset \& matching})$$

- High frequency

$$CMRR_{HF} = \frac{1 + s \cdot C_p / G_m}{s \cdot C_p / G_m} \approx \frac{1 + s \cdot \tau}{s \cdot \tau}$$

- For a load capacitor

$$C_L \rightarrow \omega = G_m / C_L \approx \frac{C_L}{C_p} \approx \frac{C_L}{G_m \cdot \tau}$$

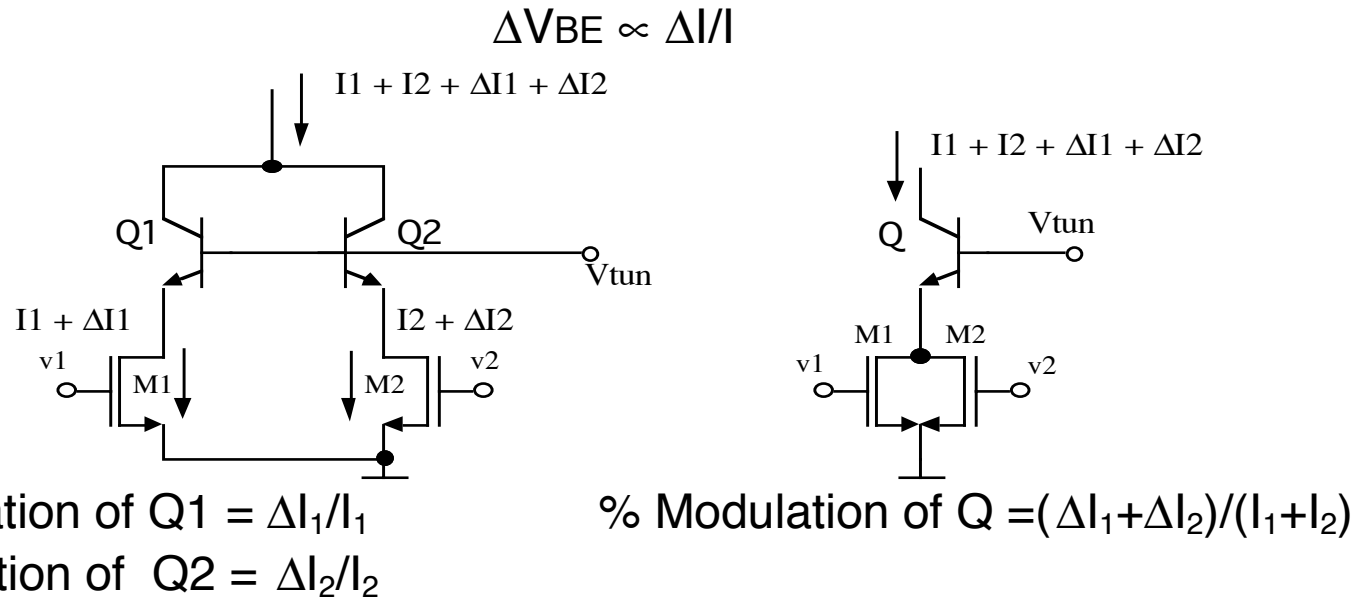


- In the PD structures the HF CMRR depends on the current mirror speed (τ)
- For τ sufficiently small \rightarrow PD solution may be better than FD
- At low frequency \rightarrow FD better than PD

Pseudo-Differential LV Gm-C Filters

☺ 2 - Linearity Performances

- The transconductor THD depends mainly on the V_{DS} variation due to the V_{BE} modulation

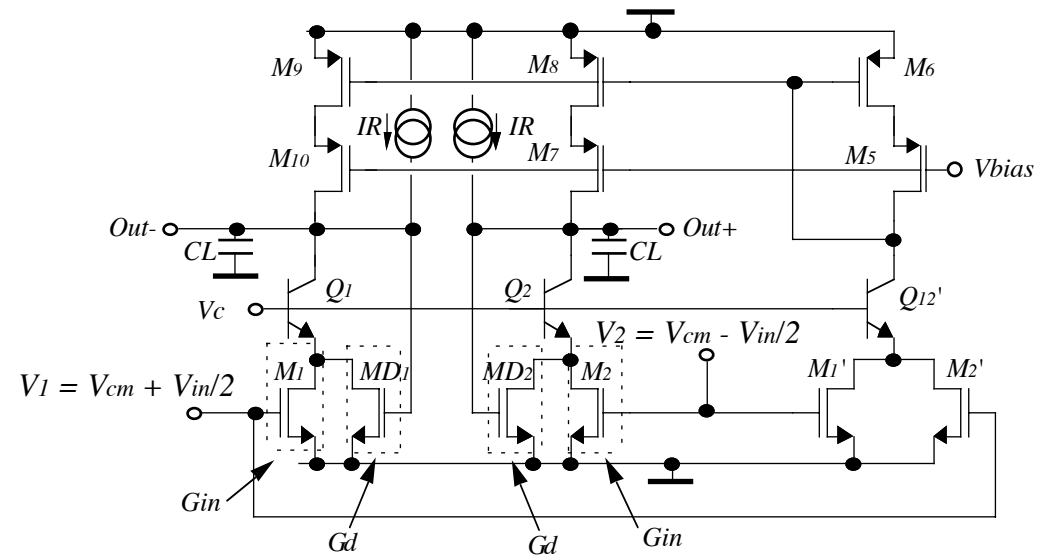
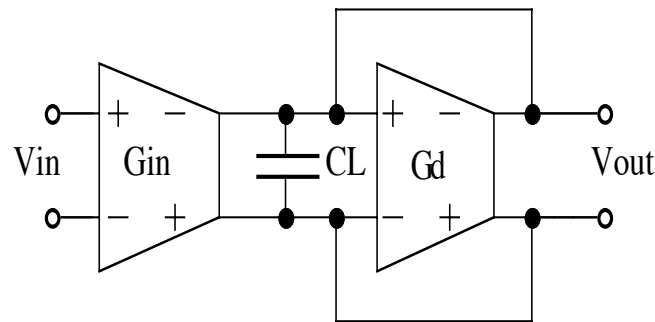


- If ΔI_1 and ΔI_2 are not in phase, the % modulation of Q is lower than each % of Q1 and Q2
- The scheme 2 shows a higher linearity at the same current level
 - (the same linearity at lower current level)

Pseudo-Differential LV Gm-C Filters

☺ 3+4 - Dumped integrator

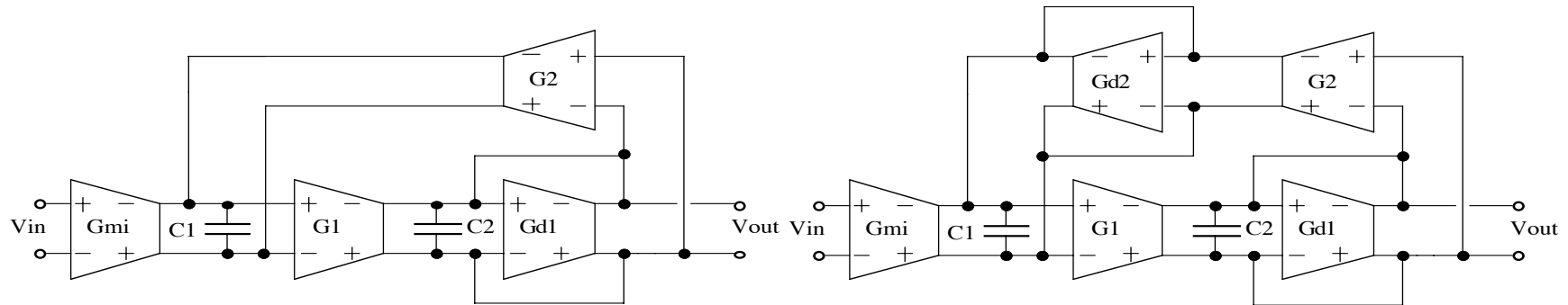
- A dumped integrator is obtained just adding two devices (MD1 and MD2)



- The dumping transconductor set the output common mode voltage (as a CMFB)
- The Biquadratic Cell uses a doubled-dumped structure for setting the CM voltage at both the nodes
- Using dumped integrator means operating with finite-gain transconductor

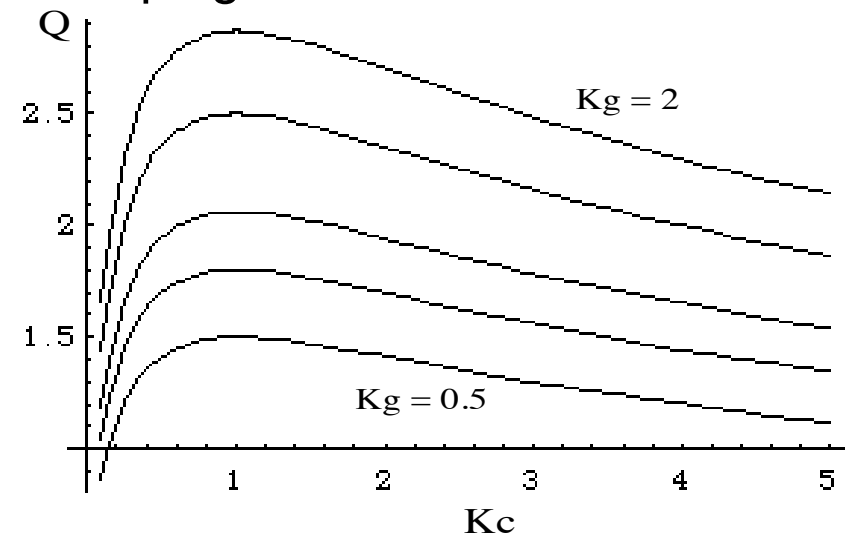
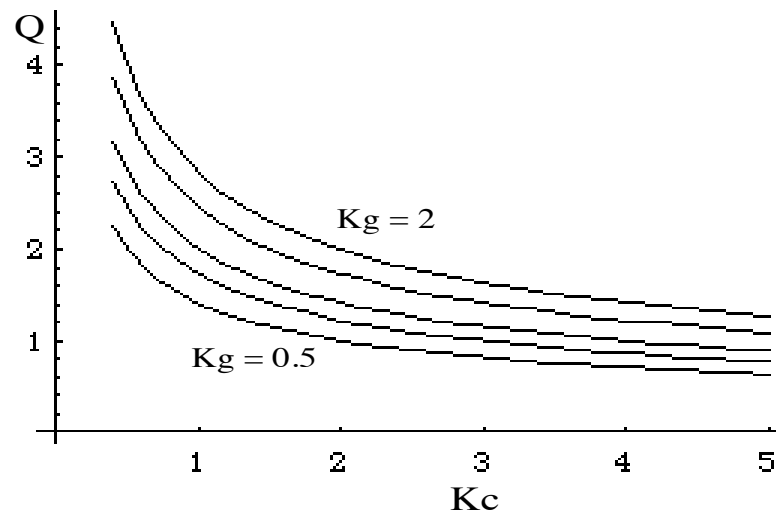
Pseudo-Differential LV Gm-C Filters

Performance sensitivity comparison: Q vs. capacitor ratio accuracy



■ Single dumping

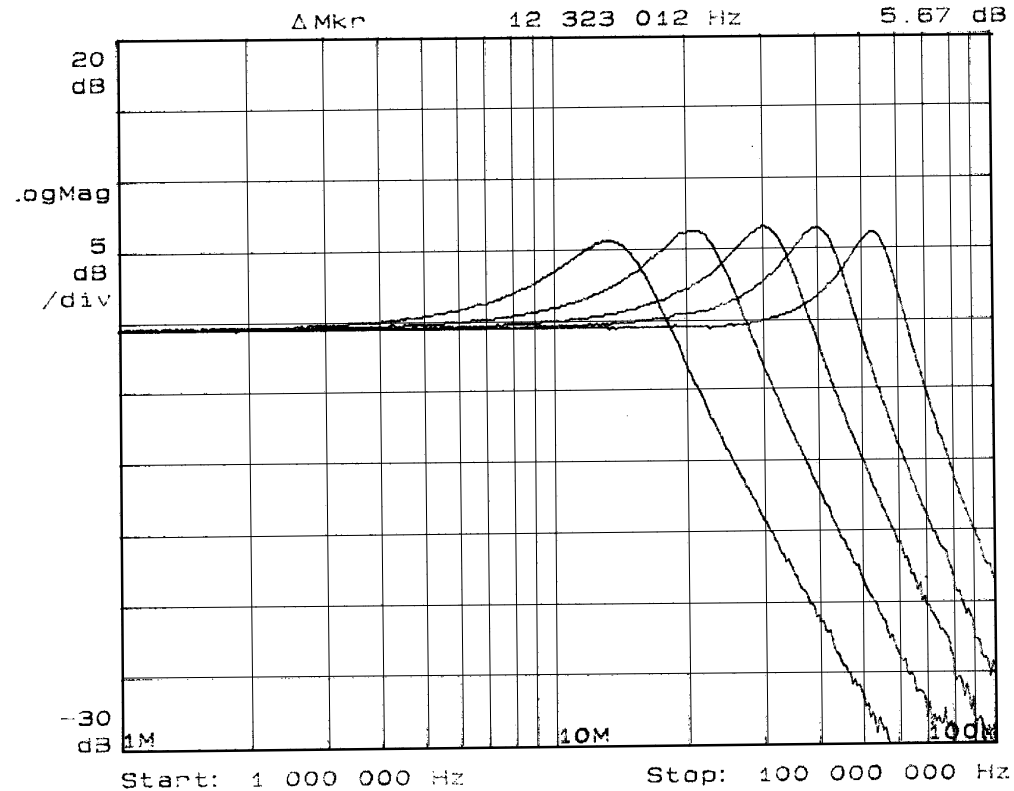
Double dumping



■ The double-dumped structure exhibits a low sensitivity of Q vs. k_c for $k_c \approx 1$

Pseudo-Differential LV Gm-C Filters

Frequency response with tuning

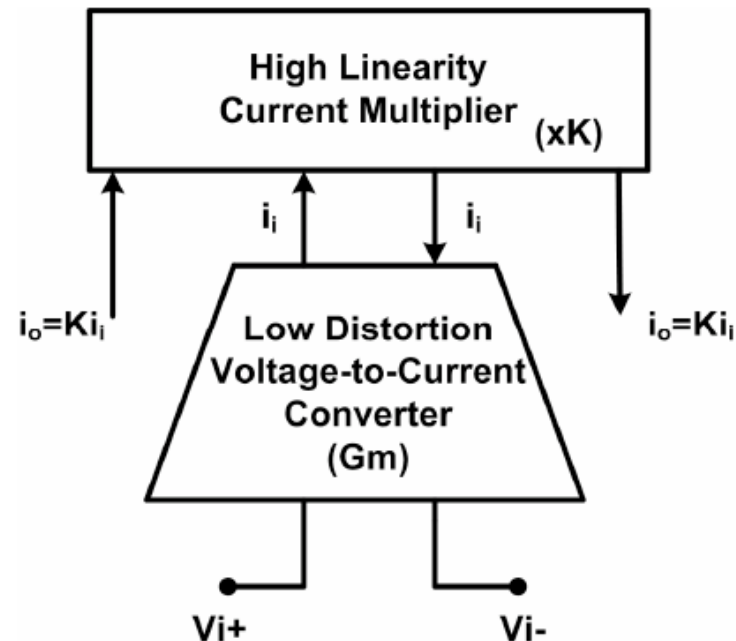


- A 12-55MHz tuning range is achieved
- The ± 0.4 dB peak-deviation is due to the parasitic pole effects (phase error)

LV Gm-C Filters

Fully-differential solution*

- Large linearity requires large V_{ov}
- An alternative solution is to separate the problem
 - Generate a high-linearity transconductor for small input signal
 - Implement additional current gain



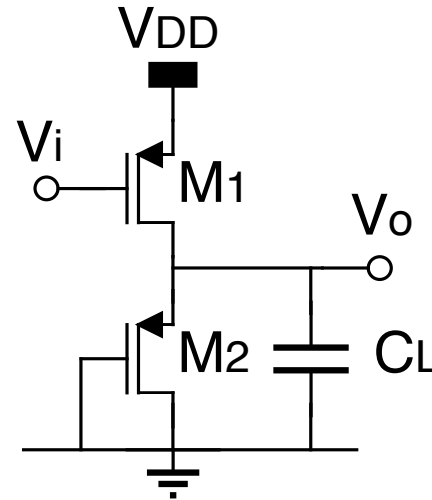
■ _____

* Tien-Yu Lo, "Low-Voltage Multi-Mode Gm-C Channel Selection Filter for Mobile Applications", CICC2007

Large Bandwidth CT Filters

Basic Gm-Gm-C filter

- 1st order cell



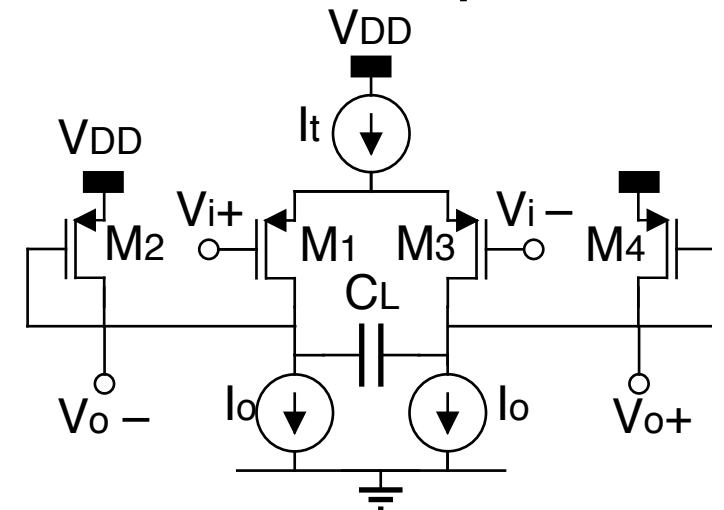
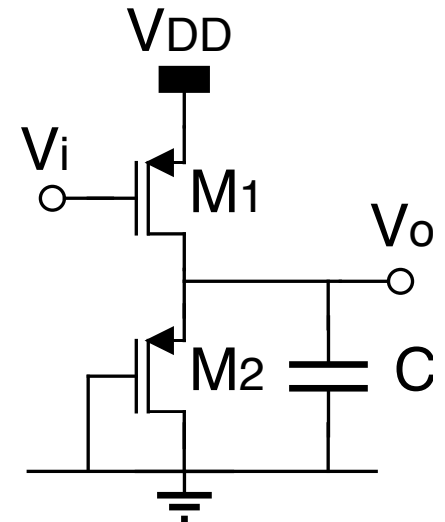
$$H(s) = \frac{V_o}{V_i} = -\frac{g_{m1}}{g_{m2}} \cdot \frac{1}{1 + s \cdot \frac{C_L}{g_{m2}}}$$

- MOS devices (M1 and M2) operates in saturation region

Large Bandwidth CT Filters

Basic Gm-Gm-C filter

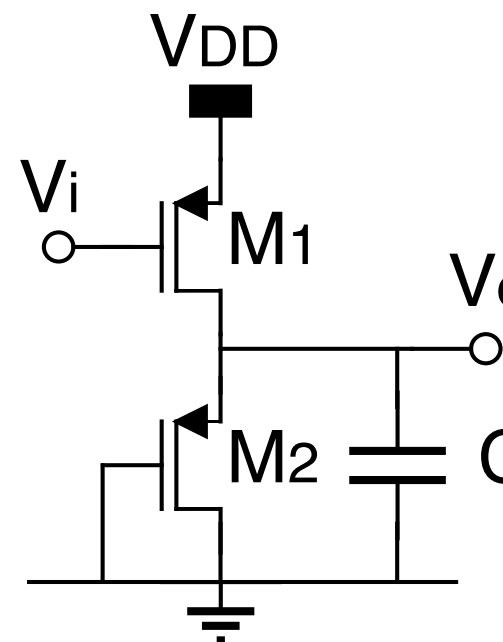
- 1st order cell – Key advantages
- Low-power consumption:
 - the same bias current is shared between the driver (M_1) and the load (M_2) device
- Accurate frequency response:
 - no non-dominant poles are present since only one node is present, and it corresponds to the desired pole
- No body effect
 - no threshold voltage variation, due to body effect occurs since only PMOS devices with $V_{SB}=0$ are present
- In FD version → No CMFB circuit
 - the output DC voltage is fixed by the V_{GS} of transistors M_5 and M_6
 - → No additional power consumption



Basic Gm-Gm-C filter

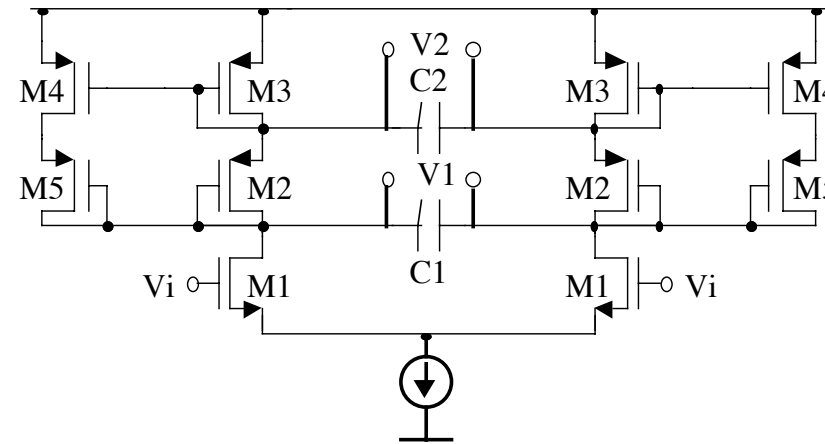
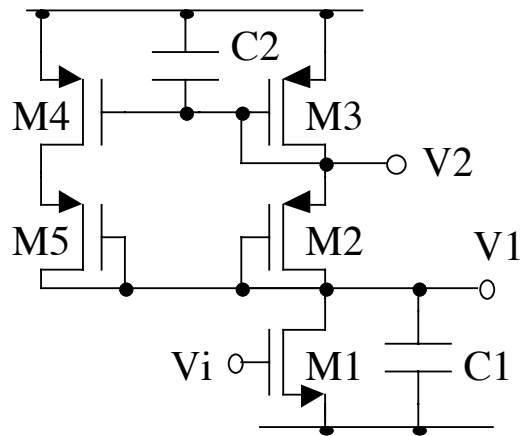
1st order cell – Key advantages

- Medium/High-linearity:
 - Driver device (M1) and load device (M2) are of the same type (PMOS)
 - Their characteristics are largely non linear,
 - BUT **the driver non-linearity** (g_{m1}) **is compensated by the opposite load non-linearity** ($\approx 1/g_{m2}$)
 - → large linear range can be achieved even with a reduced device overdrive.
 - Ex.: for a differential version, with $V_{OV} = V_{GS} - V_{TH} = V_{ov} \approx 450\text{mV}$, a THD = -50dB for a 800mVpp input signal @25MHz results.
 - In other solutions this result should be achieved by using a much larger V_{ov} .
 - → A smaller current and so a lower power is required



Basic Gm-Gm-C filter

2nd order cell



$$H_2(s) = \frac{V_2}{V_i} = - \frac{G_1 \cdot G_2}{s^2 \cdot C_1 \cdot C_2 + s \cdot (C_1 \cdot (G_3 + G_2) + C_2 \cdot G_2) + G_2 \cdot (G_3 + G_4)}$$

$$H_1(s) = \frac{V_1}{V_i} = - \frac{G_1 \cdot (G_2 + G_3 + sC_2)}{s^2 \cdot C_1 \cdot C_2 + s \cdot (C_1 \cdot (G_3 + G_2) + C_2 \cdot G_2) + G_2 \cdot (G_3 + G_4)}$$

- The MOS output impedance have been neglected since they should be much higher than node 1 and 2 impedance given by $1/G_m$

Basic Gm-Gm-C filter

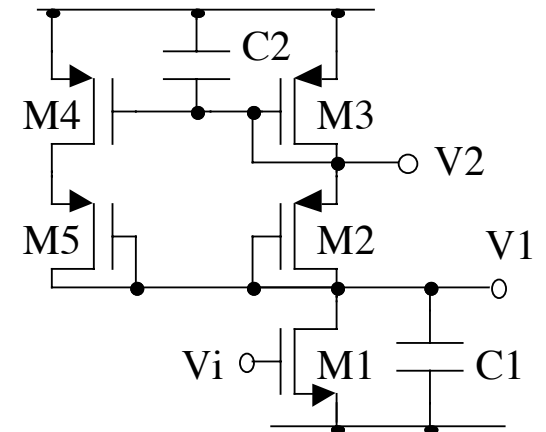
2nd order cell

$$H_2(s) = \frac{V_2}{V_i} = - \frac{G_1 \cdot G_2}{s^2 \cdot C_1 \cdot C_2 + s \cdot (C_1 \cdot (G_3 + G_2) + C_2 \cdot G_2) + G_2 \cdot (G_3 + G_4)}$$

- Assuming $G_2 = G_3$ (the same aspect ratio with same current), $G_4 = A \cdot G_3$ and $C_2 = k \cdot C_1$

$$\omega_0 = \frac{G_2}{C_1} \cdot \sqrt{\frac{1+A}{k}} \quad Q = \frac{\sqrt{k \cdot (1+A)}}{1+2 \cdot k}$$

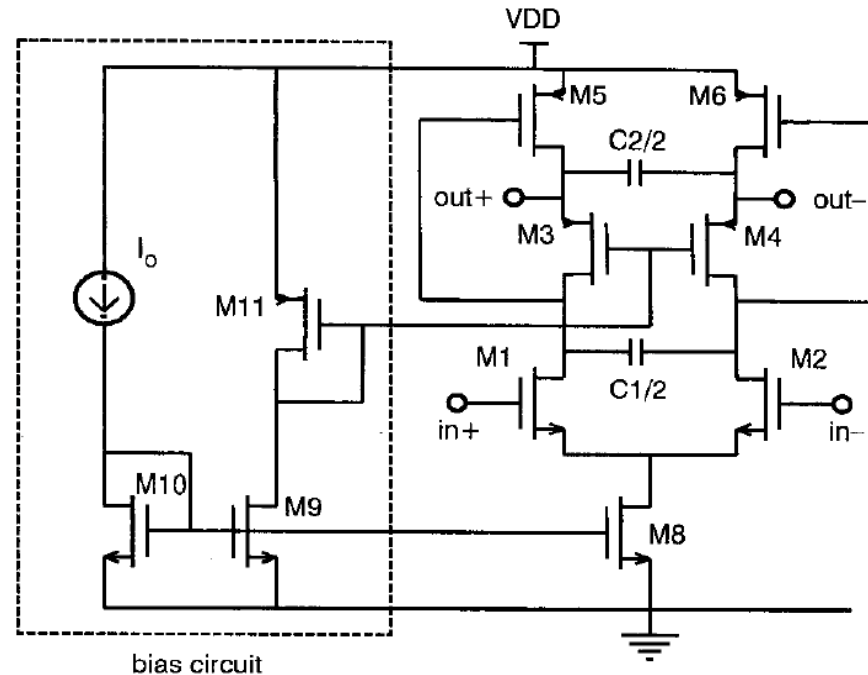
- The ω_0 depends from $G_2 \rightarrow$ tuned by the dc current level (quadratic law)
- The Q value depends only from aspects ratio \rightarrow constant w.r.t. tuning variation.
- ω_0 and Q depend only from PMOS device aspect parameters \rightarrow they are independent from technology variations
- M5 improves improve bias condition matching and consequently the current mirror accuracy between M3 and M4 is increased



Basic Gm-Gm-C filter

2nd order cell – II version

- For $g_{m3} \gg g_{ds5}$ and $g_{m5} \gg g_{ds1}$



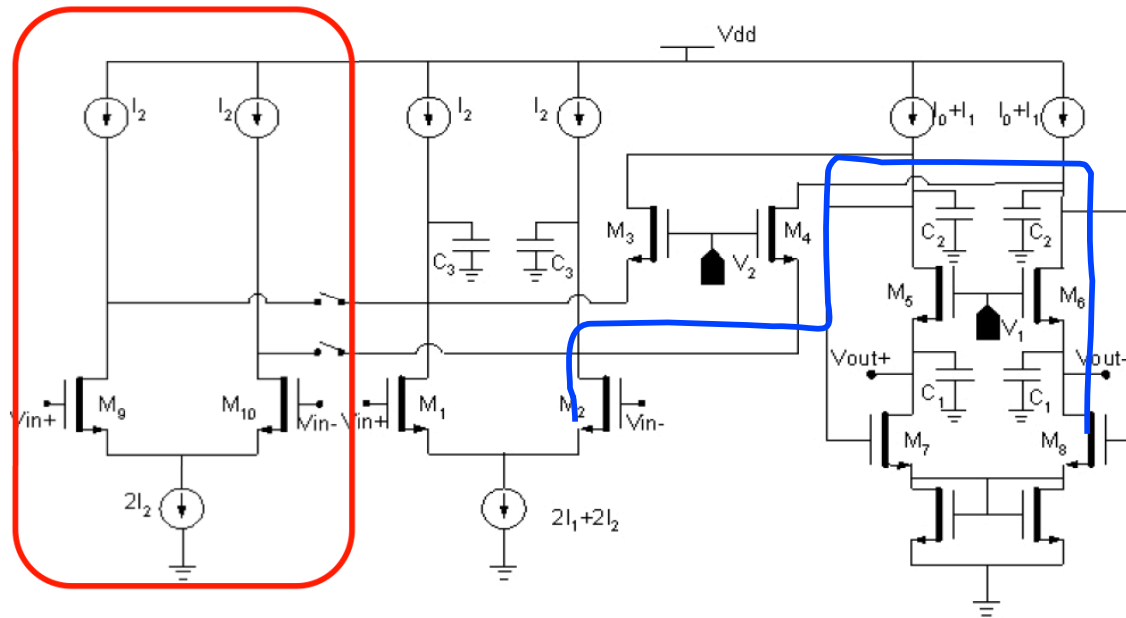
$$H(s) = \frac{V_o}{V_i} = - \frac{G_{m1} / G_{m3}}{s^2 \cdot C_1 \cdot C_2 / (G_{m3} \cdot G_{m5}) + s \cdot (C_1 / G_{m5}) + 1}$$

$$\omega_o = \sqrt{\frac{G_{m3} \cdot G_{m5}}{C_1 \cdot C_2}} \quad Q = \sqrt{\frac{G_{m5} \cdot C_2}{G_{m3} \cdot C_1}}$$

Basic Gm-Gm-C filter

3rd order cell – II version (ESSCIRC, 2007)

Additional input stage for gain control



Only NMC transistor in signal path

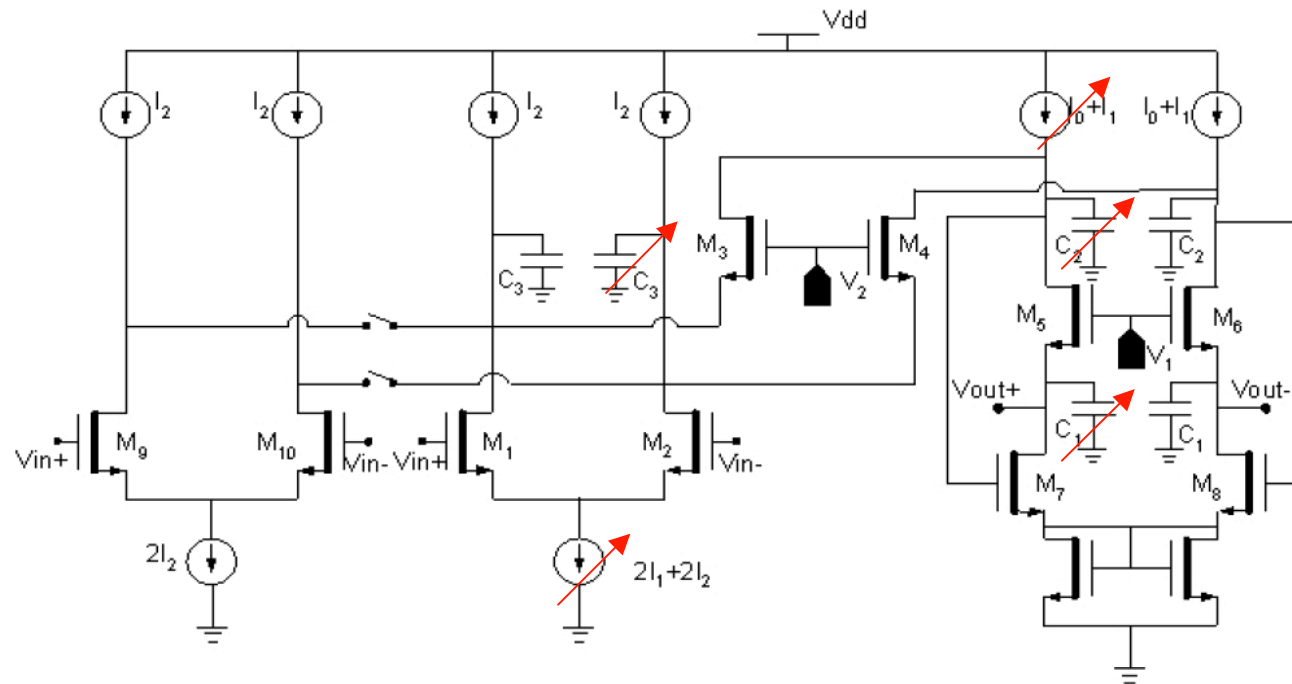
$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}/g_{m5}}{s^3 \frac{C_1 C_2 C_3}{g_{m3} g_{m5} g_{m7}} + s^2 \left(\frac{C_1 C_2}{g_{m3} g_{m7}} + \frac{C_3 C_2}{g_{m5} g_{m7}} \right) + s \left(\frac{C_1}{g_{m3}} + \frac{C_2}{g_{m7}} \right) + 1}$$

$$\omega_1 = -\frac{g_{m3}}{C_1} \quad \omega_{2/3} = \sqrt{\frac{g_{m5} \cdot g_{m7}}{C_2 \cdot C_3}} \quad Q_{2/3} = \sqrt{\frac{C_3 \cdot g_{m7}}{C_2 \cdot g_{m5}}}$$

Basic Gm-Gm-C filter

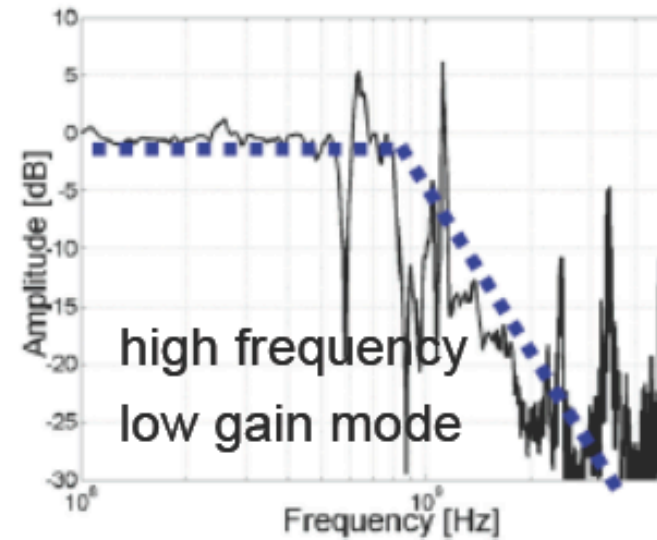
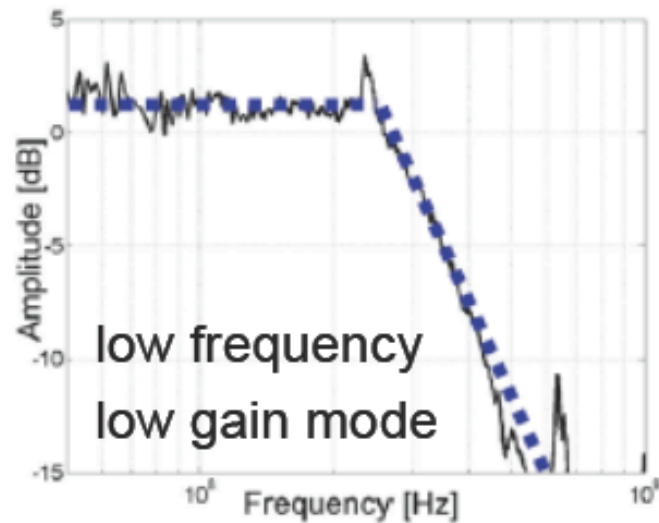
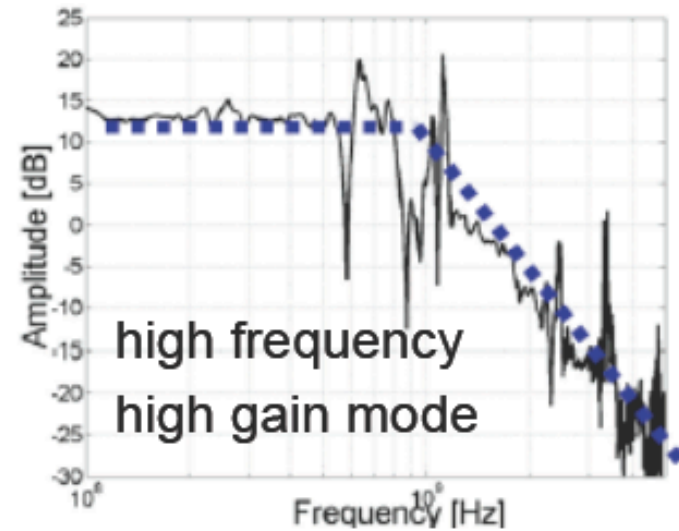
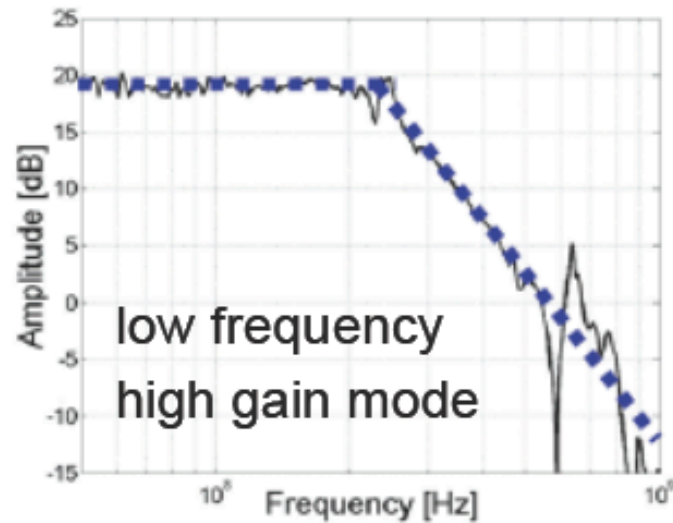
Tuning approach

- The filter cut-off frequency is programmed from 250MHz to 1GHz by:
 - Using capacitors arrays
 - Regulating the bias current (4 μ A-10 μ A).
 - → Power saving at 250MHz cut-off frequency
 - → Fine tuning to compensate the technological spread



Basic Gm-Gm-C filter

Experimental results



Basic Gm-Gm-C filter

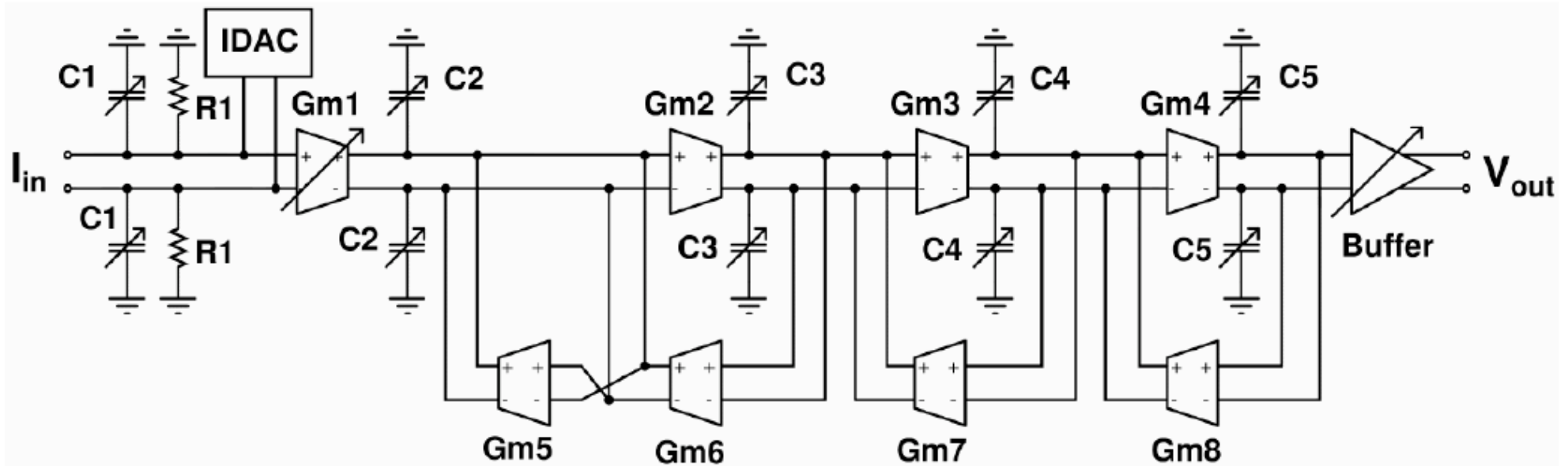
Experimental results

<i>Case</i>	<i>I</i>	<i>II</i>	<i>III</i>	<i>IV</i>
f_o [MHz]	250		1000	
DC-Gain [dB]	2	19	0	14
IR-Noise Level [nV/ $\sqrt{\text{Hz}}$] (simulated)	18	4.5	10	2.5
IR-In-band Noise [μV_{rms}] (simulated)	285	71	320	80
THD@100mVpp [dB] (simulated)	-30	-30	-32	-37
SNR [dB]	45	53	44	53
Power consumption [mW]	0.21	1.2	0.59	3.2

Alternative UWB filter

Gm-C approach (Saari, ISSCC2007)

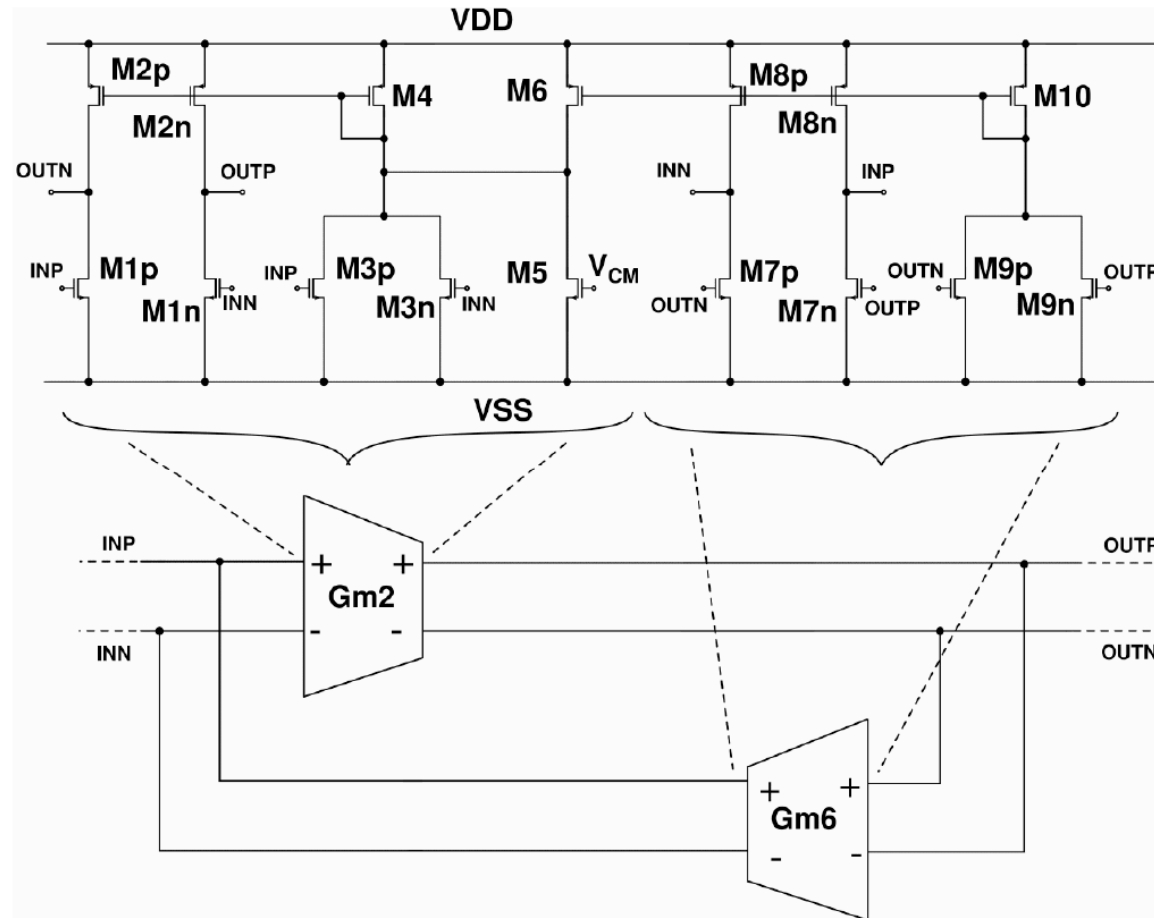
- Block diagram of the implemented filter.



Alternative UWB filter

Gm-C approach (Saari, ISSCC2007)

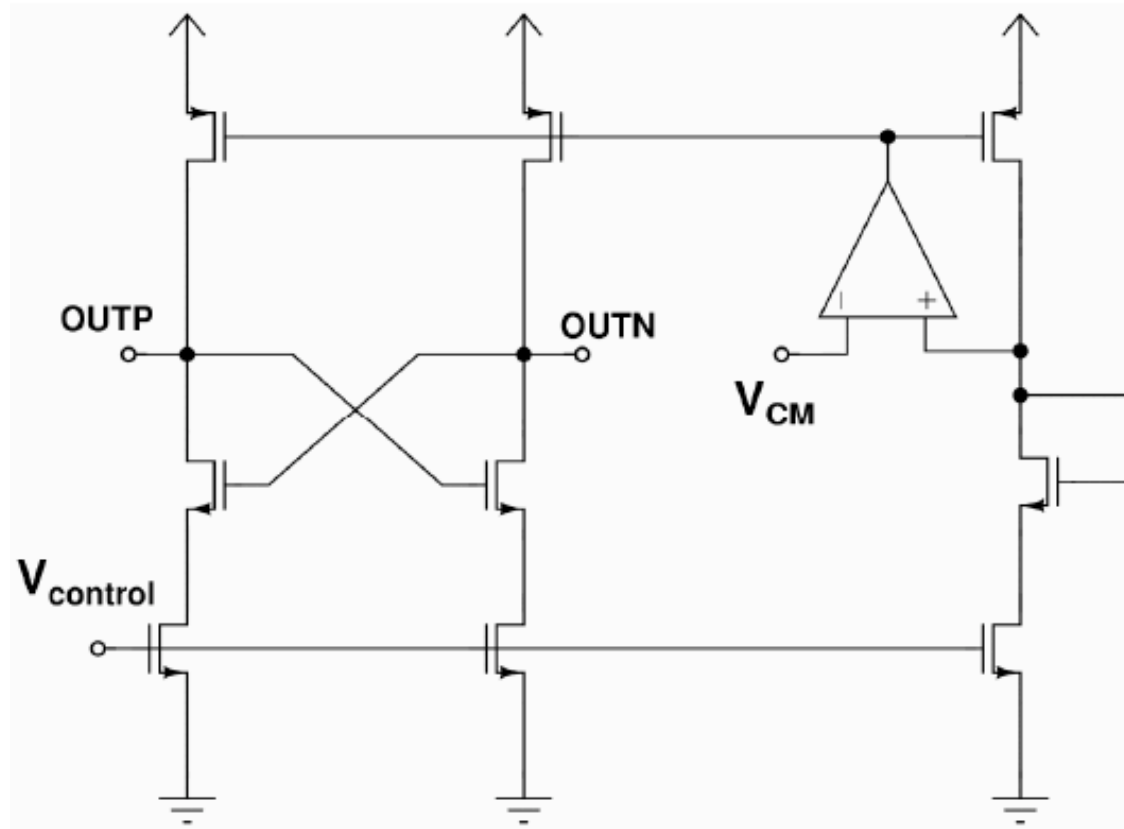
- Transconductor with CMFF and CMFB circuit



Alternative UWB filter

Gm-C approach (Saari, ISSCC2007)

- Negative-resistance circuit



Alternative UWB filter

Gm-C approach (Saari, ISSCC2007)

- Measured performance

Technology	0.13 μ m CMOS
Filter order	5
Supply voltage	1.2V
Voltage gain at 10MHz	12.9 to 47.6dB
Passband edge frequency	240MHz
Integrated input-referred noise (2 to 233MHz)	117 μ V _{rms}
Input-referred noise density	7.7nV/ \sqrt Hz
IIP3 (in-band, $f_1 = 30$ MHz, $f_2 = 50$ MHz)	-48.2dBV
IIP3 (out-of-band, $f_1 = 400$ MHz, $f_2 = 790$ MHz)	-8.2dBV
IIP2 (out-of-band, $f_1 = 410$ MHz, $f_2 = 400$ MHz)	+18.2dBV
Power consumption	24mW
Die area without pads	0.34mm ²

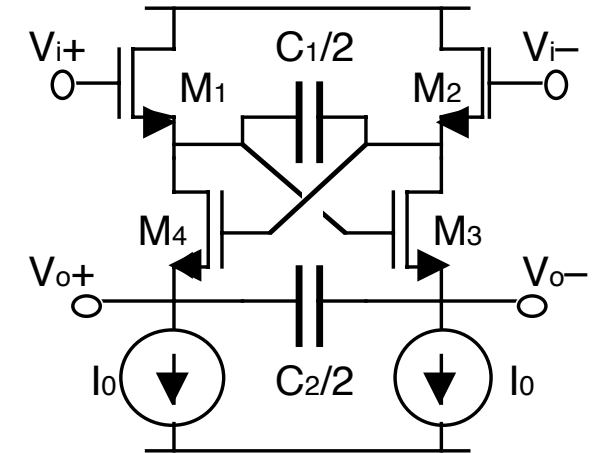
Source-follower based filters

Structure & Transfer function

- Fully-differential 2nd-order lowpass filter
- A single-branch structure
- ‘Composite’ source-follower (with an ideal unitary dc-gain)
- A positive feedback (M₄&M₃, always stable due to the presence of the MOS output impedance) internal to the source follower (M₄&M₃) synthesizes the complex-poles
- For $g_{m1}=g_{m4}=g_{m2}=g_{m3}$, the filter transfer function is:

$$H(s) = -\frac{1}{s^2 \cdot \frac{C_1 \cdot C_2}{g_{m1}^2} + s \cdot \frac{C_1}{g_{m1}} + 1}$$

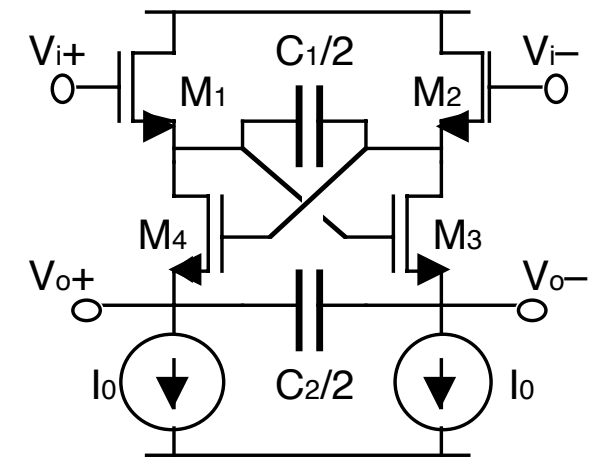
$$\omega_0 = 2 \cdot \pi \cdot f_0 = \frac{g_{m1}}{\sqrt{C_1 \cdot C_2}}; \quad Q = \sqrt{\frac{C_2}{C_1}}; \quad |K| = 1;$$



Source-follower based filters

Linearity performance

- As any feedback structure
- The linearity improves with a larger closed-loop gain
 - $G_{\text{loop}} = g_m \cdot R_{\text{out}}$
 - R_{out} is the I_o output impedance
 - g_m is the input device transconductance
 - → A larger g_m value (achieved for a lower V_{ov}) gives a better linearity.



This differs from Active-RC and G_m -C filters, where the linearity is improved for a larger V_{ov} of the input devices

- Minimizing V_{ov} corresponds to reduce the current level (and then the power consumption) to achieve a given g_m value.
 - → Power reduction for the same linearity

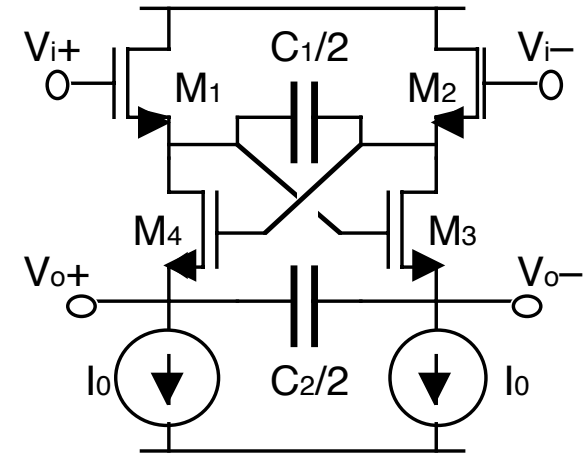
Source-follower based filters

Linearity performance

- A large g_m with a lower current features also excellent noise performance
 - A larger capacitor for a given pole frequency is used giving more robustness w.r.t. parasitic capacitance

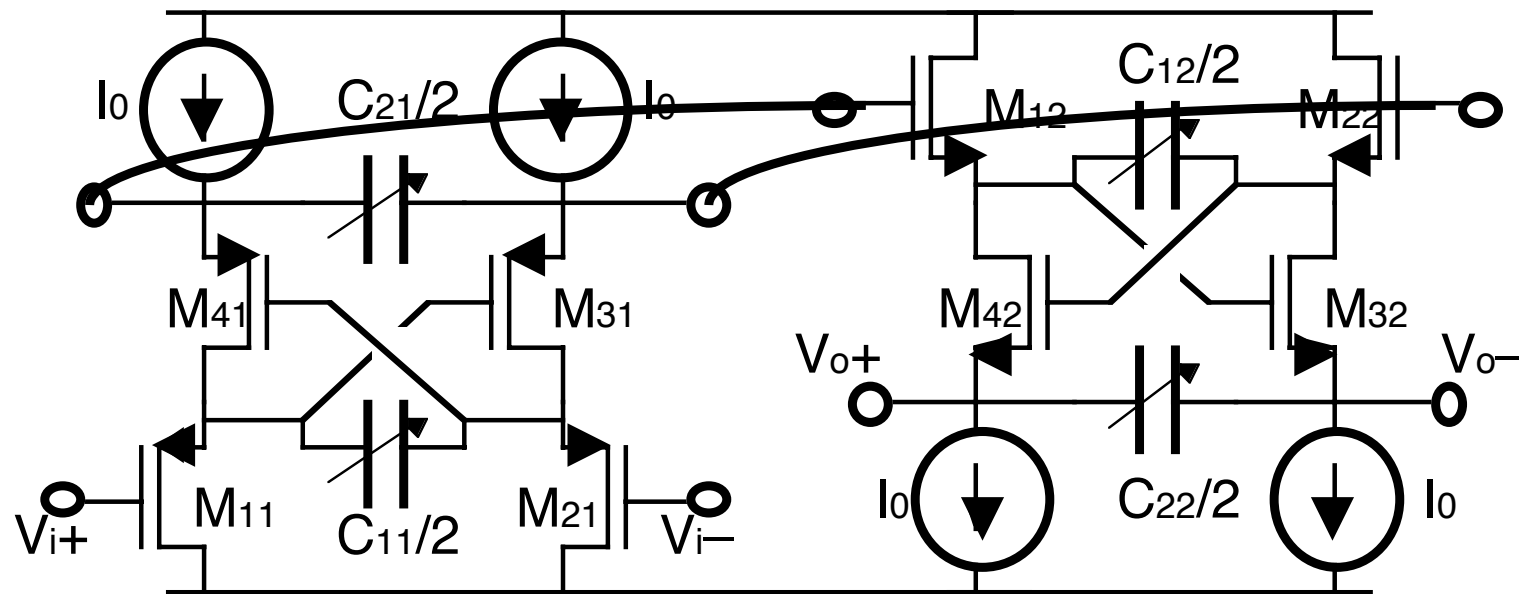
$$V_{DDmin} = V_{sat} + V_{GS1} + V_{GS3} + V_{swing} + V_{sat}$$

- For a $0.18\mu\text{m}$ technology, assuming $V_{sat} = 250\text{mV}$, $V_{GS1} = V_{GS3} = 450\text{mV}$ (to maximize g_m), $V_{swing} = 400\text{mV}$ (the peak-to-peak single ended swing), the $V_{DDmin} = 1.8\text{V}$
- Additional advantages for the power consumption reduction:
 - No circuital parasitic poles, avoiding the power cost of pushing non-dominant singularities at high frequency.
 - No CMFB circuit: the output CM voltage is fixed to be two V_{in-}
 $V_{outCM} + V_{GS1} + V_{GS3}$
 - Low output impedance



Source-follower based filters

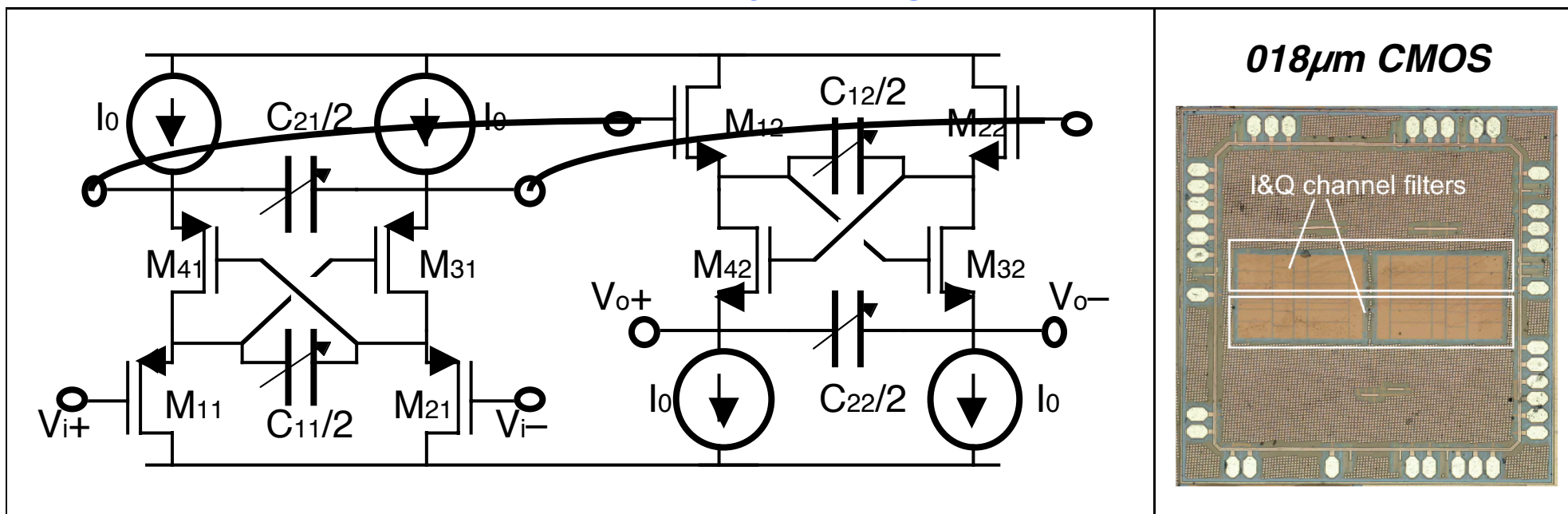
Cascading biquads



- The 1st cell is made up of PMOS's
- The 2nd one is made up of NMOS's
- Cascading PMOS and NMOS structures compensates the input-to-output CM voltage difference, typical of a source-follower

Source-follower based filters

Prototype design

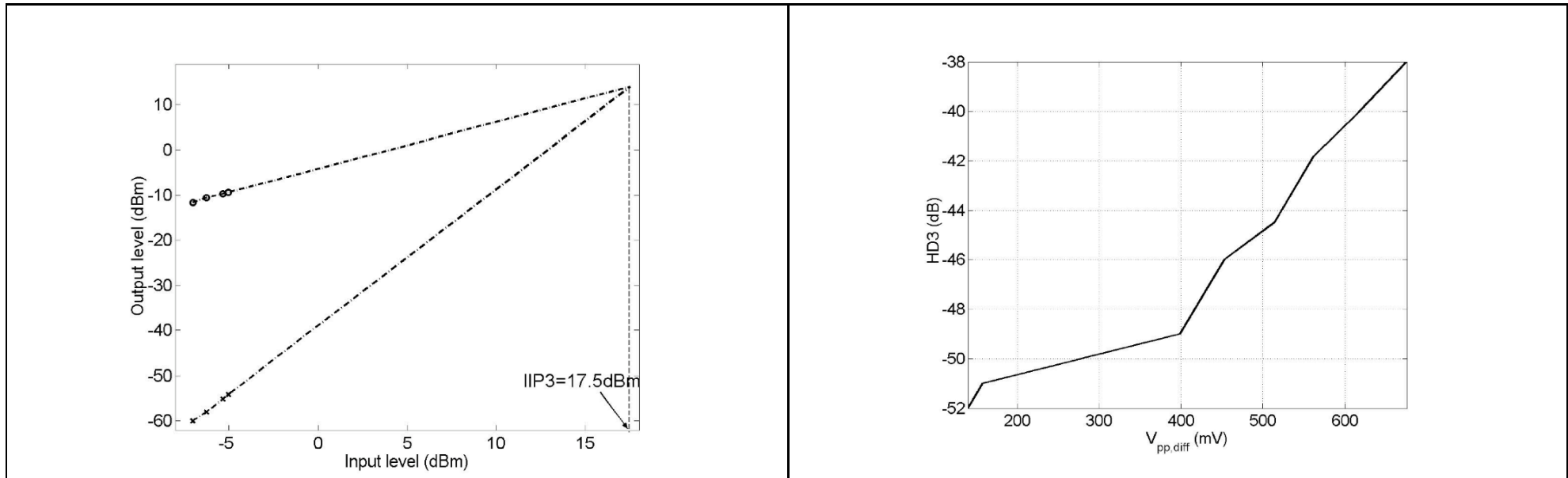


■ Design guidelines:

- All MOS devices are with $L=0.5\mu\text{m}$ to reduce output impedance effects.
- All capacitors are realized with digitally-controlled arrays.
- The filter transfer function pole is then programmable in the $\pm 40\%$ range with a 4-bit word, compensating technology, temperature and parasitic capacitance effects.
 - With tuning, the bias current (I_0) remains constant, fixing the V_{ov} and, as a consequence, the loop-gain and the linear range

Source-follower based filters

Experimental results (ISSCC06)



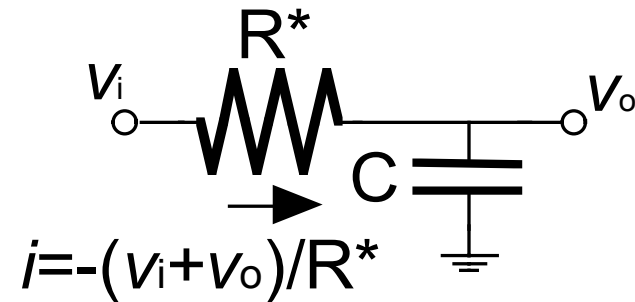
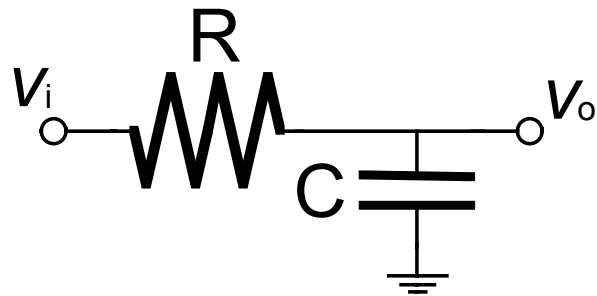
4th order Lowpass filter performance summary

Technology	0.18μm CMOS	V_{DD}	1.8V
Bandwidth	10MHz	Tuning	$\pm 40\%$
In-band IIP3	17.5dBm	HD3 (@600mV _{pp,diff})	-40dB
1dBcp	5dBm		
	1.15V _{pp,diff}		
IRN	7.5nV/ $\sqrt{\text{Hz}}$	Integrated input noise	24 μ V _{rms}
Power	4.1mW (2.24mA)	DR (@-40dB)	79dB

Diode-C filters

High-order filter

- Let's define two building blocks

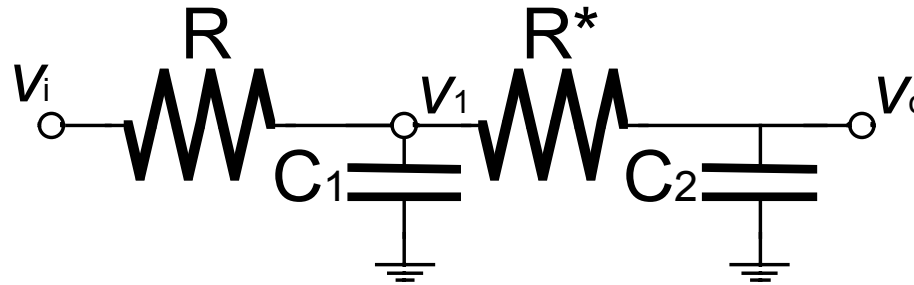


Positive and negative RC cells

$$i = -\frac{V_i - V_o}{R^*}$$

Diode-C filters

2nd-order filter

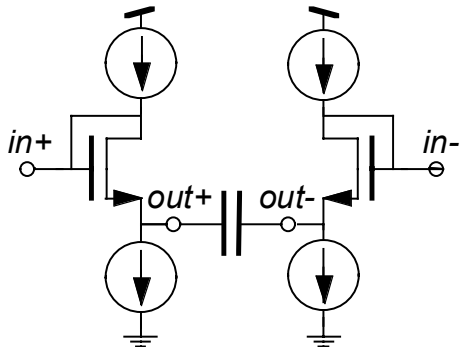
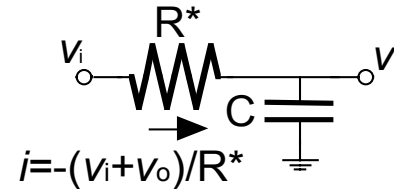
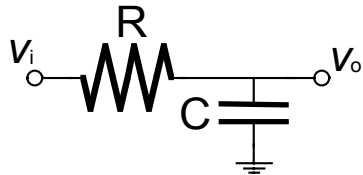
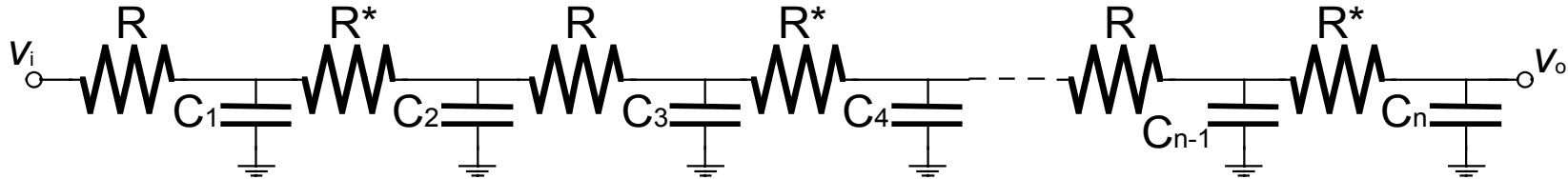


$$\begin{cases} \frac{V_i - V_1}{R} = s \cdot C_1 \cdot V_1 + \left[-\frac{V_1 + V_o}{R^*} \right] \\ \left[-\frac{V_1 + V_o}{R^*} \right] = s \cdot C_2 \cdot V_o \end{cases}$$

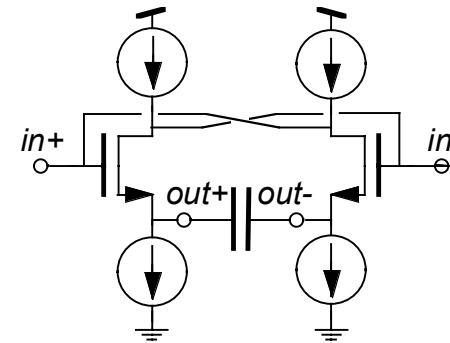
$$H(s) = \frac{V_o}{V_i} = \frac{1}{s^2 \cdot C_1 \cdot C_2 \cdot R^2 + s \cdot C_1 \cdot R + 1}$$

Diode-C filters

High-order filter



NMOS Positive source-follower RC cell

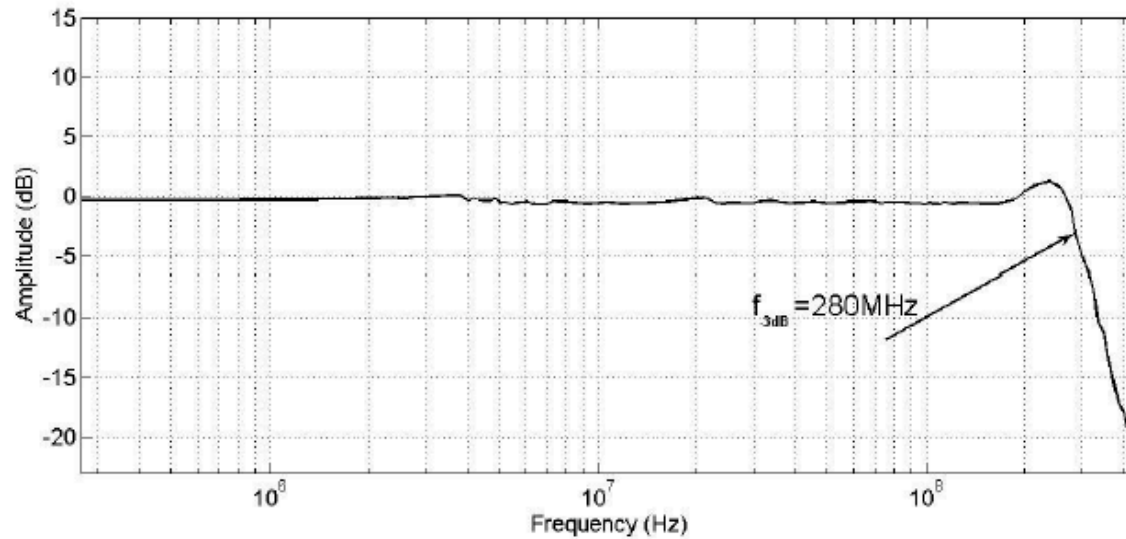
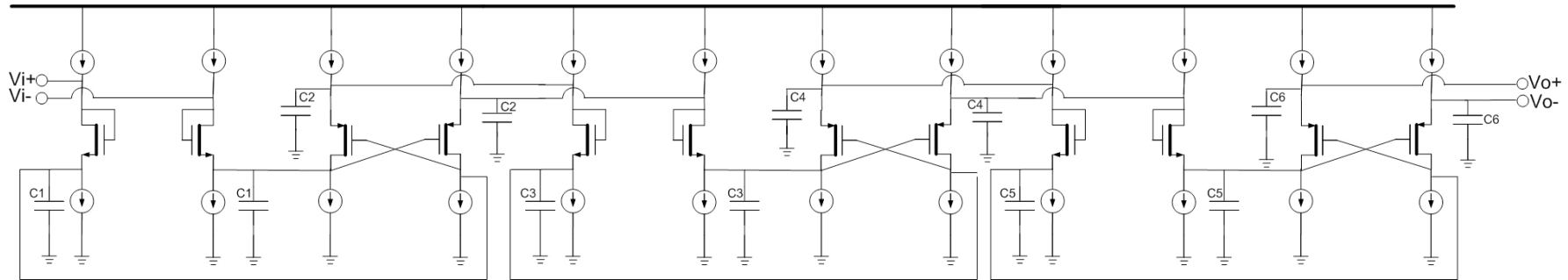


NMOS Negative source-follower RC cell

$$V_{min} = 3 \cdot V_{ov} + V_{th} + V_{swing}$$

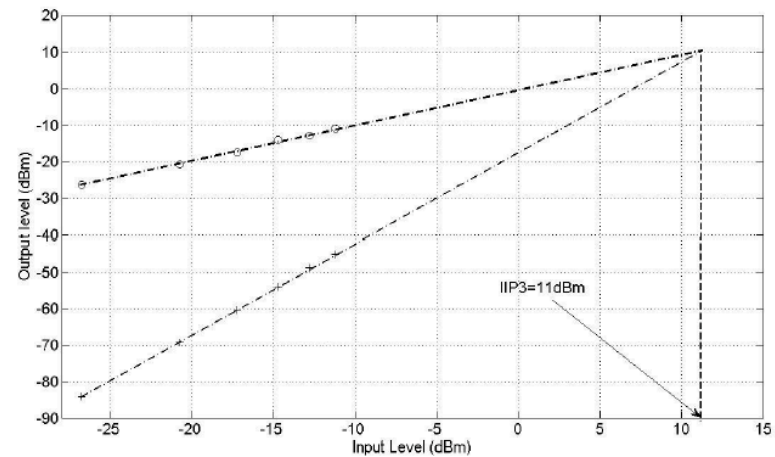
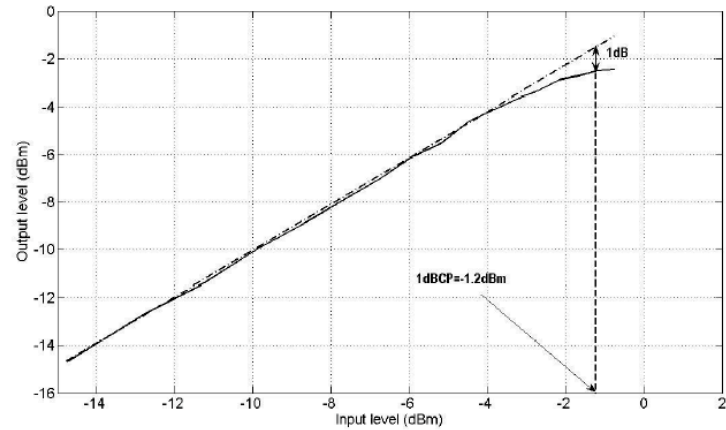
Diode-C filters

A 6th-order filter



Diode-C filters

A 6th-order filter



Diode-C filters

A 6th-order filter

Table I - Summary of the filter performance

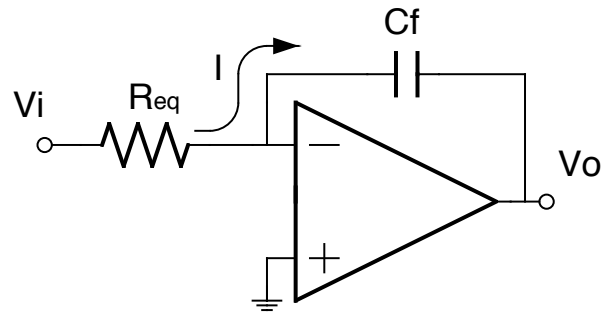
<i>Parameter</i>	<i>Value</i>
Technology	CMOS 0.13μm
Supply voltage	1.2V
Current consumption	100μA
DC-gain	0dB
Cut-off frequency	280MHz
IRN	22nV/\sqrtHz
1dBcp	-1.2dBm
IIP3	11dBm
THD(@510mV_{pp}, 1MHz)	-31dB

LV Analog Design in scaled CMOS technology

Outline

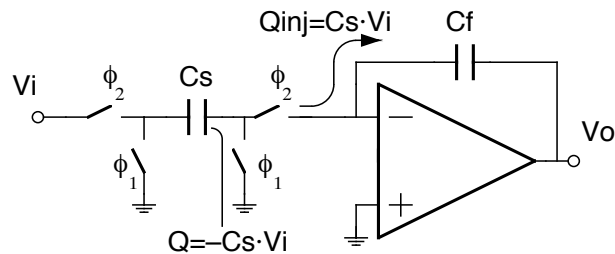
- Introduction
 - Basic CMOS operation ←←←
 - CMOS technology scaling trends
 - What is LV
 - LV Analog design
 - LV at transistor level
 - LV at circuit level
 - Current mirror
 - Opamp design
 - Basic bandgap design
 - LV at system level
 - Active-RC filter design
 - Gm-C filter design
 - SC circuit design

SC Key Concept



$$I = \frac{V_i}{R_{eq}}$$

$$R_{eq} = \frac{T_s}{C_s}$$



$$I_{mean} = C_s \cdot \frac{V_i}{T_s}$$

- This approximation is valid for V_i slowly variable with respect to the clock period
- The time constant in SC circuit are fixed by:

$$\tau = R_{eq} \cdot C_f = T_s \cdot \frac{C_f}{C_s}$$

- Thus it depends on:
 - sampling period (T_s): controlled by external quartz oscillators
 - capacitor ratio (C_f/C_s): accurate in integrated circuits

SC history

Who invented SC concept ???

Maxwell, 1867 !!!

The capacity of the condenser is thus defined by the following quantities:—

T , the time of vibration of the magnet from rest to rest.

R , the resistance of the coil.

θ , the extreme limit of the swing produced by the discharge.

ϕ , the constant deflexion due to the current through the coil R .

This method was employed by Professor Fleeming Jenkin in determining the capacity of condensers in electromagnetic measure*.

If c be the capacity of the condenser in electrostatic measure, as determined by comparison with a condenser whose capacity can be calculated from its geometrical data, $c = v^2 C$.

$$\text{Hence } v^2 = \pi R \frac{c}{T^2} \frac{\tan \phi}{2 \sin \frac{1}{2} \theta}.$$

The quantity v may therefore be found in this way. It depends on the determination of R in electromagnetic measure, but as it involves only the square root of R , an error in this determination will not affect the value of v so much as in the methods of Arts. 772, 773.

Intermittent Current.

775.] If the wire of a battery-circuit be broken at any point, and the broken ends connected with the electrodes of a condenser, the current will flow into the condenser with a strength which diminishes as the difference of the potentials of the plates of the condenser increases, so that when the condenser has received the full charge corresponding to the electromotive force acting on the wire the current ceases entirely.

If the electrodes of the condenser are now disconnected from the ends of the wire, and then again connected with them in the reverse order, the condenser will discharge itself through the wire, and will then become recharged in the opposite way, so that a transient current will flow through the wire, the total quantity of which is equal to two charges of the condenser.

By means of a piece of mechanism (commonly called a Commutator, or *wippe*) the operation of reversing the connexions of the condenser can be repeated at regular intervals of time, each interval being equal to T . If this interval is sufficiently long to

* Report of British Association, 1867, pp. 463-468.

allow of the complete discharge of the condenser, the quantity of electricity transmitted by the wire in each interval will be $2EC$, where E is the electromotive force, and C is the capacity of the condenser.

If the magnet of a galvanometer included in the circuit is loaded, so as to swing so slowly that a great many discharges of the condenser occur in the time of one free vibration of the magnet, the succession of discharges will act on the magnet like a steady current whose strength is $\frac{2EC}{T}$.

If the condenser is now removed, and a resistance coil substituted for it, and adjusted till the steady current through the galvanometer produces the same deflexion as the succession of discharges, and if R is the resistance of the whole circuit when this is the case,

$$\frac{E}{R} = \frac{2EC}{T}; \quad (1)$$

or
$$R = \frac{T}{2C}. \quad (2)$$

We may thus compare the condenser with its commutator in motion to a wire of a certain electrical resistance, and we may make use of the different methods of measuring resistance described in Arts. 345 to 357 in order to determine this resistance.

776.] For this purpose we may substitute for any one of the wires in the method of the Differential Galvanometer, Art. 346, or in that of Wheatstone's Bridge, Art. 347, a condenser with its commutator. Let us suppose that in either case a zero deflexion of the galvanometer has been obtained, first with the condenser and commutator, and then with a coil of resistance R_1 in its place, then the quantity $\frac{T}{2C}$ will be measured by the resistance

of the circuit of which the coil R_1 forms part, and which is completed by the remainder of the conducting system including the battery. Hence the resistance, R , which we have to calculate, is equal to R_1 , that of the resistance coil, together with R_2 ; the resistance of the remainder of the system (including the battery), the extremities of the resistance coil being taken as the electrodes of the system.

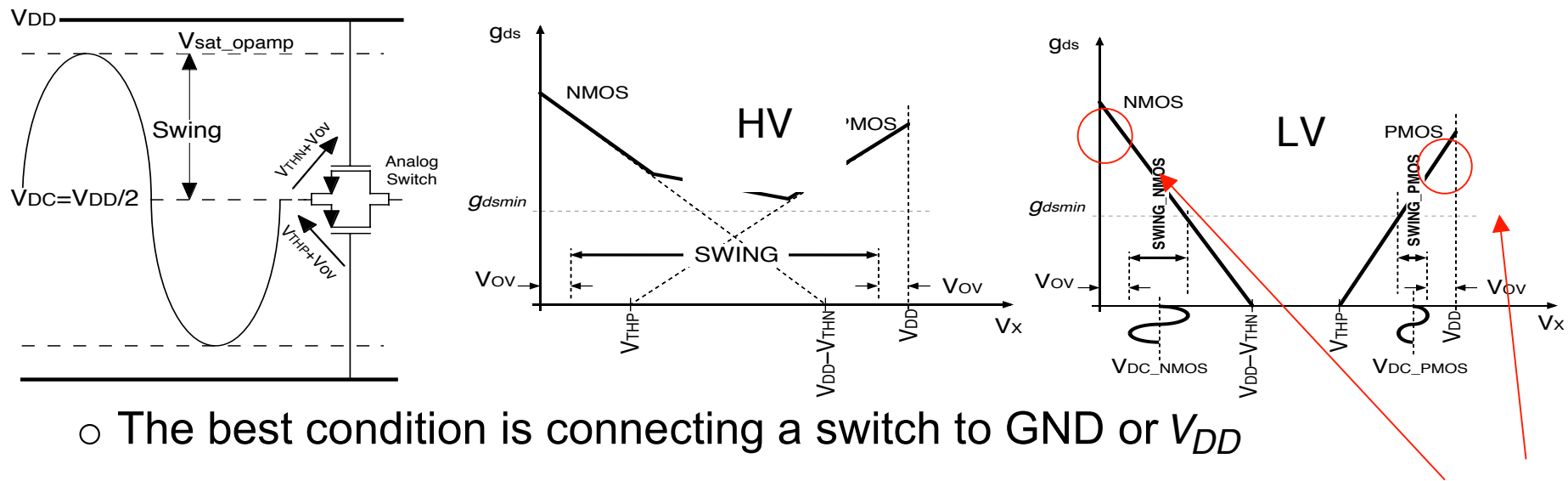
In the case of the differential galvanometer and Wheatstone's Bridge it is not necessary to make a second experiment by substituting a resistance coil for the condenser. The value of

$R_{eq} =$

LV Switched-Capacitor

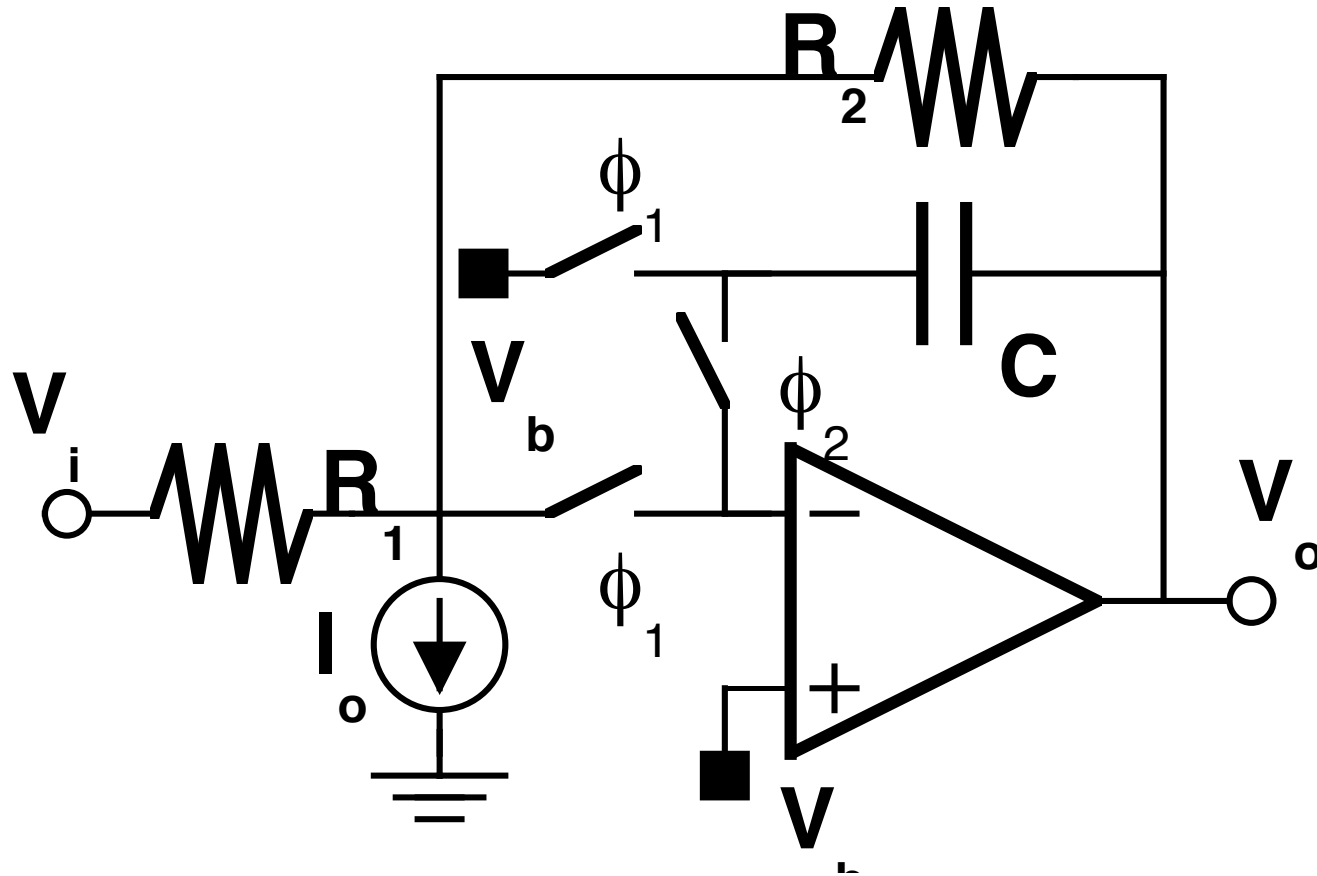
Building blocks

- Capacitors
 - OK
- Switches
 - With reduced clock amplitude proper operation must be guaranteed for all the signal swing



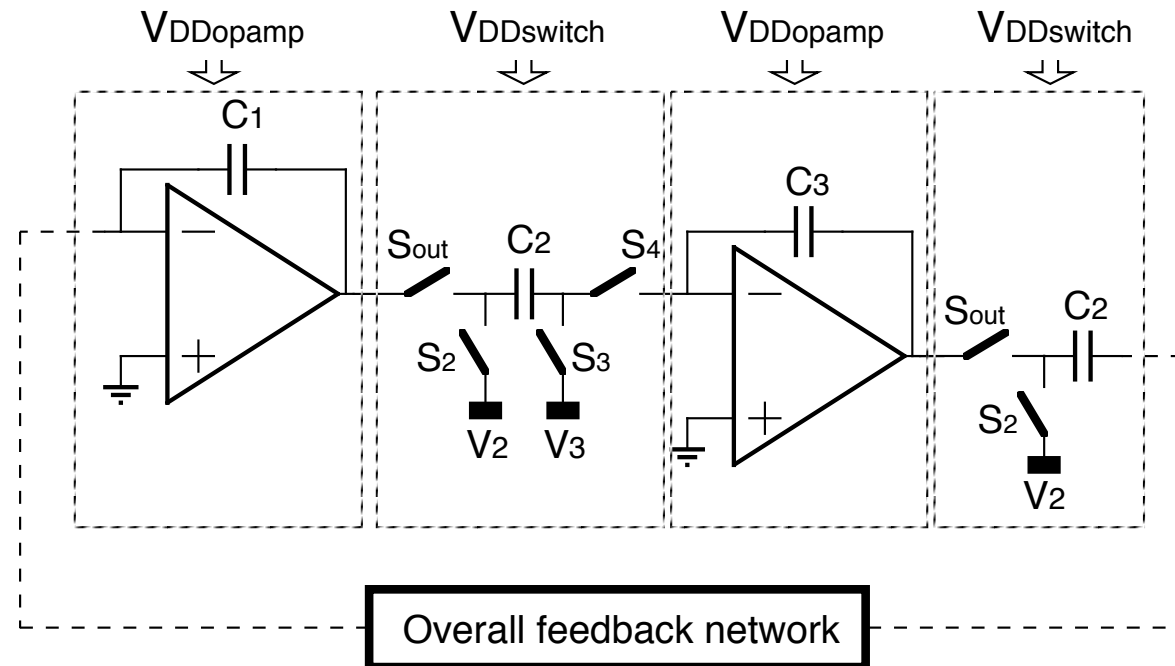
- Opamps:
 - New structures to operate at reduced supply with rail-to-rail output swing

LV Sampler



LV SCN

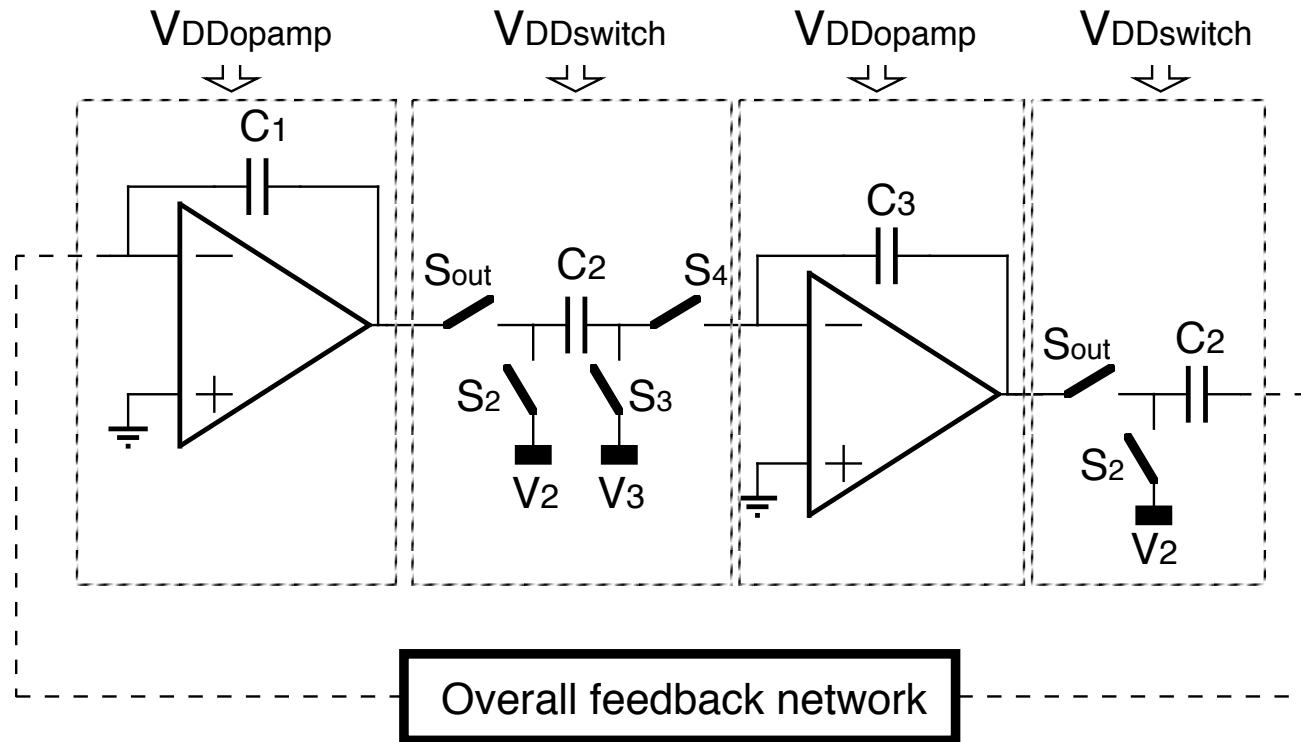
- | | |
|---|--|
| Standard design at low V_{DD} | } => No rail-to-rail but no new research |
| <ul style="list-style-type: none"> • Supply voltage multiplication • Clock voltage multiplication • Switched opamp technique | } => Rail-to-rail but new research |



- For $V_{out_DC} = V_{DD}/2$ (max. output swing), S_{out} operates in critical region
- Proper operations for S_2 , S_3 and S_4 are obtained with proper choice of V_2 , V_3 , and V_4

On-chip supply multiplication*

- Concept
- An auxiliary supply V_{DDmult} generated on-chip is used to power the complete SC filter ($V_{DDswitch}=V_{DDopamp}=V_{DDmult}$).



■ _____

* G. Nicollini, A. Nagari, P. Confalonieri, and C. Crippa, "A -80dB THD, 4Vpp switched-capacitor filter for a 1.5V battery-operated systems", *IEEE J. of Solid-State Circuits*, pp. 1214-1219, August 1996



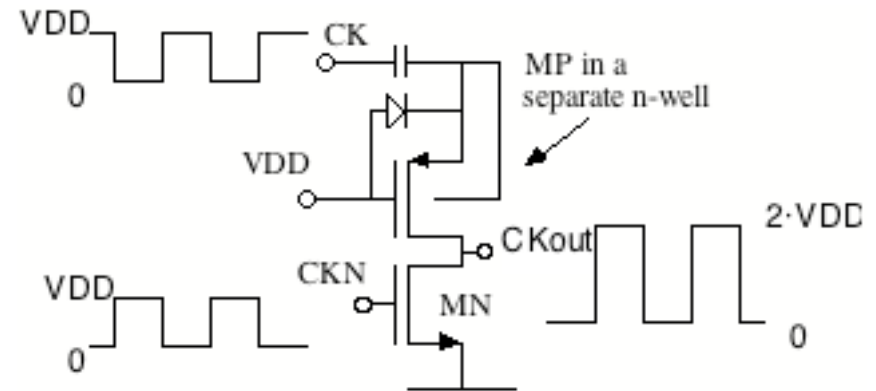
On-chip supply multiplication

- Advantages
- *Re-use know-how*: the SC designer re-uses available analog cells for opamp and switch
- *Large dynamic*: complementary transmission gates and opamps powered with a higher supply allows a larger signal swing (Ex.: a -80dB THD with a 4Vpp signal amplitude at 1.5V supply with 80dB dynamic range is reported)
- Disadvantages
- *Technology robustness*: $V_{DD_{mult}}$ is limited by the maximum acceptable electric field between gate-channel and between drain-source in scaled-down technology
- *External components*: an external capacitor
- Power efficiency: the less than 100% conversion efficiency of the charge-pump could limit the application in battery operated portable systems

LV SC

On-chip clock multiplication

- Concept
- An auxiliary clock generated on-chip (charge pump) is used to drive the switches*
- The opamps are operating at the low supply voltage

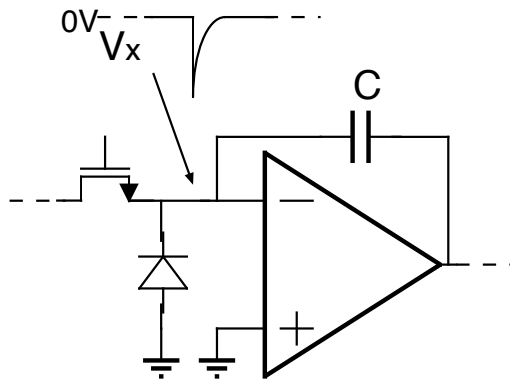


- Advantages
- *Large dynamic*: complementary transmission gates can be used for any signal swing (supported by the opamp)
- *Minimum supply* ($V_{TH}+2\cdot V_{ov}$): is achieved using opamp input dc voltage set to ground.

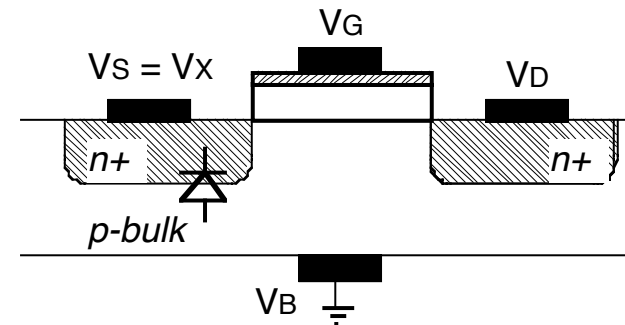
* J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique", *IEEE J. of Solid-State Circuits*, Vol. SC-11, no.3, pp.374-378, June 1976
Y. Nakagone, H. Tanaka, K. Takeuchi, E.Kume, Y. Watanabe, T. Kaga, Y. Kawamoto, F. Murai, R. Izawa, D. Hisamoto, T. Kisu, T. Nishida, E. Takeda, K. Itoh, "An experimental 1.5V 64Mb DRAM" *IEEE JSSC*, Vol. 26, no. 4, pp. 465-472, April 1992
F. Krummenacher, H. Pinier, A. Guillaume, "Higher sampling frequency in SC circuits by on-chip clock voltage multiplier" 1983 European Solid State Circuits Conference, pp. 123-126.

On-chip clock multiplication

- Disadvantages
- *Technology robustness*: Long-term oxide reliability problem
- Charge loss during the transient through parasitic diode in NMOS switch due to possible negative excursion of the virtual ground (using opamp input dc voltage set to ground)



Negative spikes at node X are caused by:



NMOS switch structure
 a negative charge transfer
 clock feedthroug
 finite opamp speed-of-response

- Ex.: a 5ns-500mV spike results in a 0.5mV voltage error on a 1pF integration capacitor at 100 °C with a min. size diode

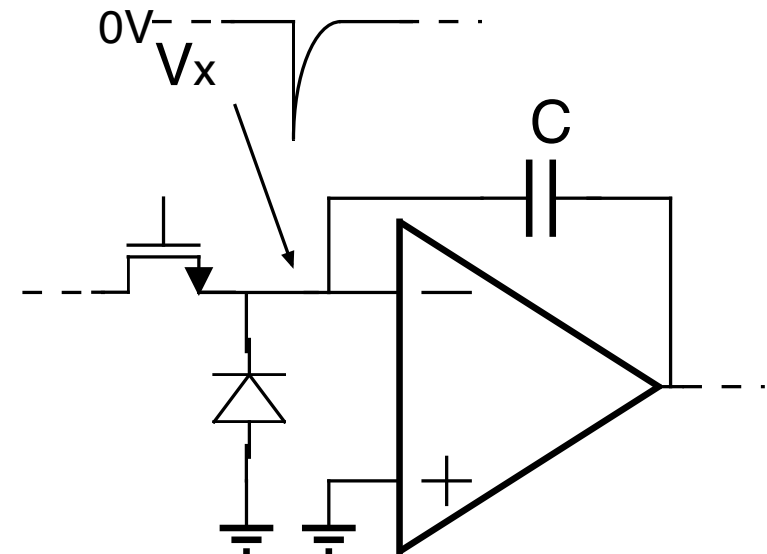
LV Analog Switch

Charge loss during the transient

- The size of the spikes is proportional:
 - to the signal level (i.e. limited by the opamp supply)
 - to the clock amplitude (i.e. the clock supply).

- The importance of this problem becomes lower with the opamp and clock supply reduction

- The spike due to the charge transfer tends to become negligible for low output swing (i.e. low opamp supply)

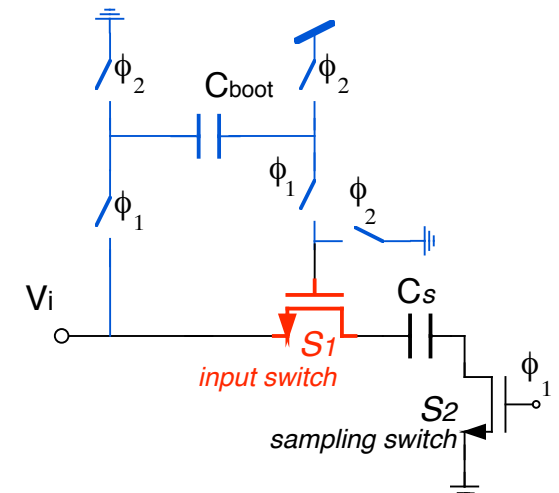
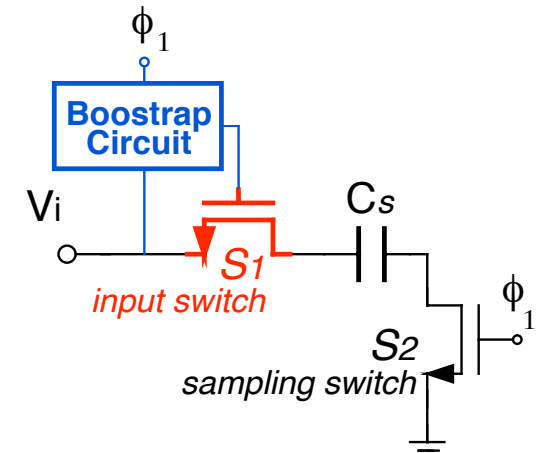


- The clock feedthrough effect remains important due to the large clock signal amplitude (i.e. large -multiplied- clock supply)

On-chip clock multiplication improvement

Signal reference clock drive (Clock boosting)*

- The clock signal is dependent on the input signal amplitude
- All the switches operates with a fixed $V_{ov}=V_{DD}$
- A constant switch conductance is ensured and this reduces also signal-dependent distortion.
- It requires a specific charge-pump for each switch, increasing area, power consumption and noise injection



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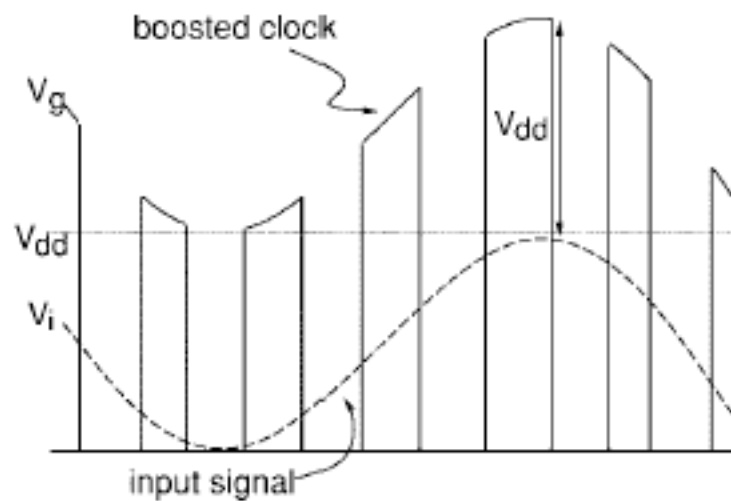
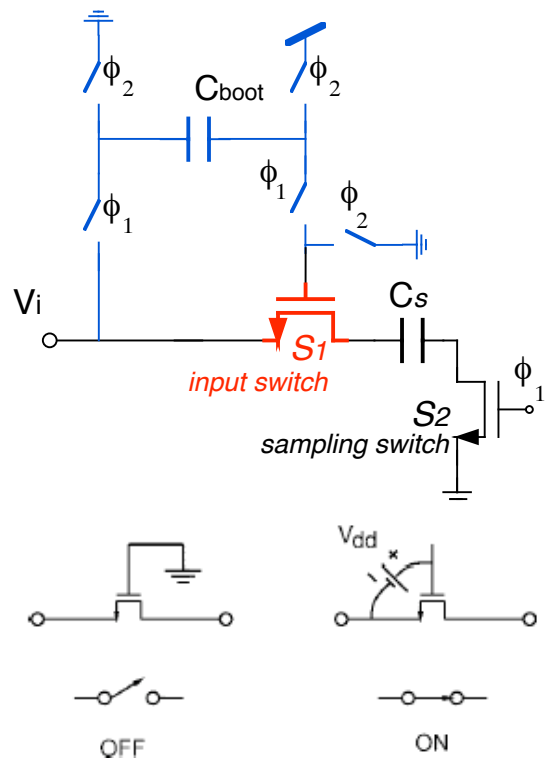
* A. M. Abo, Paul R. Gray; A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter, IEEE JSSC, May 1999

M. Dessouky, and A. Kaiser, "Very Low-Voltage Digital-Audio $\Sigma\Delta$ Modulator with 88-dB Dynamic Range Using Local Switch Bootstrapping", IEEE JSSC, Mar. 2001

LV Analog Switch

Bootstrap switch

- A charge pump is used
 - The switch operates with a fixed $V_{ov}=V_{DD}$
 - Using a constant overdrive, the R_{on} is constant for all the swing
- The gate voltage can go higher than the supply
- A specific charge-pump for each switch increases area, power consumption and noise injection

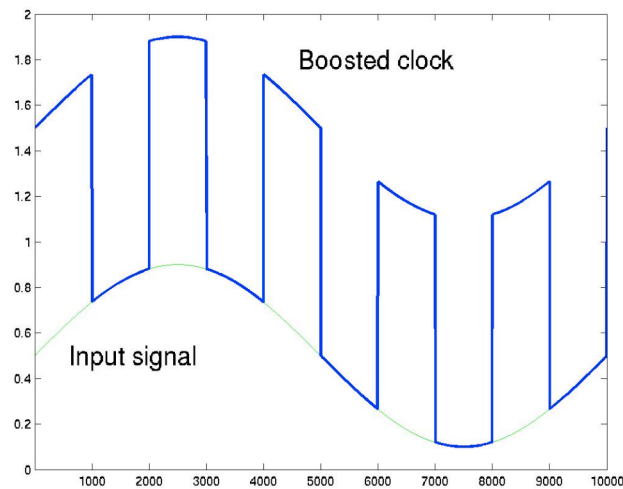


OFF: Grounded gate ensures OFF state
ON: V_{GS} fixed to V_{DD} ensures ON state without overdriving gate

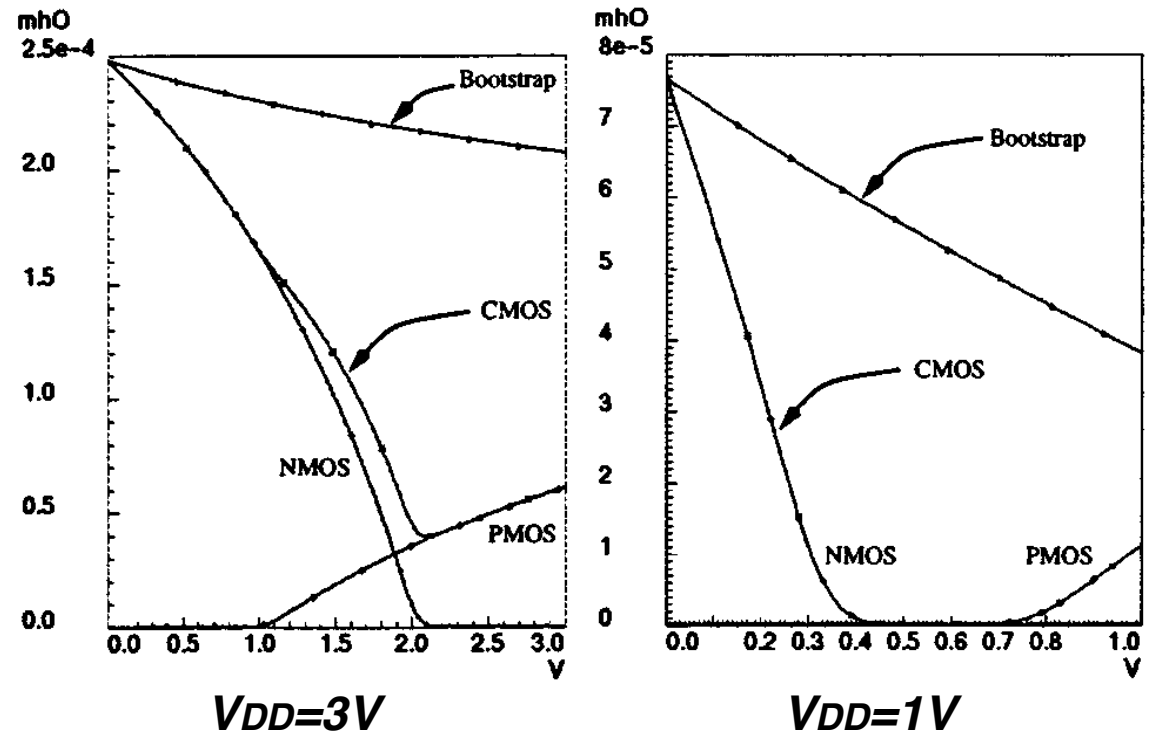
LV Analog Switch

Bootstrap switch

Waveforms



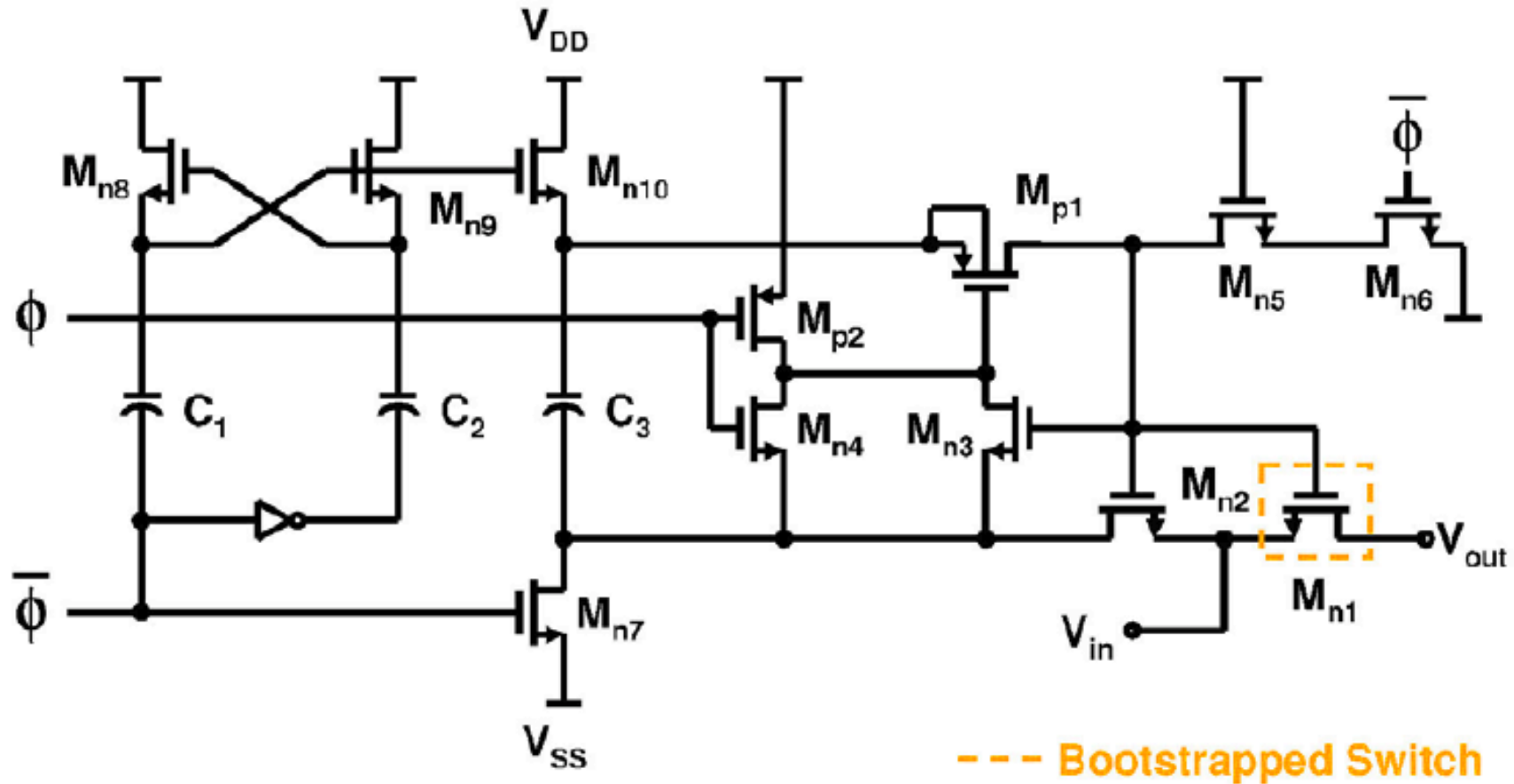
Switch conductance



LV Analog Switches

On-chip clock multiplication *

- Booster switch complexity

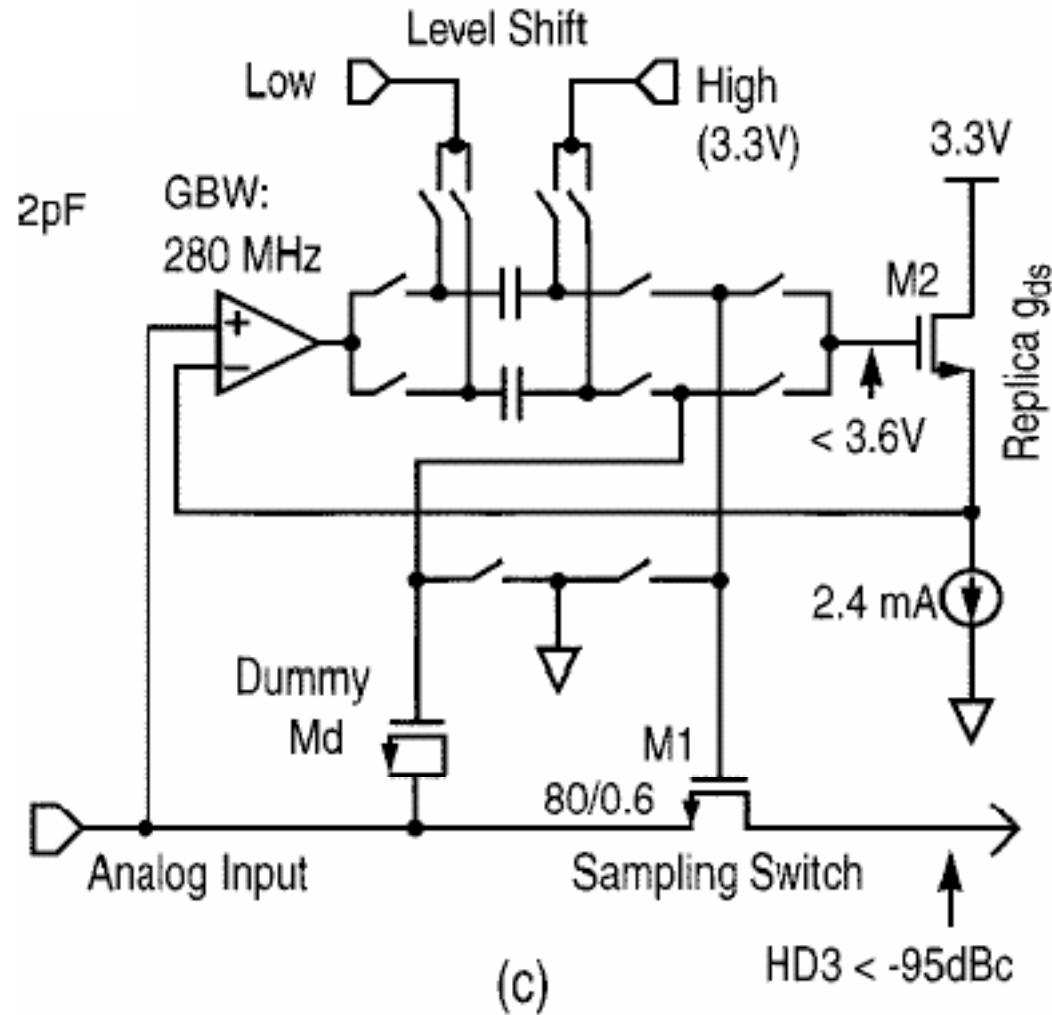


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◆ * A. M. Abo and P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipelined Analogto-Digital Converter," *IEEE J. Solid-State Circuits*, vol. 34, pp. 599-606, May1999.

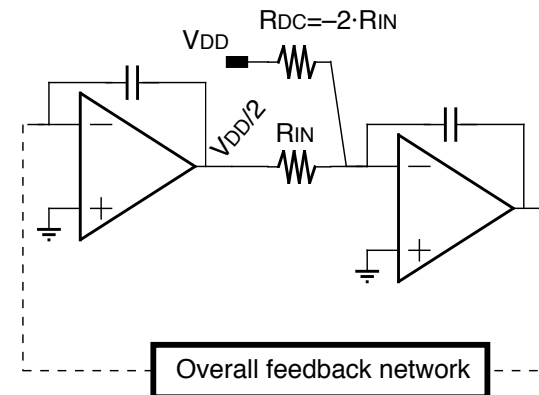
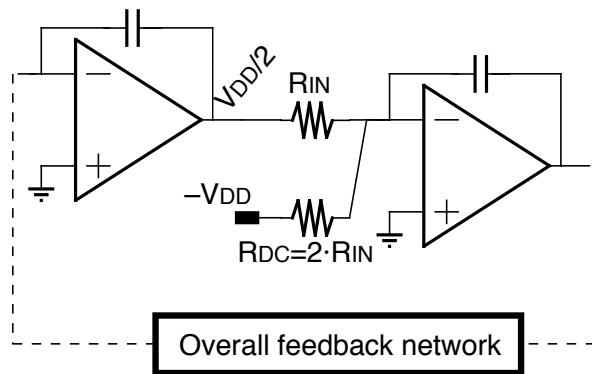
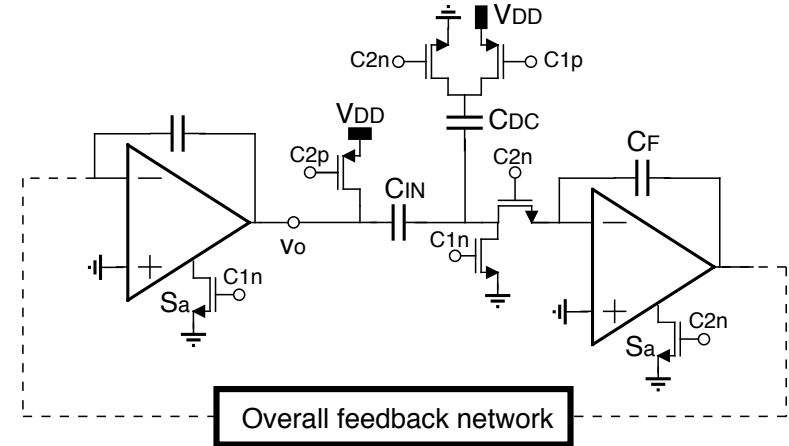
LV Analog Switch

Advanced clock boosting: Cancelling body effect



Switched-opamp technique*

- Concept
- The critical switch at the opamp output is eliminated
- Its function is implemented turning-on and off the opamp
- A level shift is realized with C_{DC}
- → V_{out_DC} and V_{in_DC} are chosen independently



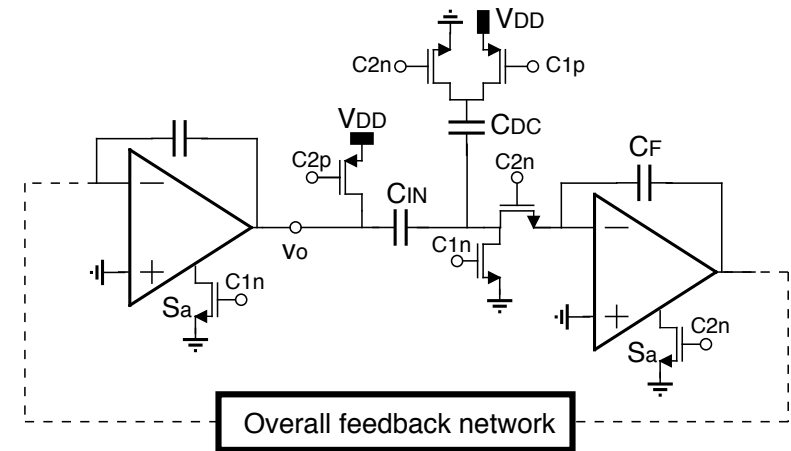
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* J. Crols, and M. Steyaert, "Switched-Opamp: an approach to realize full CMOS switched-capacitor circuits at very low power supply voltages", *IEEE J. of Solid-State Circuits*, Vol. SC-29, no.8, pp.936-942, August 1994

A. Baschiroto, R. Castello, "A 1V 1.8MHz CMOS Switched-opamp SC filter with rail-to-rail output swing", *IEEE J. of Solid-State Circuits* - December 1997 - pag. 1979-1986

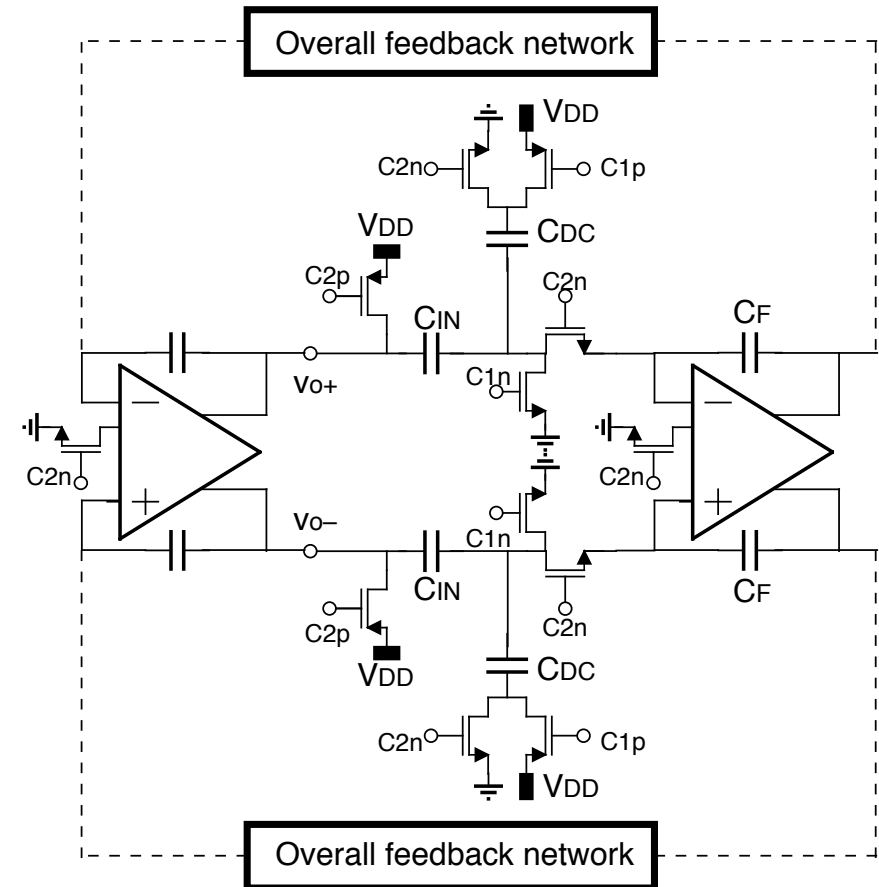
Switched-opamp technique

- Advantages
- Optimum bias (with $C_{DC} = C_{IN}/2$):
- $V_{out_DC} = V_{DD}/2$ (for max swing)
- $V_{in_DC} = GND$ (for switch operation)
- Optimum switch operation:
- S_3, S_4 connected to GND => NMOS (max V_{ov} , no body effects)
- S_2 is connected to V_{DD} => PMOS (max V_{ov} , no body effects)
- Minimum supply: $V_{DDmin} = V_{TH} + V_{ov}$ (if the opamp is ideal)
- No threshold dependent voltage references are needed
- Disadvantages
- Only the non-inverting and delayed integrator is available
- C_{DC} size errors result in an extra offset
- All the noise present on V_{DD} and GND is injected into the signal path



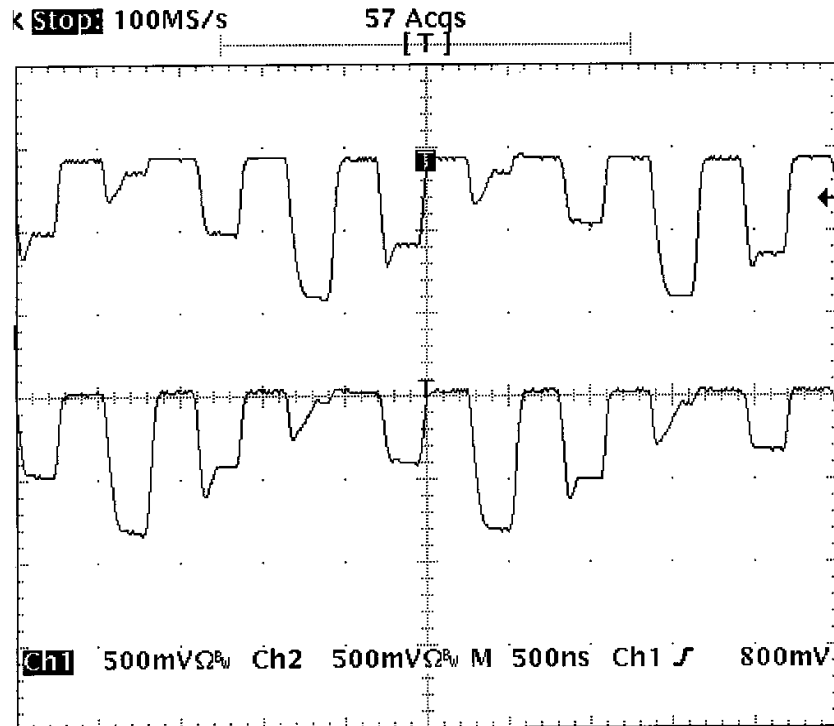
Switched-opamp differential integrator structure

- Advantages
 - It doubles the swing
 - The charge injected by C_{DC} is a CM signal and is greatly rejected
 - The noise from V_{DD} and GND is rejected
- Disadvantages
 - Fully-differential opamp needs CMFB circuit

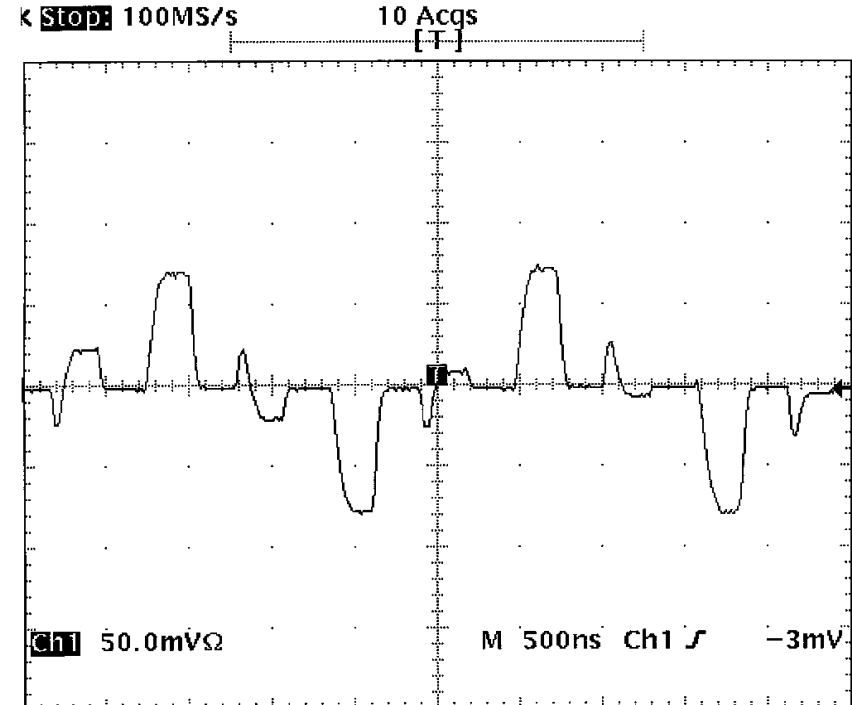


Switched-opamp integrator example

Output waveforms ($V_{DD} = 1V$)



Output single-ended waveform with $1.6V_{pp}$ differential input signal



Output differential waveform with $1.6V_{pp}$ differential input signal

Switched-opamp integrator structure

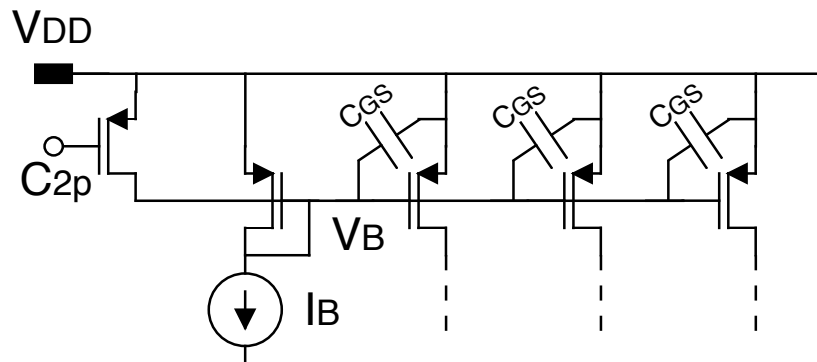
Limitations

- **Opamp turn-on time** limits the maximum sampling frequency.
- **Charge loss at the virtual ground node** still exists but it is less important since the clock amplitude is lower.
- **Gain loss:** The output signal is valid only during one clock phase.
 - In the other phase the output is zero.
 - This gives:
 - a gain loss of 2
 - an increased distortion due to the large output steps resulting in slew-rate-limited signal transient and glitches.
 - This problems can be eliminated with a S&H at the output (ex.: ADC)
- **Input dc-coupling switch** remains a problem (???)

Switched-opamp Technique

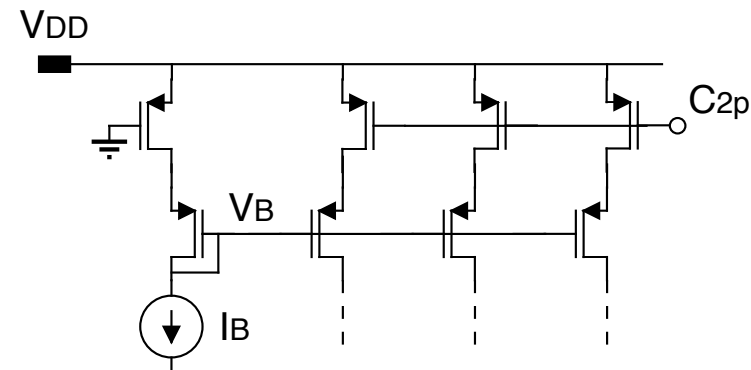
Turn-on time reduction

- Key objective: to minimize the opamp turn-on-time to maximize the sampling frequency.
- Key problem: re-charge capacitance $\left\{ \begin{array}{l} \text{Current sources cap.} \\ \text{Compensation cap.} \end{array} \right.$
- #1 - Current source turn-off



Basic scheme

CGS's
are re-charged through IB



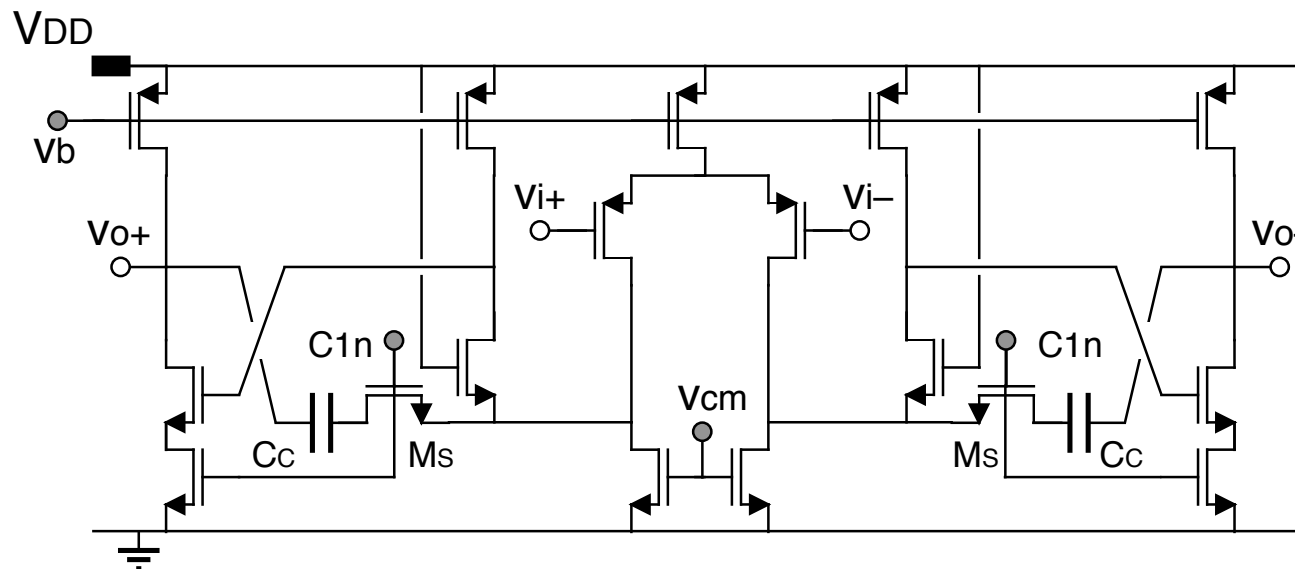
Improved scheme

CGS's are not discharged
Each Coi is charged through Idi

Switched-opamp Technique

Turn-on time reduction

- #2 - Opamp turn-off:
- turn-off only parts of the full opamp, maintaining the rest on and ready at the turn-on instant

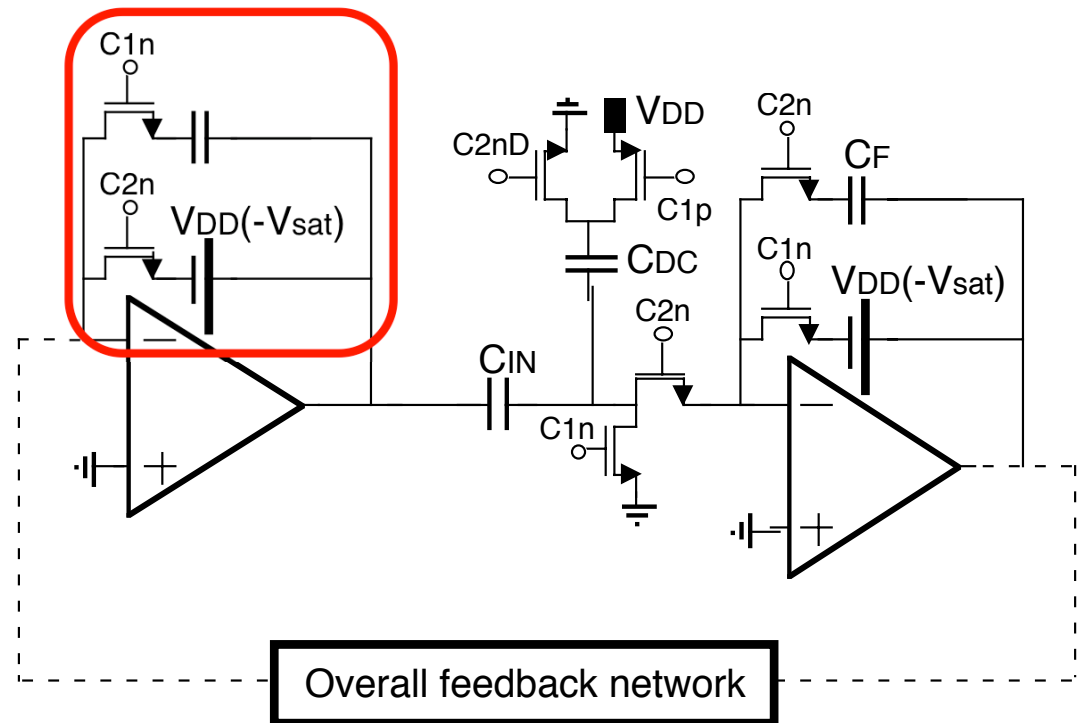


- Only the second stage (an inverter) is turned off
- The Miller capacitance is disconnected in the off phase
- It is kept charged for the following on phase

Turn-on Time Reduction

The Unity-Gain Feedback Technique*

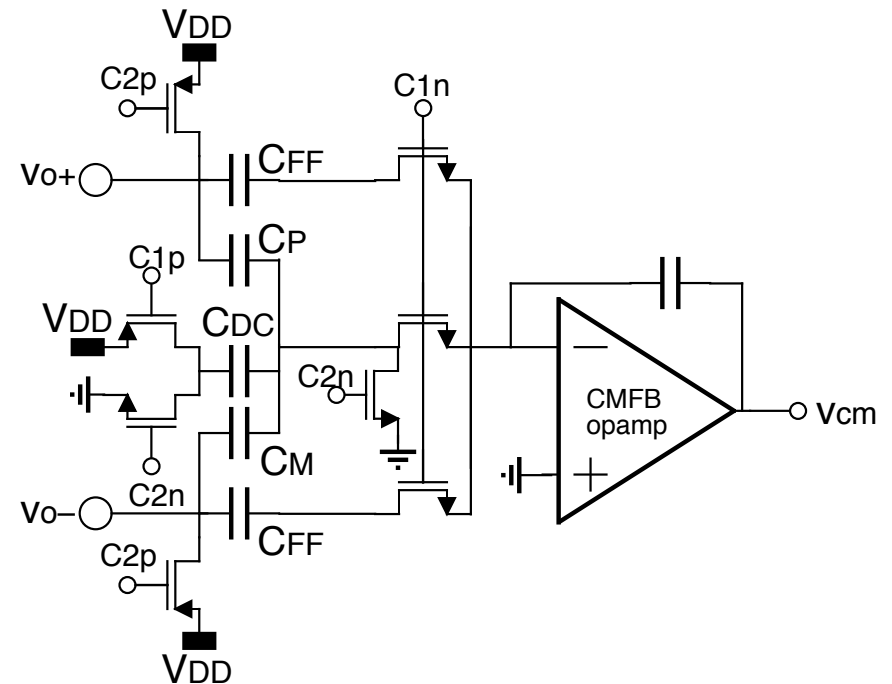
- During the off phase, the opamp is not completely turned-off
- it is biased in a stand-by condition, ready to be quickly turned on
- Higher sampling frequency
- Possible draw-back: the residual signal at the output during the off-phase



Switched-opamp Technique

Low-Voltage Active CMFB

- The key problem is still that the input signals of the CMFB circuit (i.e. the differential opamp output nodes) are centered at $V_{DD}/2$
- Pseudo-differential structures do not need CMFB
- Switched-opamp solution*
- CM input of CMFB opamp is set to GND
- Level shift is realized with C_{CM}
- C_{FF} creates an additional zero
- All switches connected to V_{DD} or GND
- It does not increase the minimum overall opamp supply



■ _____

* A. Baschiroto, A. Nagari, and R. Castello " Common-mode control circuit for a switcheable fully-differential opamp ", European patent (granted) pat. n. 0836274, 15/4/98 - USA patent (pending)- 948,986 -

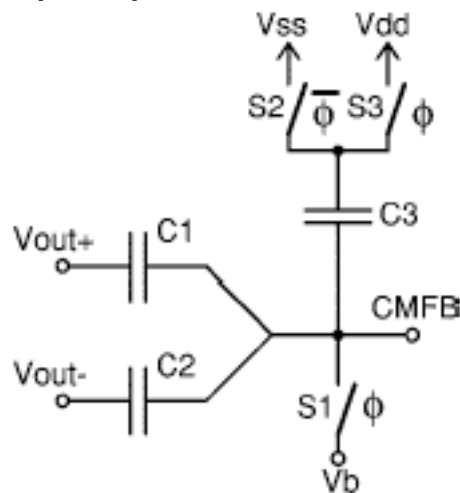
LV Opamp Design

CMFB: Switched-Opamp Solution

- The key problem is still that the input signals of the CMFB circuit (i.e. the differential opamp output nodes) are centered at $V_{DD}/2$
- Pseudo-differential structures do not need CMFB

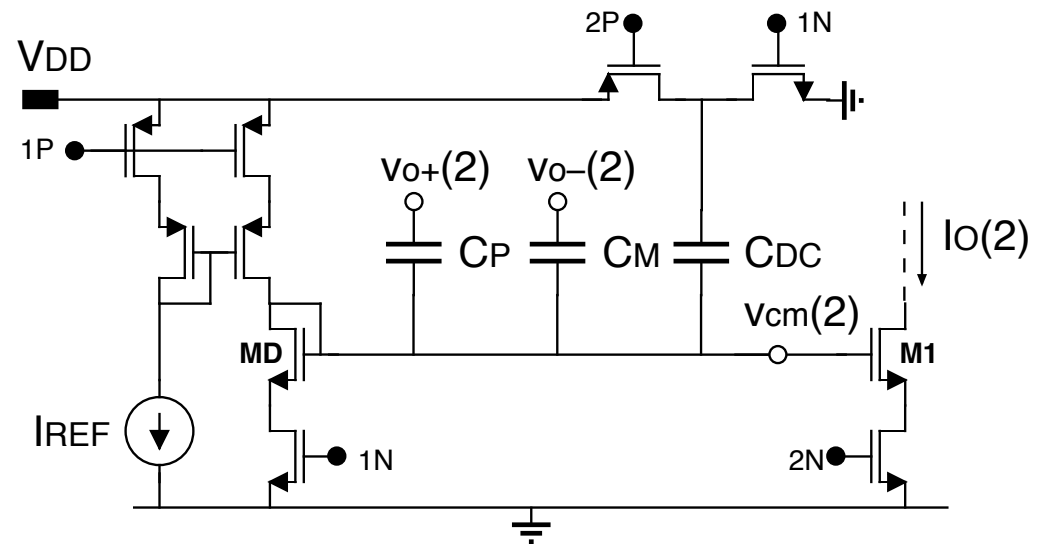
Basic solution

No opamp in these schemes



S1 increases minimum VDD

Improved solution

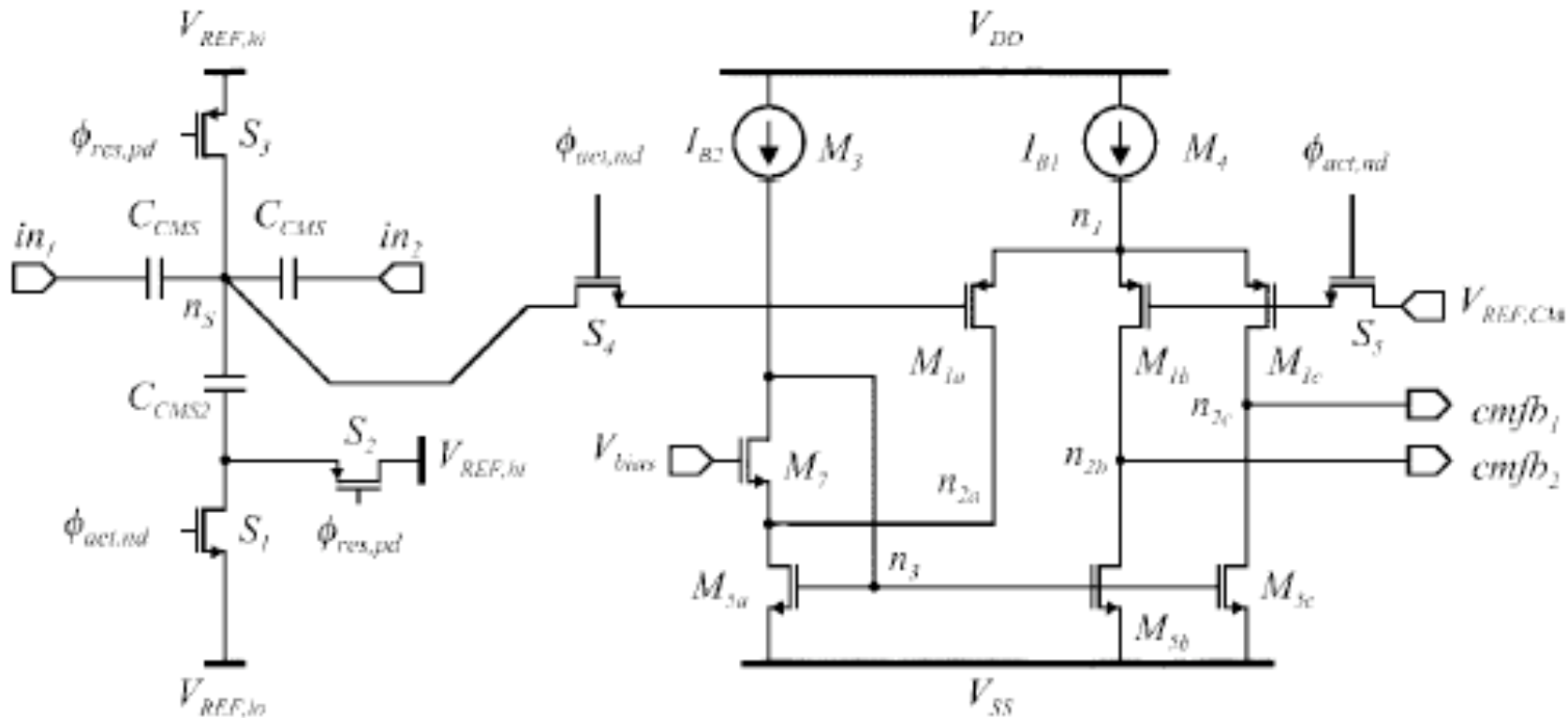


All switches connected to GND or VDD

Switched-opamp Technique

Input partition for a LV CMFB*

- An error-amplifier-based CMFB with a dividing common-mode sampling scheme



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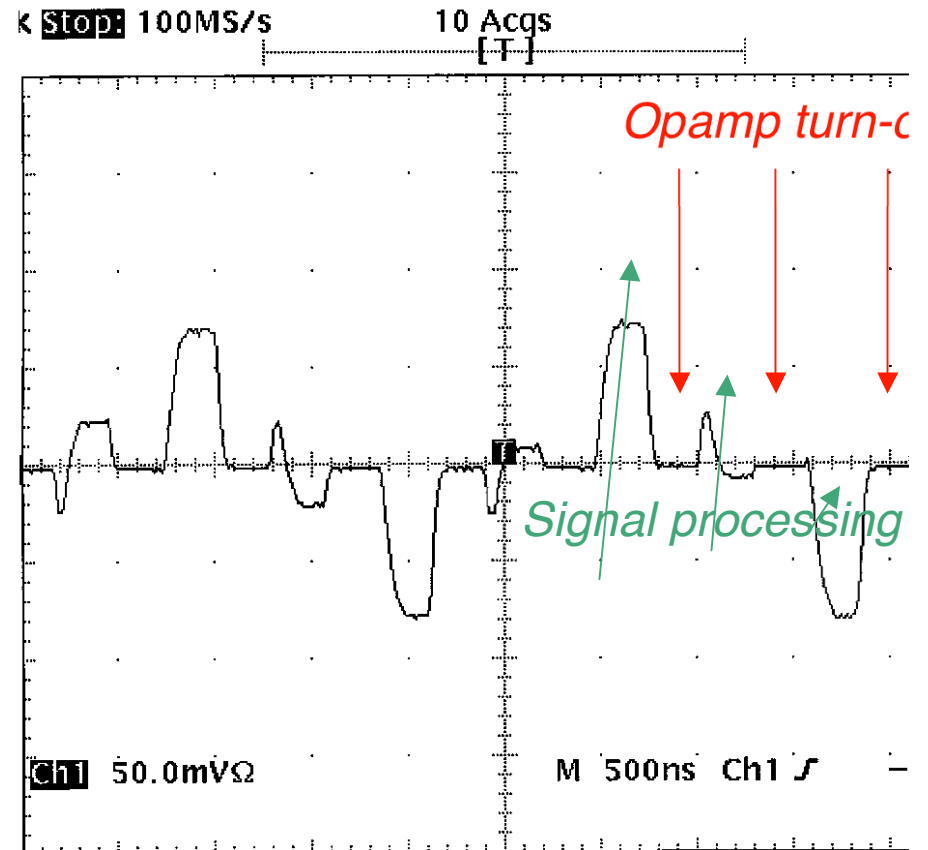
* V. Peluso, P. Vancorenland, A. Marques, M. Steyaert, W. Sansen, "A 900mV 40μW Switched Opamp ΣΔModulator with 77dB Dynamic Range", IEEE JSSC, Dec. 1998



Switched-Opamp Technique

Limitations

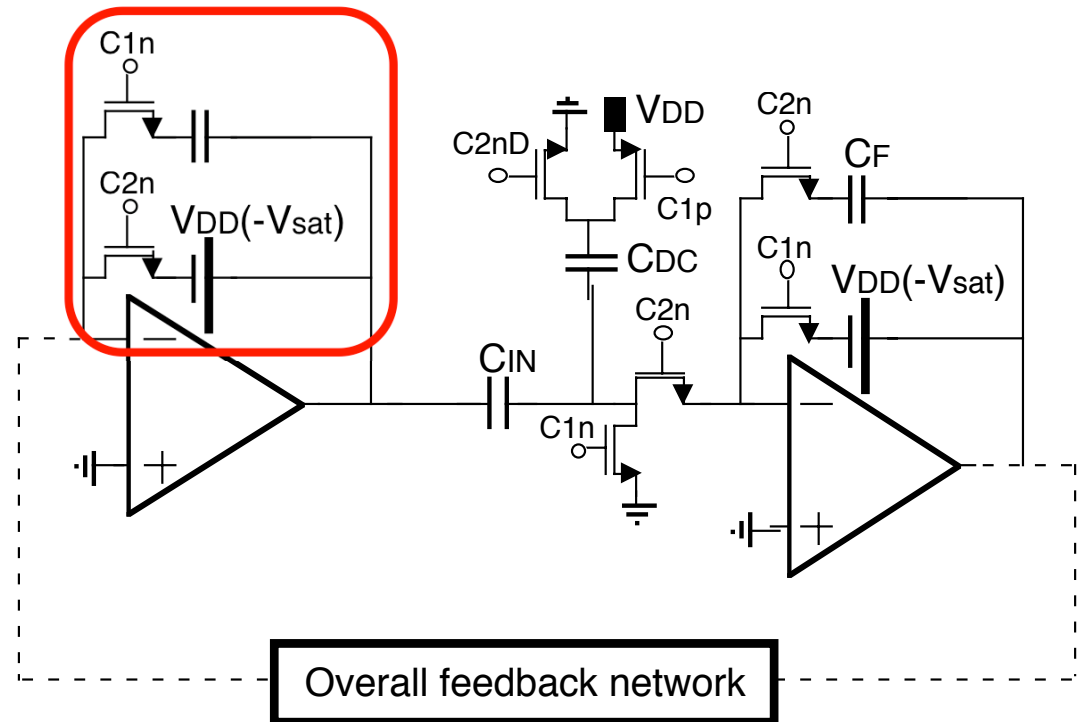
- Opamp turn-on time limits the sampling frequency
- V_{out} is valid only during one clock phase
- In the other phase $V_{out} = 0$
- A gain loss of 2
- An increased distortion due to the large output steps, slew-rate and glitches
- Solved problems with an output S&H (ex.: ADC)



Unity-Gain-Reset Opamps Technique*

Turn-on Time Reduction: The Unity-Gain Feedback Technique

- During the off phase, the opamp is not completely turned-off
- it is biased in a stand-by condition, ready to be quickly turned on
- Higher sampling frequency
- Possible draw-back: the residual signal at the output during the off-phase



■ _____

* M. Keskin, U.-K. Moon, , and G. C. Temes, "A 1-V 10-MHz Clock-Rate 13-Bit CMOS SD Modulator Using Unity-Gain-Reset Opamps", IEEE JSSC, July 2002