MUX 2010

Integrated Power Conversion

Power electronics?

- Analog Electronics: the ensemble of techniques and circuit solution to project systems to elaborate the information in analog way
- Digital Electronics: the ensemble of techniques and circuit solution to project systems for the logical and numeric elaboration of the information
- Power Electronics : the ensemble of techniques and circuit solution to project systems to control the energy transfer from a source to a load

Targets

- The principles that defines the quality of product are
  - Small dimension → Compact and efficient power distribution system
  - High performance → High consumption
  - Small power consumption otherwise high battery life for portable systems → High efficiency
  - Low cost → Small component and high efficiency

Normally a good product design requires a good power management system

Figures of merit

- Analog electronics: precision (low offset and high signal noise ratio), high speed (bandwidth), low consumption and low area
- Digital electronics: high elaboration frequency, low energy for operation and low area
- Power electronics: high conversion efficiency that implies high power density (ratio between the circuit volume and the power utilized).

$$\eta = \frac{P_{out}}{P_{in}} \qquad P\_Density = \frac{P_{out}}{Volume}$$

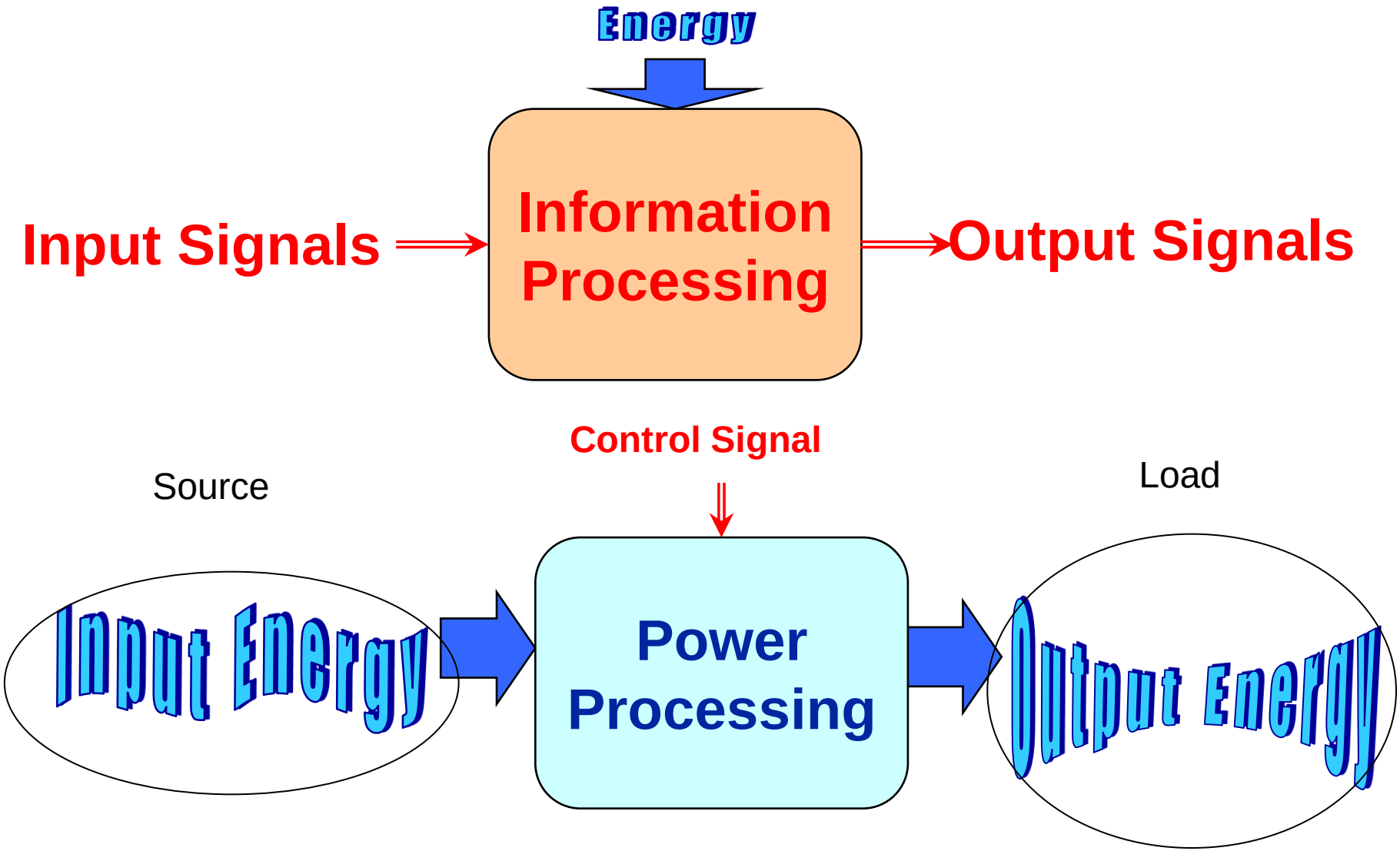
Chip technologies Figures of merit

- Analog electronics : low offset for area unit, high devices cut off frequency
- Digital electronics : high number of gates for area unit
- Power electronics : low resistance for area unit, low charge to drive the switch and low reverse recovery charge

Outline

- Conversion topologies design strategies
  - Linear conversion
  - Switched capacitor conversion
  - Magnetic conversion
- Integrated power devices and parasitcs effects
  - Power mosfet
  - Parasitic effetcs

Power flux control

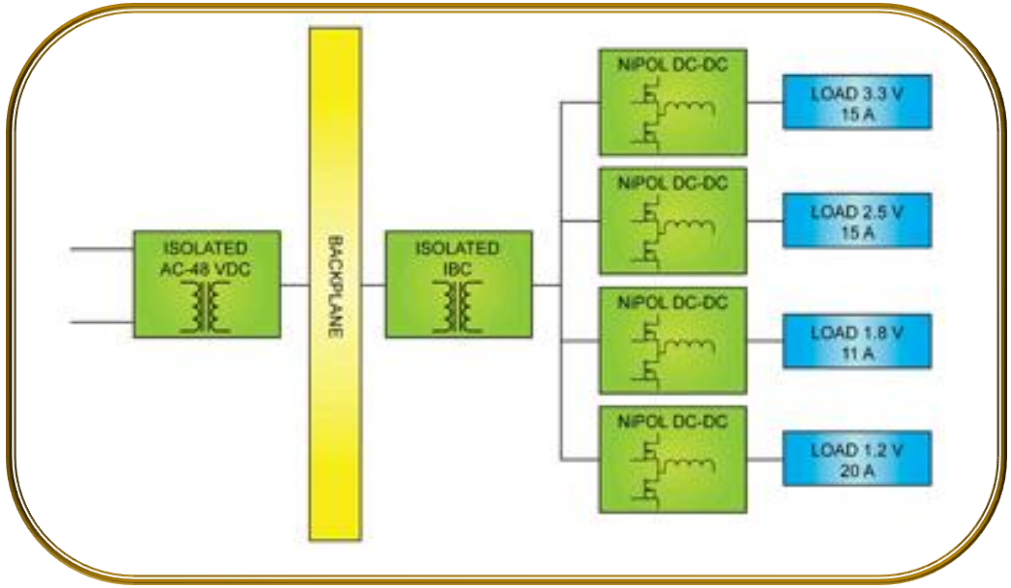


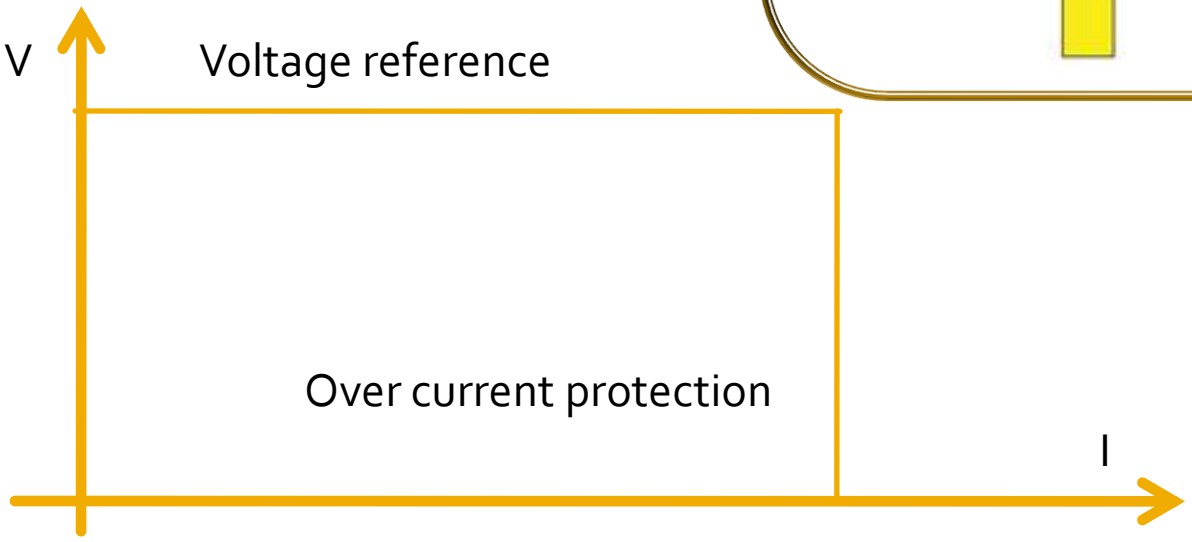
Power source

- Specification: $f(V_{source}, I_{source}, t) = 0$
  - VI characteristic and type of source (AC/DC)
  - Energy available (limited or unlimited)
- Rules to utilize the source
  - Safe operating area
  - Rules on the type of load connected to the source ex:
    - Maximum power point tracking requirement
    - Power factor correction requirement
  - Limit on the Instant power requirement
  - EMI Rules

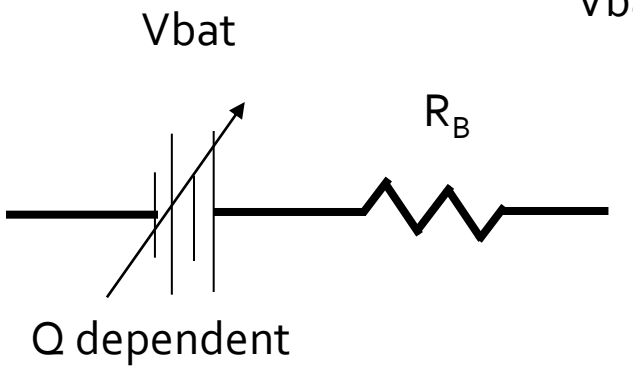
Power source example: Power distribution system

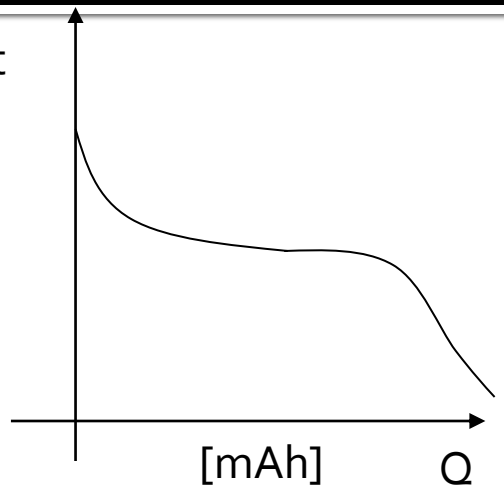
- VI characteristic
- EMI rules





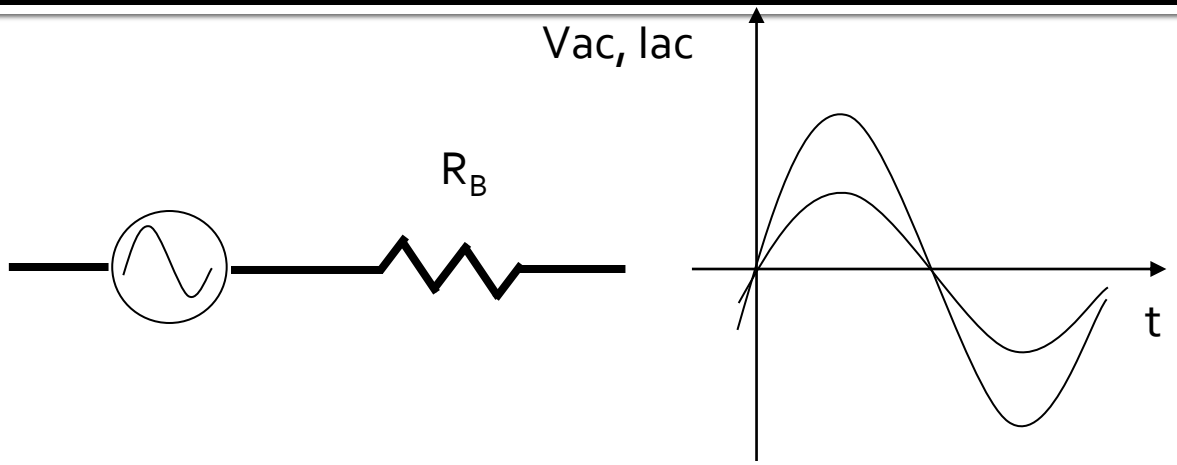
Power source examples: Batteries





- The characteristic depends on charge level
- The quality of a battery on the ratio between the charge stored and the volume
- For the rechargiable batteries another important figure of merit is the number time cycles

Power source examples: AC line power source



- The ac line power source requires a high power factor in order to have only current that gives a mean output power:
  - No high order harmonics
  - Current waveform proportional to the voltage waveform

Power Load

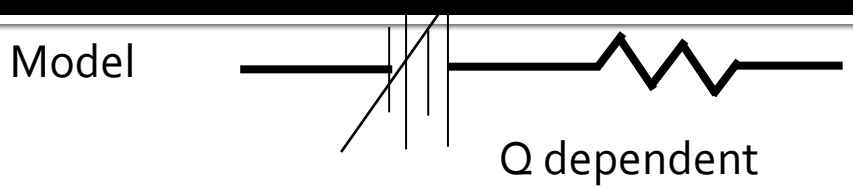
- Specification:
  - Load specification
  - Characteristic (Model)
    - Static
    - Dynamic
- Rules to utilize the load
  - Safe operating area
  - Precision on current/voltage regulation
  - EMI Rules: Maximum ripple

$$g(V_{LOAD}, I_{LOAD}, t) = 0$$

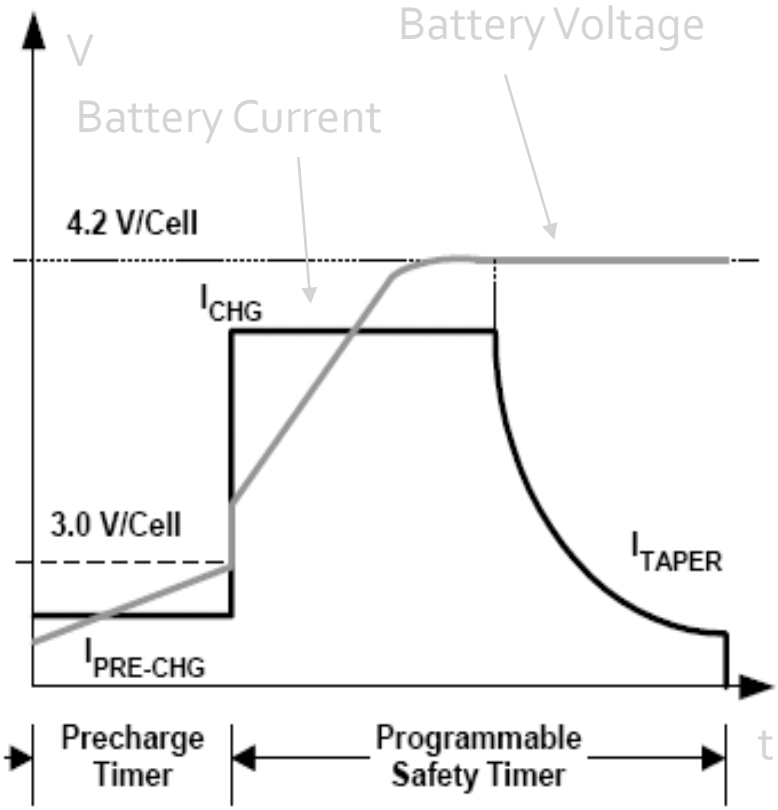
$$h(V_{LOAD}, I_{LOAD}, t) = 0$$

$$\begin{cases} g(V_{LOAD}, I_{LOAD}, t) = 0 \\ h(V_{LOAD}, I_{LOAD}, t) = 0 \end{cases}$$

Power load examble: Battery charger

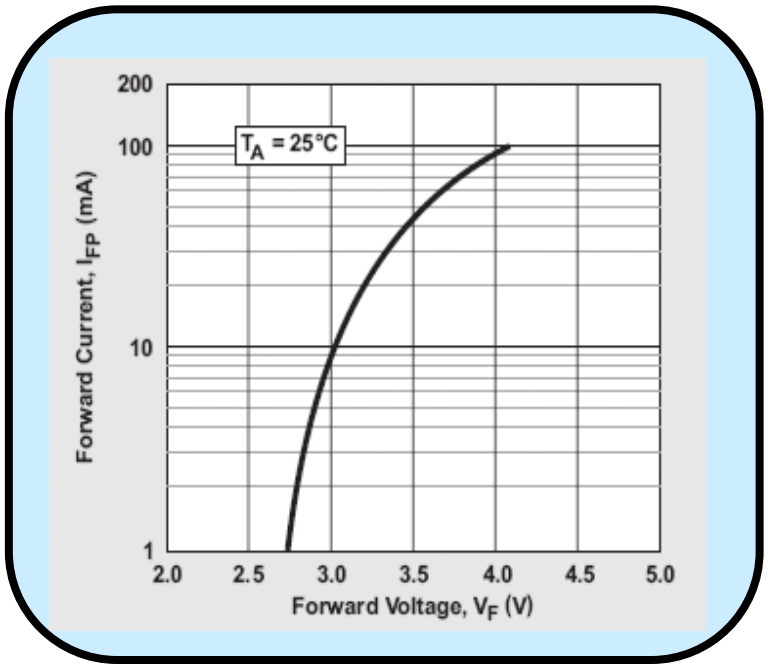


Charge Profile for a Li-Ion battery



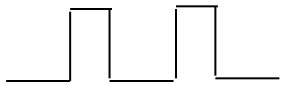
- The charge current is equal to I_{pre-ch} when the battery is below 3V.
- The battery is charged with I_{ch} when the battery voltage is $4.1V > V_{batt} > 3\,V$.
- After the charge goes in a control voltage charge phase in which the charge current depend on the error voltage $I_{ch}=K(4.2 - V_{batt})$

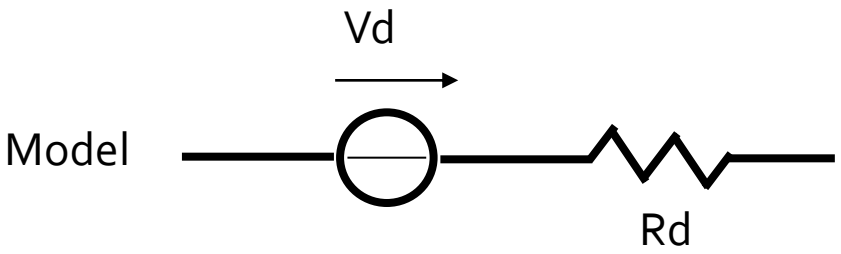
Power load examble: WLED



- Optical power of a LED is proportional to the current present on the device
- The voltage in approximately constant
- For the driving is used a pulsed current

$I_d = I_{fixed} P_{(t)}$ $P_{(t)}$:





Power Load examples: uP power supply

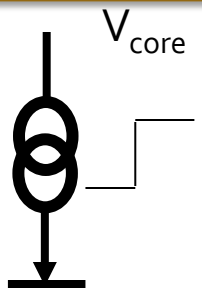
Specication VRD 10.x per Intel P4 Prescott

	VRD 10.0 –VRD 10.1
Maximum VID (Voltage Identification)	1.4V
Vcc Ratings (VID)	0.8375-1.6V
VID step	12.5mV
Vcc Tolerance Band (TOB)	± 19mV
Max Load Current	91A for VRD 10.0 115A for VRD 10.1
Voltage identification	6 bit
Over Voltage Protection	VID + 200mV (Proposed)
Over Current Protection	Not fixed (Proposed)
Maximum overshoot voltage allowed over VID	50mV
Maximum overshoot time duration over VID	25µs
Dynamic VID	Up to 61 steps (12.5mV/5µs)
dI_{OUT}/dt_{MAX}	>50A/µs
Load Line Impedance (R_{DROOP})	1mΩ /1.4mΩ

- Small voltage variation
- High current
- High slew rate

$$h(V_{LOAD}, I_{LOAD}, t) = 0$$

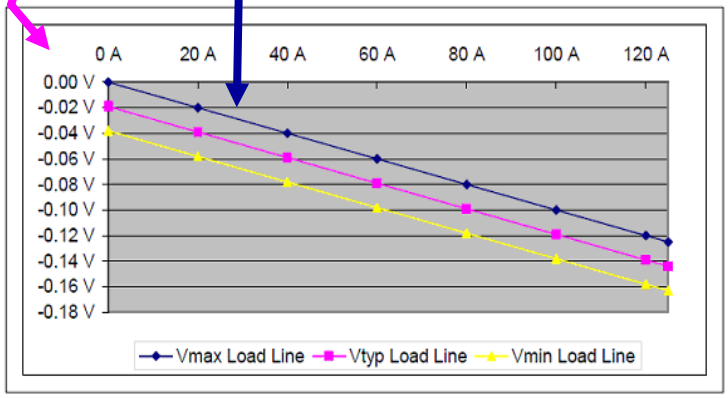
Model



Output impedance resistive required

$$g(V_{LOAD}, I_{LOAD}, t) = 0$$

$$V_{TYP,out} = VID - |TOB| - R_{DROOP} \cdot I_{load}$$

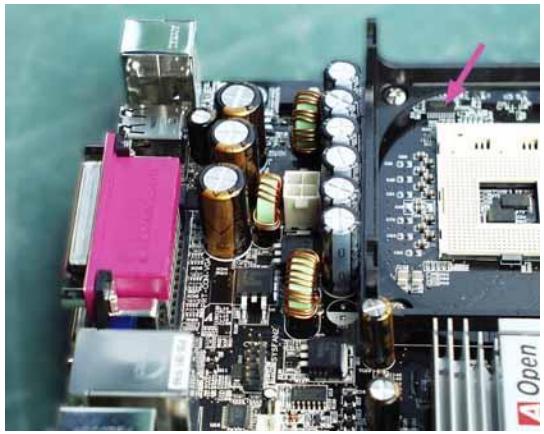


NOTE: 1: Presented as a deviation from VID

2: Socket load line Slope = 1.0 mOhms, TOB = +/-19 mV

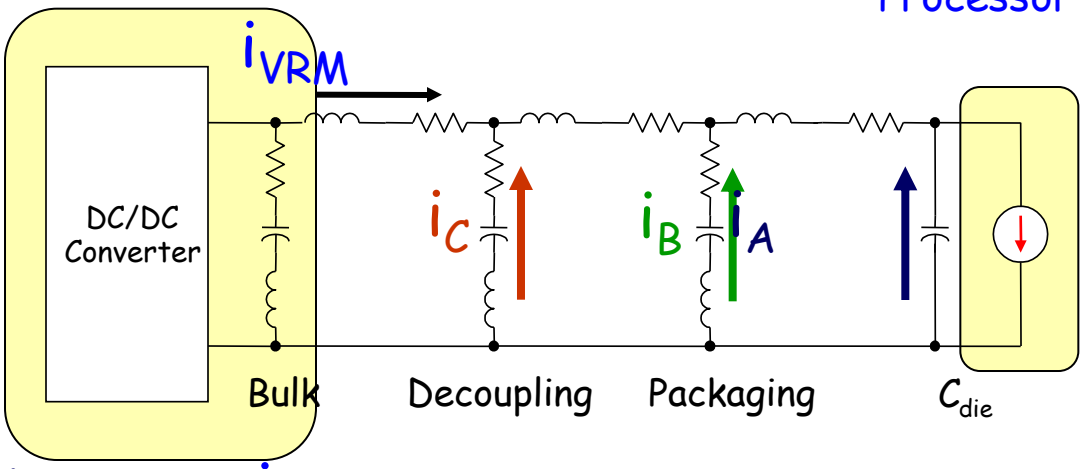
"Droop Function" or "Adaptive Voltage Positioning"

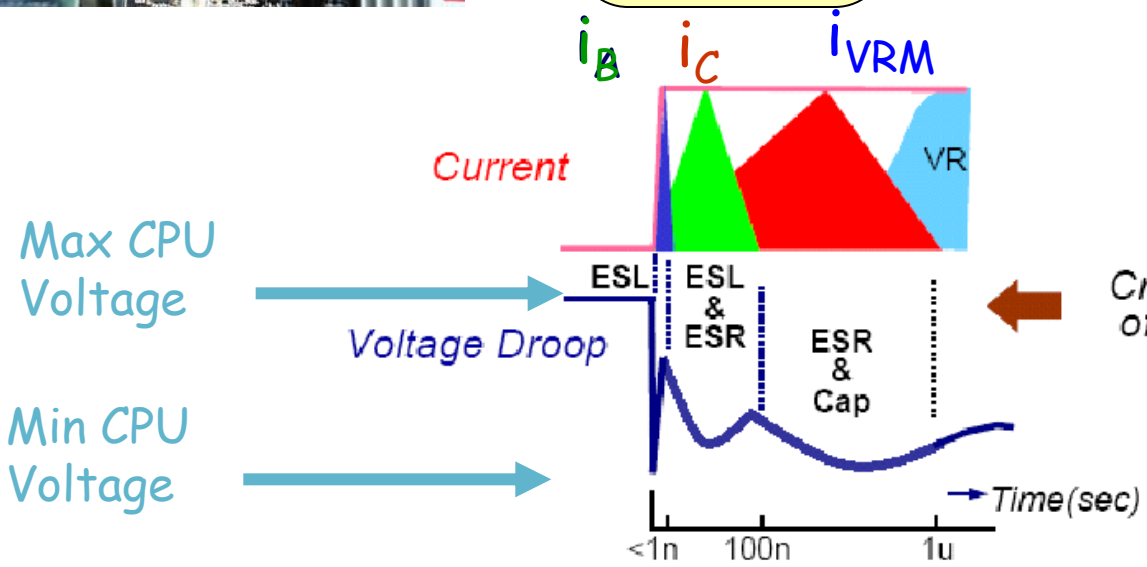
Transient



Synchronous buck converters

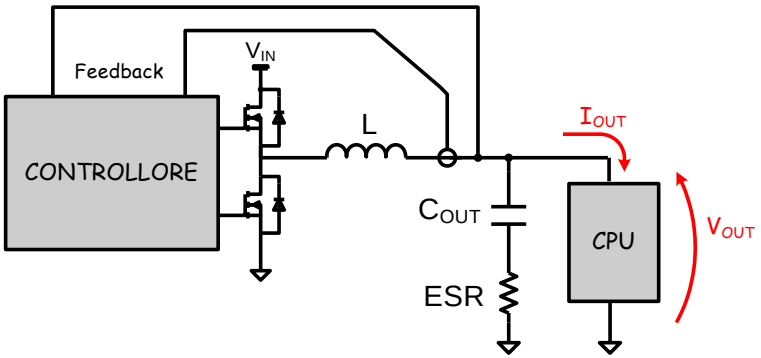
Processor

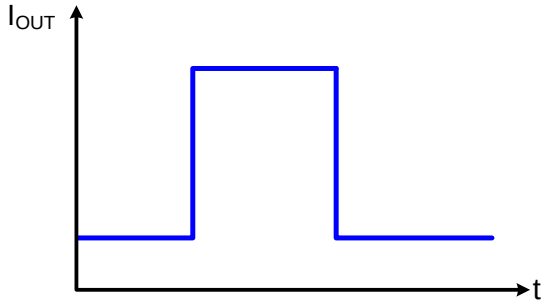




Power Load examples: uP power supply

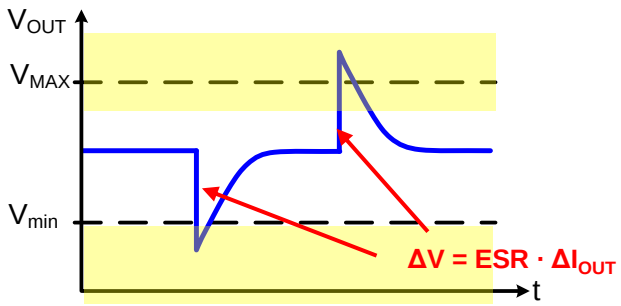
Load current step variation





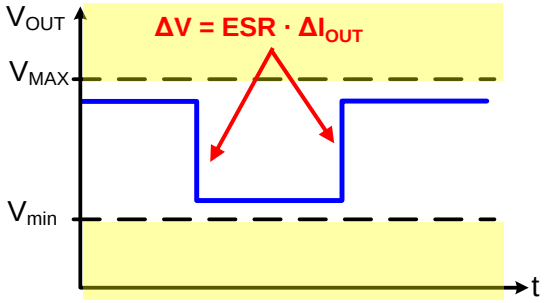
Output voltage response:

Without Droop Function



Tolerance Band NOT respected

With Droop Function

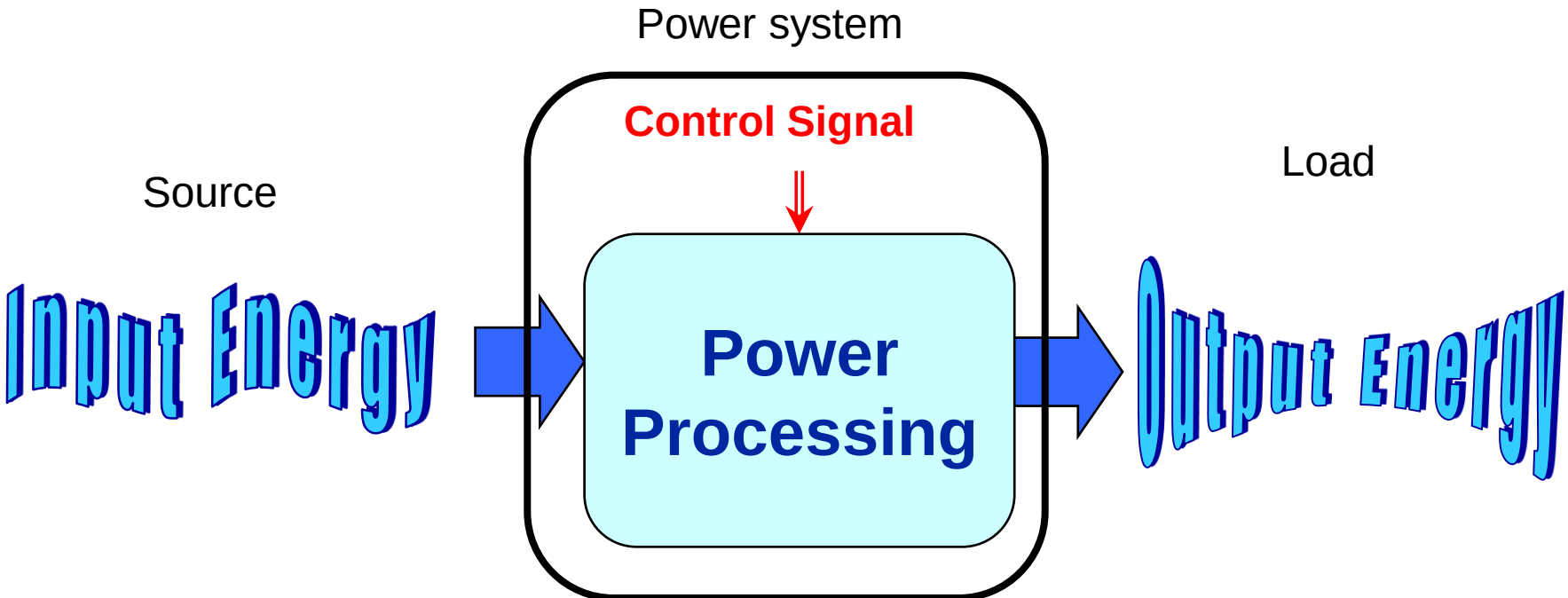


Tolerance Band respected

The Power System

The total power system composed by the power circuits and the control circuits

- meets the specifications of the power source and the power load
- maximizes the power transfer.



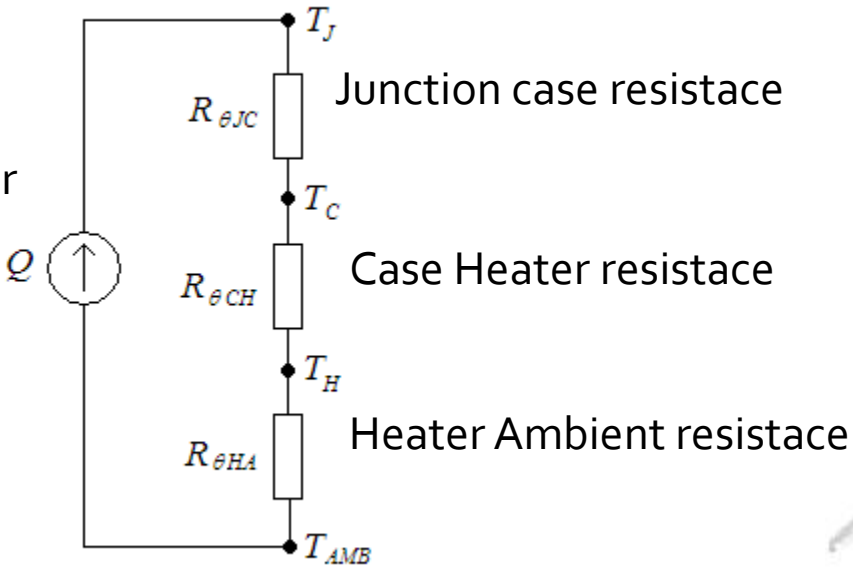
Choose of the correct architecture

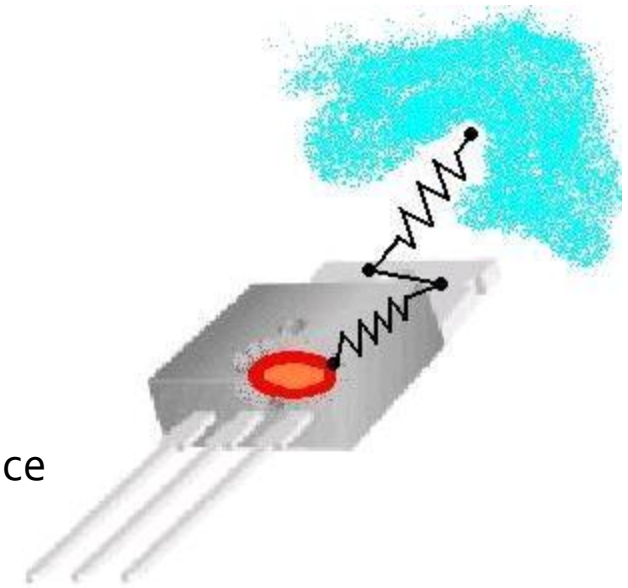
- In a integrated the power architecture selection is driven by
  - Type of conversion (non isolated)
    - Step down (voltage of the source in all codition is major than the voltage of the load)
    - Step up (voltage of the source in all condition is the same of the load)
    - Step down and up (when the voltage of the source and the load can have a common interval of values).
  - Maximum power utilized
    - Low power
    - Medium power
    - High power
  - Complexty of the architecture

Determinate the maximum power

The maximum power consumed by the system is limited by:

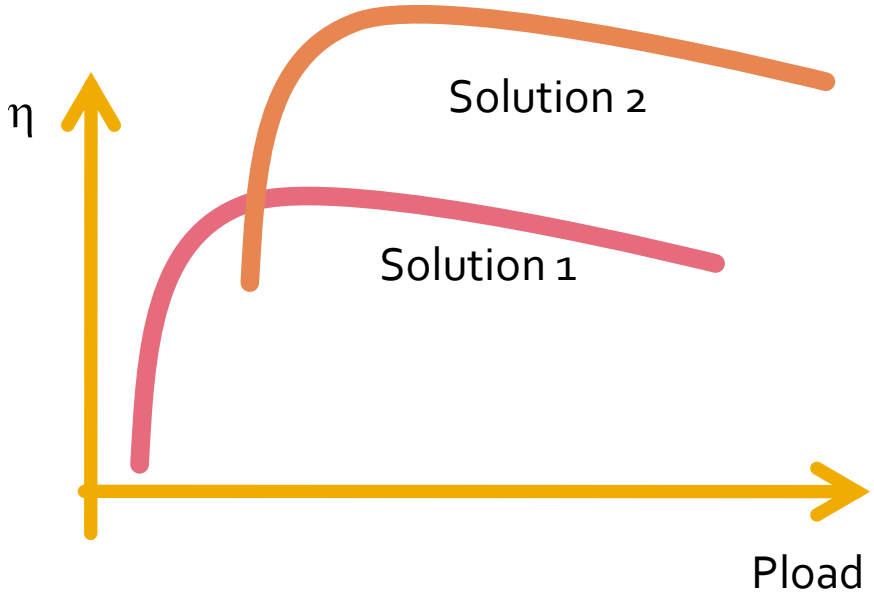
- The package
- The cooling system

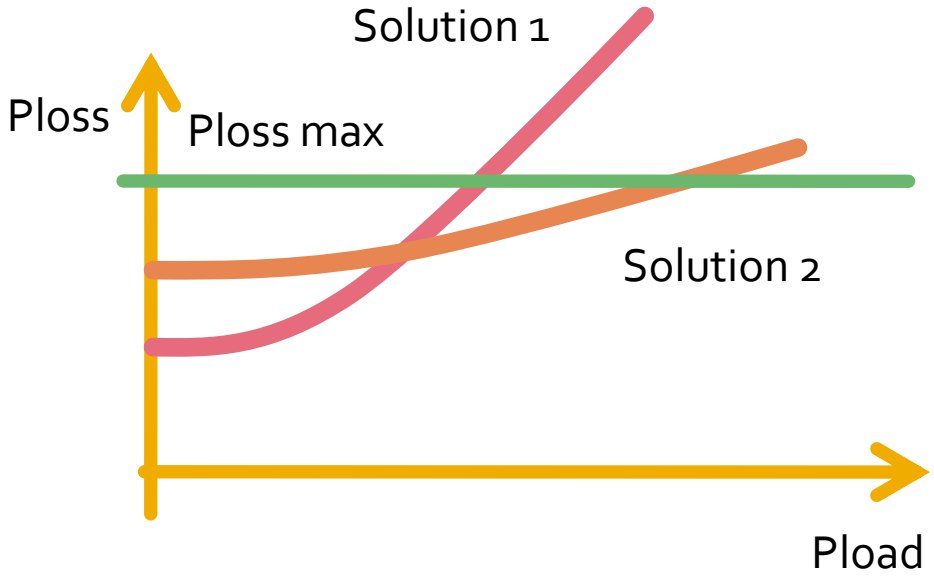




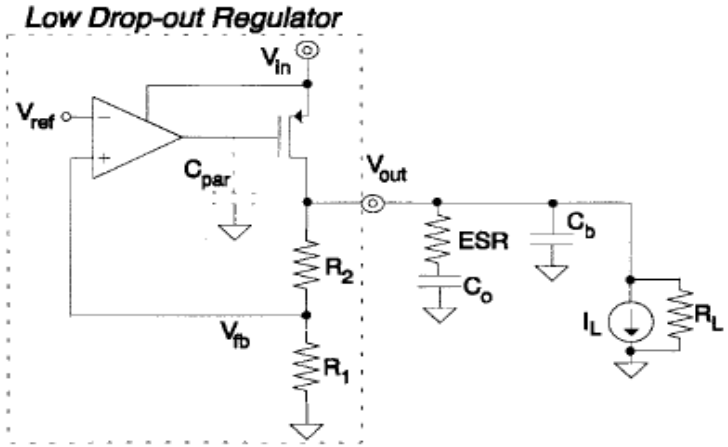
Choose the correct architecture

Dependely on the architecture the power related to the converter can be plotted as reported





Linear conversion

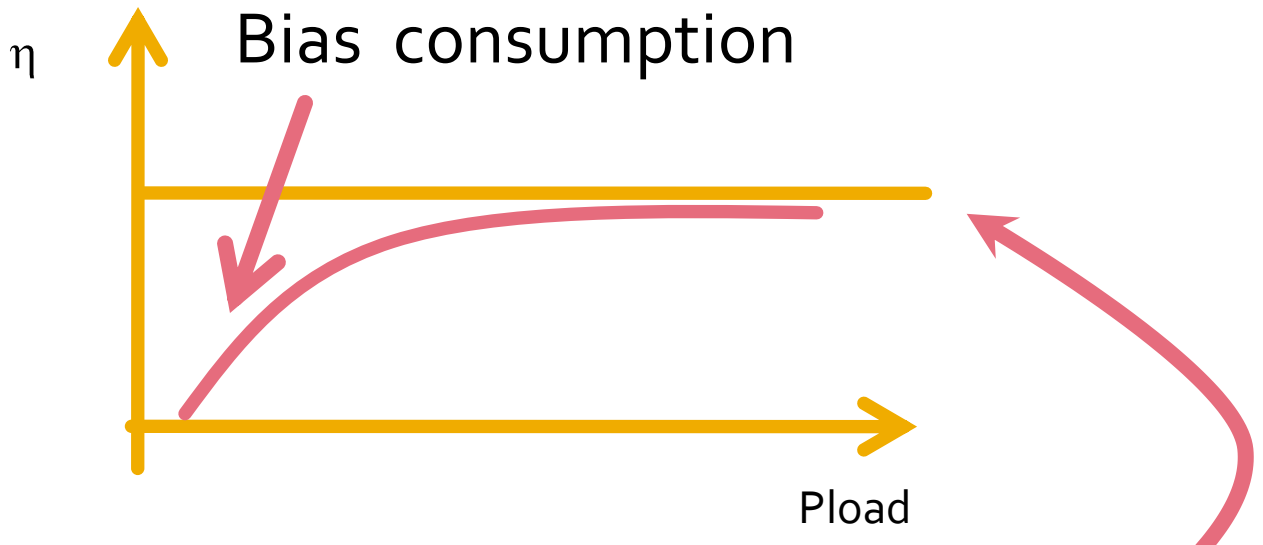


This scheme, commonly used to stabilize low power supply, is designed to meet the load specification by using the analog strategies but it doesn't maximizes the power transfer

- High power loss ⇒ low efficiency ⇒ low power density

$$\eta = \frac{P_{out}}{P_{in}} = \frac{I_{out}\,V_{out}}{I_{in}\,V_{in}} \cong \frac{V_{out}}{V_{in}}$$

Linear conversion efficienty

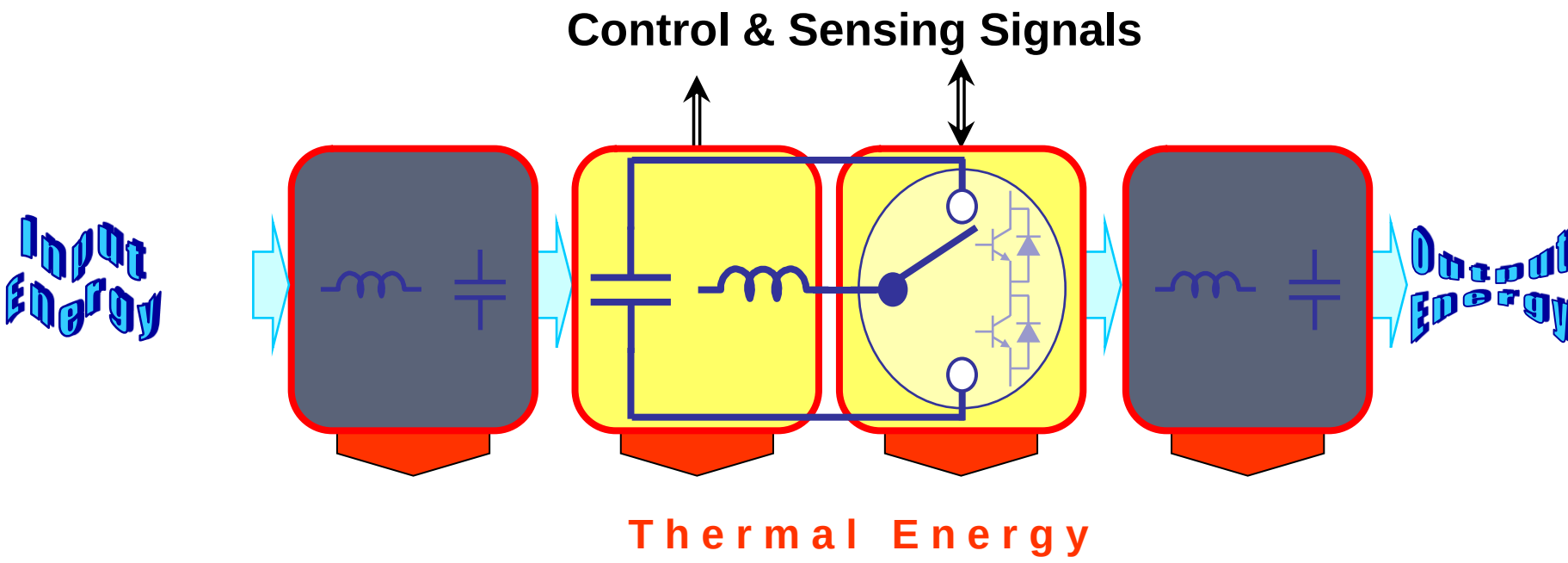


$$\eta = \frac{P_{out}}{P_{in}} = \frac{I_{out}\,V_{out}}{I_{in}\,V_{in}} \cong \frac{V_{out}}{V_{in}}$$

Switched-mode conversion

To maximizes the energy transfer the power systems must be designed using energy storage elements (inductor and capacitor) and switches :

- Capacitive (Charge Pump)
- Magnetic

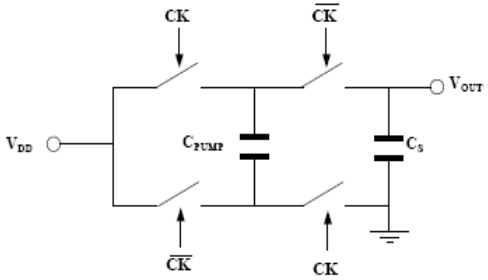


Capacitive Switch- mode conversion : Charge Pump

The energy is periodically stored into and released from the E filed of the Pump or Flying capacitors. They are typically used in applications requiring relatively small amounts of current.

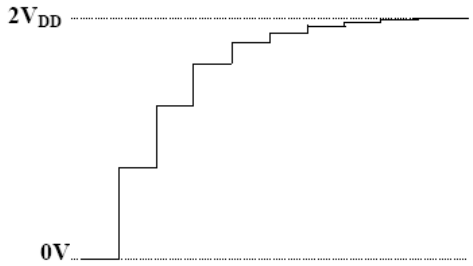
- Reduced components
- Integration

Example Voltage Step-Up



This scheme is the simpler Charge pump structure and its dynamic output voltage is

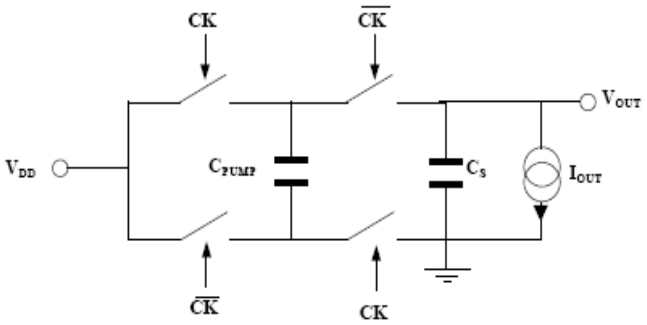
$$\Delta V_{OUT}(n \cdot T_{SW}) = \frac{C_{PUMP}}{C_{PUMP} + C_S} \cdot [2 \cdot V_{DD} - V_{OUT}((n-1) \cdot T_{SW})]$$



Without output current we have

Capacitive Switch- mode conversion : Charge Pump

In case of load



$$Q = I_{OUT} \cdot T_{SW}$$

The voltage is reduced

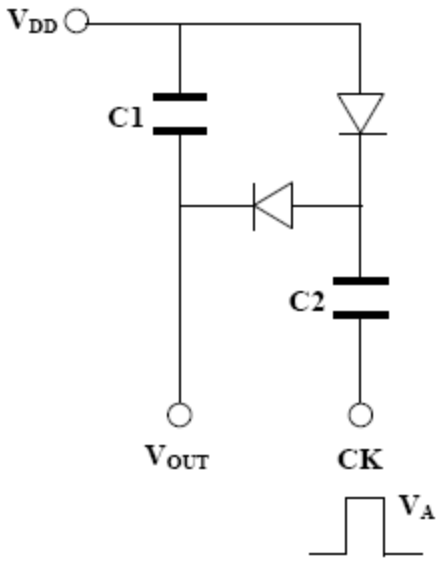
$$\Delta V = \frac{Q}{C_{PUMP}} = \frac{I_{OUT}}{C_{PUMP} \cdot f_{SW}} \qquad R_{OUT} = \frac{1}{C_{PUMP} \cdot f_{SW}}$$

The variable available to control the converter in the frequency

With Ideal components the efficiency is

$$\eta = 1 - \frac{I_{out}}{4 f_{sw} C_{pump} V_{dd}}$$

Capacitive Switch- mode conversion : Charge Pump (discrete)



$$V_{DD} + V_2 + \Delta V_2 + \Delta V_1 - V_1 = V_A$$

$$\Delta Q_1 = \Delta Q_2 \quad \Rightarrow \quad \Delta V_1 = \Delta V_2 \cdot \frac{C_2}{C_1}$$

$$\Delta V_2 \cdot \left(1 + \frac{C_2}{C_1}\right) = V_A - V_2$$

$$\Delta V_2 = \frac{C_1}{C_1 + C_2} \cdot (V_A - V_2)$$

$$V_{DROP} = 2 \cdot V_D + \frac{I_{OUT}}{f_{SW} \cdot C_1}$$

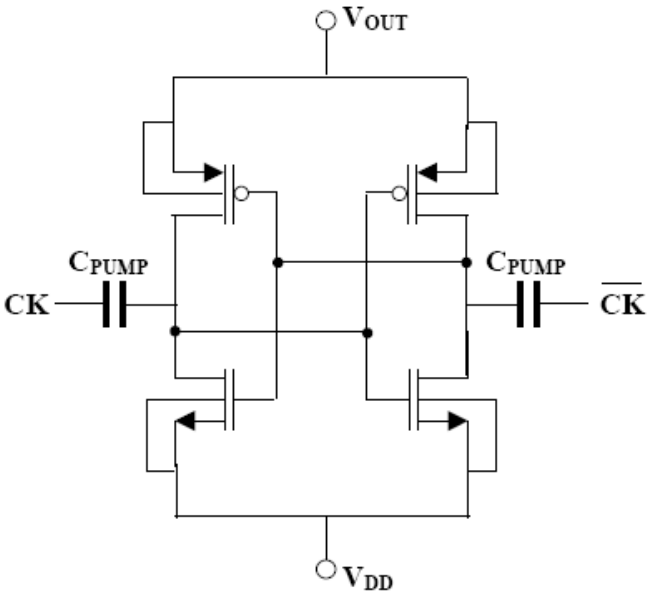
$$V_{OUT} = N \cdot V_{DD} - (N-1) \cdot V_{DROP} = N \cdot V_{DD} - (N-1) \cdot \left(2 \cdot V_D + \frac{I_{OUT}}{f_{SW} \cdot C_1}\right)$$

Switched capacitor with MOS

- Two phase charge Pump

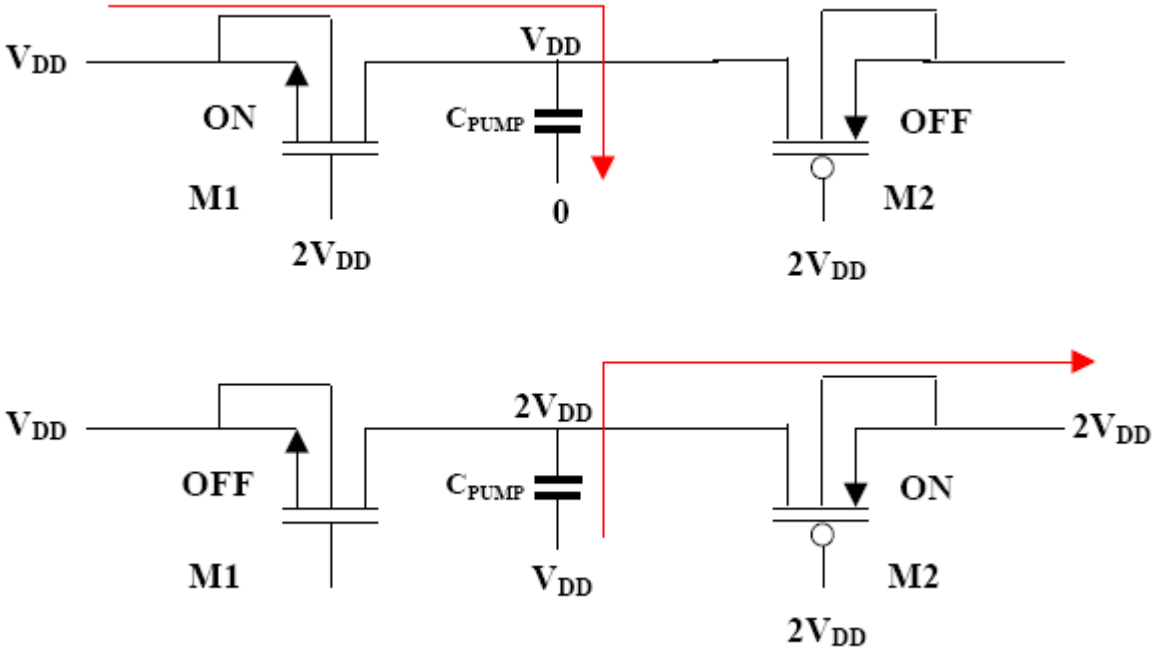
$$R_{OUT} = \frac{1}{2 \cdot f_{SW} \cdot C_{PUMP}}$$

$$R_{OUT} = \frac{1}{2 \cdot f_{SW} \cdot C_{PUMP}} \cdot ctnh\left(\frac{1}{4 \cdot f_0 \cdot R \cdot C_{PUMP}}\right)$$



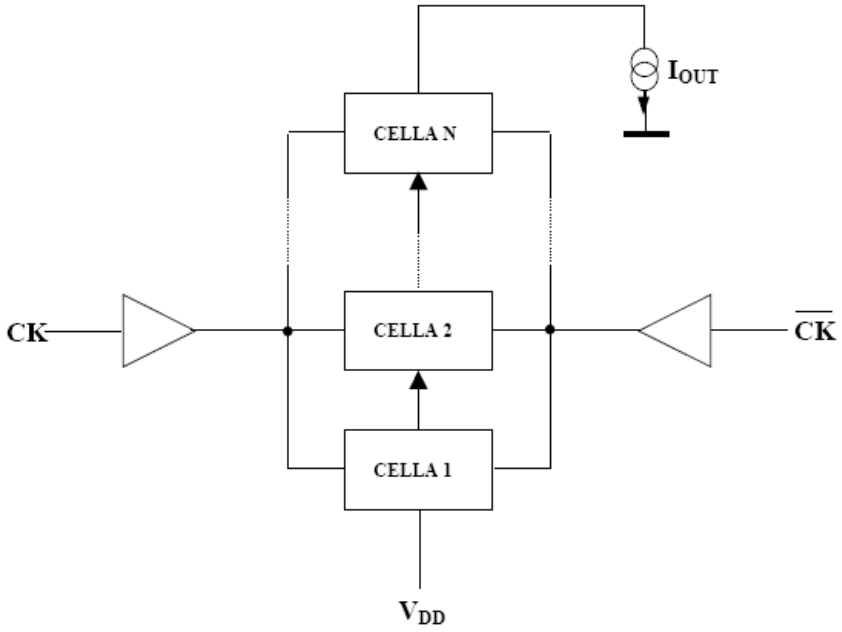
If the RdsON is big the equivalent resistance is higher because during the turn on time the pump capacitor it isn't completely charged.

Detailed description



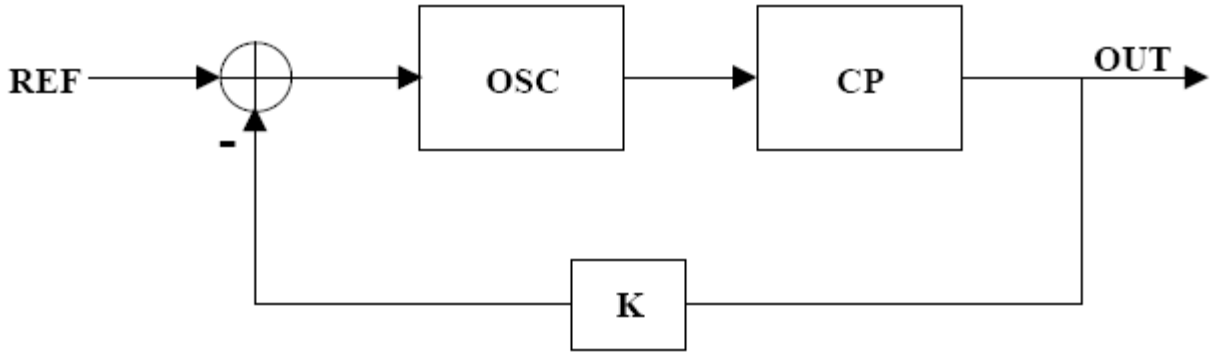
Big Step Up function

- For an higher output voltage the cell can be connected

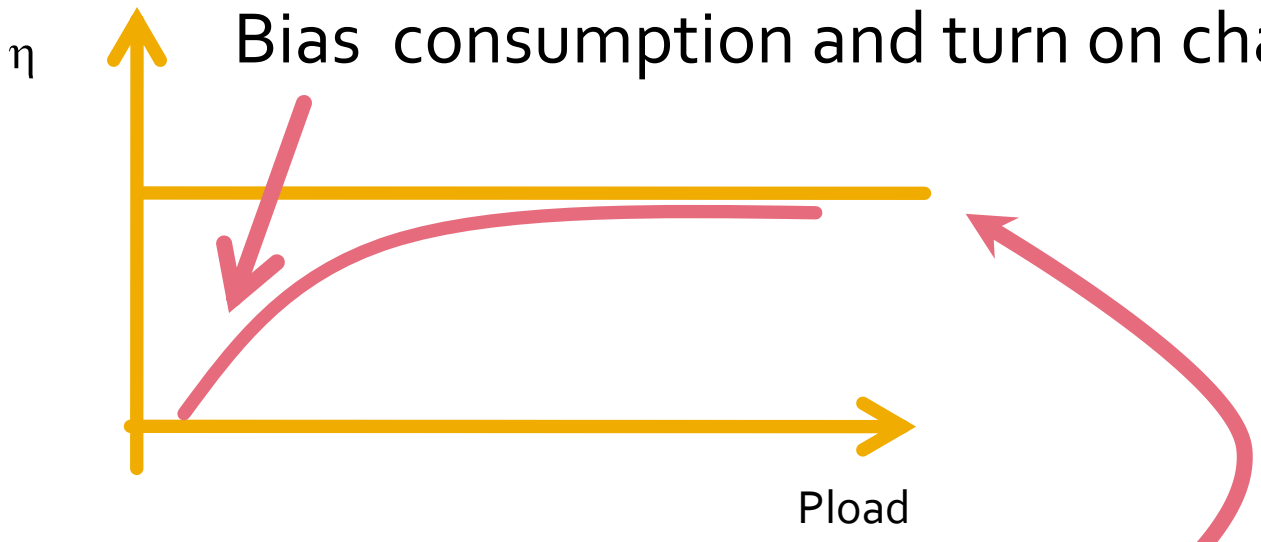


Charge pump control system

- If the Charge pump is controlled it modulates its equivalent resistance in order to achieve the output voltage level. From an efficienty point of view it is equivalent to a LDO



Switch cap conversion efficienty



$$\eta = \frac{P_{out}}{P_{in}} \cong \frac{V_{out}}{2V_{in}}$$

Magnetic power conversion

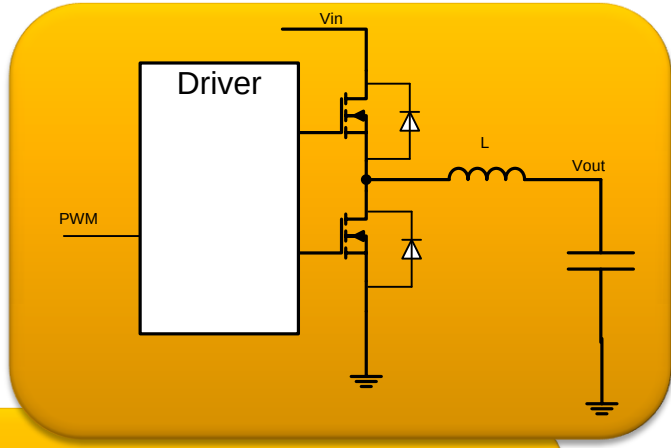
This type of circuits are based on using the magnetic field to store the energy of inductor or transformer other than the electric field of the capacitors.
It's possible classifying the converter on the basis of

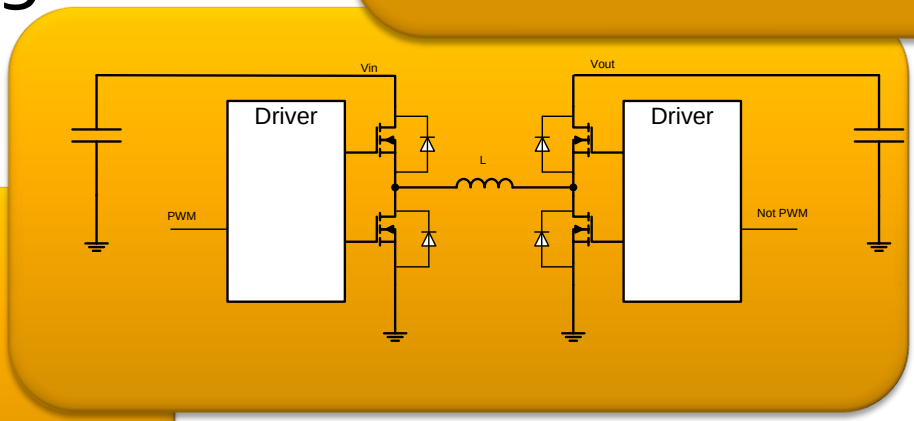
- type source and load
  - AC-AC
  - AC-DC Rectifier
  - DC-AC Inverter
  - DC-DC
- presence or not of a transformer
  - Non isolated
  - Isolated
- mode of operation
  - DCM
  - CCM
- switching condition
  - Hard switching
  - Resonant

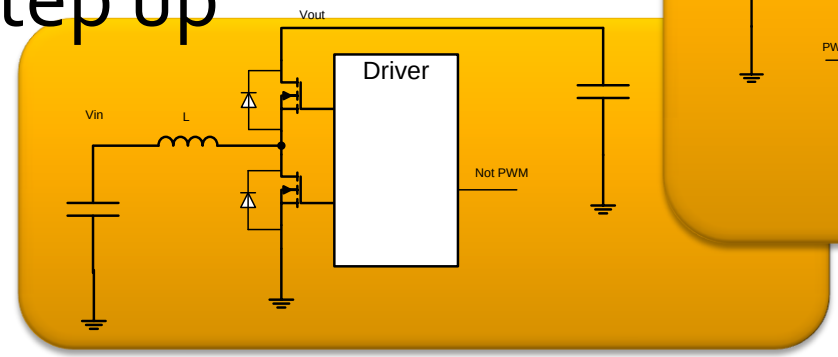
Type of converter

In general application IC integrated the different soultion utilized are

- Step down
- With the same voltage rate
- Step up



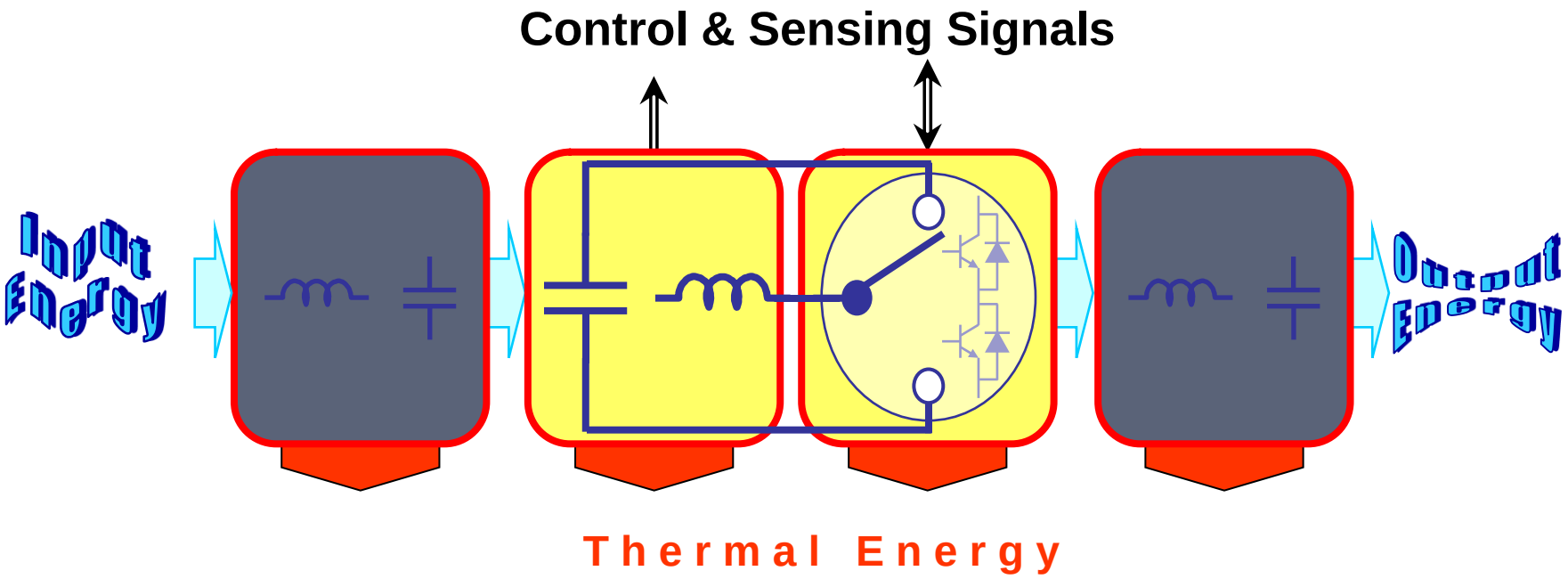




Switched-mode control

To meet the load and source specification is needed a control system :

- Voltage mode if the sensing signal is only the voltage
- Current mode if in the sensed signal there is the current



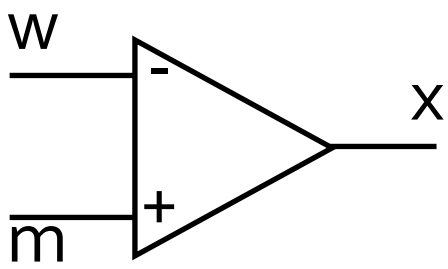
Modulation

Each switch has two possible level so the control system can only modulate the duration of each state:

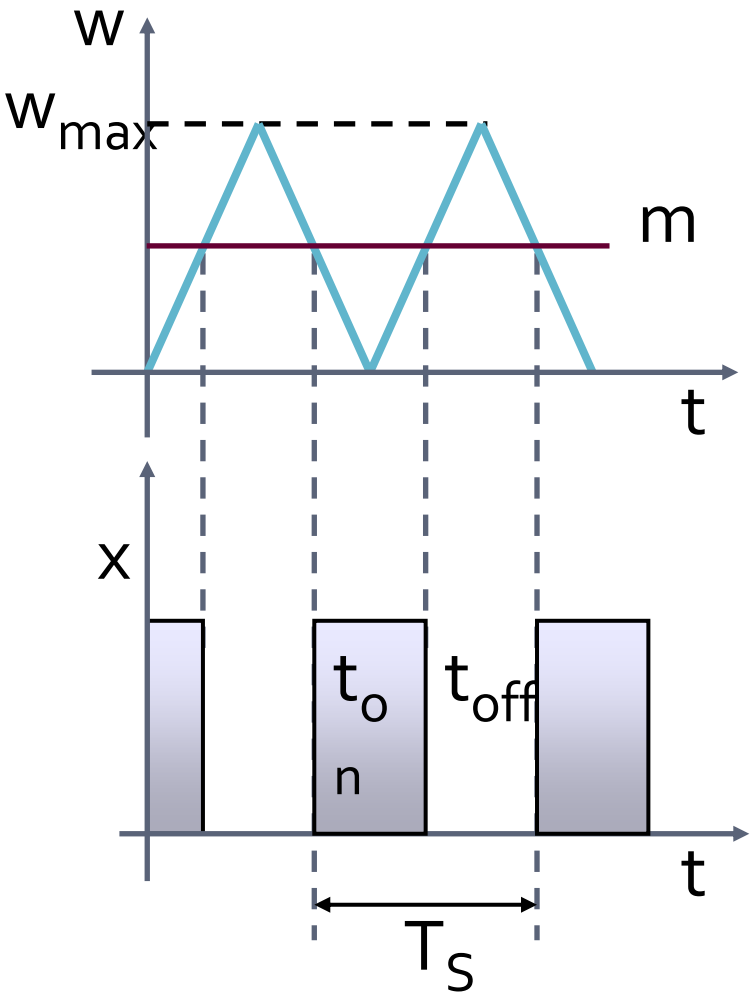
- **Frequency modulation**
  - Ton constant
  - Toff constant
  - Duty constant
- **Fixed frequency**
  - Pulse width modulation

Pulse width modulation at constant frequency

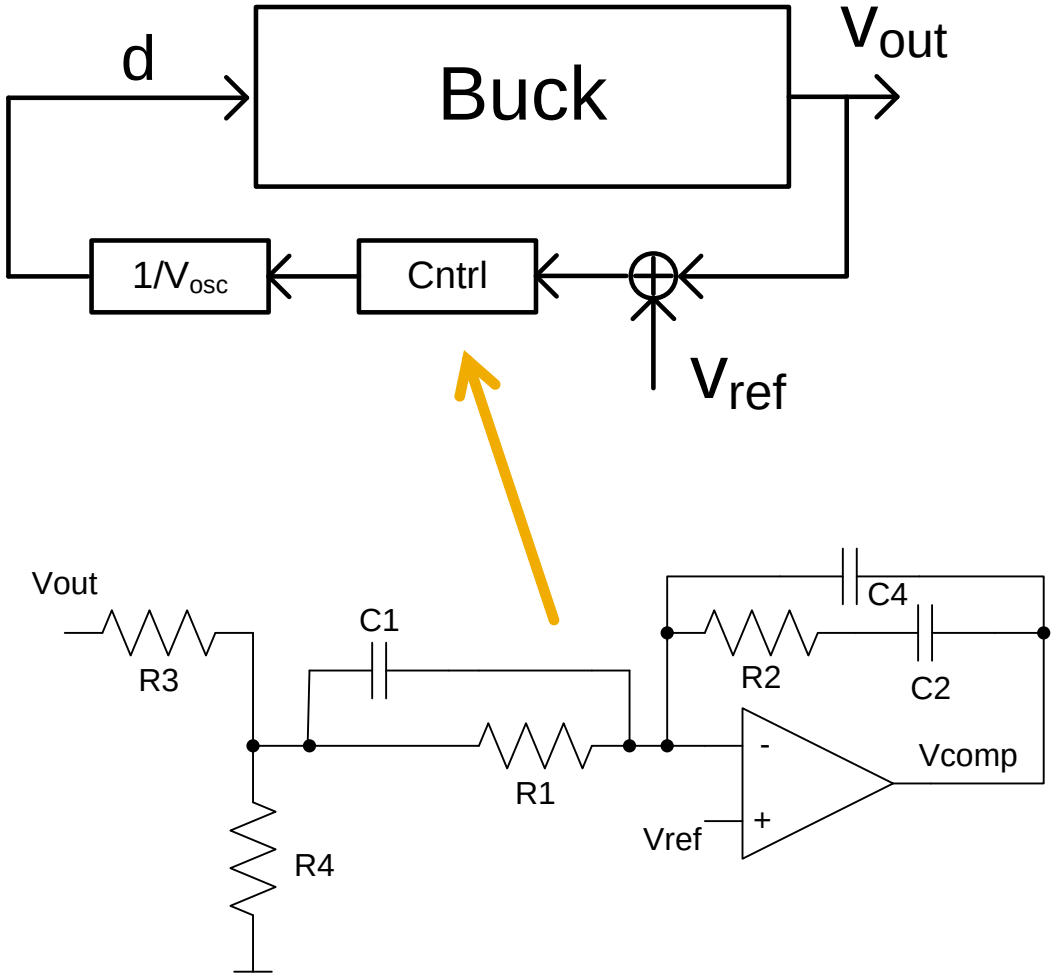
m = Constant



$$\delta = \frac{t_{on}}{T_S} = \frac{m}{W_{max}}$$



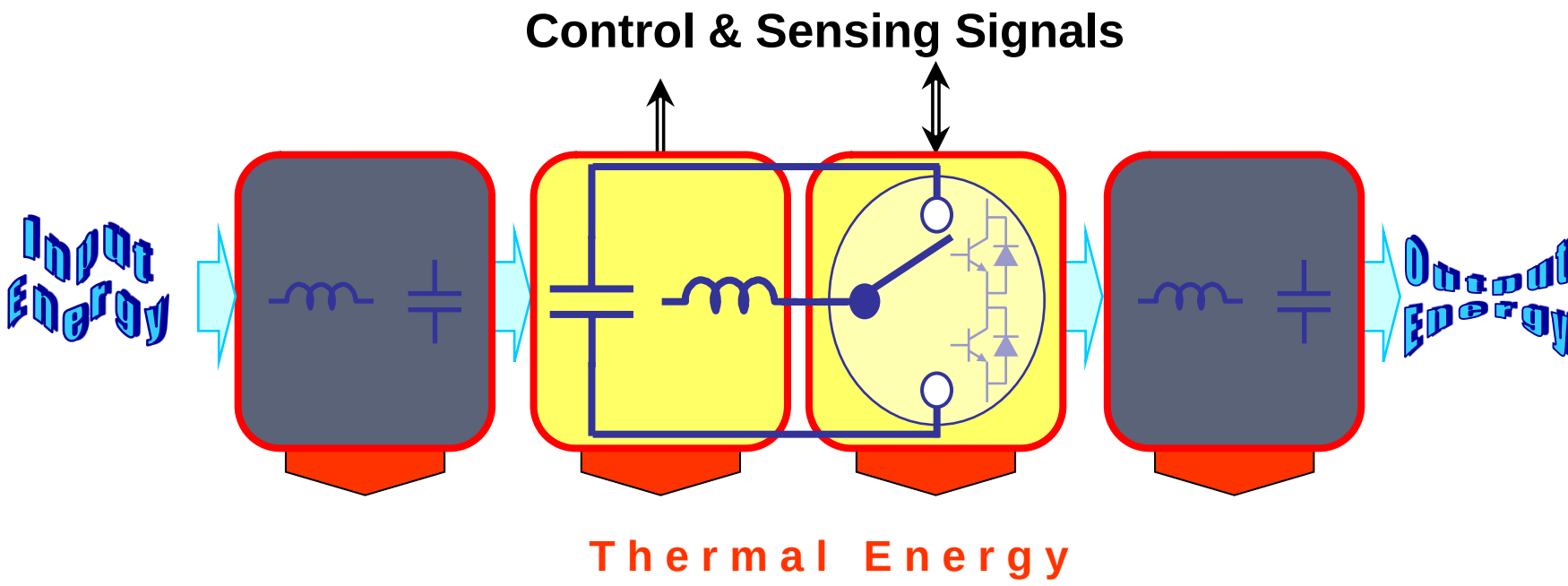
Control loop



Switched-mode control

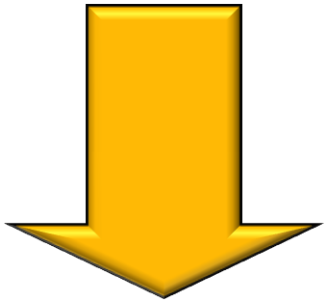
To meet the load and source specification is needed a control system :

- Voltage mode if the sensing signal is only the voltage
- Current mode if in the sensed signal there is the current



Power Switch: Power MOS

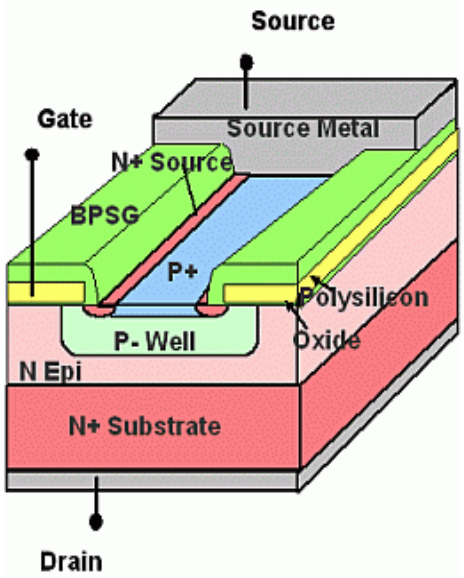
- Power switch requirements for MOSFET:
  - Low Rdson $\Rightarrow$ Low L and high W
  - High breakdown $\Rightarrow$ Body region low doped

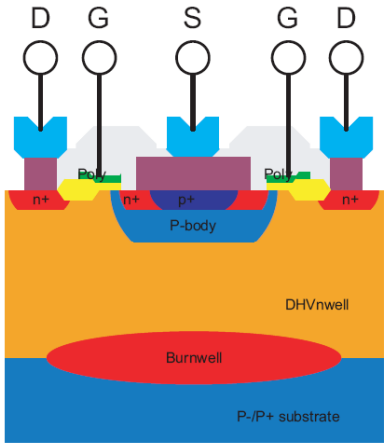


Punch through when the channel is fully depleted

Power MOSFET

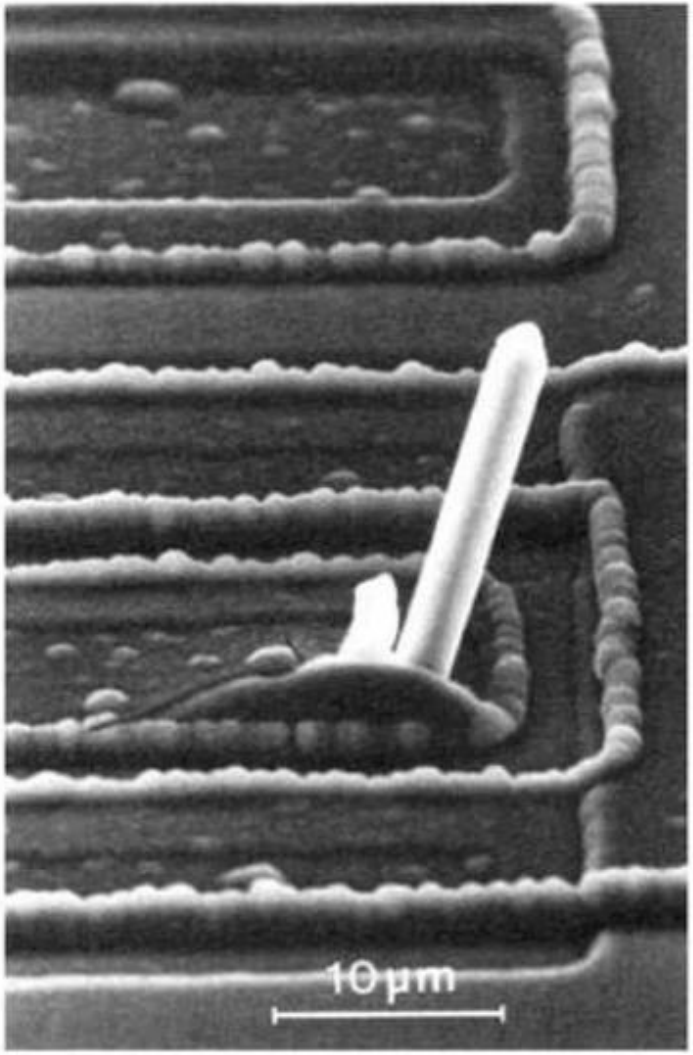
Vertical power MOS

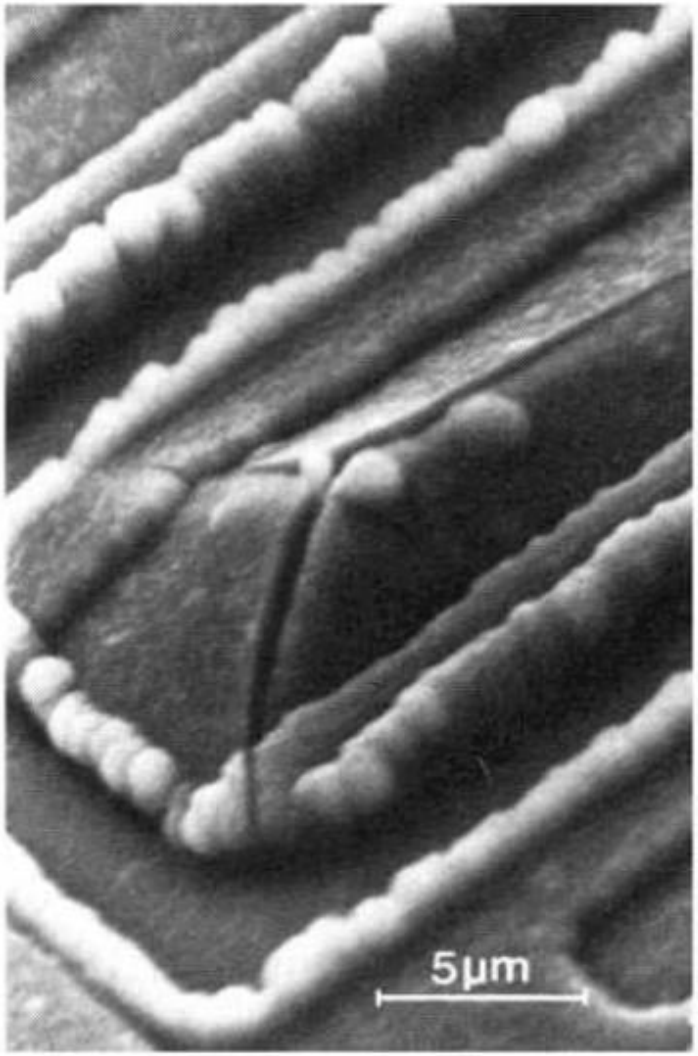




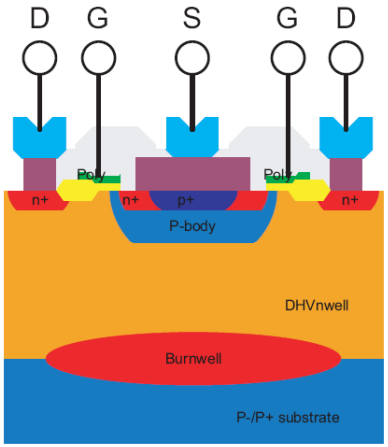
- This structure has the high breakdown voltage and low Rdson:
  - During the off state the depletion region is present in the Nepi
  - The Rds on decreases by reducing the channel length

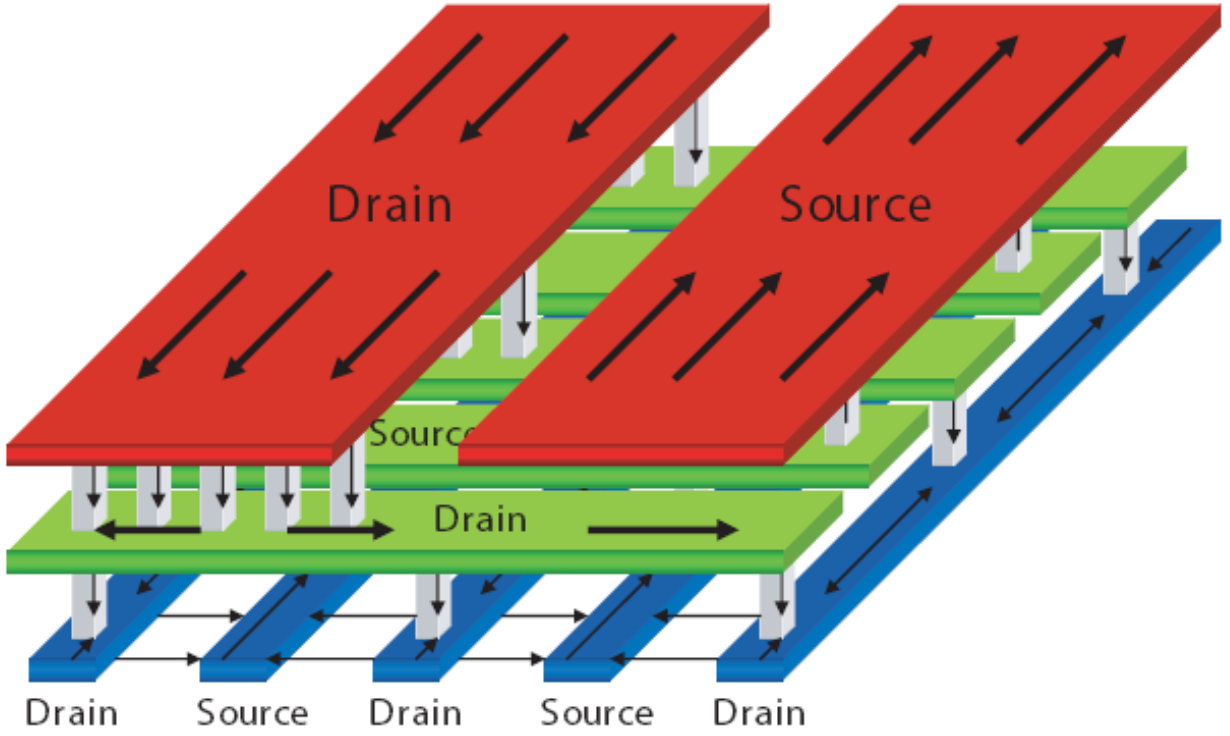
Electromigration problem



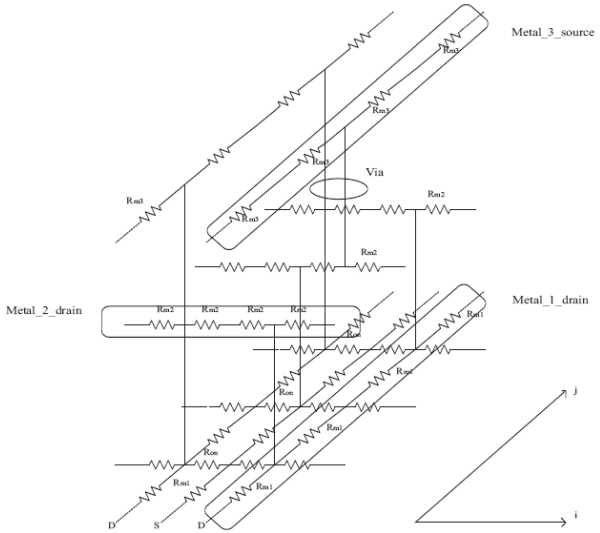


Layout power MOSFET

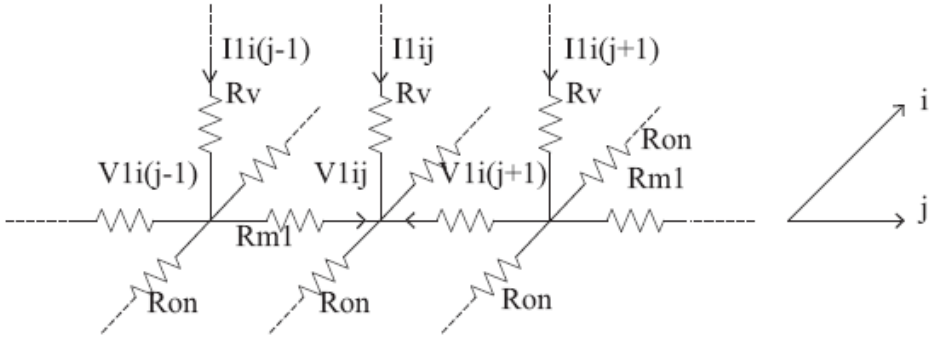




Rdson contributions

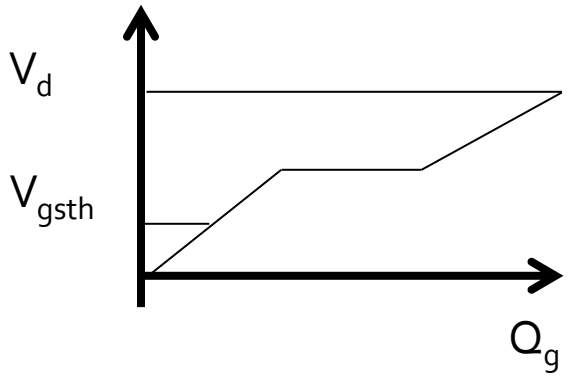


R_{totale}	$410m\Omega$	100%
$R_{bonding}$	$80m\Omega$	20%
R_{metal}	$40m\Omega$	10%
R_{mos}	$290m\Omega$	70%



POWER MOS commutations: Gate charge curves

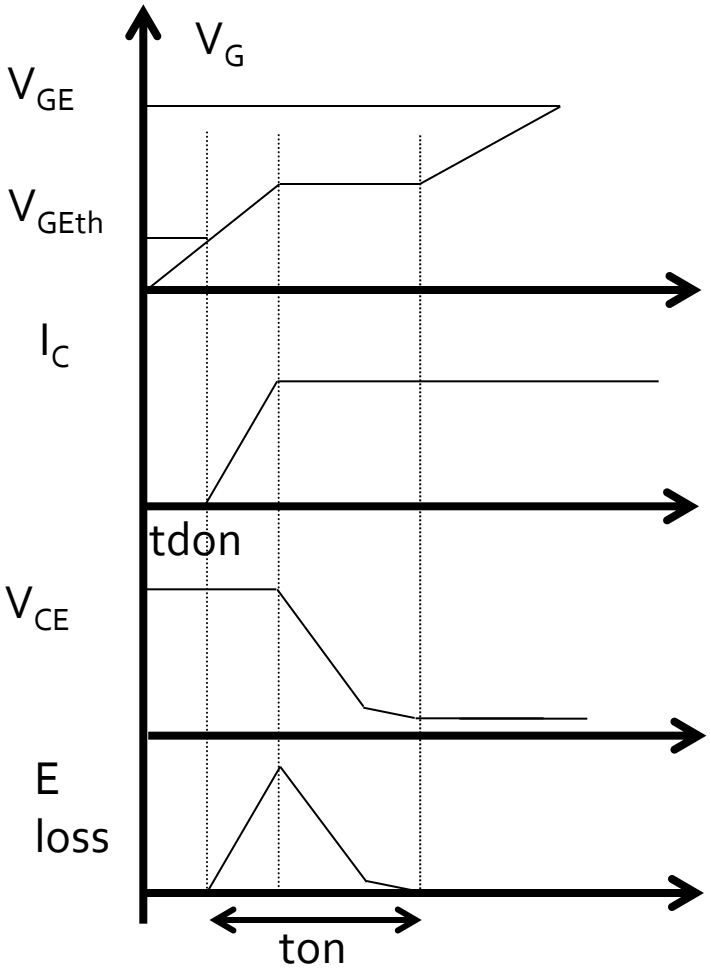
- The MOS commutation characteristic with an inductive load is described by the gate charge curves
- This curves is a charge controlled representation of the power MOS. They report the relation between the Vgs voltage and the charge injected in the gate to drive the device in relation with the switching condition (Ids, Vds)



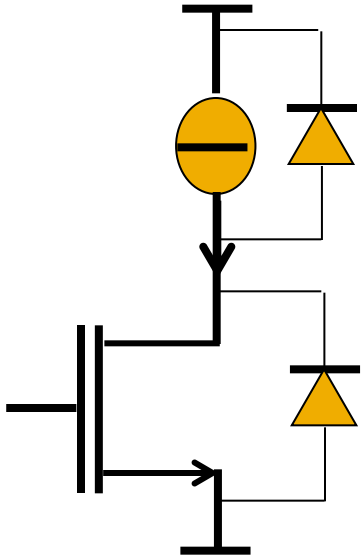
POWER MOS commutations: Gate charge curves

- The importance of the gate charge curves is related to the driving circuit design because they represent the relation between the driving mode and the switching losses.
- The gate charge curves depends on the switching condition (Il ,Vds) and on the parasitic present on the application but almost they don’t depend on the driving circuit.

POWER MOS commutations: Gate charge curves



- The ideal inductive commutation
- With a fixed inductor current level and voltage level
- Considering an ideal diode



Gate charge in real condition

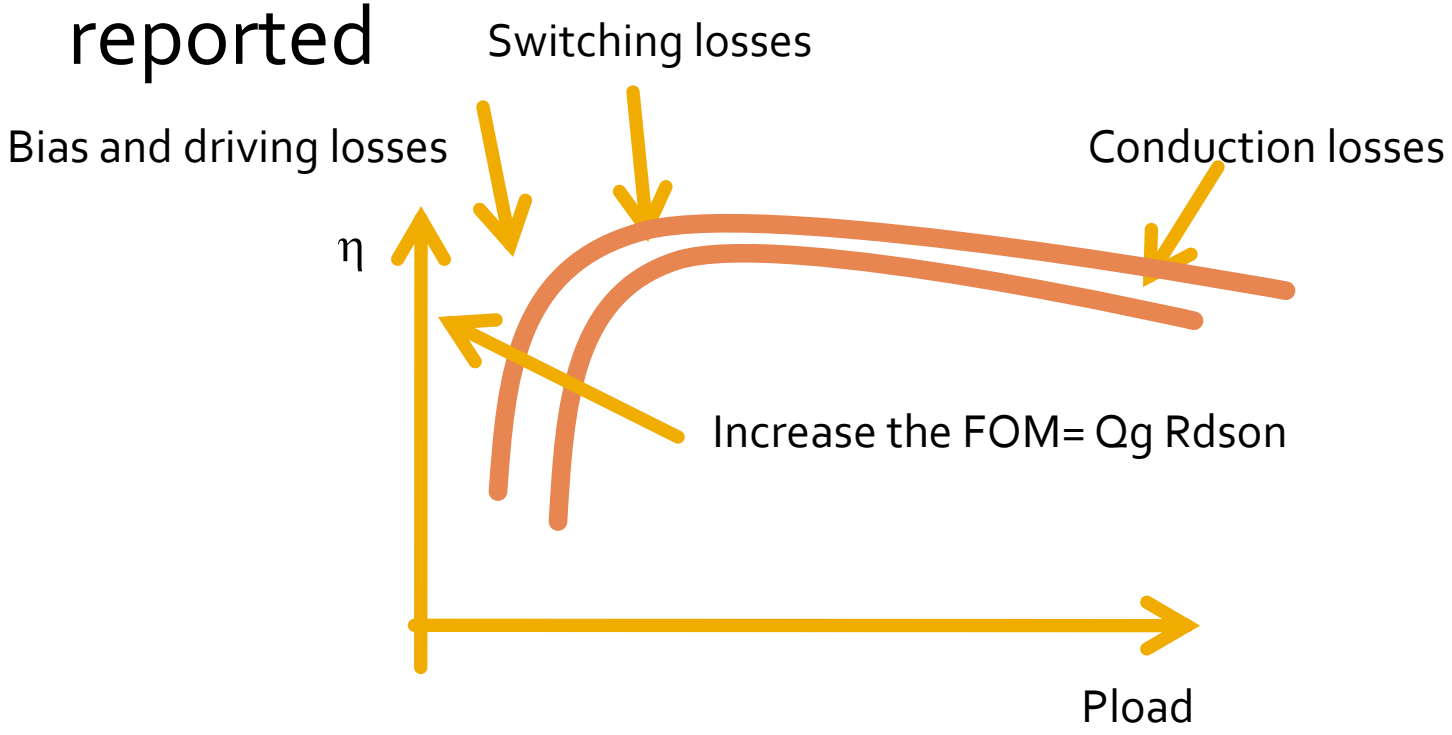
- The parasitcs elements presents on the applications change the gate charge of the turn on and the turn off
  - The capacitor of the Vds
  - The diode reverse recovery
  - The parasitc inductor Ls and Ld

Driving specification depending on gate charge

- The driver ideal commutation can be calculated in the application considering the condition of maximum current but is a rare approssimation.
  - The driver current depends on the impedance
- The real commutation depend on the voltage hence the impedance present on the application that depend on many parameters:
  - Ls that is vary important because it effects is amplified by
  - Lgate and Rgate limits the driving capabiity

Choose the correct architecture

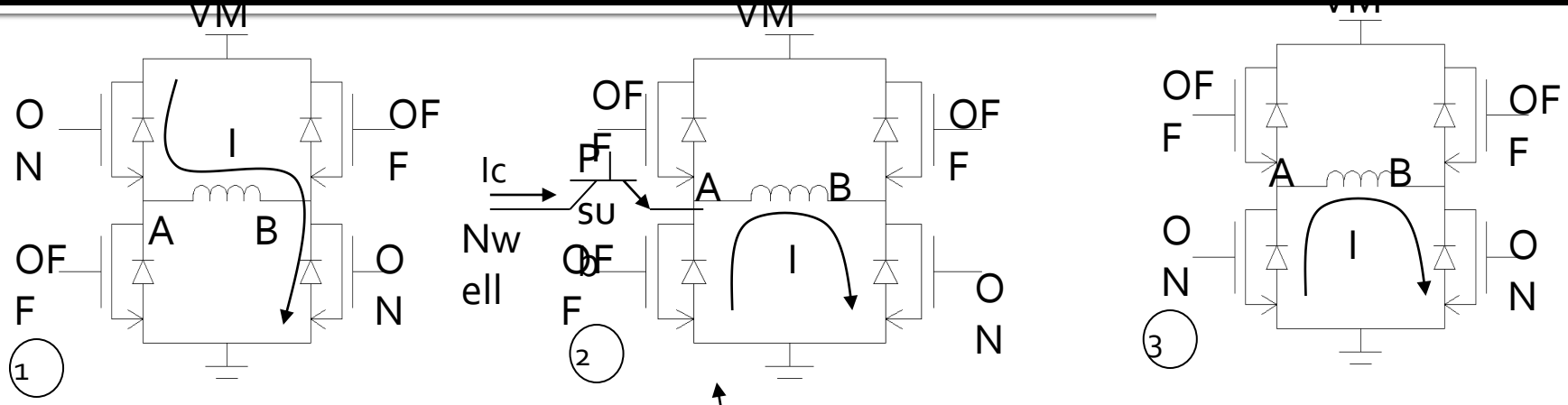
Dependely on the architecture the power related to the converter can be plotted as reported



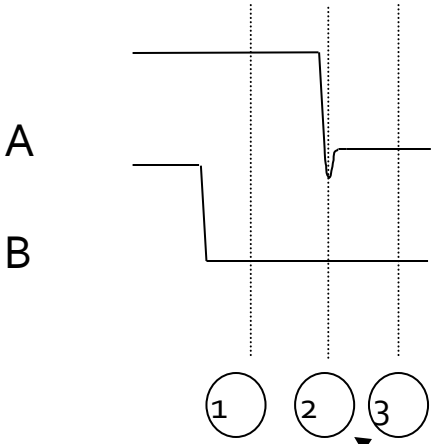
Power MOS limitations

- The limitations of the power MOS is for the High current and voltage application:
  - To increase the operating voltage (during turn off) it is necessary increase the width of the n-epi region
  - The $R_{ds\ on}$ depends also by the R_{epi} resistance
  - Trade off between max turn off V_{ds} and $R_{ds\ on}$

When does NPN turn on?



Fly-BACK PHASE

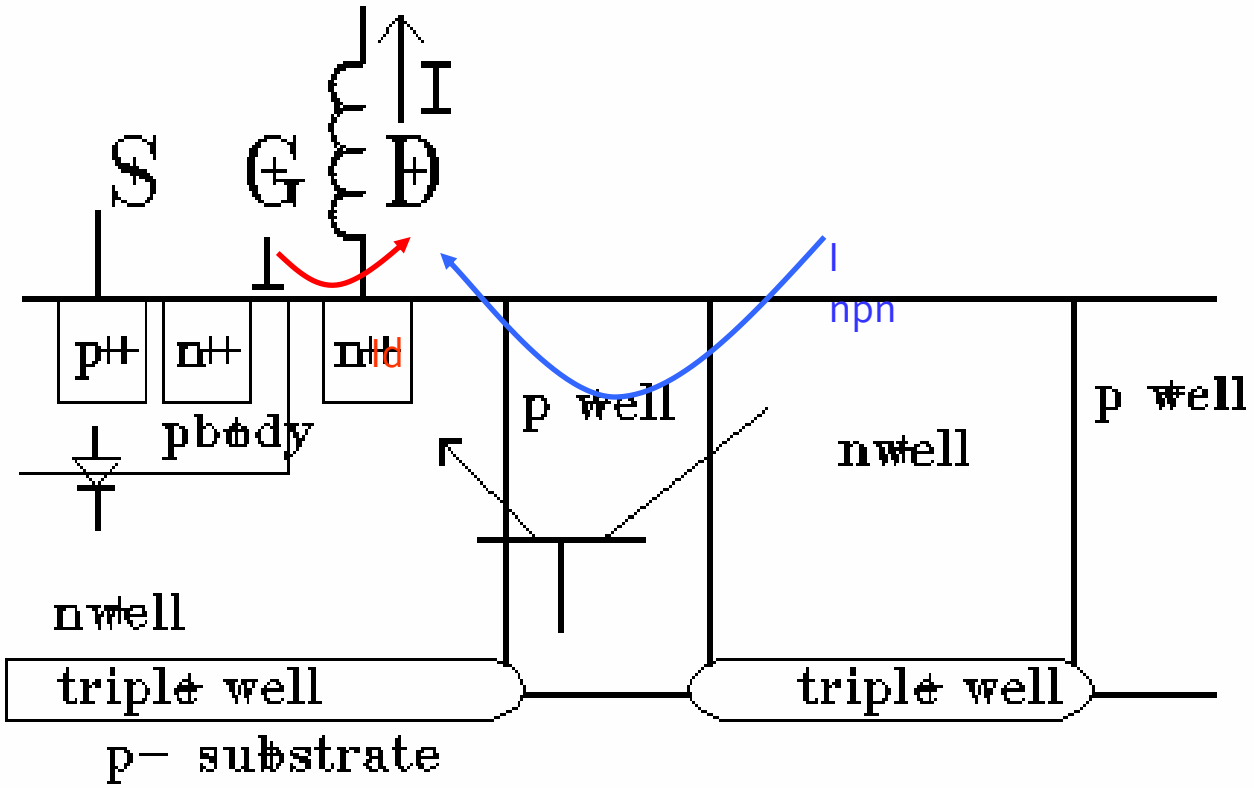


During phase 2 (high to low transition of A) both HSD and LSD are OFF due to the cross conduction control.

In this phase the inductor current flows through the intrinsic diode turning on the parasitic NPN.

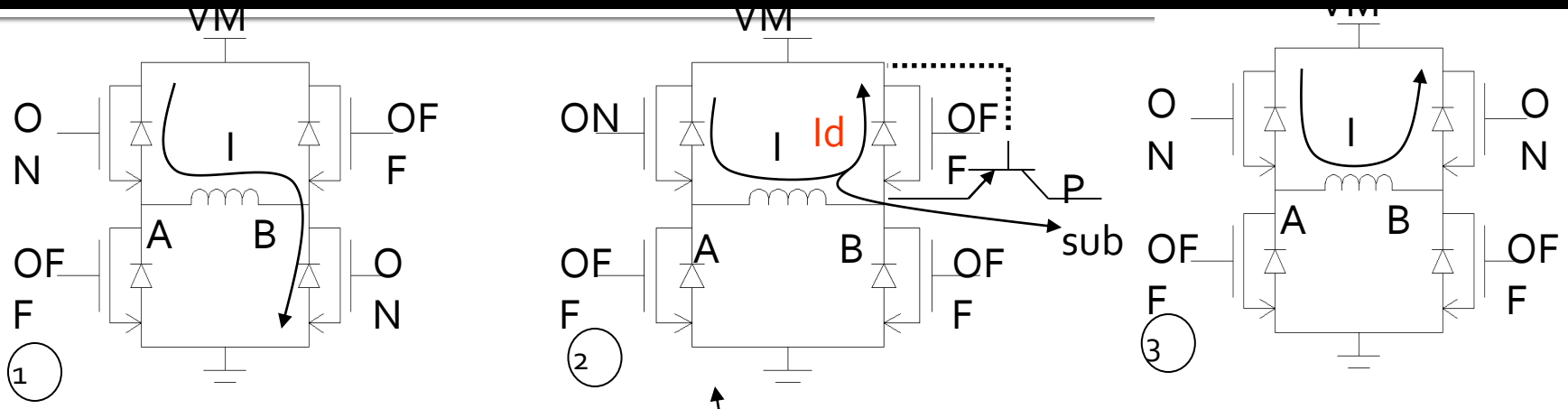
Parasitic NPN

negative fly back phase

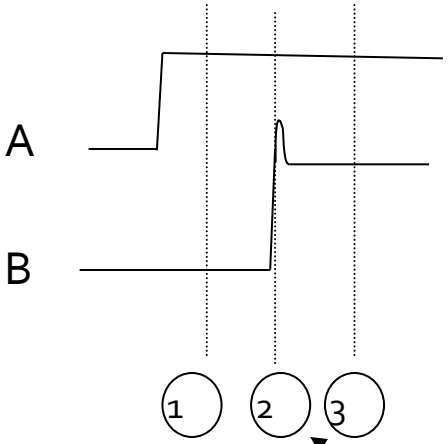


The Collector current flows from other pockets close to the Power.

When does PNP turn on?



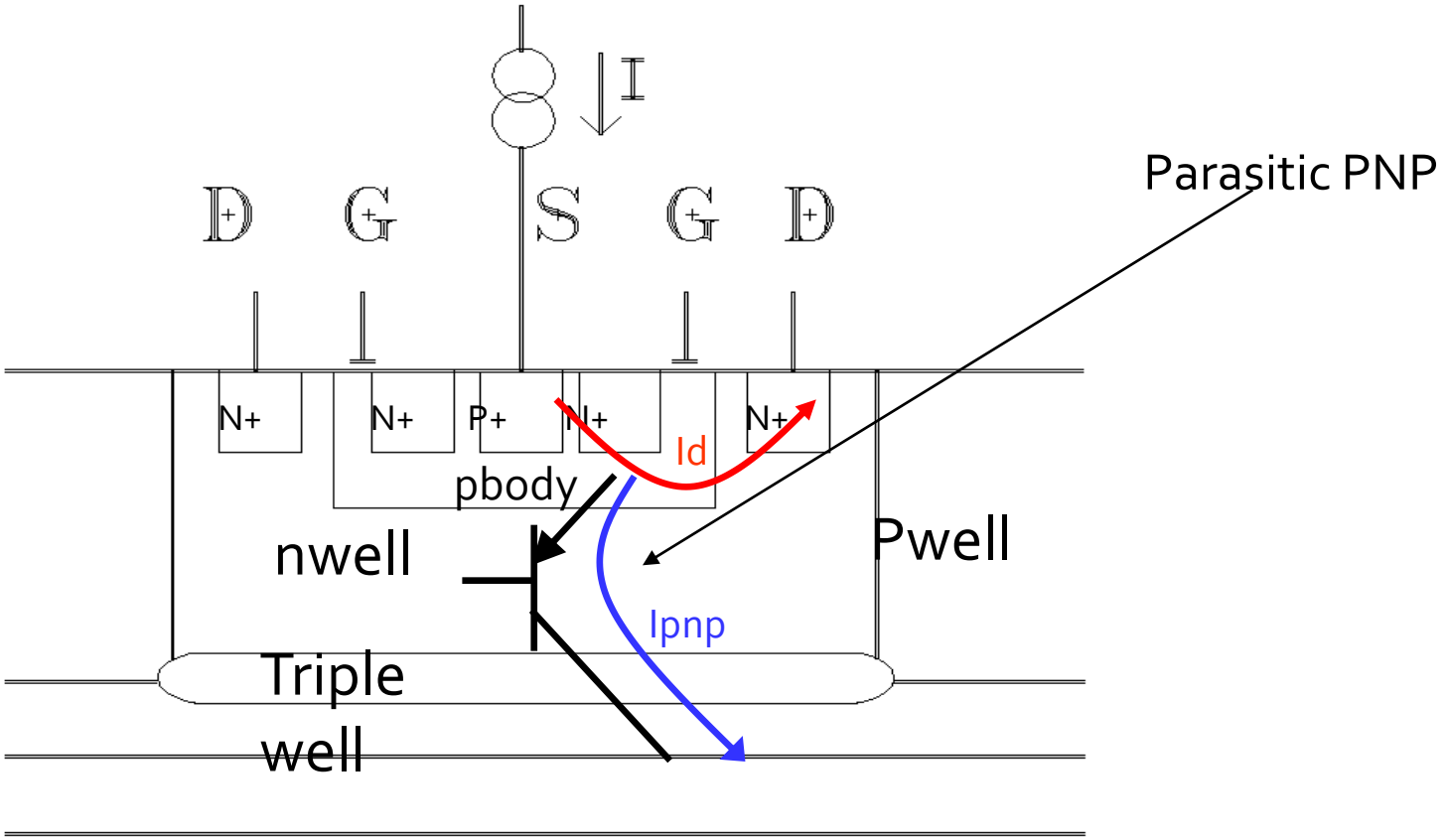
Positive Fly-BACK PHASE



During phase 2 (low to high transition of B) both HSD and LSD are OFF due to the cross conduction control.

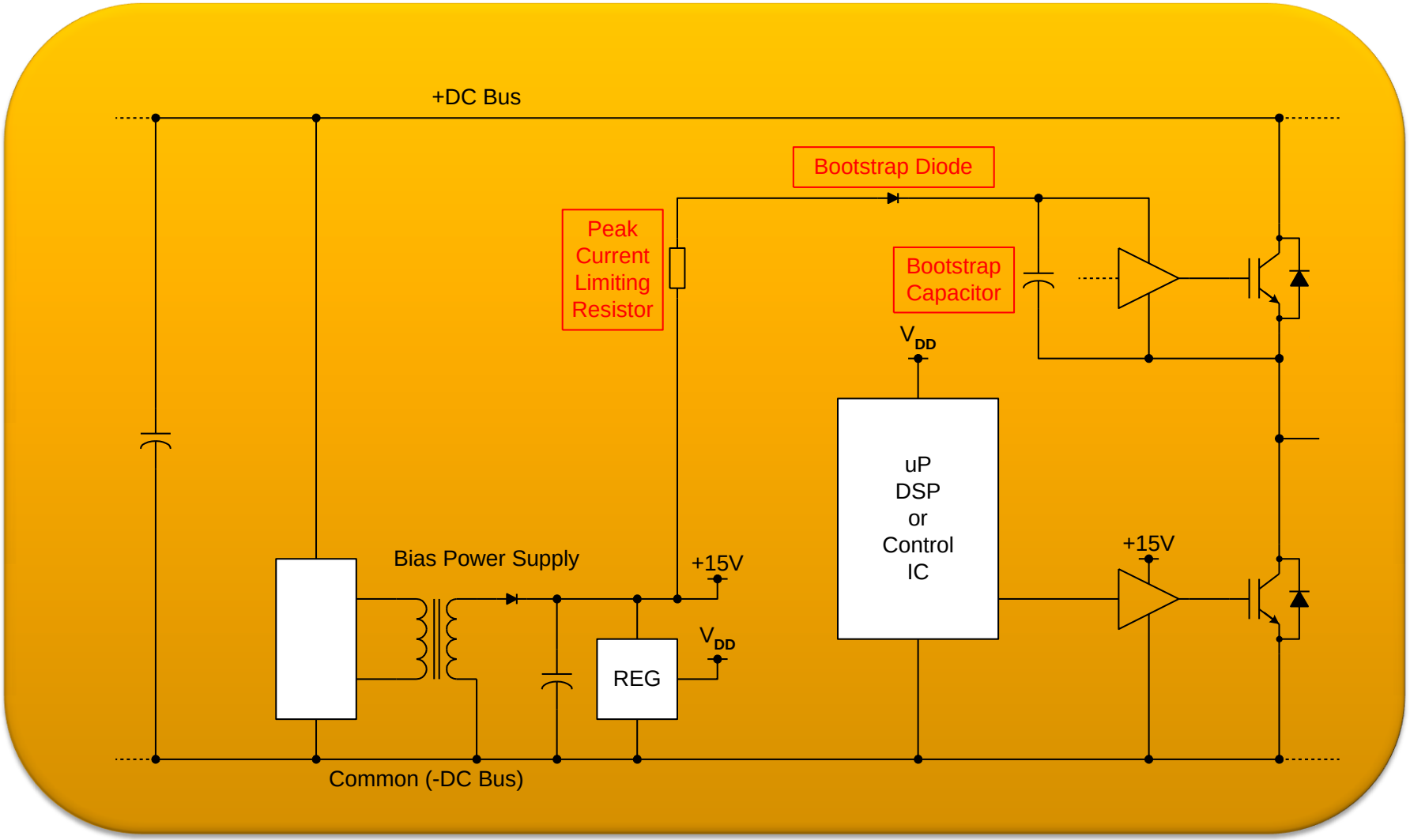
In this phase the inductor current flows through the intrinsic diode "Id" turning on the intrinsic parasitic PNP.

Parasitic PNP
positive fly back phase

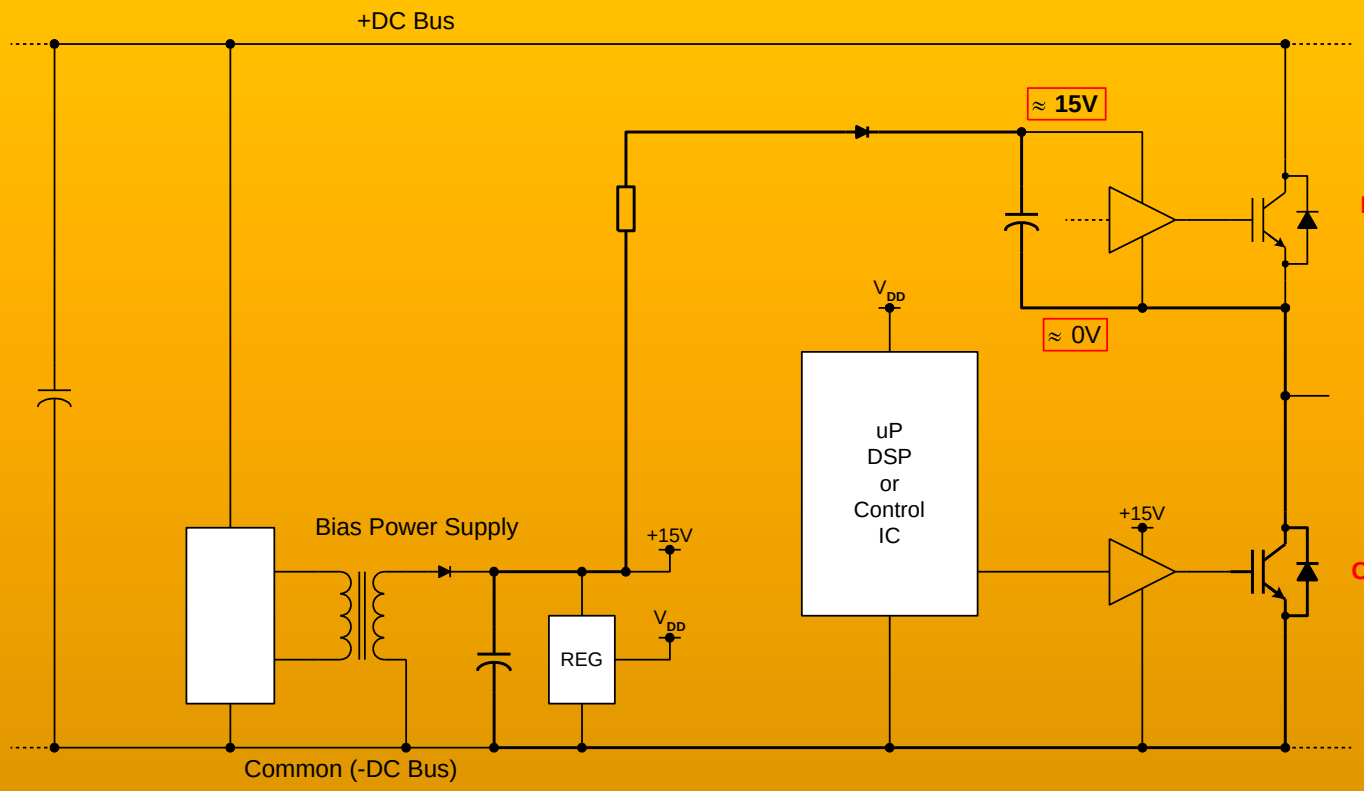


The PNP Collector current flows into the substrate rising its voltage

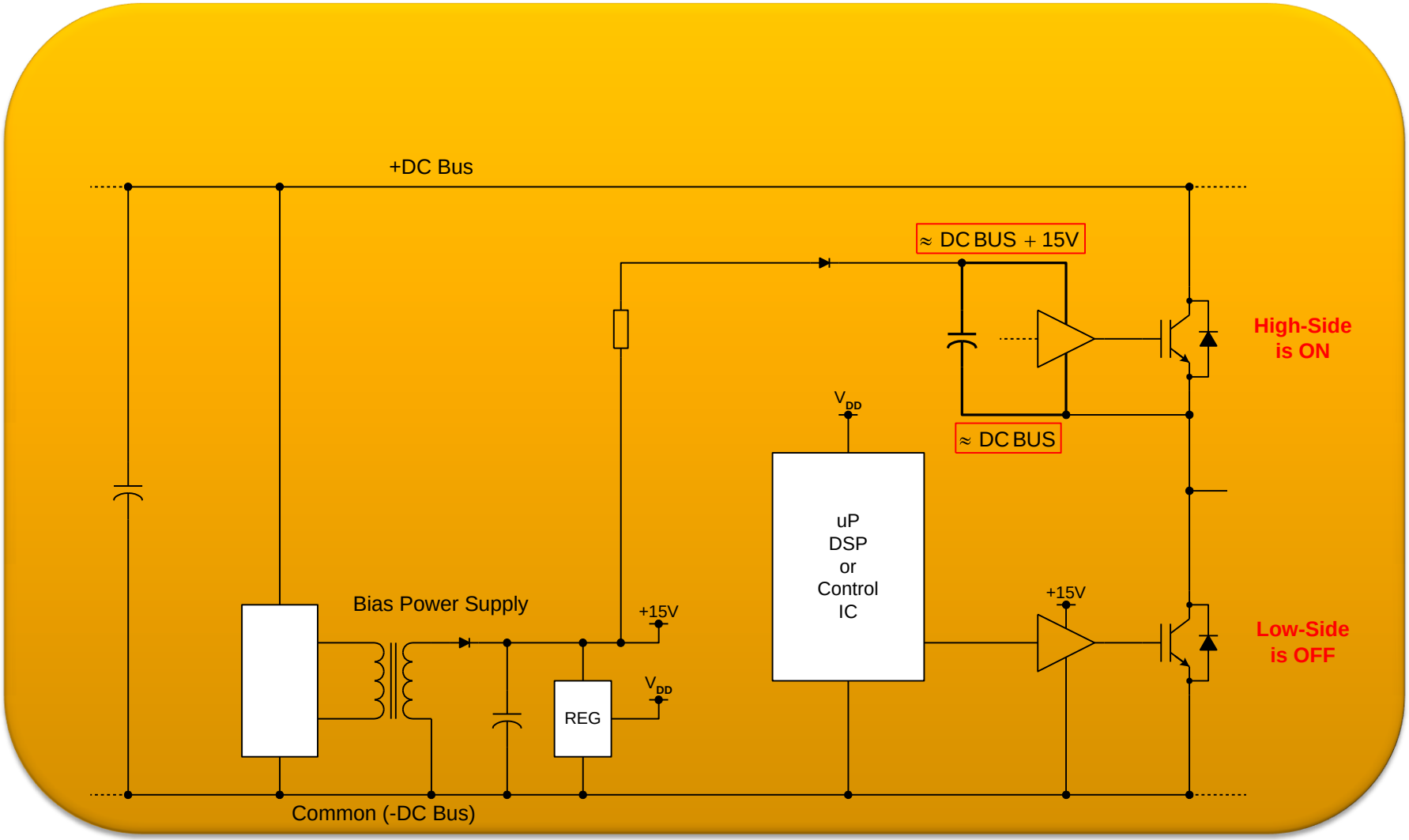
"Bootstrap" Supply for High-Side Power



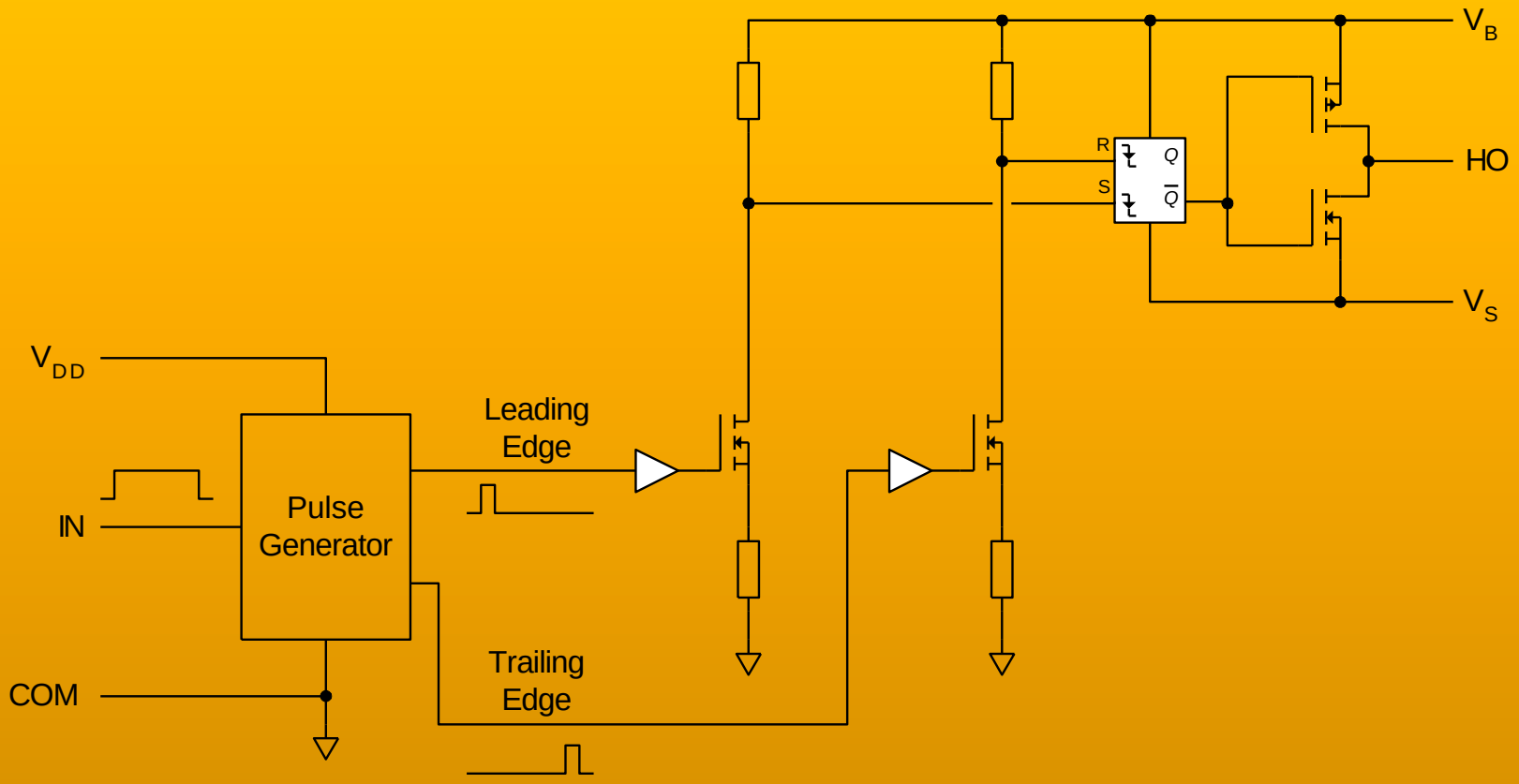
Bootstrap Cap Charges When Lo-Side ON



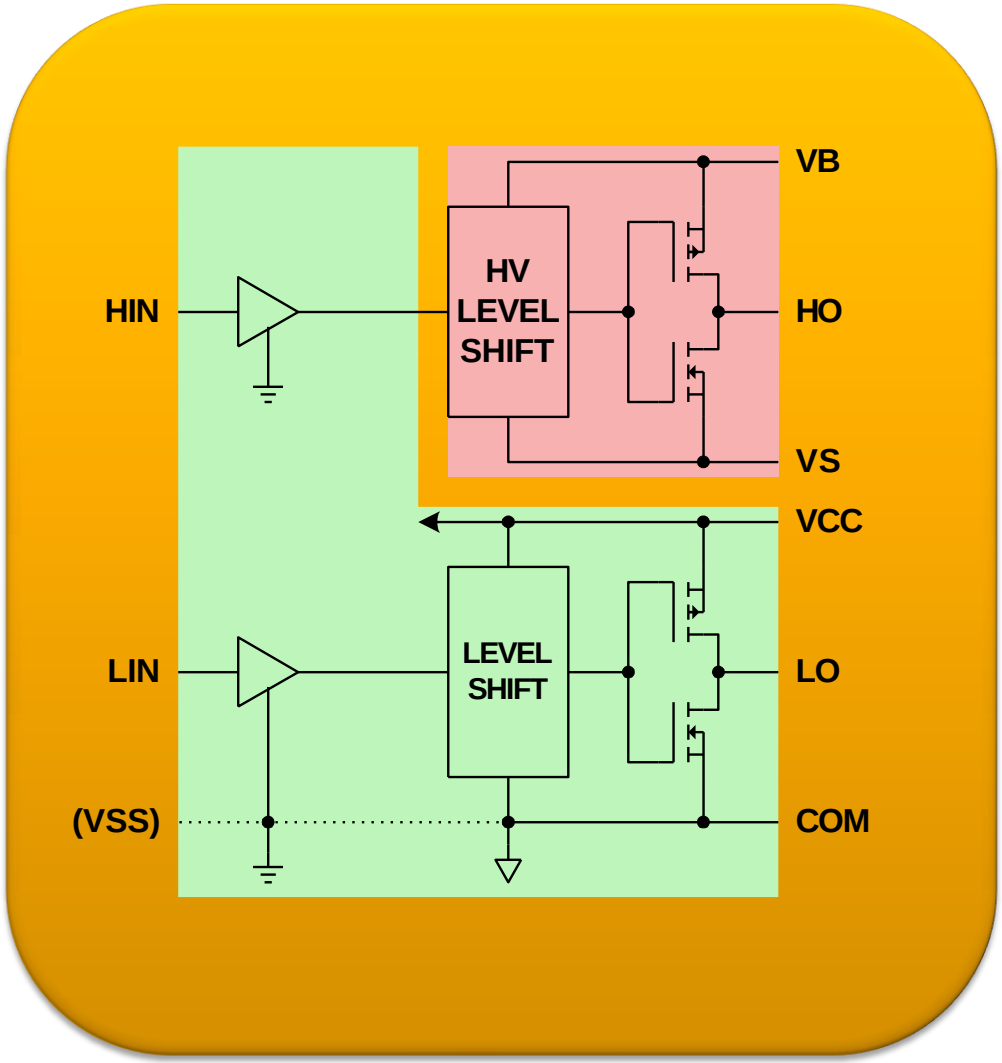
Cap Supplies Power When Hi-Side ON



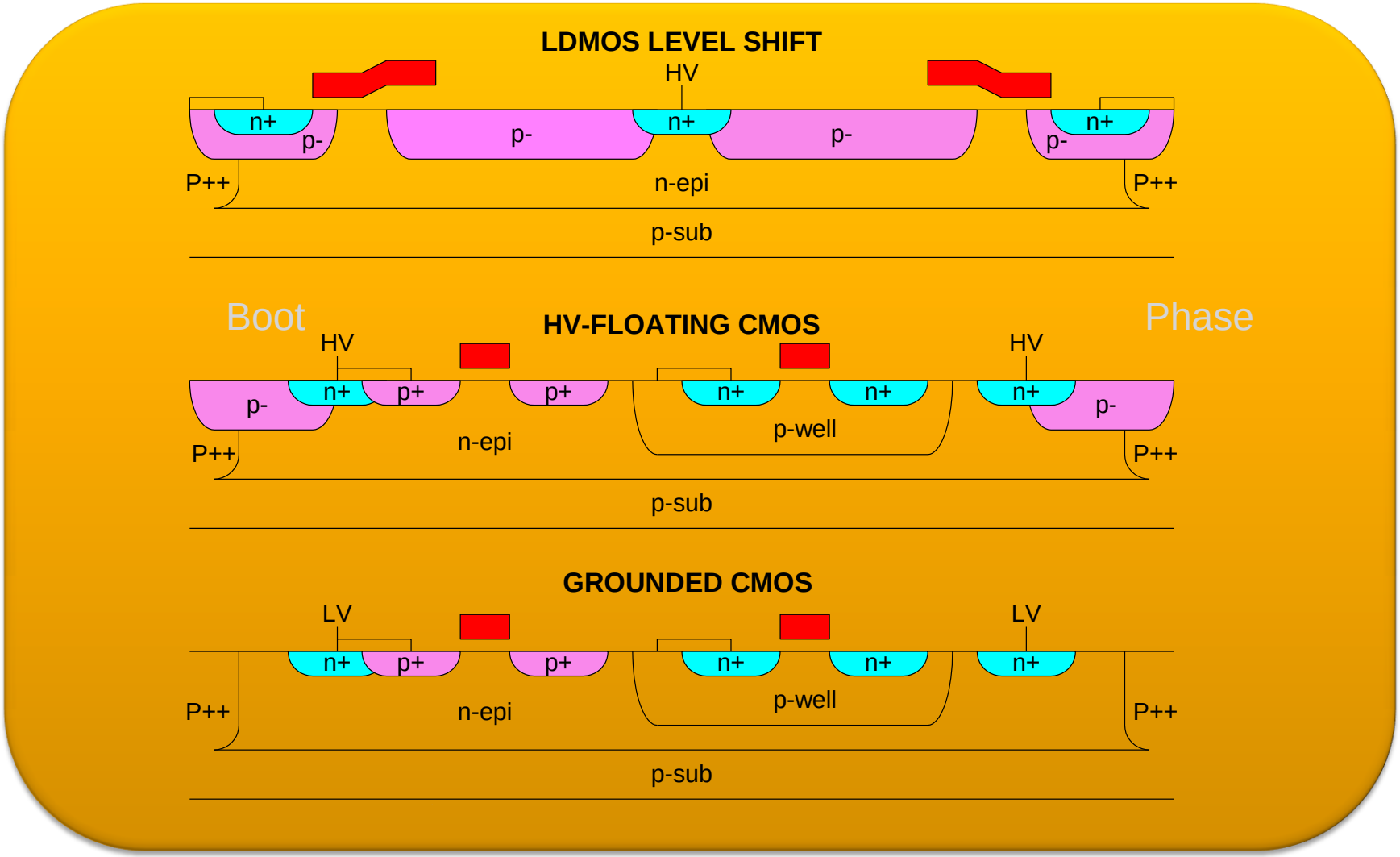
High Voltage IC Level-Shifting Driver



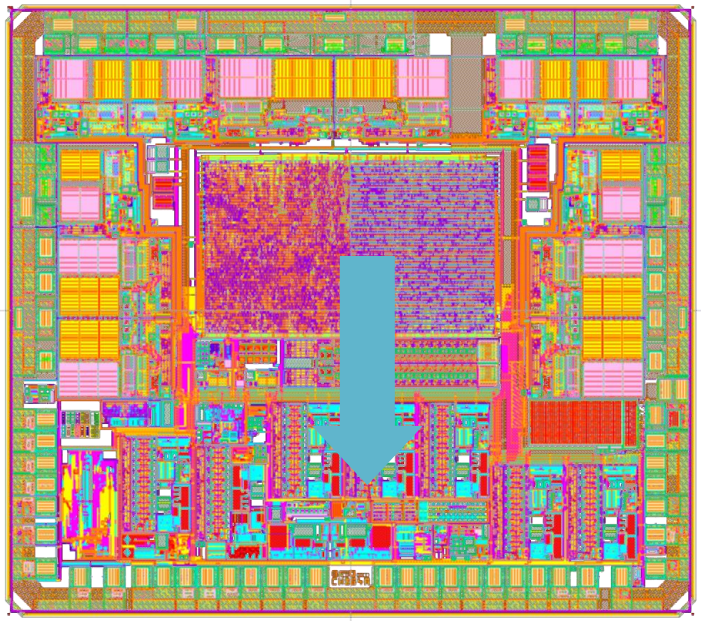
HVIC Block Diagram for Half-Bridge Driver



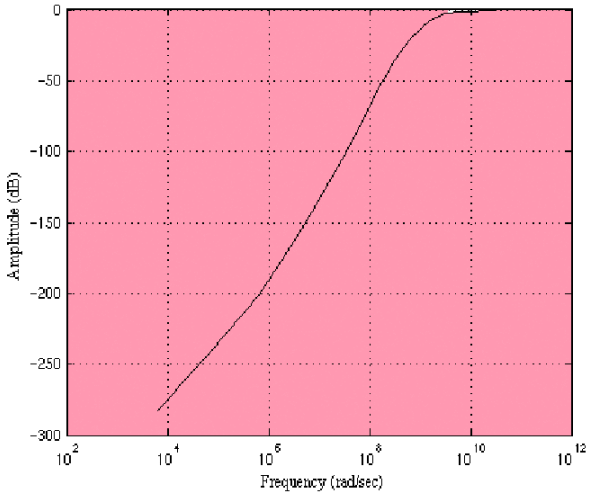
Junction Isolated CMOS HVIC Driver

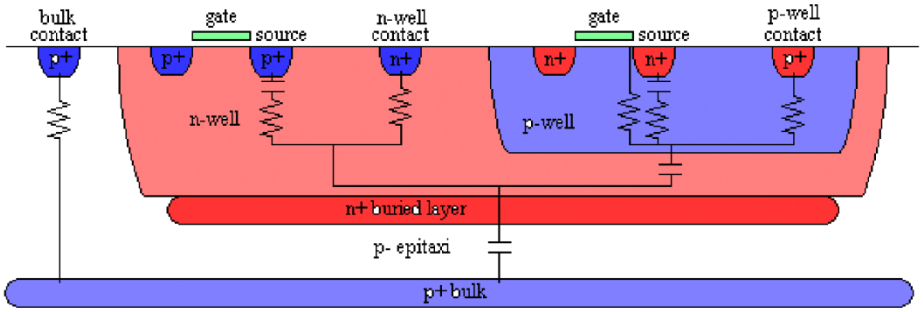


Substrate coupling

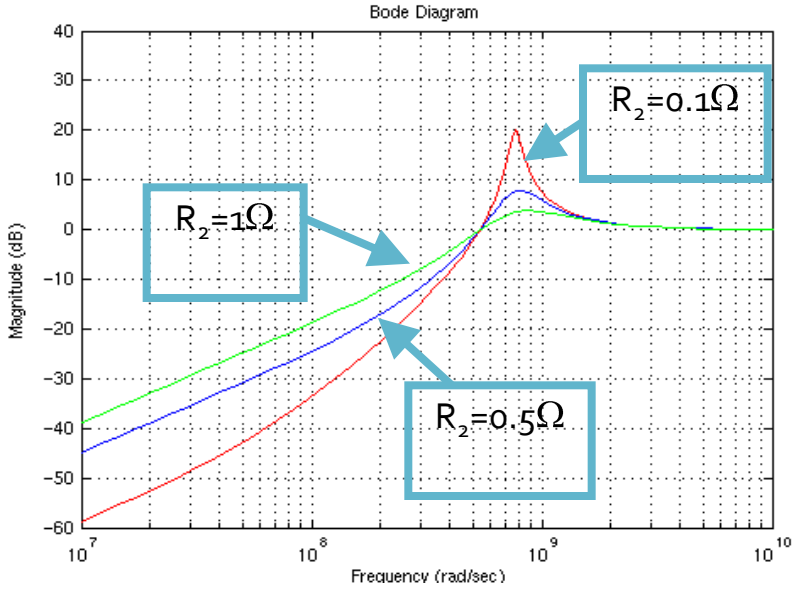


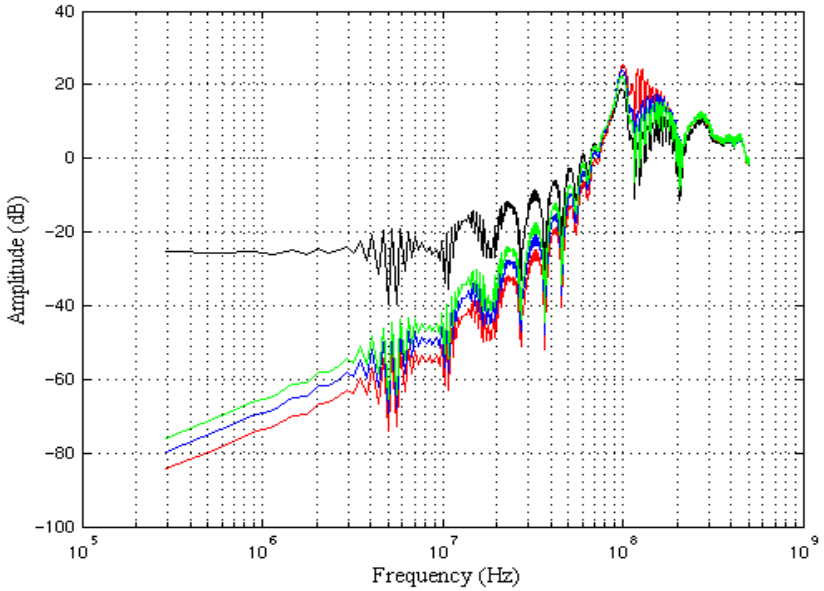
Transfer functions of the substrate coupling

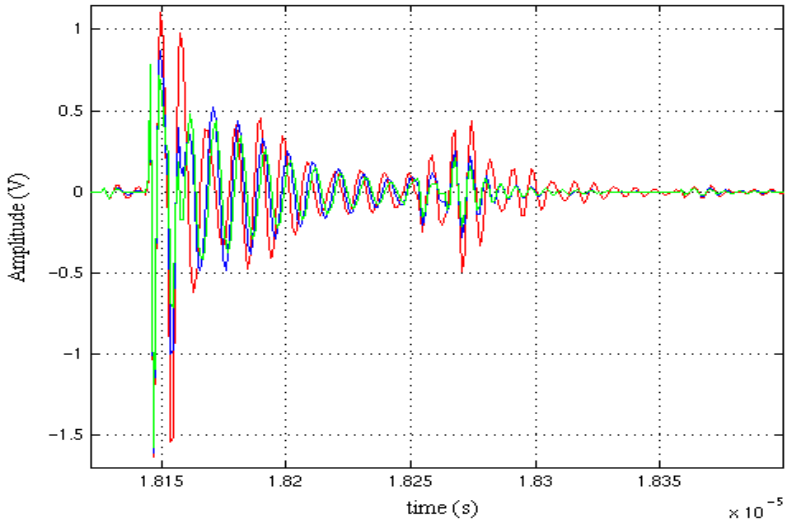


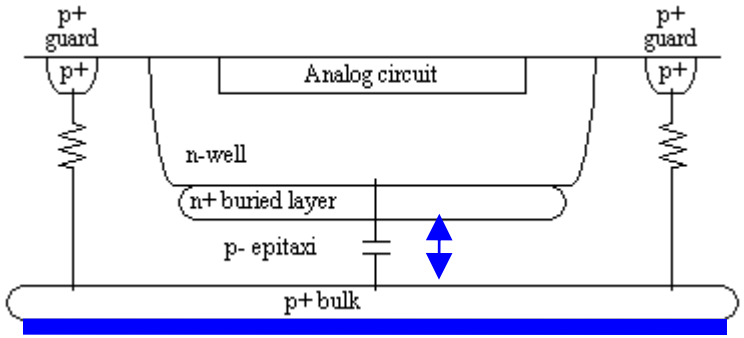


Substrate coupling









Conclusions

- Voltage Conversion topologies (LDO, Switched cap,SMPS)
- Power devices
- Design problems