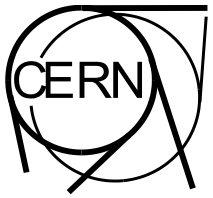


Comparing 130 and 90 nm process for FE designs intended for silicon strip detectors

Jan Kaplon

Outline

- General requirements for silicon strip detectors electronics
- Technology scaling and its consequences
- Improving the open loop gain of amplifier stages
  - Motivations
  - Methods
- Operating in weak inversion
  - Motivations
  - Costs
- Comparison between front end amplifiers designed for short strip (5 to 10pF detector capacitance) in 130 and 90nm process
  - Architecture
  - Performance
- Matching (provisional – low statistics from MPW runs)

General requirements for the Front-End tracker electronics for SLHC detectors

- Detector capacitance in the order of pico Farads
- Low power (<1mW/channel), low noise (S/N>15 → ENC < 1500e-)
  - optimization of power for a minimum affordable noise level → influence on the architecture (single ended)
- Collisions of particles every 25 ns → data time tagging to the given BCO (peaking times <25ns)
- Low input impedance → efficient charge collection and low cross talk signals
- Stability → required phase margin above 85 to 90 degree
- Optimum PSRR (large systems, difficult to provide clean power supply)
- Radiation hardness – doses >2 10^{14} N/cm^2 (1MeV) and >10MRad (CMOS front end preferred)

CMOS technology scaling

- Technology scaling ; formerly proportional reduction of all transistor features size (tox, L, W) scaled together with voltage supply and vt threshold voltage (constant field scaling). Smaller feature size → higher integration scale, lower power consumption/higher speed etc.
- Constant field scaling required proportional scaling of threshold voltage → this is limited by subthreshold slope of the MOS transistor (limit for minimum Vt >200mV)
- Scaling today ; constant voltage scaling introducing short channel effects
  - mobility reduction(vertical and longitudinal field)
  - degradation of output conductance (channel length modulation, Drain Induced Barrier Lowering (decreasing of Vt for higher Vds))

Comparison of basic analogue parameters for three generations of IBM CMOS processes

IBM CMOS	250nm RF	130nm RF	90nm LP (low power)
t_{ox} physical/effective	5nm/6.2nm	2.2nm/3.12nm	2.1nm/2.8nm
K_a $(C_{ox}\cdot\mu)$ NMOS	330 uA/V^2	720 uA/V^2	800 uA/V^2
Vdd	2.5V	1.2V (1.5V)	1.2V
g_m/g_{ds} Weak Inv.	70	30	18
Peak ft	35 GHz	94 GHz	105 GHz

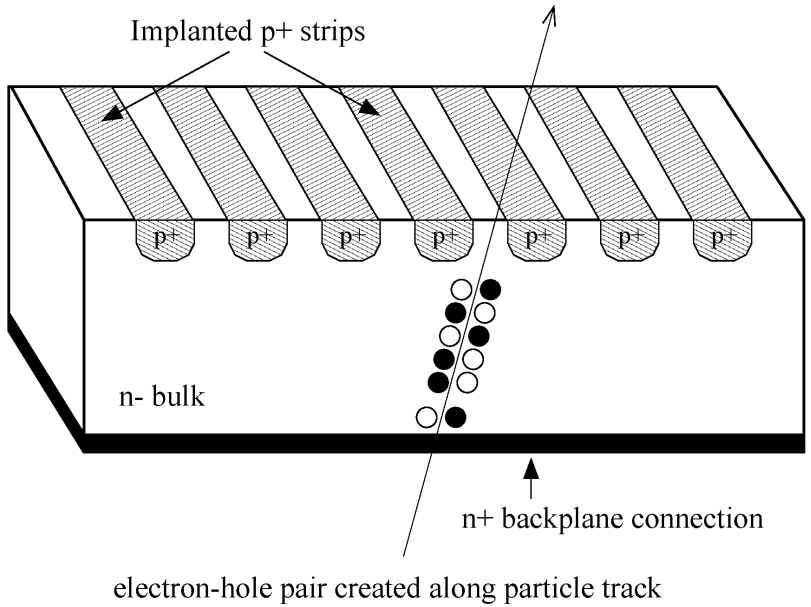
Scaling advantages; higher ft, higher Ka

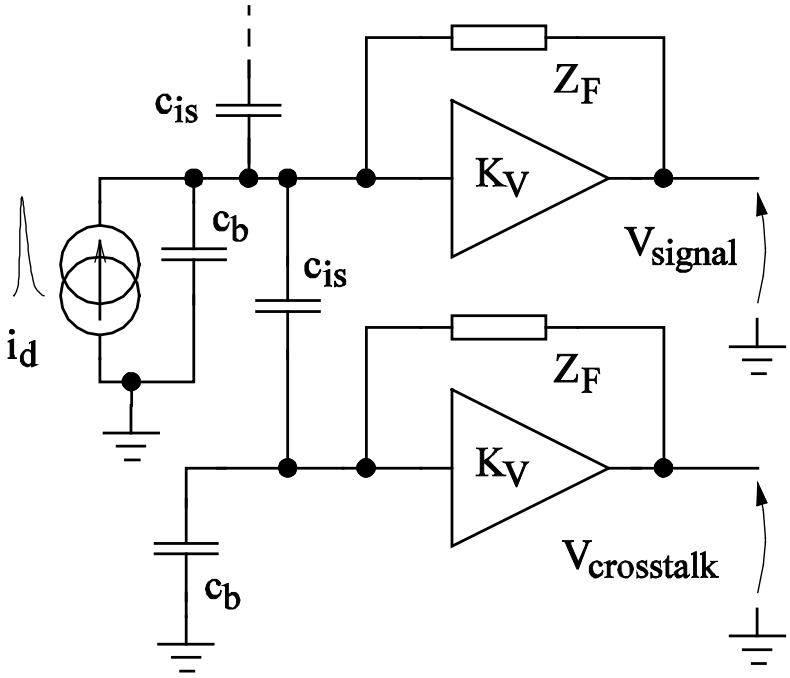
Challenges for front end; lower Vdd (lower dynamic range), lower intrinsic transistor gain

Motivations to increase open loop gain

- **Optimizing feedback impedance (i.e. pulse gain of the preamplifier) versus input impedance**
- **Lower input impedance of preamplifier;**
  - better charge collection efficiency
  - lower cross talk
- PSRR (all single ended stages)

Charge collection from silicon strip detectors, cross talk signals





$$Z_{IN}(s)=\frac{Z_F(s)}{K_V(s)}$$

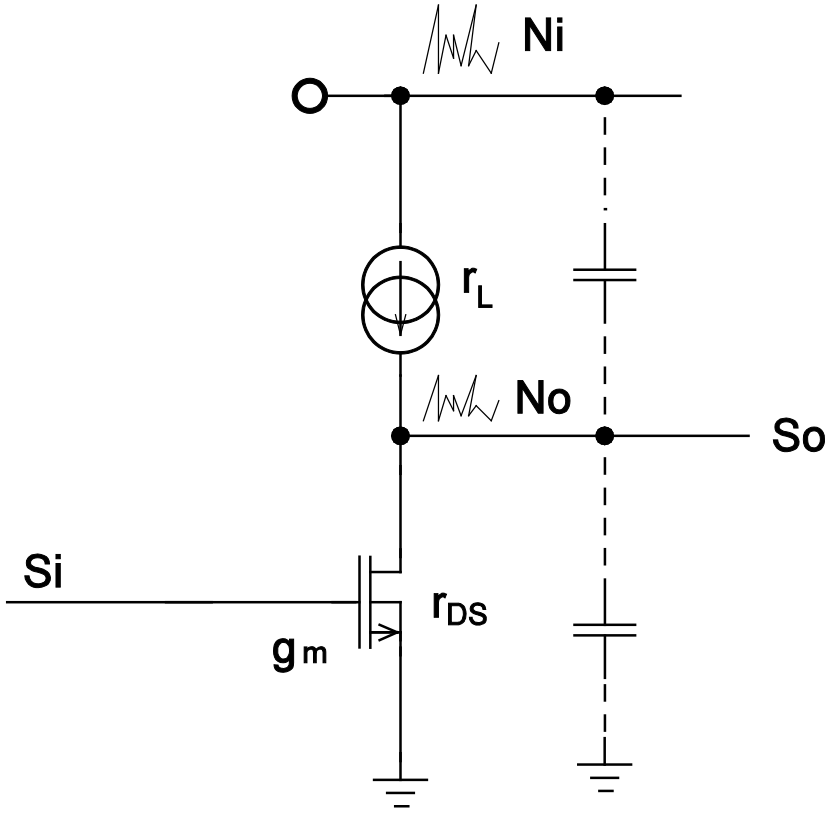
$$Cross\ Talk(s)=\frac{Z_{IN}(s)}{Z_{IN}(s)+Z_{IS}(s)}$$

Optimal open loop gain preamplifier designed for 5 to 20pF detector capacitance is around **70 to 80dB** (in order to provide cross talk less than 5%)

Motivations to increase open loop gain

- Optimizing feedback impedance (i.e. pulse gain of the preamplifier) versus input impedance
- Lower input impedance of preamplifier;
  - better charge collection efficiency
  - lower cross talk
- **PSRR (all single ended stages)**

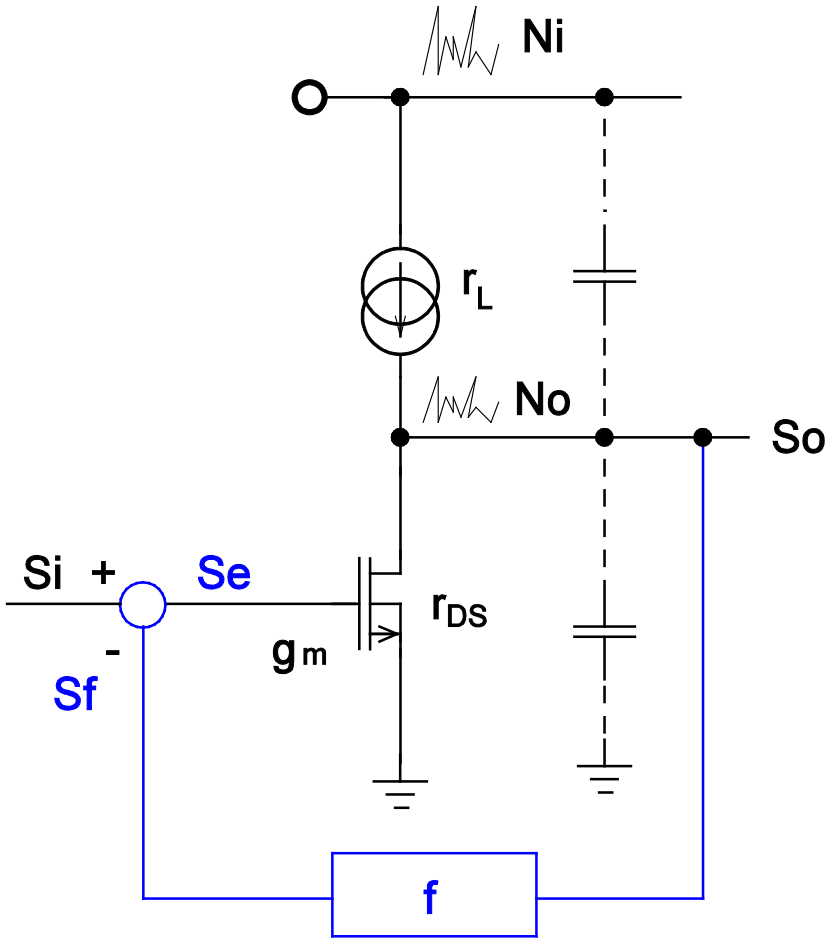
PSRR for single ended stage (1)



$$K_U = \frac{So}{Si} = g_m \cdot \left(r_L \parallel r_{DS} \right)$$

$$N_O = N_i \cdot \frac{Z_{DS}(s)}{Z_{DS}(s) + Z_L(s)}$$

PSRR for single ended stage (2)



$$S_O = K_U \cdot S_e + N_O$$

$$S_f = f \cdot S_O$$

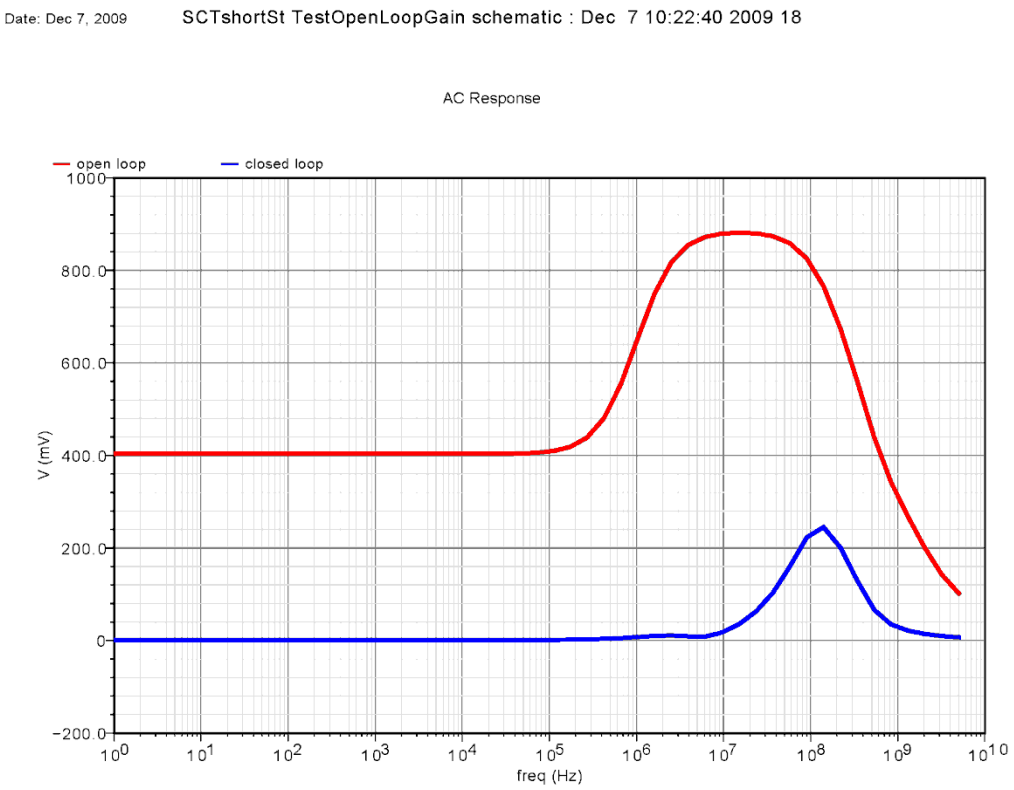
$$S_e = S_i - S_f$$

$$S_O = S_i \frac{K_U}{1 + K_U \cdot f} + N_O \frac{1}{1 + K_U \cdot f}$$

Loop gain

Driving K_U improves PSRR.
All single ended stages should be designed as feedback amplifiers with high open loop gain.

PSRR for single ended stage (3)

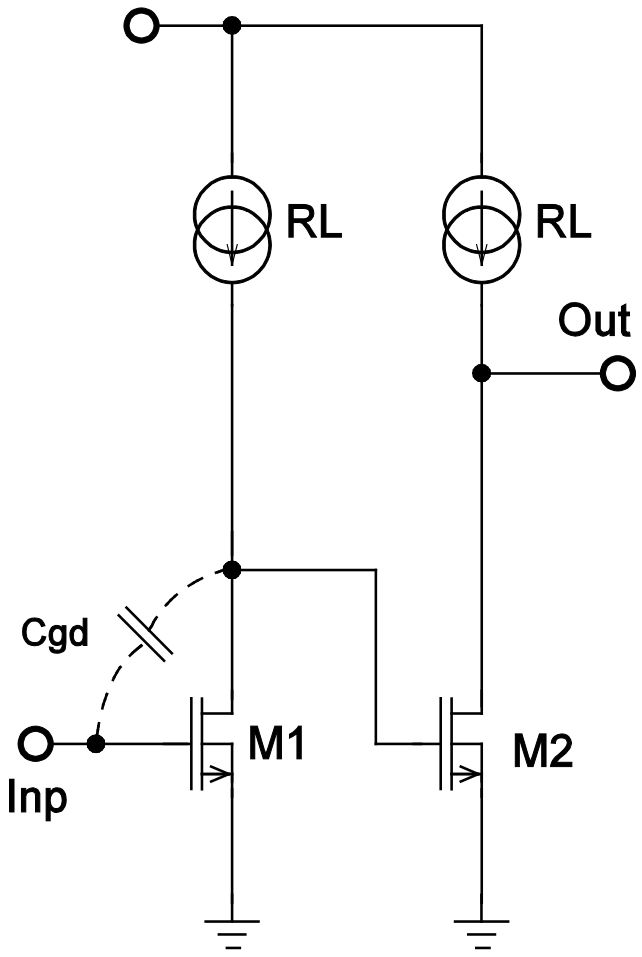


Power supply disturbance (1V) seen at cascode output working in open loop configuration (red) and in transimpedance preamplifier (blue). 130nm version of front end.

Basic configurations for gain boosting

Intrinsic gain in 130nm ~30 V/V → we need 70 to 80dB (2000 to 10000 V/V)…

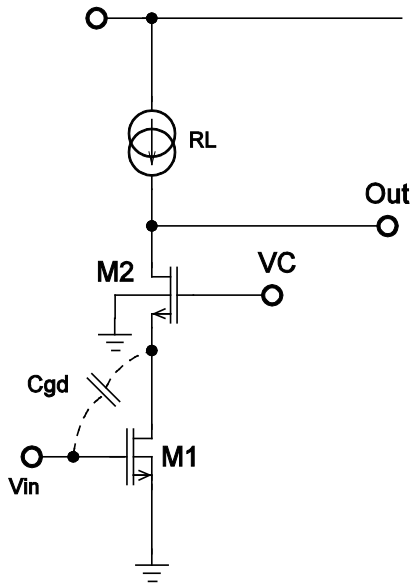
Cascade

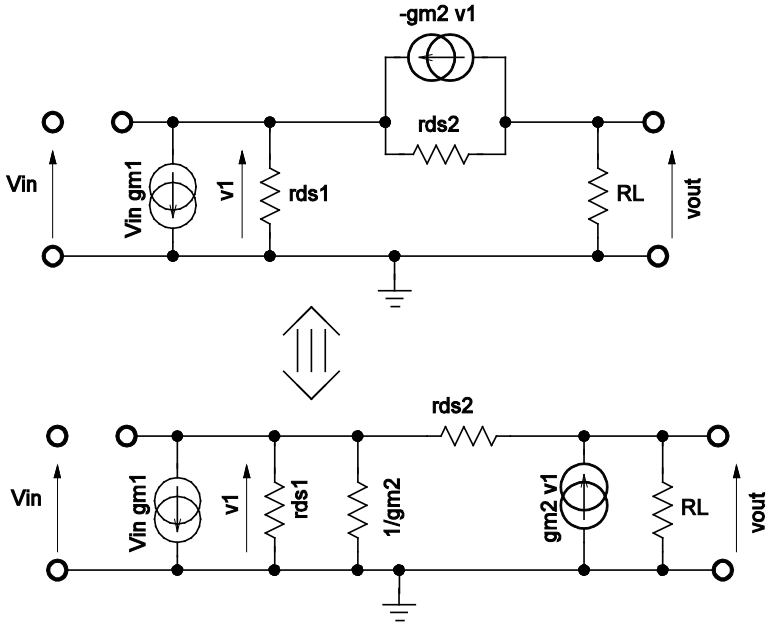


$$K_U = \frac{g_{m1}}{g_L + g_{DS1}} \cdot \frac{g_{m2}}{g_L + g_{DS2}}$$

- Two stage i.e. two pole circuit; needs to be stabilized
- Significant gain after first stage; Miller effect in case of driving from high impedance (as for silicon detector) → not used as an preamplifier stage
- PSRR defined by gain of first stage only
- In 90 nm the gain of cascade is significantly degraded because of intrinsic transistor gain, some circuits which works in 250nm version shows bad PSRR characteristic

Cascode; common source – common gate amplifier





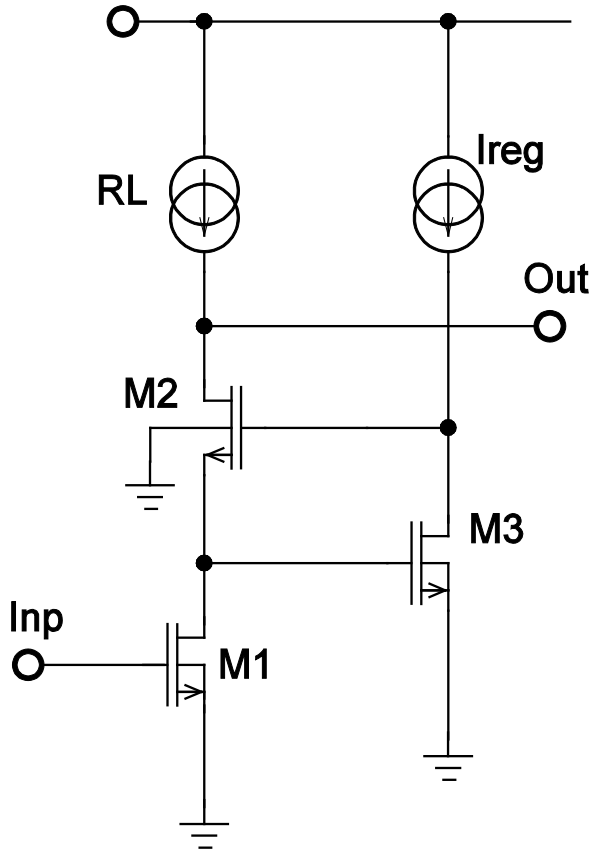
$$K_U = \frac{-g_{m1}}{g_{DS1}\dfrac{g_{DS2}+g_L}{g_{m2}+g_{DS2}}+g_L}$$

$$K_{U1} = \frac{-g_{m1}}{g_{m2}}\frac{g_{DS2}+g_L}{g_L}$$

$$GBW = \frac{g_{m1}}{2\pi\, C_{OUT}}$$

- single stage amplifier; one dominant pole
- good PSRR
- no Miller effect (low gain of common source stage)
- If cascode load R_L very high the overall gain K_U comparable with cascade

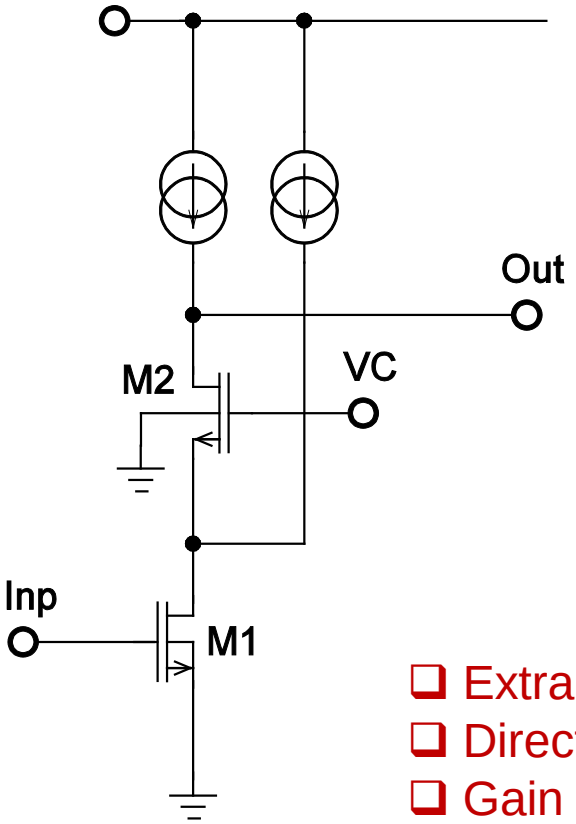
Regulated cascode



$$K_U \cong \frac{-g_{m1}}{\frac{g_{DS1} \cdot g_{DS2}}{g_{m2}} \cdot \frac{g_{DS3}}{g_{m3}} + g_L}$$

- Cascode transistor controlled with common source amplifier
- Higher output conductance of cascode; possible higher gain
- GBW the same as for simple cascode

Boosting bandwidth and gain in cascode

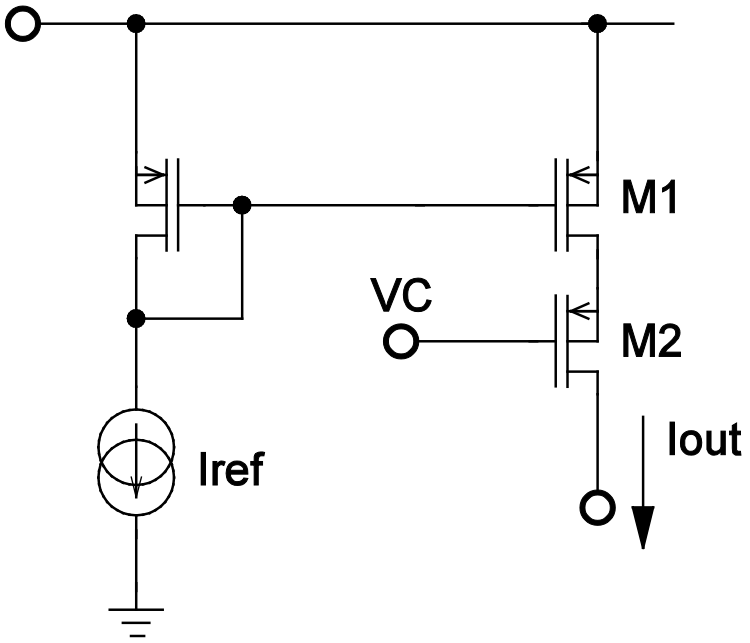


$$GBW = \frac{g_{m1}}{2\pi\, C_{OUT}}$$

$$K_U \cong \frac{-g_{m1}}{\frac{g_{DS1} \cdot g_{DS2}}{g_{m2}} + g_L}$$

- Extra current source to drain of M1 → increase of g_{m1}
- Direct impact on gain bandwidth
- Gain changed according to output conductance of cascode and active load

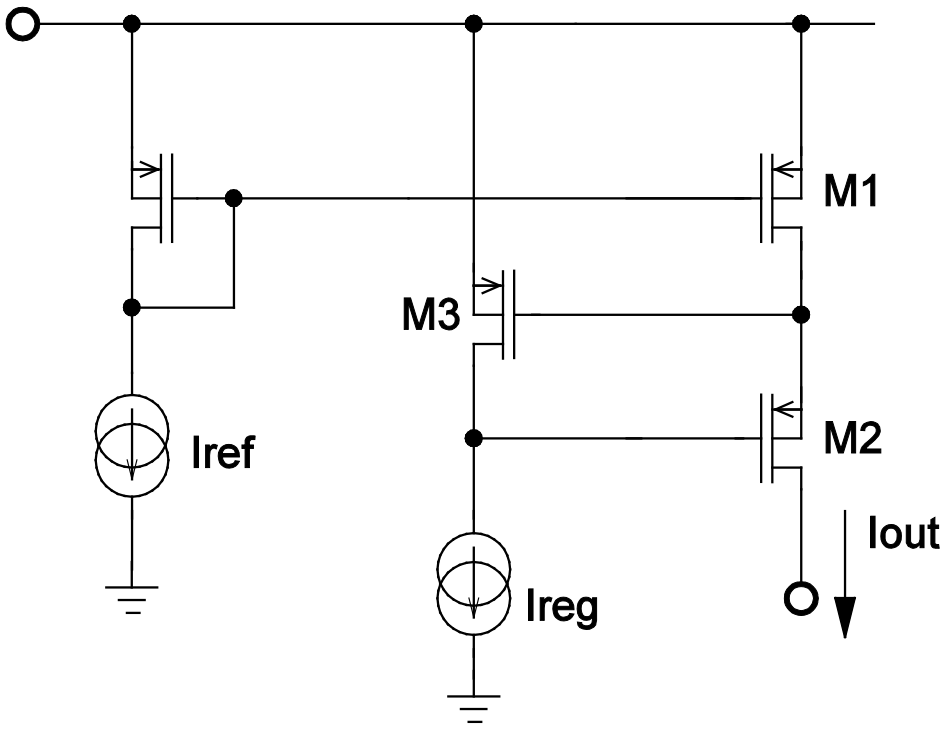
Active load for cascode stage (cascode load)



$$r_{OUT} \cong g_{m2} \cdot r_{DS2} \cdot r_{DS1}$$

- Amplification of r_{DS1} by g_{m2}
- For short SSD application; OK for 250nm, not sufficient for 130 & 90nm

Active load for cascode stage (regulated cascode load)

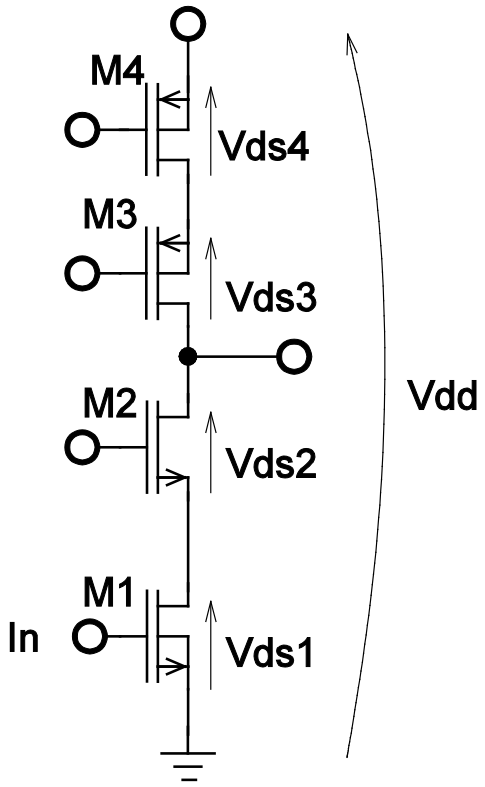


$$r_{OUT} \cong g_{m2} \cdot r_{DS2} \cdot g_{m3} \cdot r_{DS3} \cdot r_{DS1}$$

- Amplification of r_{DS1} by g_{m2} and g_{m3}
- Used in 130 & 90nm versions of preamplifiers

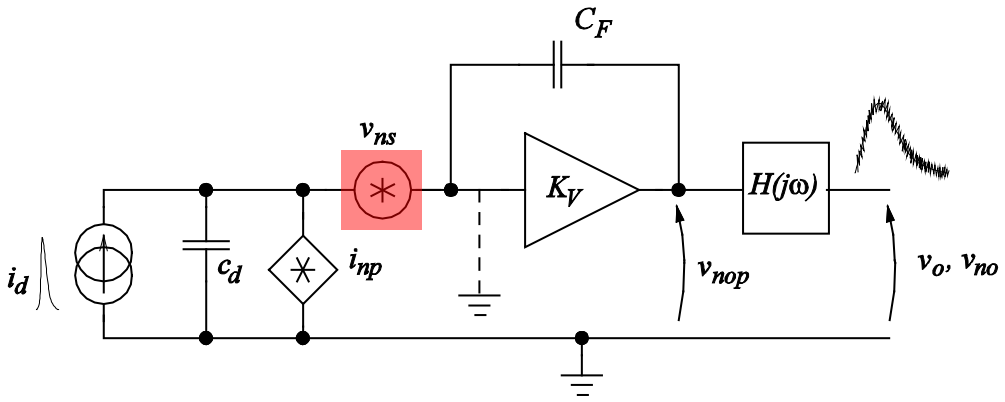
Biasing transistors in weak inversion; motivations

Biasing of the cascode



- ❑ All, four, transistors must be in the saturation ($V_{DS} \geq V_{GS} - V_T$)
- ❑ Technology scaling → Vdd diminished from 2.5V in 250nm to 1.2V in 130nm and 90nm CMOS → possible problems with dynamic range
- ❑ **Solution → subthreshold operation ($V_{GS} \approx V_T$)**
- ❑ Minimum $V_{DS\ SAT}$ for weak inversion roughly 5 U_T (125mV)

Noise optimization in CR-RC^n filters for multi-channel FE electronics



$$ENC[C] = F_V \cdot \frac{\overline{v_{ns}}}{\Delta f} \cdot c_d \Big/ \sqrt{t_{peak}} \oplus F_i \cdot \frac{\overline{i_{np}}}{\Delta f} \cdot \sqrt{t_{peak}}$$

$$\frac{\overline{v_{n\,thermal}}}{\Delta f} = \sqrt{\frac{4 \cdot k \cdot T \cdot n \cdot \gamma}{g_m}}$$

Transconductance in MOS transistor (EKV model)

Specific current

$$I_S = 2 \cdot n \cdot K_P \cdot \frac{W}{L} \cdot U_T^2 \qquad U_T = \frac{k \cdot T}{q}$$

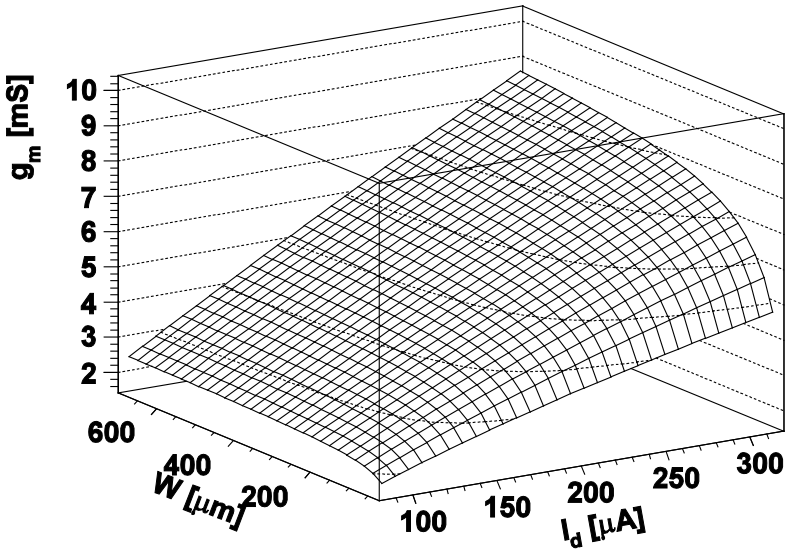
WI/SI interpolation for $I_f = I_D / I_S$

$$G(I_f) = \frac{1}{\sqrt{I_f + \frac{1}{2} \cdot \sqrt{I_f} + 1}}$$

Transconductance:

$$g_m = G(I_f) \cdot \frac{I_D}{n \cdot U_T}$$

g_m in weak inversion

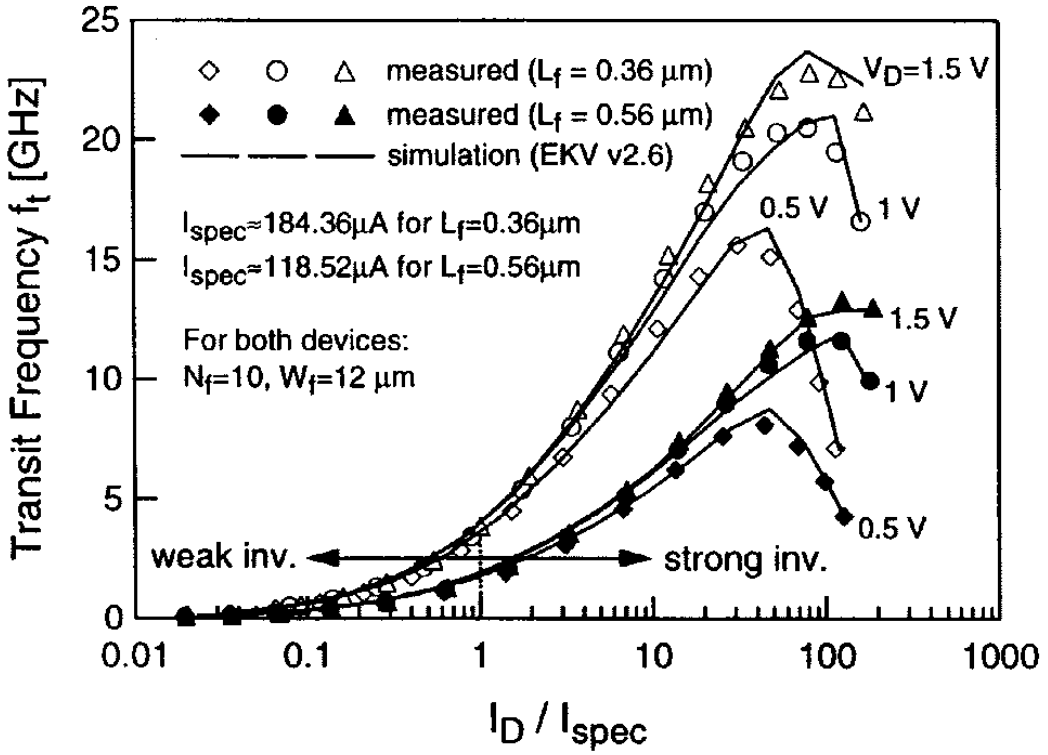


IBM 130nm
NMOS
L=300nm

- Weak inversion provides highest transconductance at a given bias current
- Some technologies report excess noise for devices in strong inversion
- **Conclusion; weak inversion in input transistor is good from the standpoint of power consumption/noise optimization**

Biasing transistors in weak inversion; some consequences

Impact of the inversion order on the speed of CMOS circuit

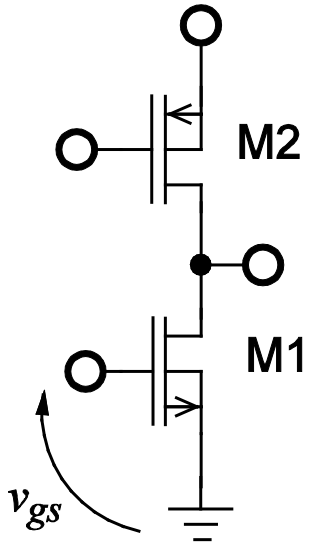


Transit frequency ft as a function of inversion order for 250nm CMOS technology *

For devices biased in weak inversion we never obtain highest possible speed of a given technology

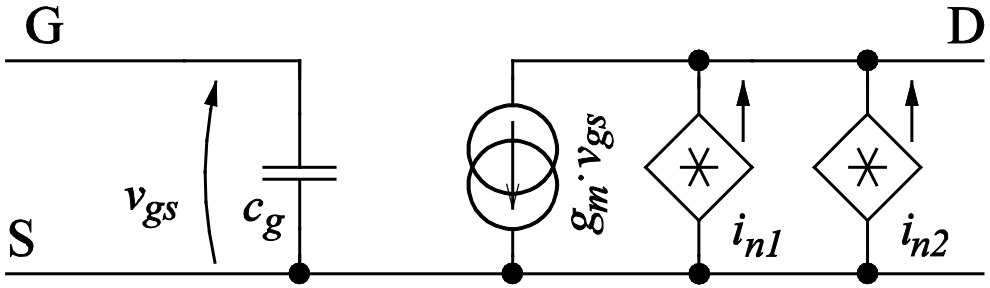
* C.Enz, "MOS transistor modeling for RF IC design", *IEEE J.Solid-State Circ.,* vol. 35, no. 2, pp.186-201)

Noise of the active load (1)



for weak inversion gm1=gm2

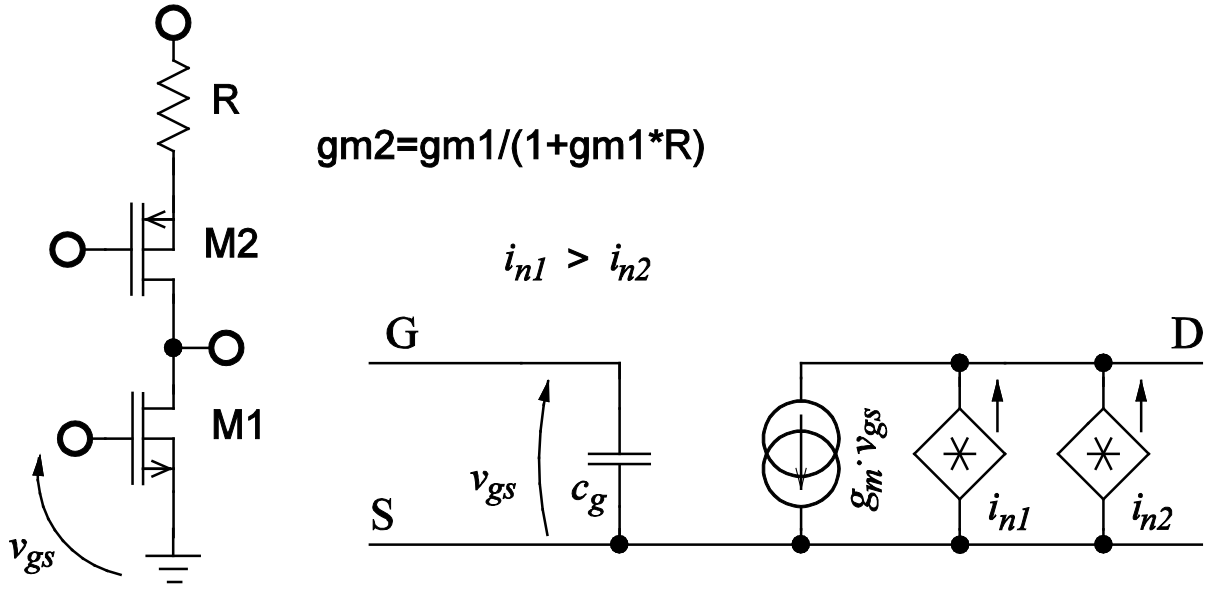
$i_{n1} = i_{n2}$



If all transistor in weak inversion the gm is defined only by current → all gm the same

Increase of input series noise by ~40%!

Noise of the active load (2)

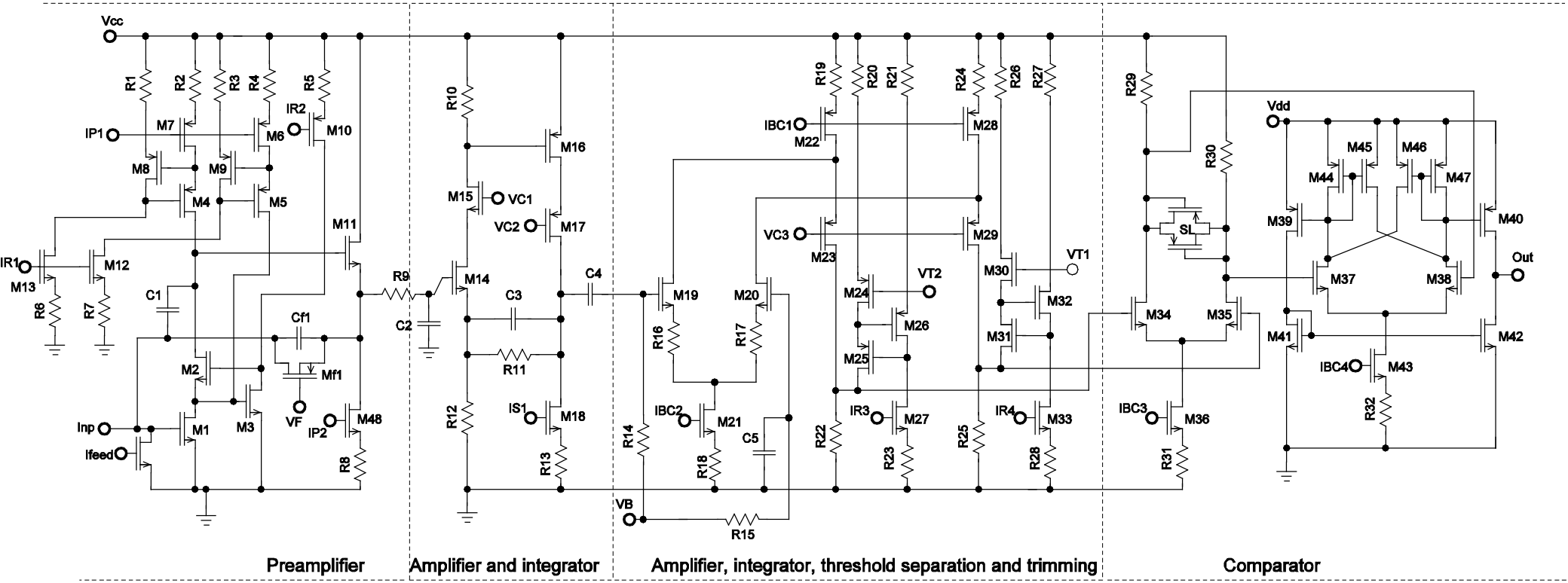


Resistive degeneration of gm works

But we have to spend another ~100mV taken out from Vdd…

Architecture of front ends implemented in 130 & 90nm processes

Front end channel in 130nm & 90nm technology (SCT short strips)

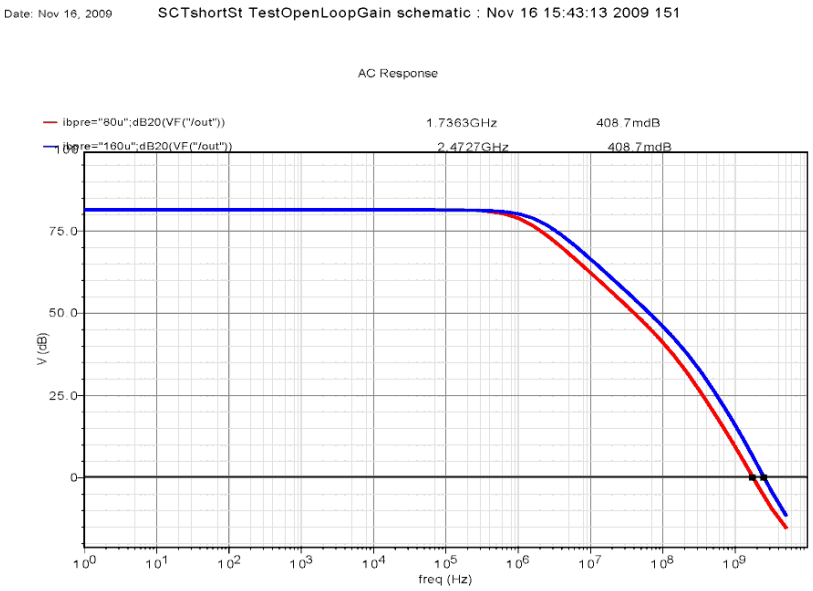


5.5 mV/fC
tp 8 ns

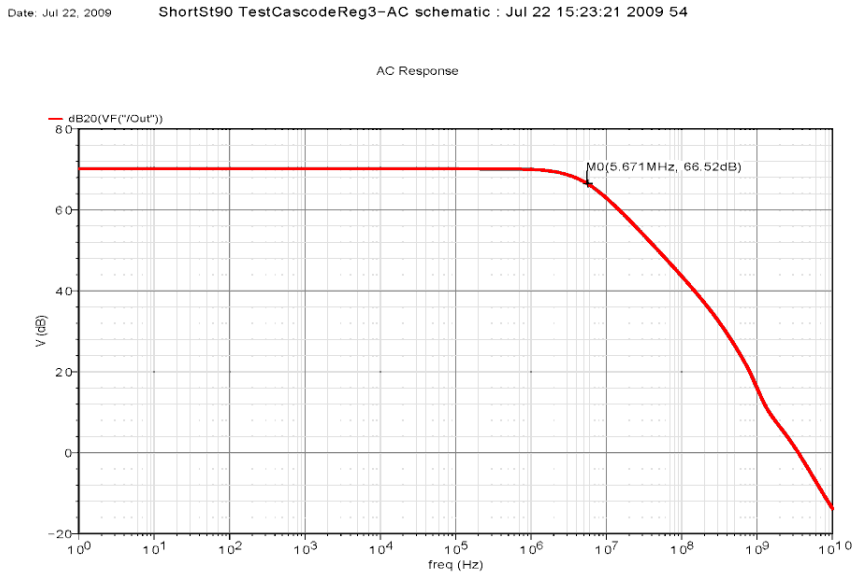
30 mV/fC
tp 18 ns

100 mV/fC
tp 22 ns

Preamplifiers open loop gain

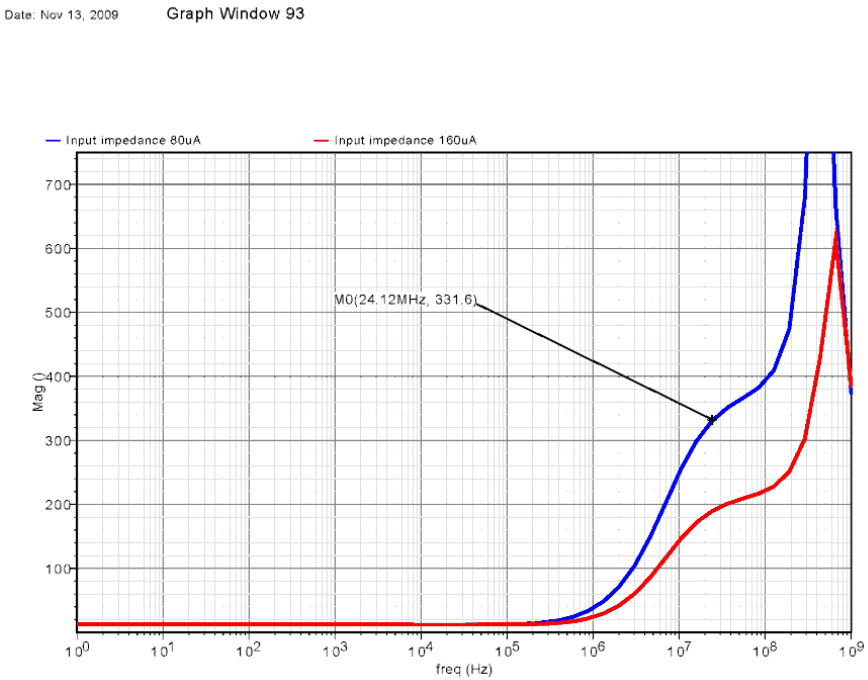


130nm, 80dB, GBW=2GHz
Iin=80uA

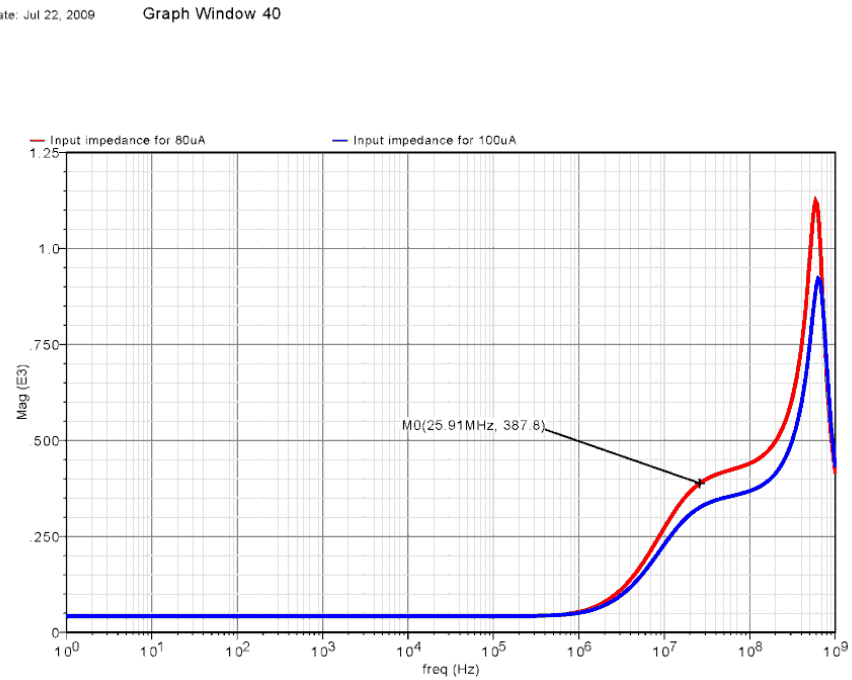


90nm, 70dB, GBW=3.5GHz
Iin=80uA

Preamplifiers input impedances



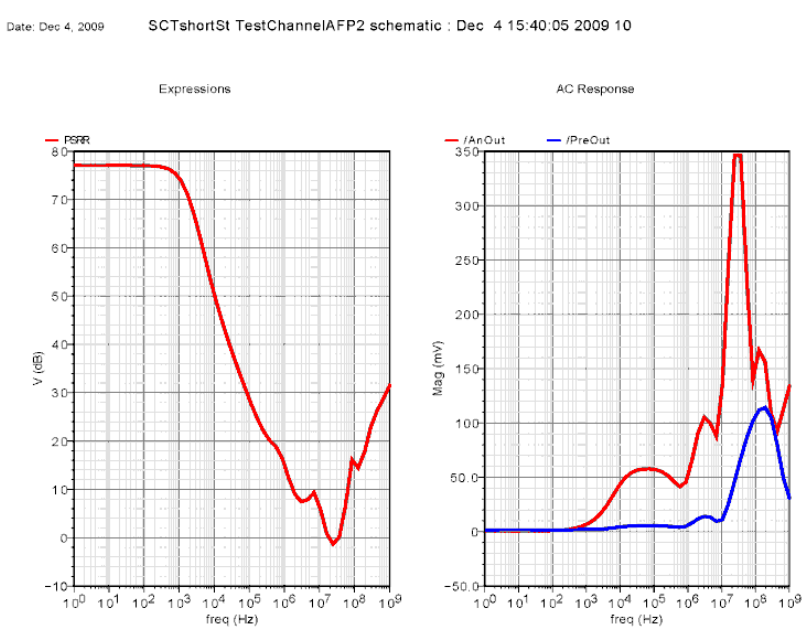
130nm, 330Ω @25MHz
Iin=80uA



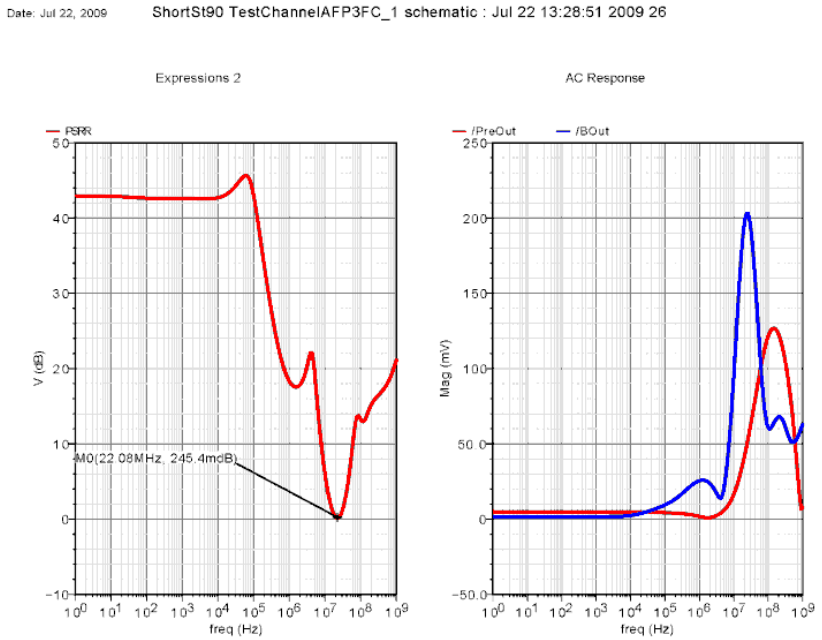
90nm, 380Ω @25MHz
Iin=80uA

In both cases the cross talk signals less than 3%
Detector 1.5 pF to bulk + 2x 1.6 pF to neighbor

PSRR *



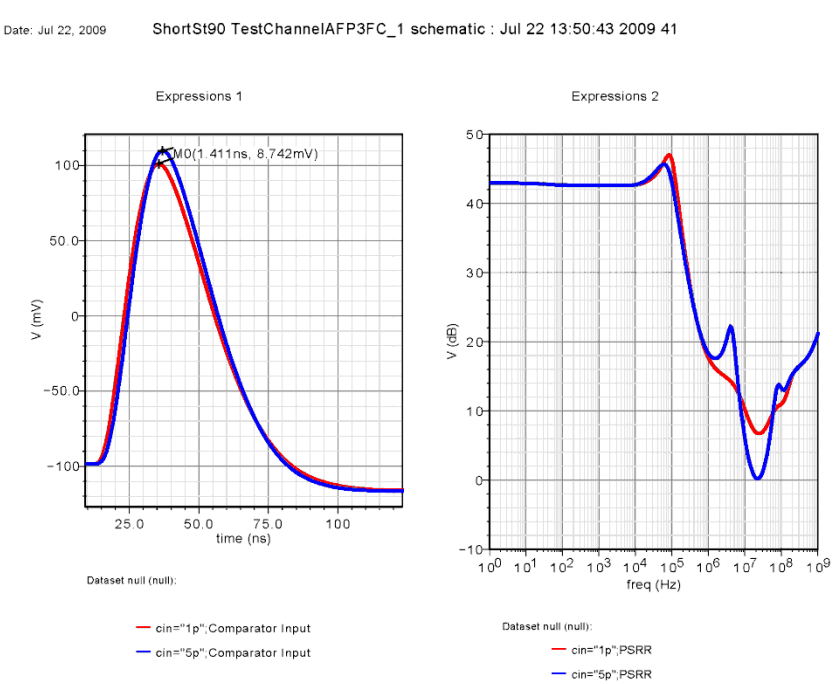
130nm, -0.5dB @ 25MHz
Iin=80uA, Cin=5pF to GND

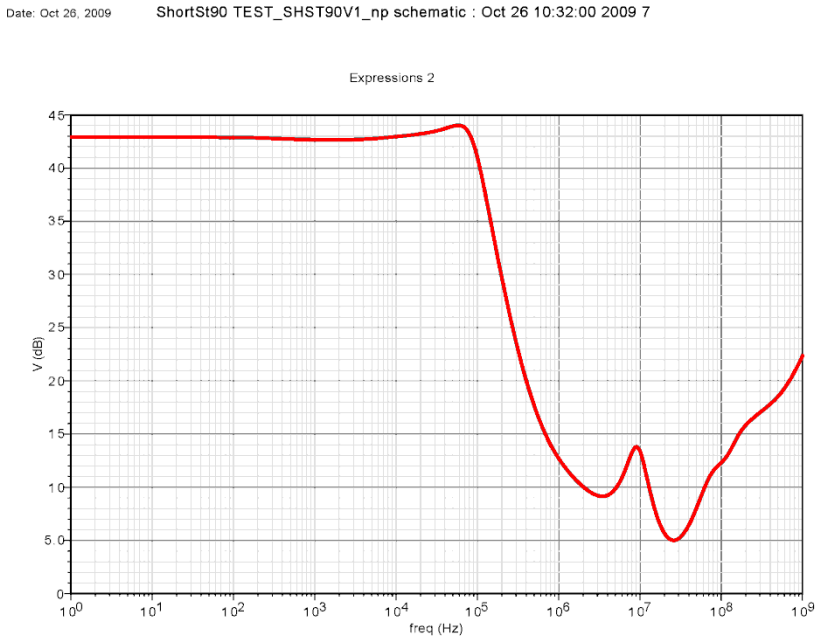


90nm, +0.5dB @ 25MHz
Iin=80uA, Cin=5pF to GND

* PSRR defined as the ratio of the 1V signal at the power supply line to the signal at the output. For two different front end one should also look at the charge gain!

PSRR (2)

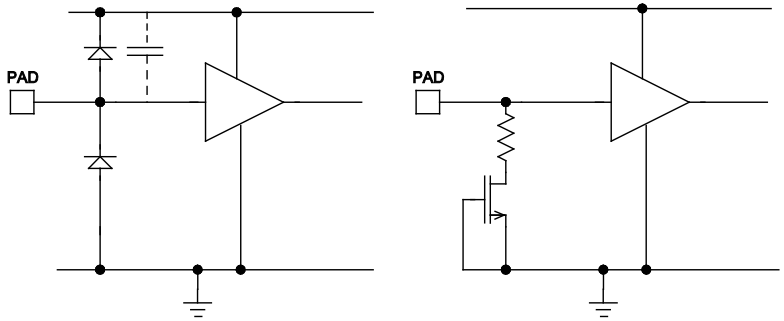


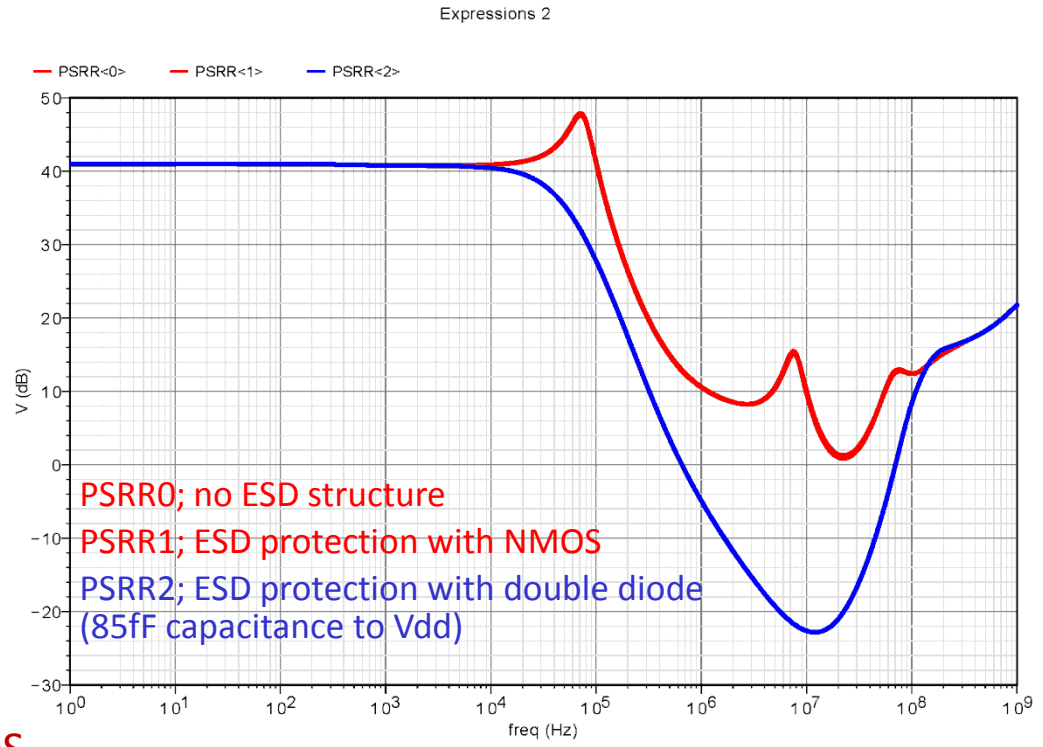


PSRR improves when:

- Cin decreases (also in case of real detector when part of the detector capacitance is connected to neighboring channel)
- Bias current increases (GBW increases → loop gain increases)

PSRR (3)

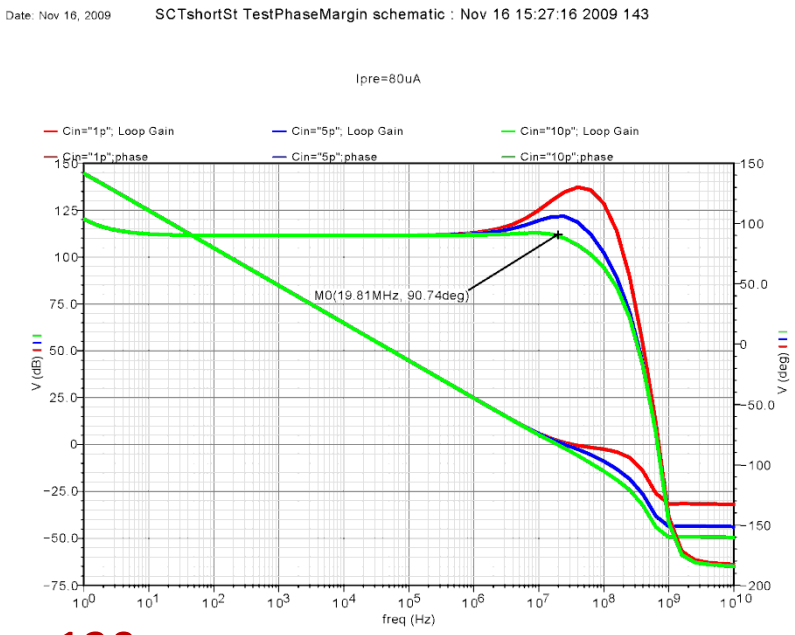




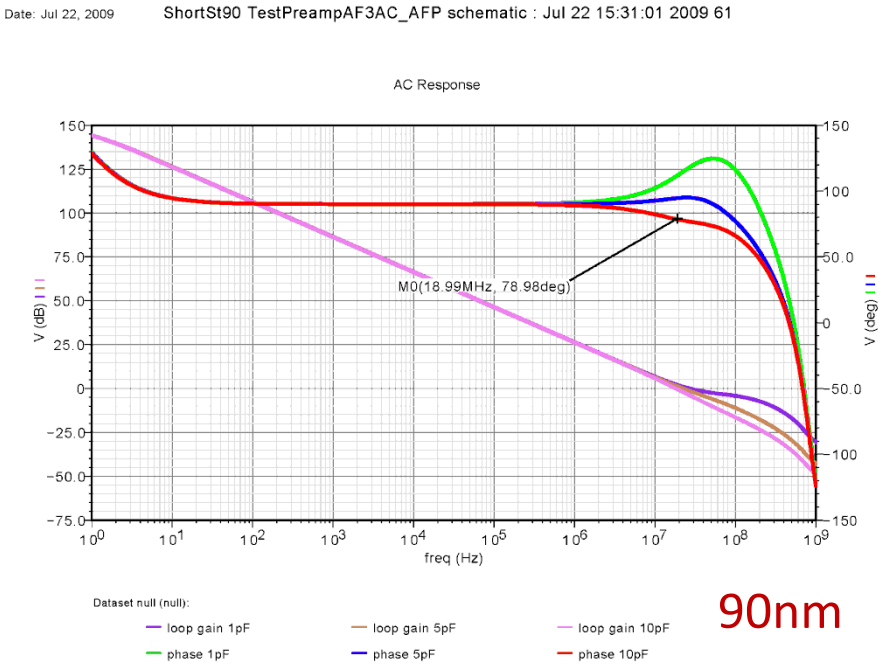
PSRR might be broken by input protections:

- ❑ double diode structure not admitted
- ❑ preferable structure; silicide blocked NMOS
  - ❑ drawback → higher capacitance

Phase margin



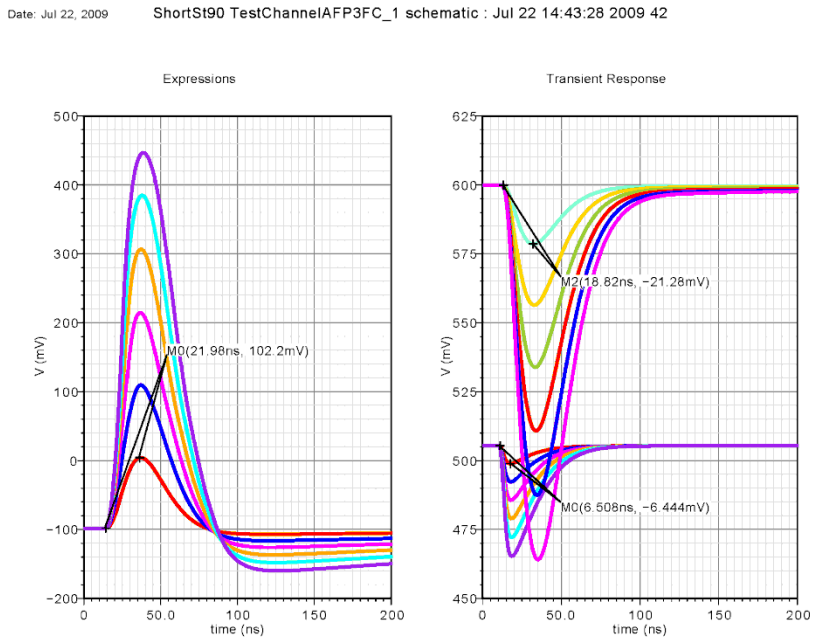
130nm

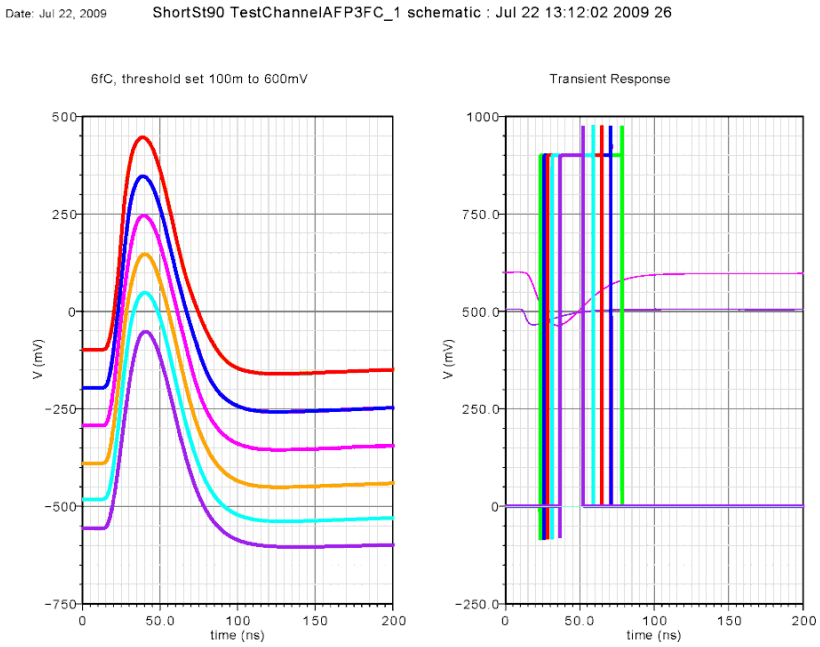


90nm

We want to have 90 degree for nominal input capacitance (5pF), this has impact on input impedance and PSRR but safety first.

Linearity and dynamic range



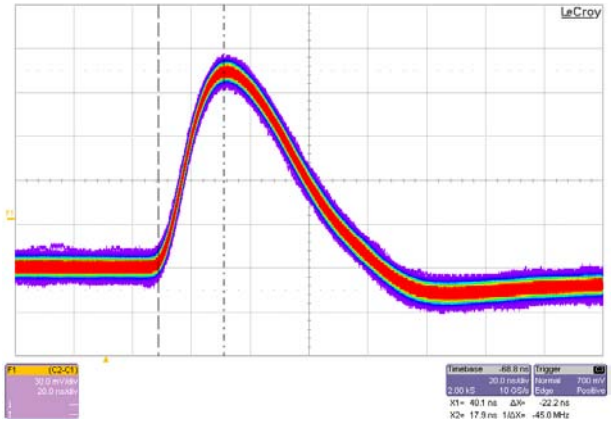


In 130nm and 90nm versions dynamic range up to 6 fC (good linearity up to 4fC)
Same 1.2V Vdd *)

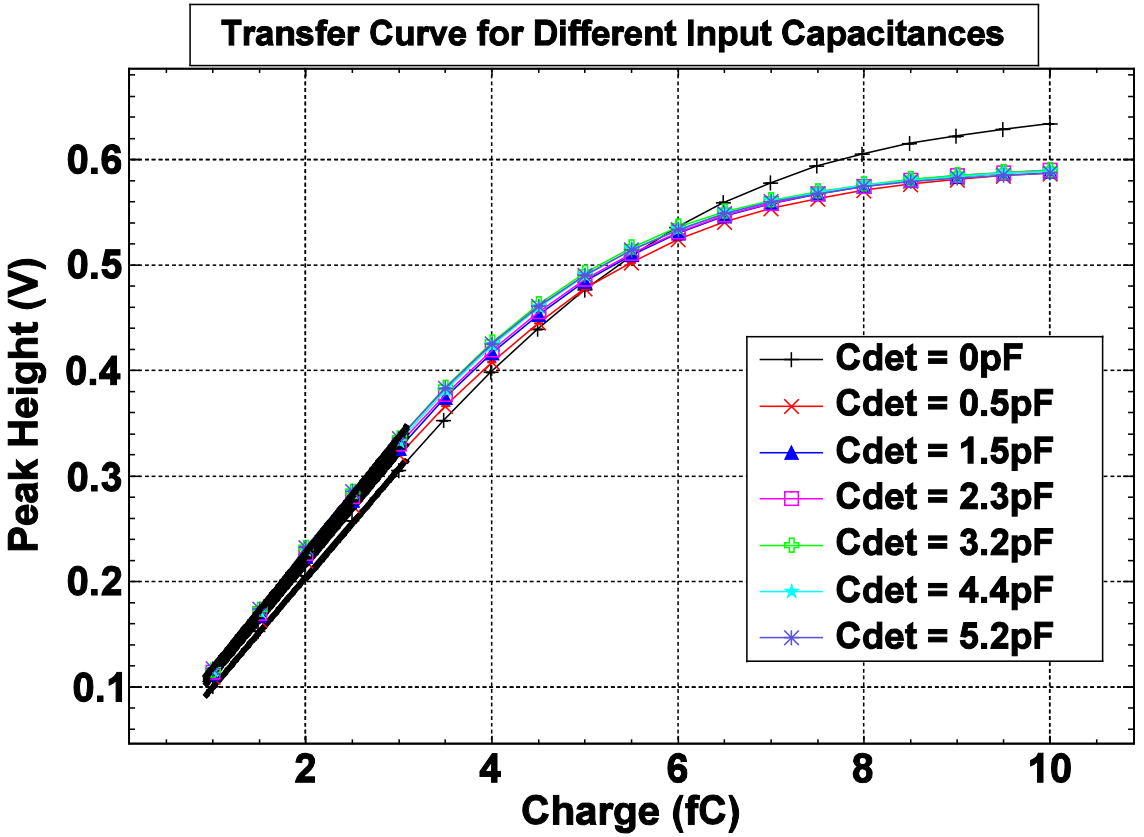
*) in 250nm version the dynamic range (limit in discriminator stage - might be adjusted) is about 12fC

Results from 90nm front end (130nm version of Front End for short strips (ATLAS SCT upgrade) back in the end of 2010)

Dynamic range and linearity (90nm)

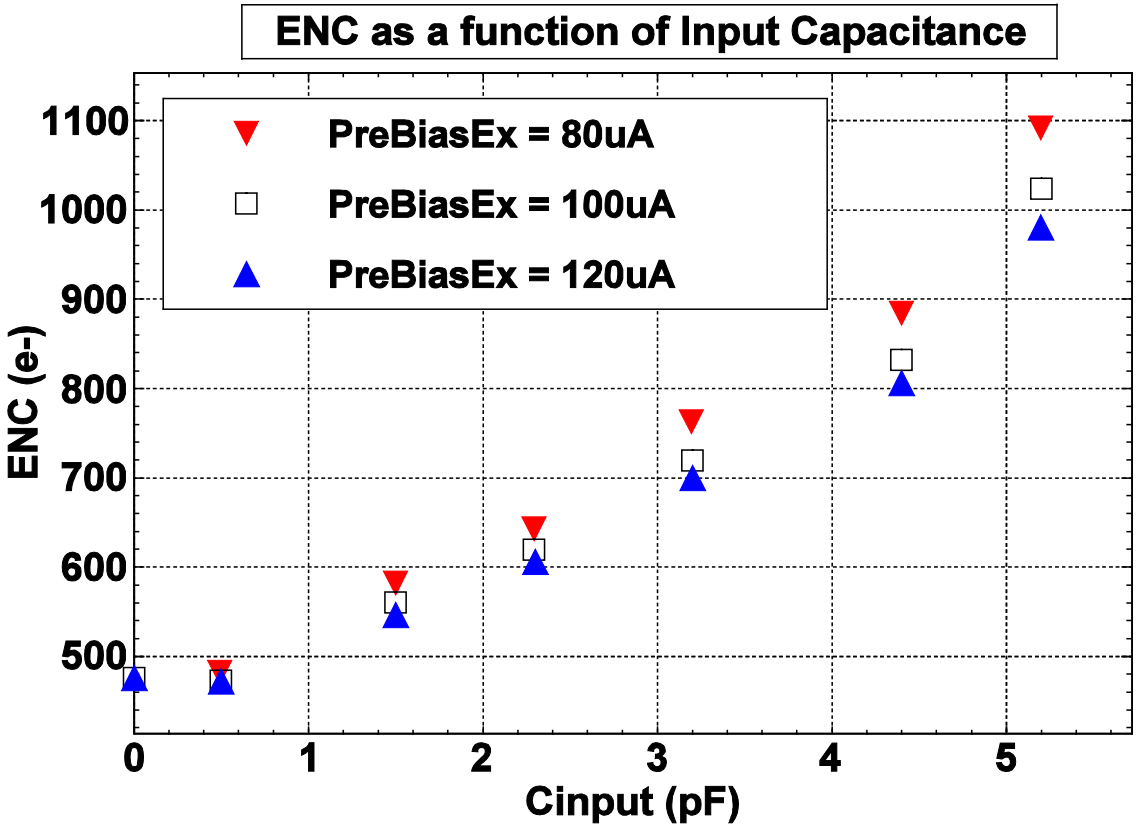


Peaking time 22ns
Gain 100mV/fC



Good linearity up to 4fC (400mV signal range)
Dynamic range up to 6fC (limit set by the bias of the differential stage).
Good agreement with simulation → the same estimates for 130nm version

Noise performance (90nm)



ENC at 0 input capacitance as simulated (470e-)
ENC at 5pF roughly 10% higher than simulated.
Estimates for 130nm version the same → data will be available next year

Comparison of power consumption at constant ENC for Cdet=5pF and ENC = 800e-

	250nm	130nm	90nm
I_{input}	140uA*	100uA (*?)	100uA (*120uA)
I_{total}	280uA*	180uA (*?)	180uA (*200uA)
Vdd	2.5V (2.2V)	1.2V	1.2V

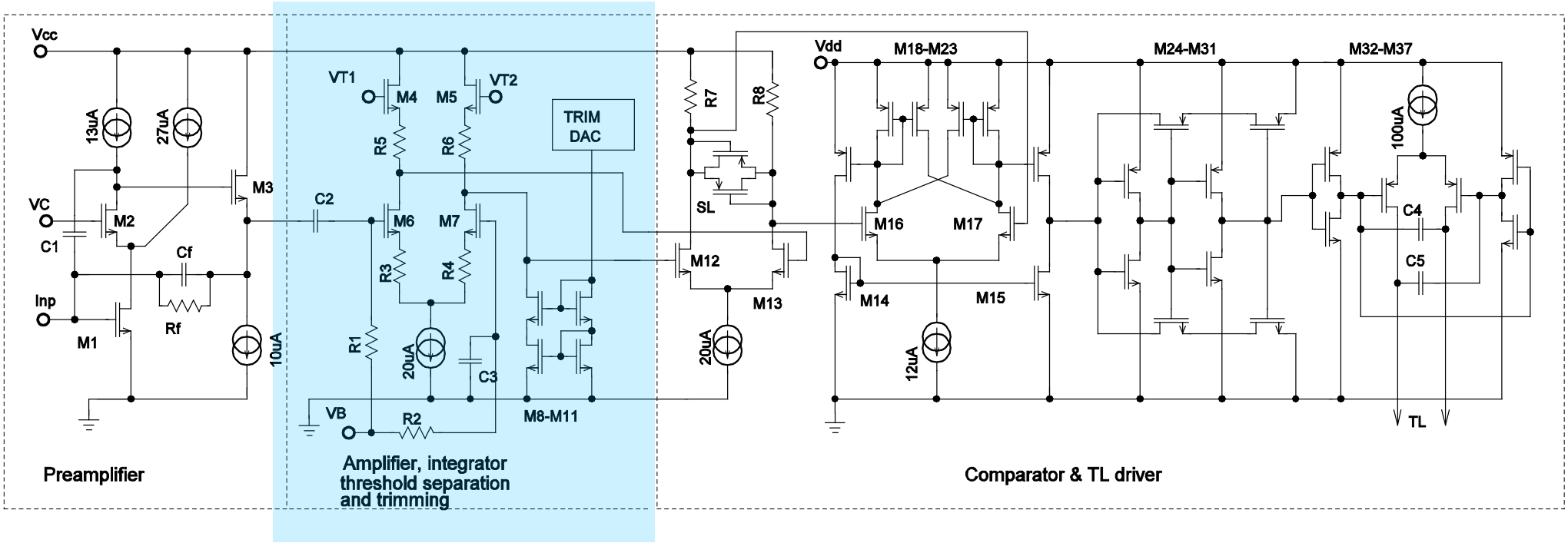
* measured

First look at matching in 130 and 90nm IBM processes

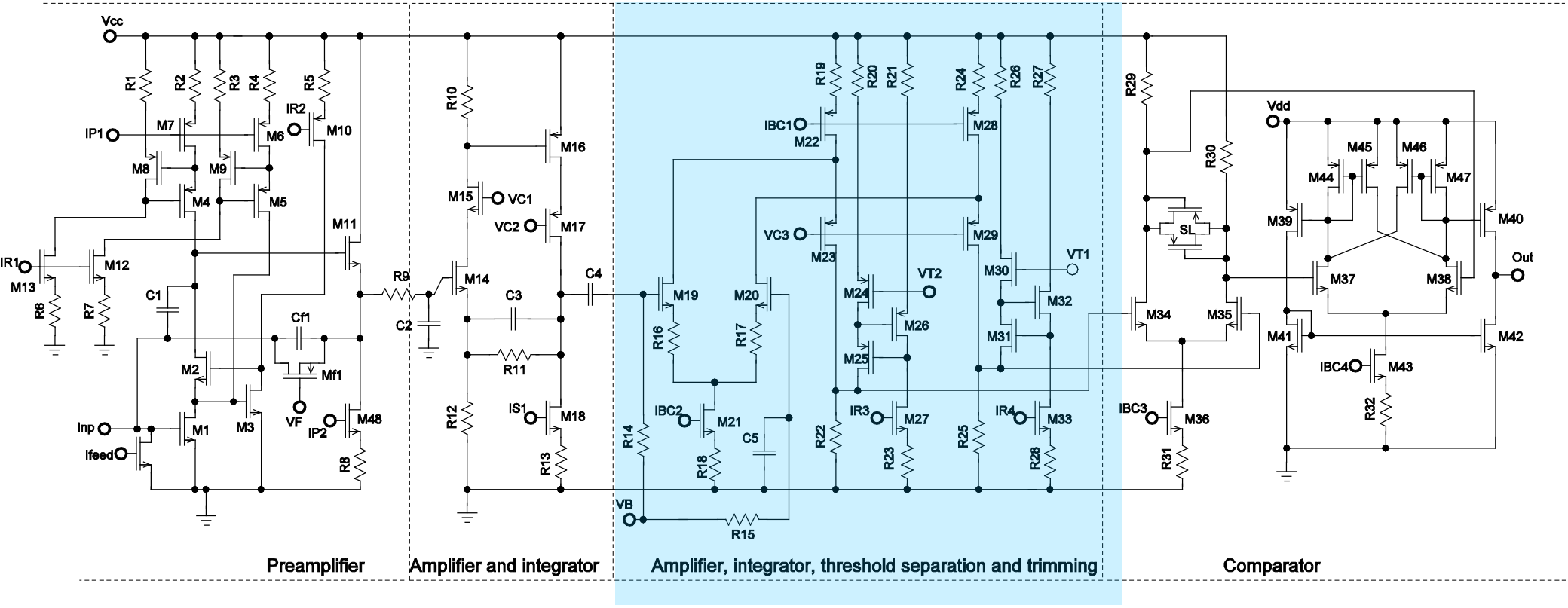
- Detailed study of matching issues requires high statistics (engineering runs with high number of samples)
- In our circumstances we limit statistic to some number of multichannel chips submitted to one or two MPW
- Data for matching in 130nm available at the moment from GTK front end chip (130nm front end for short strips back from foundry at the end of 2010)
- One should stress that our architecture is sometimes sensitive to matching.
  - we rely on matching of devices placed over the whole chip area
  - for the presented designs generation of filling structures have been done by IBM.

Matching data for 130nm process; GTK Front End

- Front end for silicon pixel 300x300um (250fF detector capacitance)
  - Transimpedance preamplifier/shaper 5ns peaking time / ENC 180e-
  - Comparator working in voltage mode



Comparator for short strips (130 & 90nm)



Matching, comparison between MC and measurements

	Gain [mV/fC] Measured/Simulated	RMS Gain [mV/fC] Measured/MC	RMS Offset [mV] Measured/MC
130nm FE GTK	**72 ←→ 70**	**1.5 ←→ 1.5**	**11 ←→ 6**
90nm FE short SSD	**97 ←→ 100**	**6 ←→ 2**	**11 ←→3**

- Architecture of 90nm comparator more sensitive to matching but final numbers for 90 and 130nm chips practically the same → is 90 nm process intrinsically better?
- Discrepancy between MC and data → MC models are too optimistic or problems are related to non optimum layout?
- High mismatch for 90nm FE gains under investigation (non Gaussian distribution → pk-pk <18mV/fC.

Conclusion

- Practically the same estimates for noise/power performance of 130nm and 90 nm processes
- Some improvements in AC characteristics due to higher bandwidth in 90nm process (better PSRR). 90nm shows higher bandwidth but lower gain than 130nm. This has slight impact on differences between input impedance and phase margin.
- The same dynamic range (related to gain and Vdd) in 90nm and 130nm. The 6fC range with gain of 100mV/fC is sufficient for tracking applications.
- Visible discrepancies between simulated and measured comparator matching both in 130nm and 90nm processes → this issue has to be investigated.