



Swiss CTA Day 2020

The Swiss Landscape Detector Technology developments

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EPFL

Swiss Cherenkov Telescope Array Day 2020

aqua**lab**

Outline

- Introduction to [aqualab](#)
- SPADs, SiPMs
- An image sensor for FLARE
- 3D integration
- Conclusions

Some Acronyms:

CTA: Cherenkov Telescope Array

CTAO: CTA Observatory

LST: Large Size Telescope

DiPC: Digital Photon Counter

FACT: Fast G-APD Cherenkov Telescope

IACT: Imaging Atmospheric Cherenkov Telescope

The Advanced Quantum Architecture ([aqualab](#))

EPFL Microcity Neuchâtel



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EPFL Neuchâtel

The Canton of Neuchâtel is hosting an important part of EPFL's Microengineering Institute (IMT). It is the biggest academic institute in Switzerland, with research activities covering topics such as health, microsystems, photovoltaic or watchmaking.

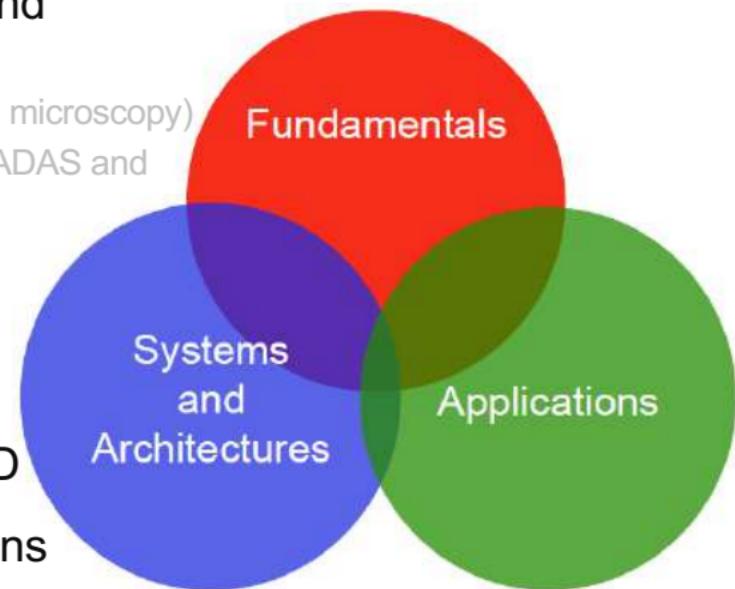


The people of aqualab

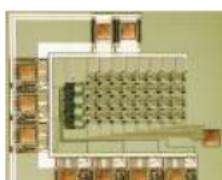


aqualab activities

- Quantum imaging (single-photon generation and detection)
 - Biosensors (PET, FLIM, FRET, NIRI, NIROT, super-resolution microscopy)
 - Automotive sensors (long distance, high speed telemetry for ADAS and autonomous driving)
 - Time-to-digital converters in ASIC and FPGA
 - Space sensors (guidance and docking in space)
- Ultra-fast imaging (1Gfps camera)
- Quantum random number generators and QKD
- Cryo-CMOS for quantum computing applications
 - analog and digital circuits at 4K and below



Some aqualab designs (2004-2020)



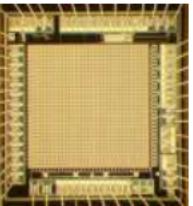
ISSCC 2004



ISSCC 2007 bts



IISW 2011



ISSCC 2005



ISSCC 2009



ISSCC 2013



SPIE 2006



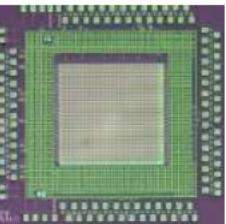
JSTQE 2019



Sensors 2018



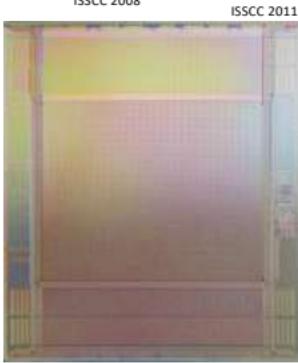
ISSCC 2007



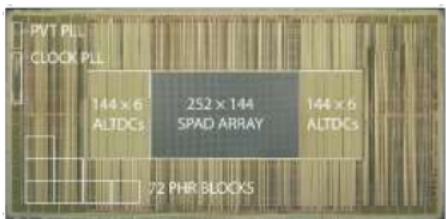
ESSCIRC 2009



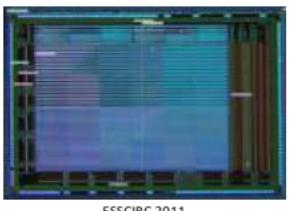
ISSCC 2015



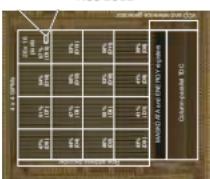
IISW 2013



VLSI 2018 / JSSC 2018



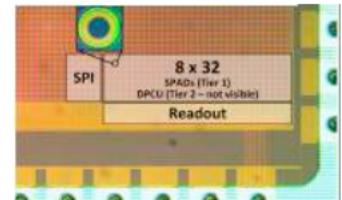
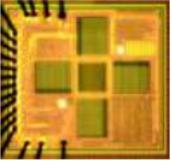
ESSCIRC 2011



NSS 2012



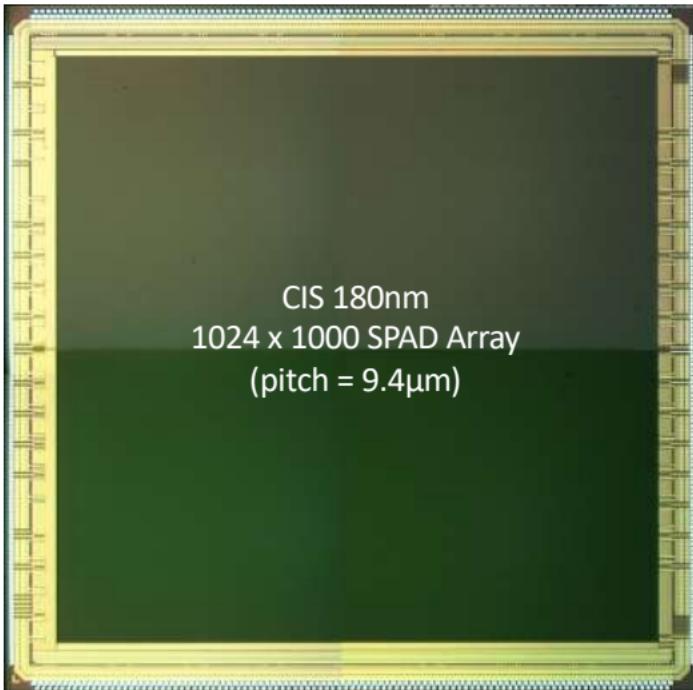
IEDM 2013



ISSCC 2018

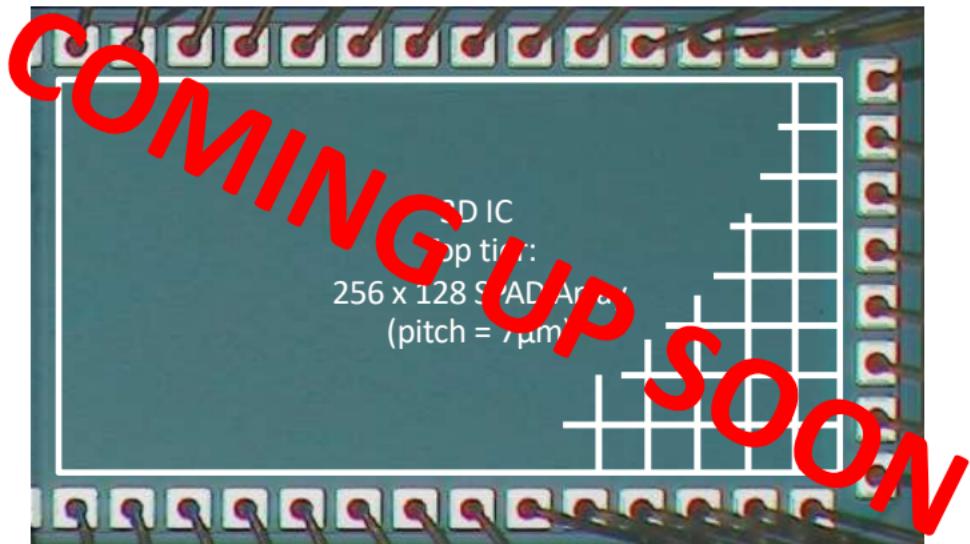
Recent aqua**lab** designs (2020-2021)

MegaX



Optica 2020

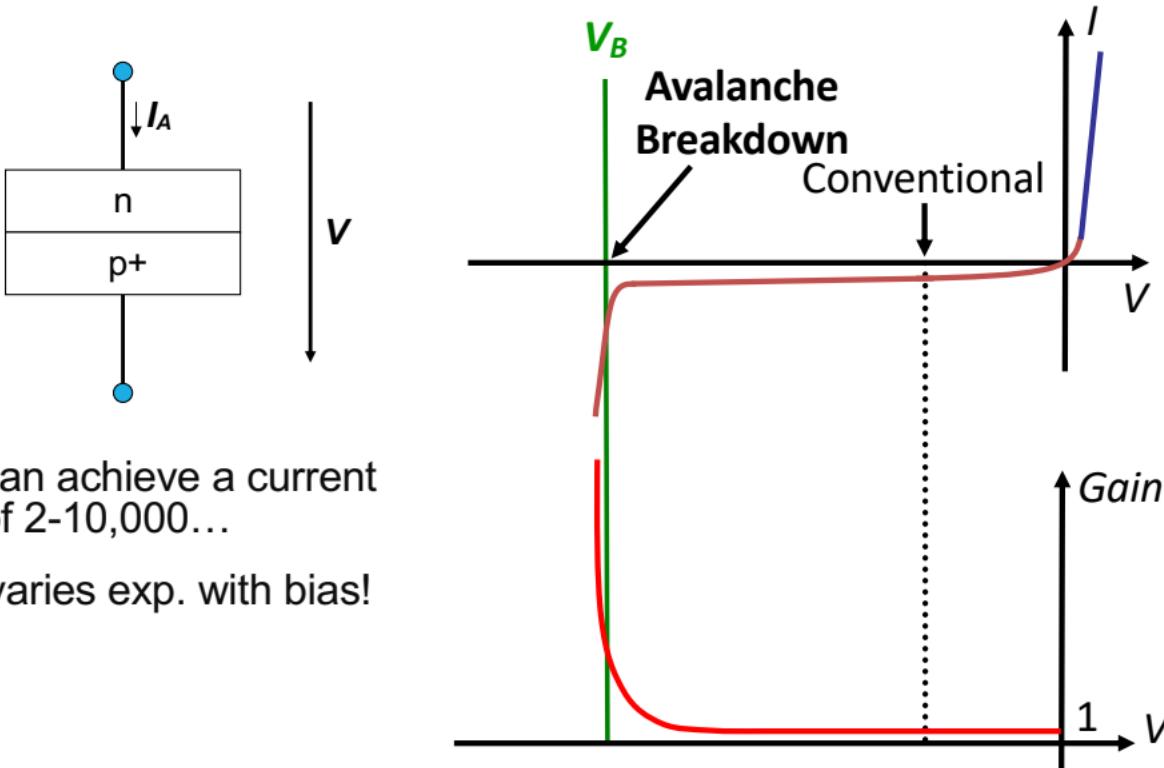
Jatayu



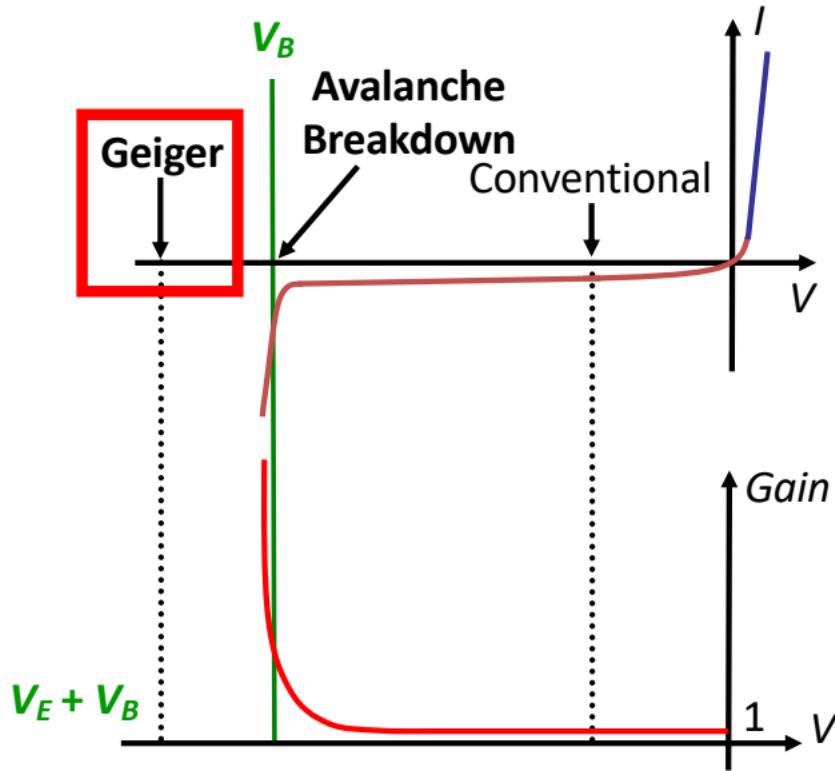
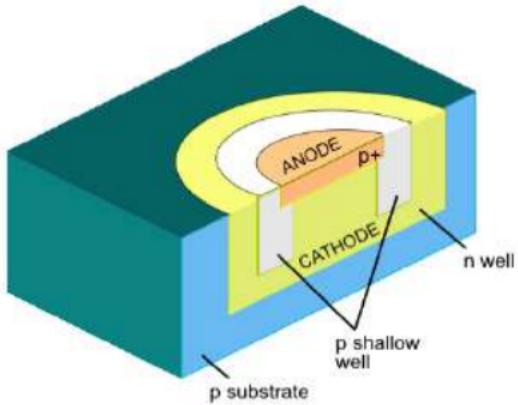
SPADs, SiPMs

SPADs, SiPMs

Avalanche Photodiodes (APDs)

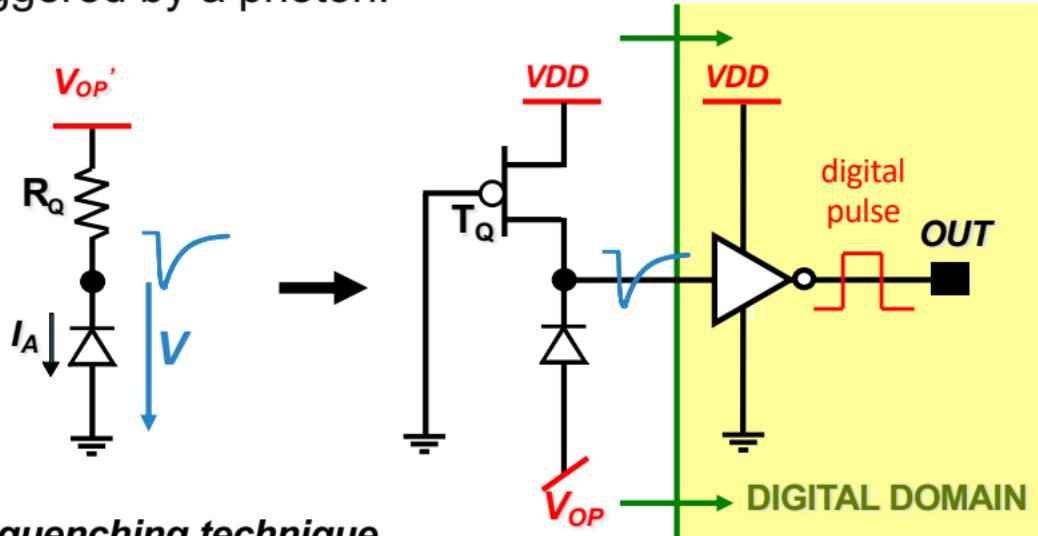


Single-Photon Avalanche Diodes (SPADs)



Quenching a SPAD in CMOS

- The SPAD becomes like any other digital device but it is triggered by a photon!

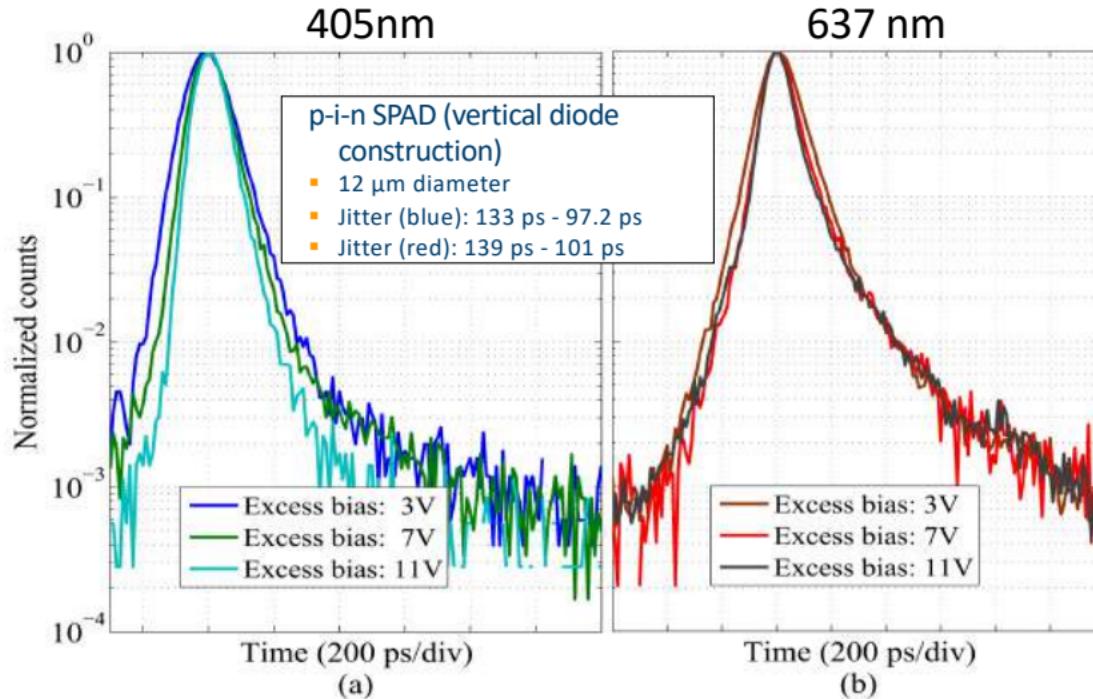


Passive quenching technique

Characterization of SPADs

- Timing resolution (**~10-100ps**)
- Sensitivity
 - Photon Detection Probability (PDP) (up to **50-60%**)
 - Fill-factor (**40-80%**)
- Dead time (**10-100ns**) -> spatial/temporal oversampling
- Dark counts (cps-kcps)
- Afterpulsing (**0.1-10%**)

Timing Resolution



C. Veerappan & E. Charbon, IEEE TED(63) 2016

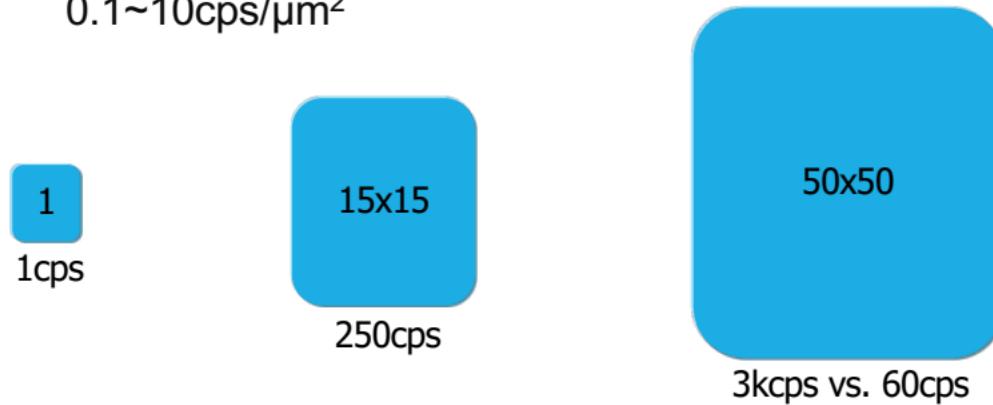
Noise: Dark Count Rate (DCR)

State-of-the-art SPADs in dedicated technology:

$$0.04\text{--}1\text{cps}/\mu\text{m}^2$$

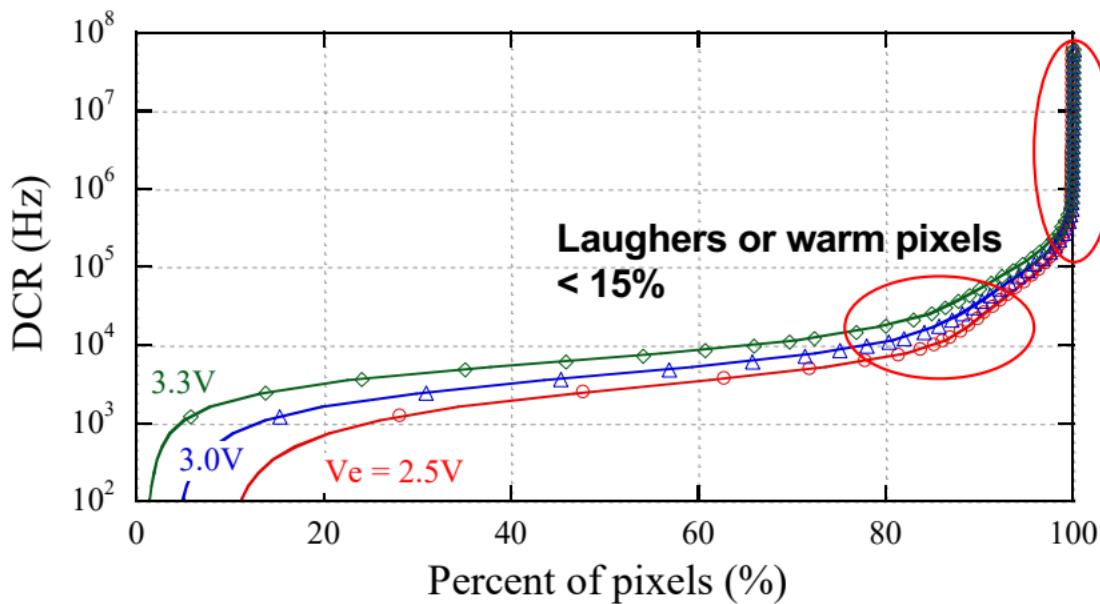
State-of-the-art CMOS SPADs:

$$0.1\text{--}10\text{cps}/\mu\text{m}^2$$



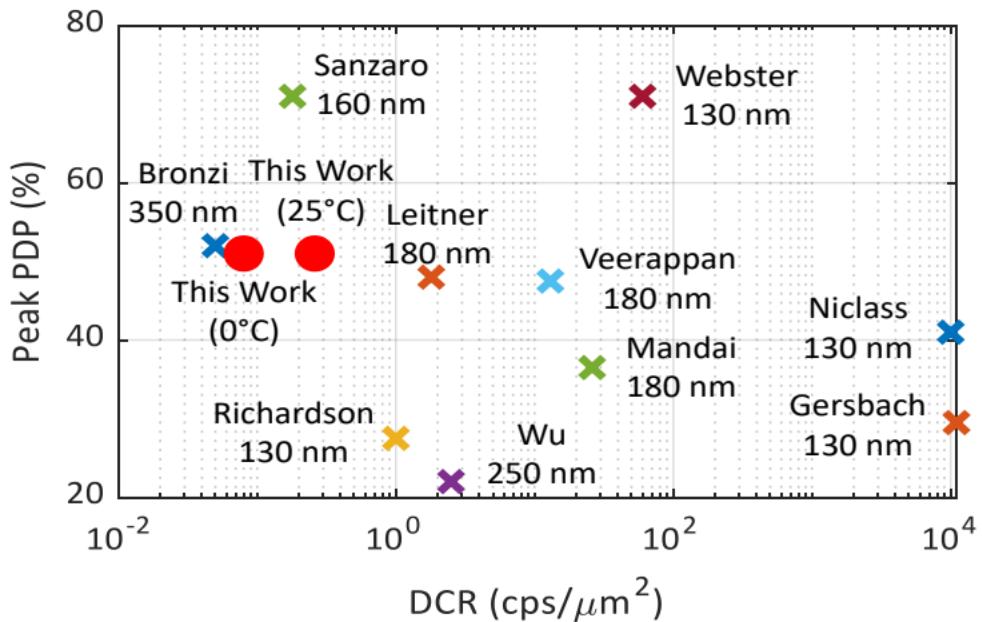
DCR Uniformity

Screamers or
hot pixels
 $< 0.04\%$

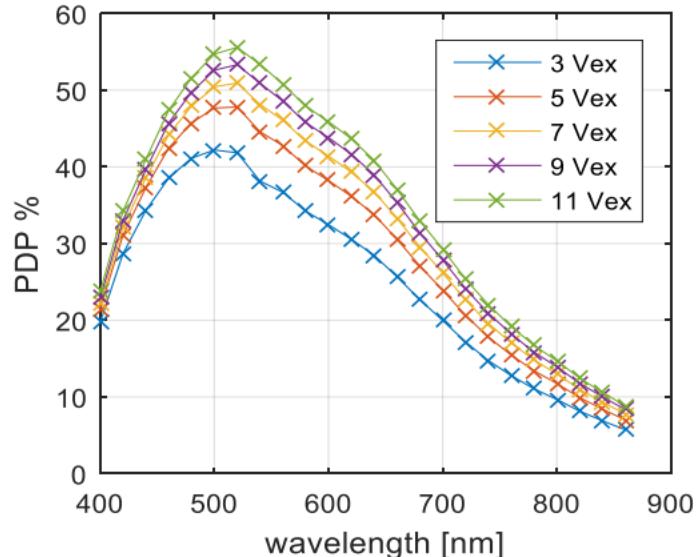


Courtesy: Yuki Maruyama, JPL, Pasadena, USA

PDP vs DCR



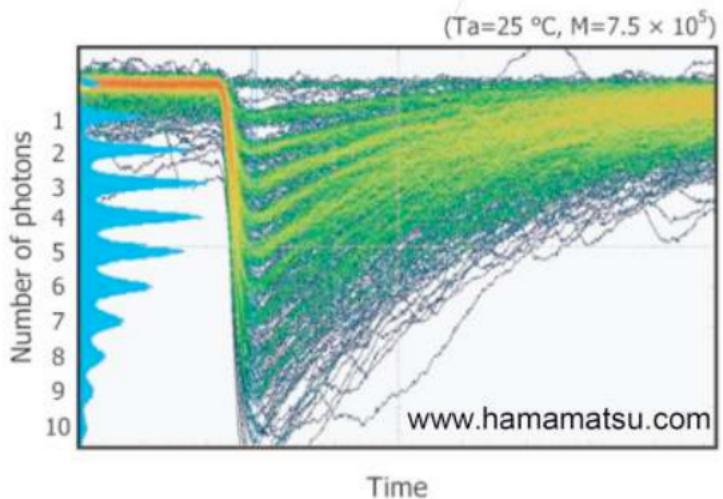
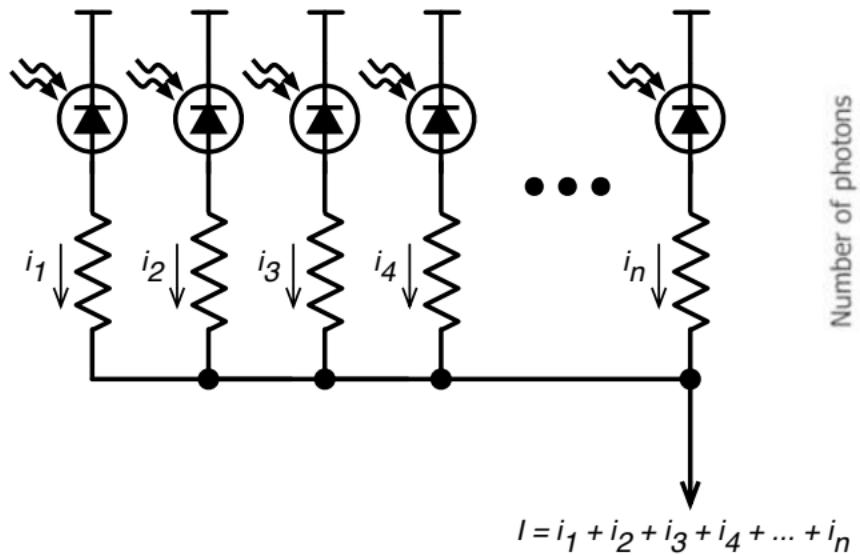
C. Veerappan et al., IEEE Trans. Electron Devices 63(1), 2016
 A. Ulku et al., JSTQE 2019



I. M. Antolovic, C. Bruschini, E. Charbon, Optics Express 2018

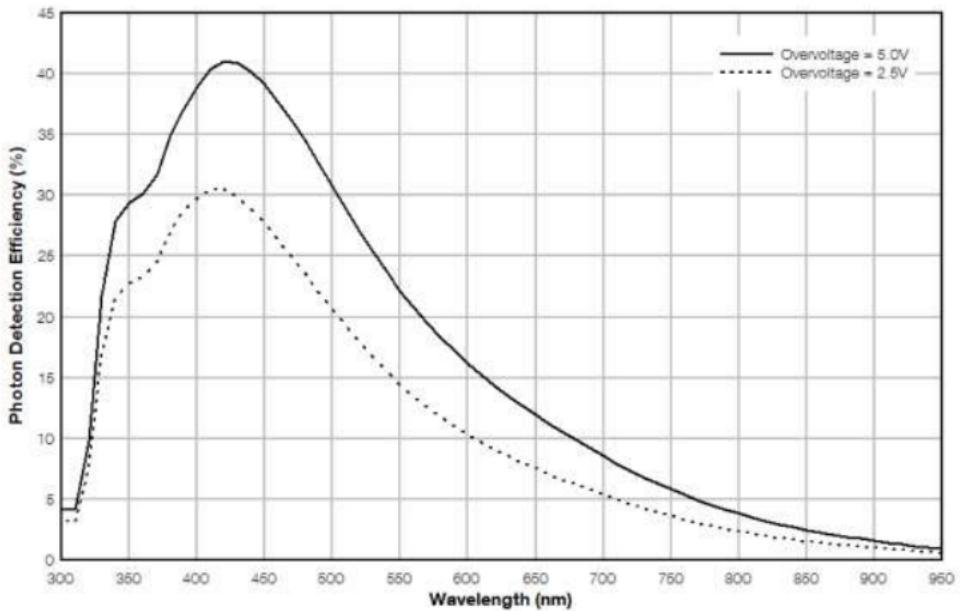
SPADs, SiPMs

Analog Silicon Photomultipliers (A-SiPMs)

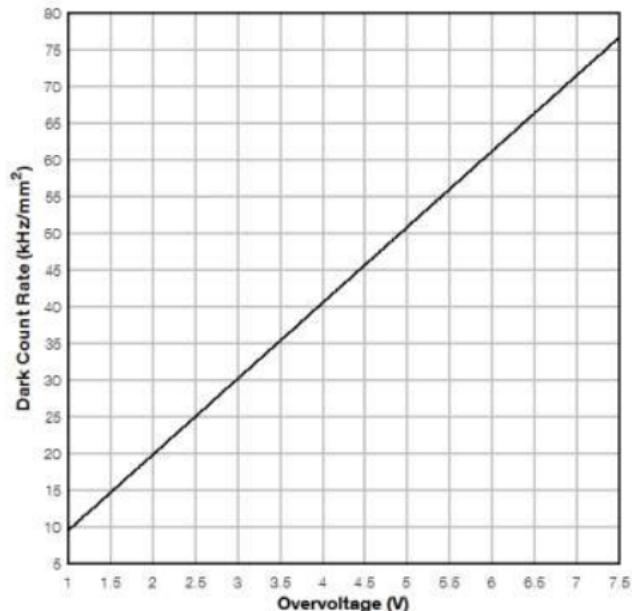


A-SiPM performance (ex: C-series)

PDE

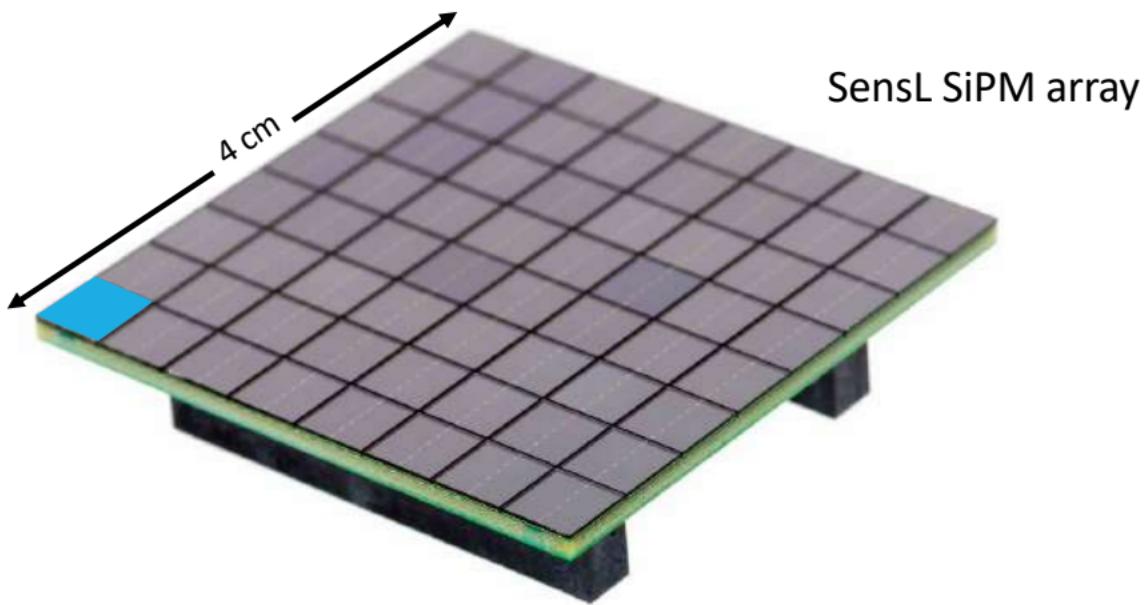


DCR

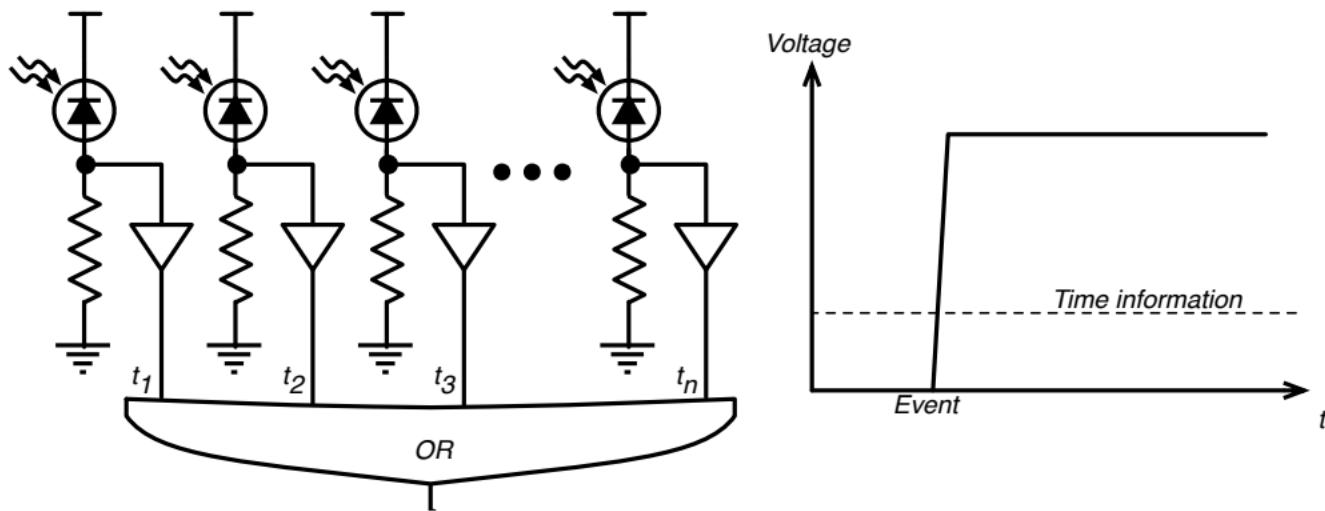


Source: SensL/ON Semi

A-SiPM arrays



Digital Silicon Photomultipliers (D-SiPMs)



An Image Sensor for FLARE

FLARE

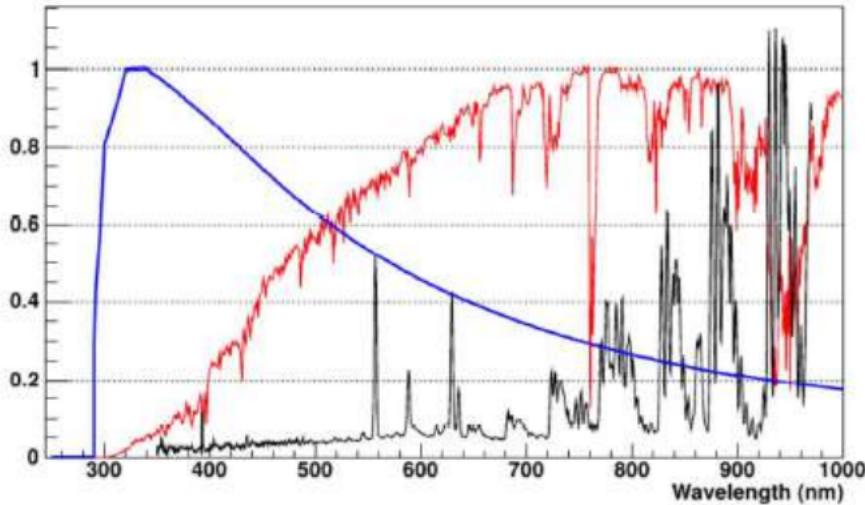
- Objective: build an innovative camera for the advanced LST
- Proposed solution:
 - A-SiPM + Front-end-electronics (FEE) ASIC + Fast A/D converter (FADC) ASIC + FPGA
 - DiPC + FPGA
- Aim: fully digital processing with ML image filtering as close as possible to the sensors

ASIC: Application-specific integrated circuit

FPGA: field-programmable gate array

DiPC: digital photon counter

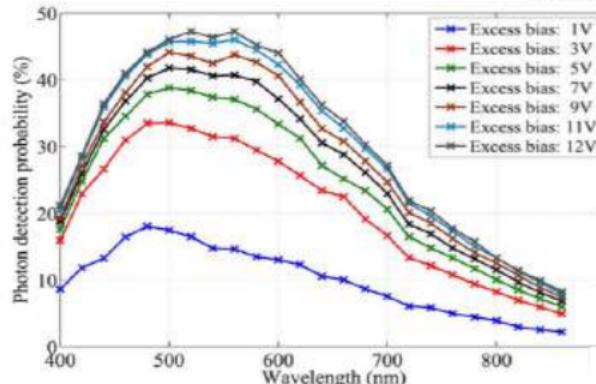
Spectrum of interest



Cherenkov Spectrum

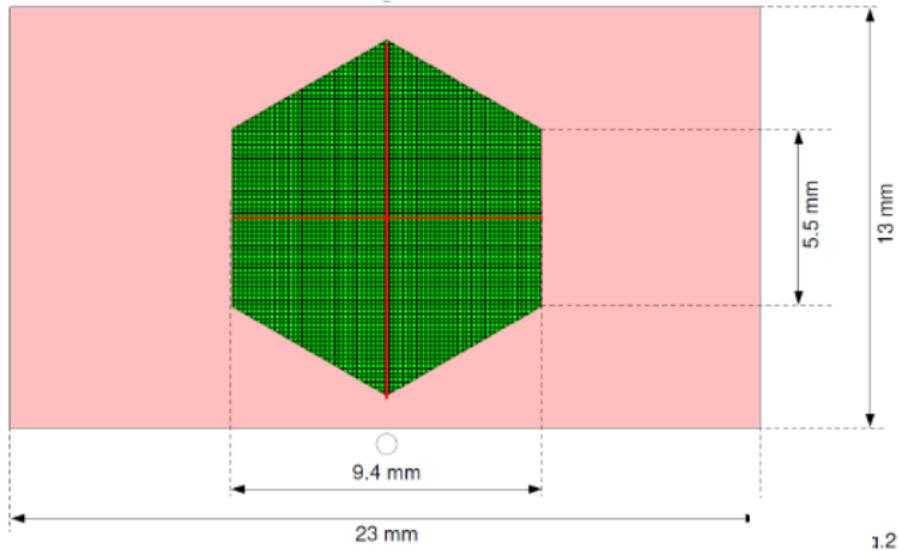
Night-Sky Background Spectrum

Moon Spectrum

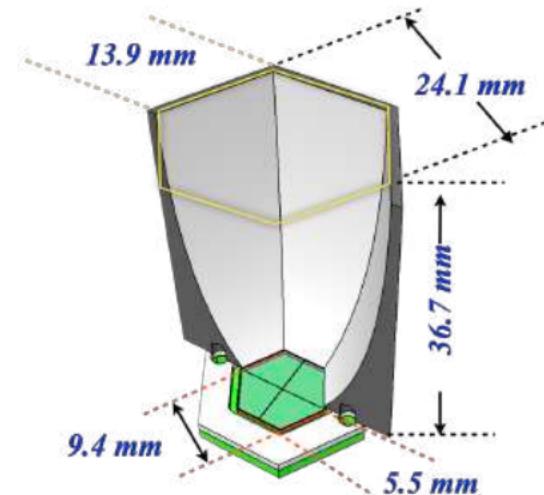


SPAD PDP

Pixel



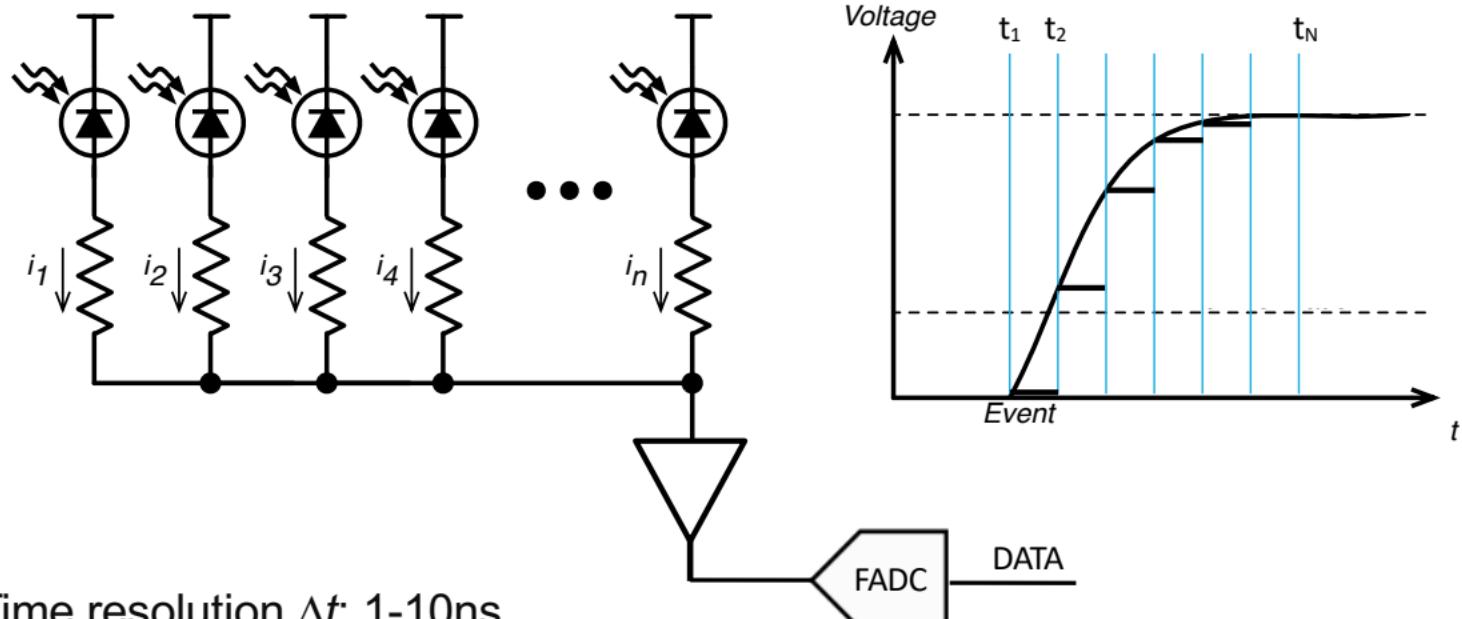
Pixel Boundary Conditions
Active SPAD area
Maximum area per pixel



A-SiPM

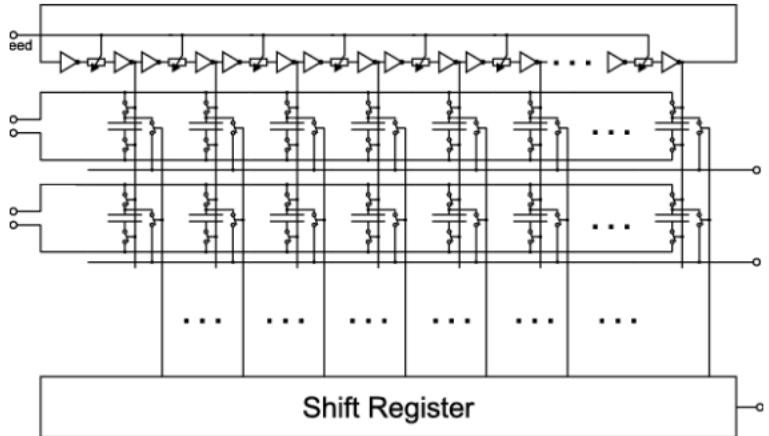
- For small Cherenkov telescopes, Silicon Photo Multipliers of **3mm x 3mm** is enough
- For larger telescopes, larger SiPMs are preferred
- SiPMs beyond **6mm x 6mm** with analog readout are not feasible, unless composite detectors are used
- Photons will arrive within few ns
- A SPAD area of **50μm x 50μm** or **100μm x 100μm** is a good compromise

A-SiPMs + FEE + fast ADC (FADC)



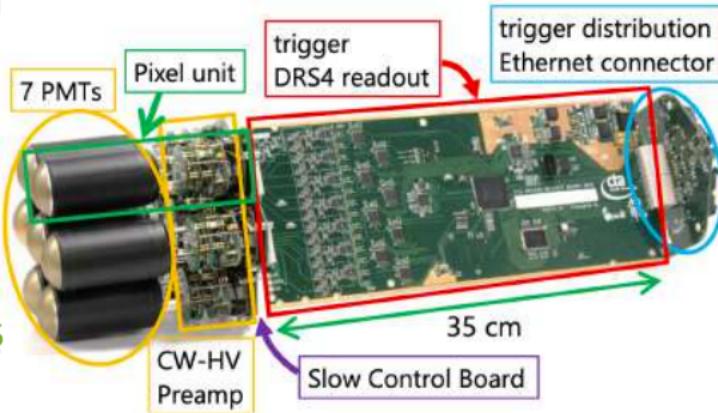
- Time resolution Δt : 1-10ns
- Amplitude resolution: 8-12 bits (256-4096 voltage bins)

Commercial FADC

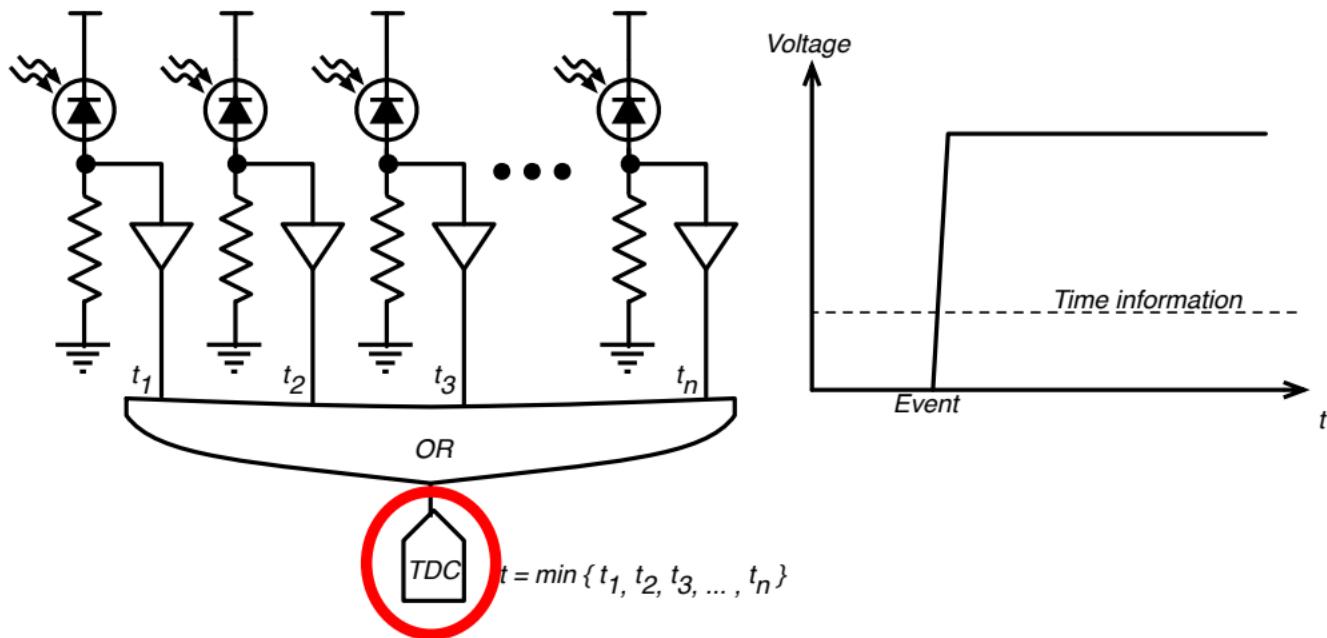


DRS4 (Radec)

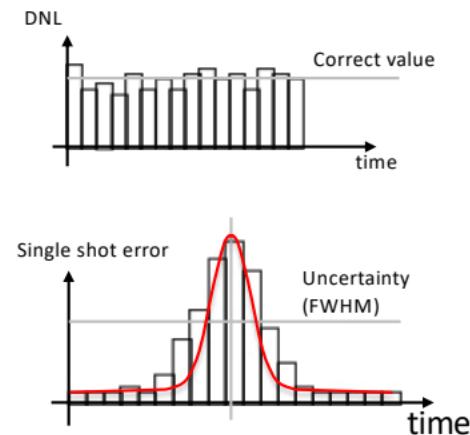
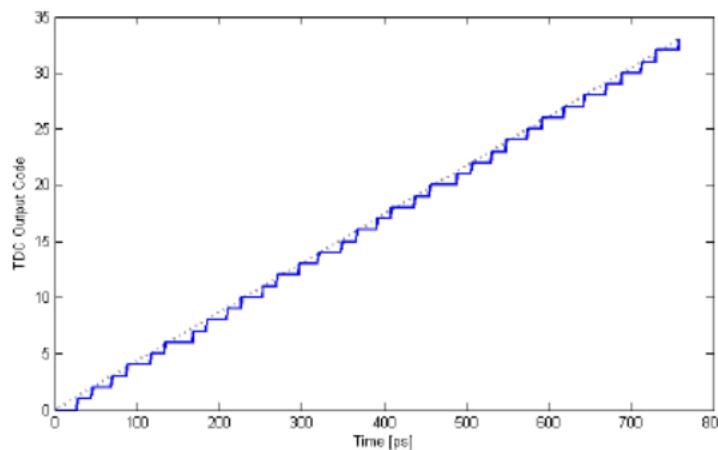
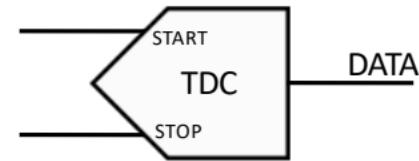
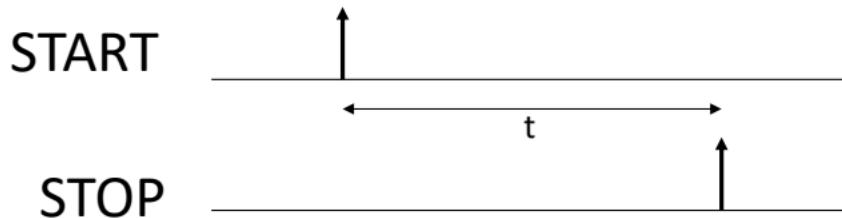
[arXiv:1509.00548v1 \[astro-ph.IM\]](https://arxiv.org/abs/1509.00548v1) 2 Sep 2015



D-SiPM

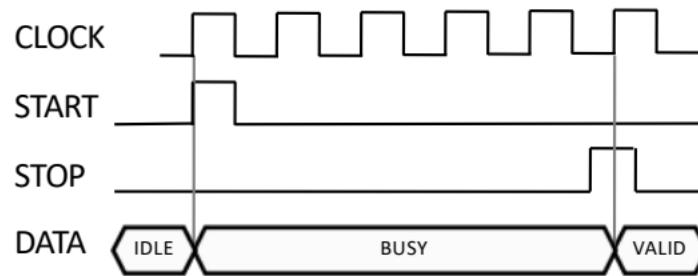
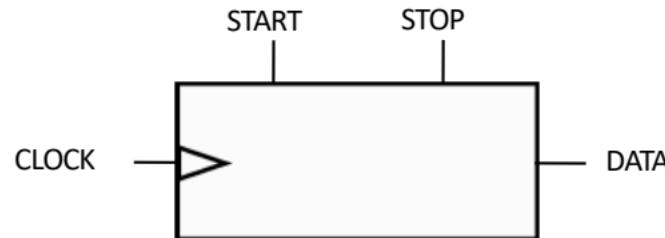


Time-to-digital converter (TDC)



The simplest TDC: a counter

- Resolution: $\tau = 1/f_{\text{clock}}$
- Conversion rate = 1/latency

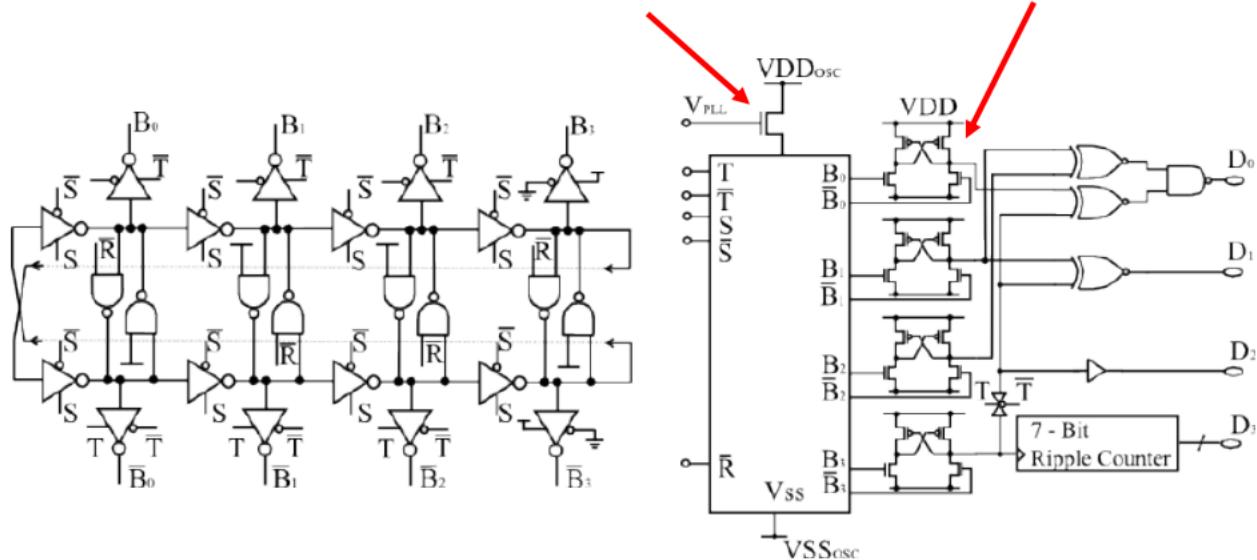


Advanced TDC: a coupled, fast RO

Example

- Resolution LSB = 30ps
 - Multi-input conversion
 - Resource reallocation
- DNL: $\pm 0.3\text{LSB}$
- INL: $\pm 0.8\text{LSB}$

Analog techniques allow greater architecture flexibility



Single-gate delay means less power, faster transitions

C. Veerappan, E. Charbon, et al. ISSCC2011

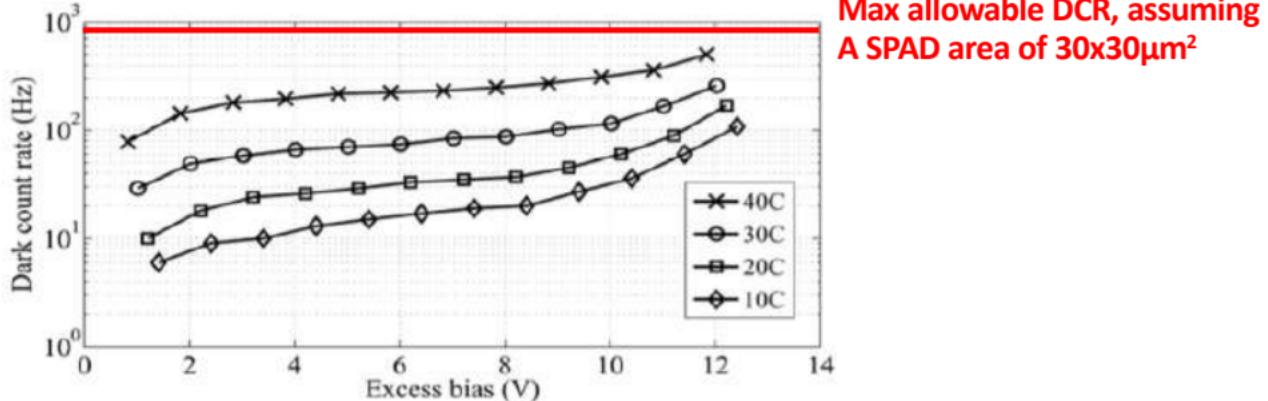
DiPC architecture

original idea due to Adrian Biland, ETHZ

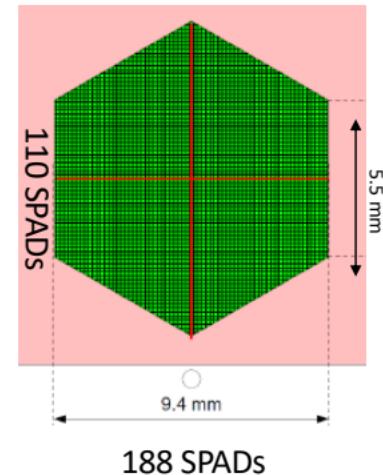
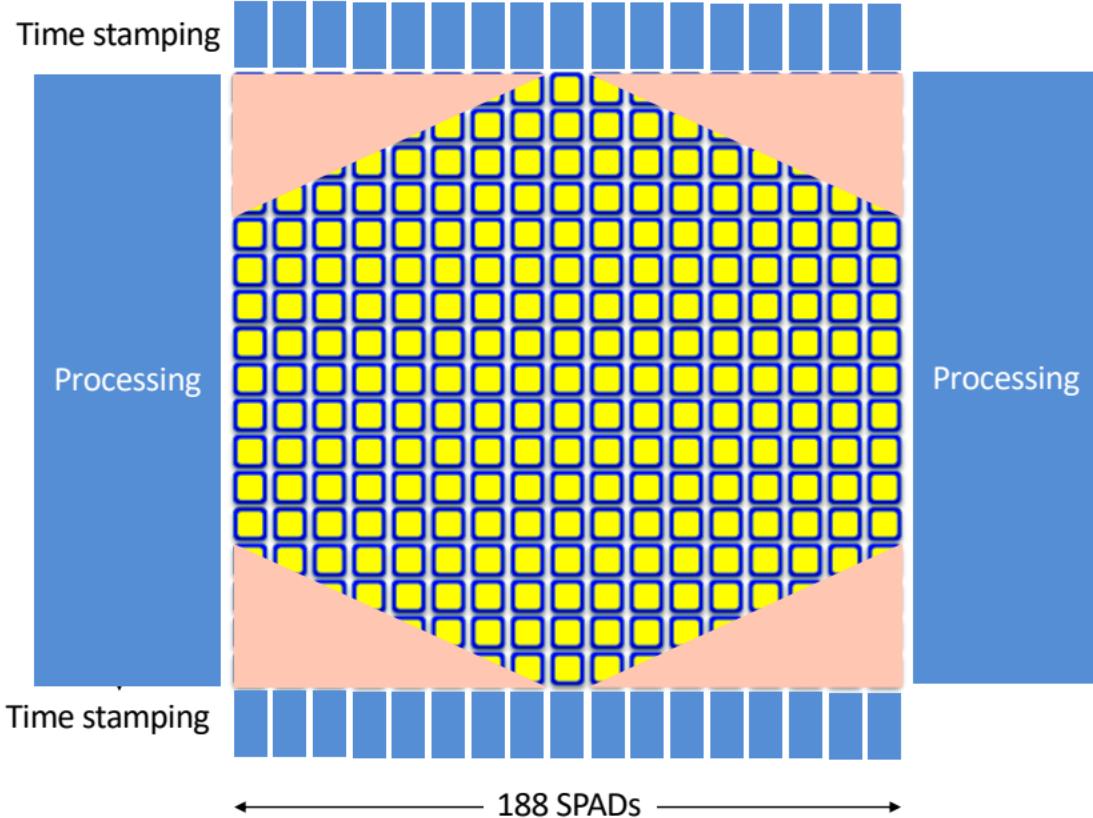
- We DO NOT store
 - all analog signals coming from the SiPM (DRS4 style)
 - all the analog signals ad 1GSa/s or higher
- Instead,
 - **we will count** (possibly time stamp) **only SPADs that have fired** over the last 5 μ s
(example: LSB=75ps; depth=16 bits)
 - since the firings will be sparse, we will have a small data volume
 - we can perform **coincidence** on chip and reduce data volume further
 - **1000 DiPCs in parallel** can be handled
- In addition, we can get
 - distribution of signals among neighboring pixels, and possible time gradient over the full signal.
 - with time stamps, more advanced analysis schemes will be possible

Dark count rate (DCR)

- Even in the darkest nights there is plenty of Night-Sky Background photons ($4\text{Mcps}/\text{mm}^2$)
- A dark noise (DCR) of $1\text{Mcps}/\text{mm}^2$ is acceptable
=> $1\text{cps}/\mu\text{m}^2$, this is not too challenging in SPADs
- DCR is not a concern for Cherenkov telescopes

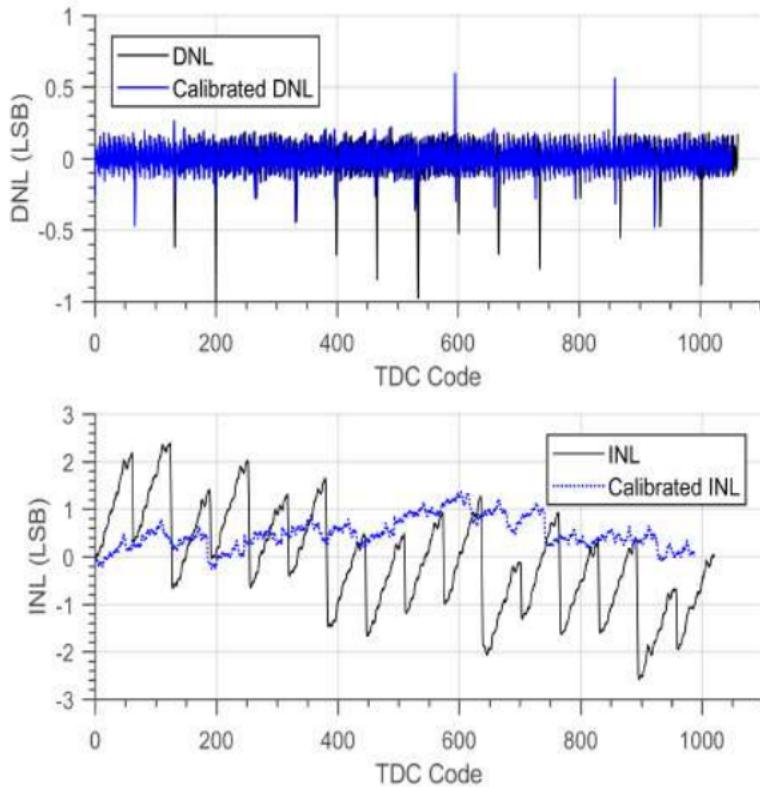


DiPC architecture

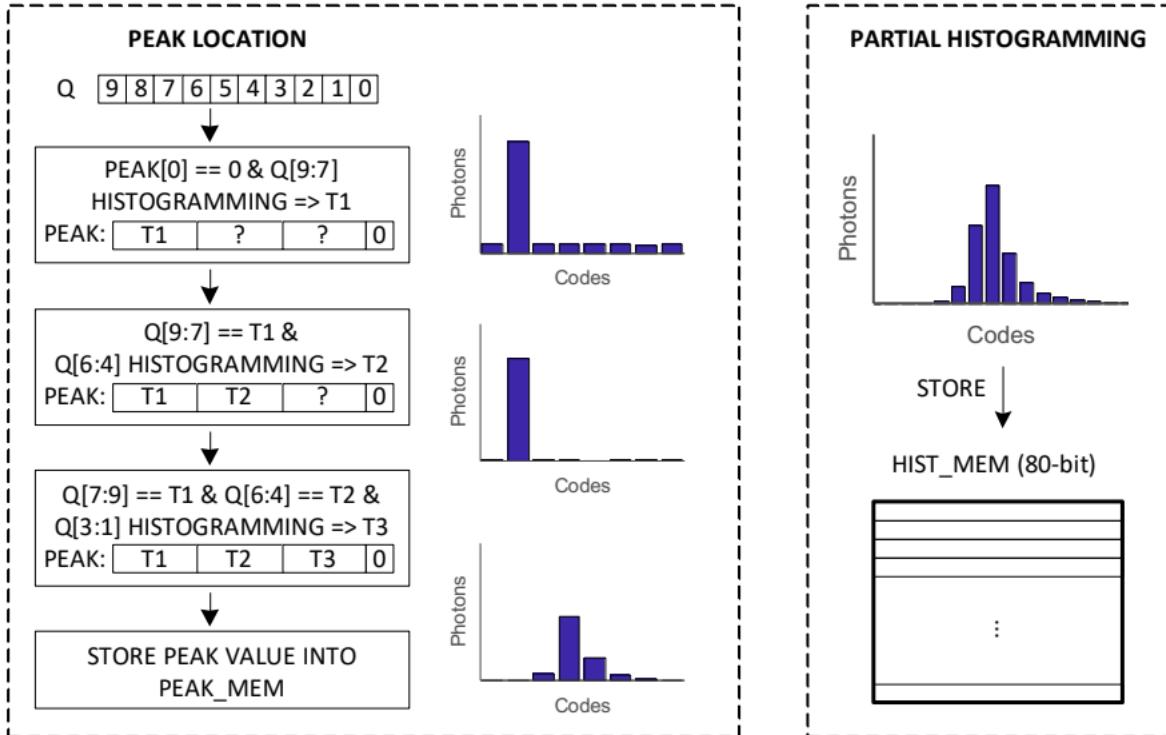


Example: 1728 TDCs

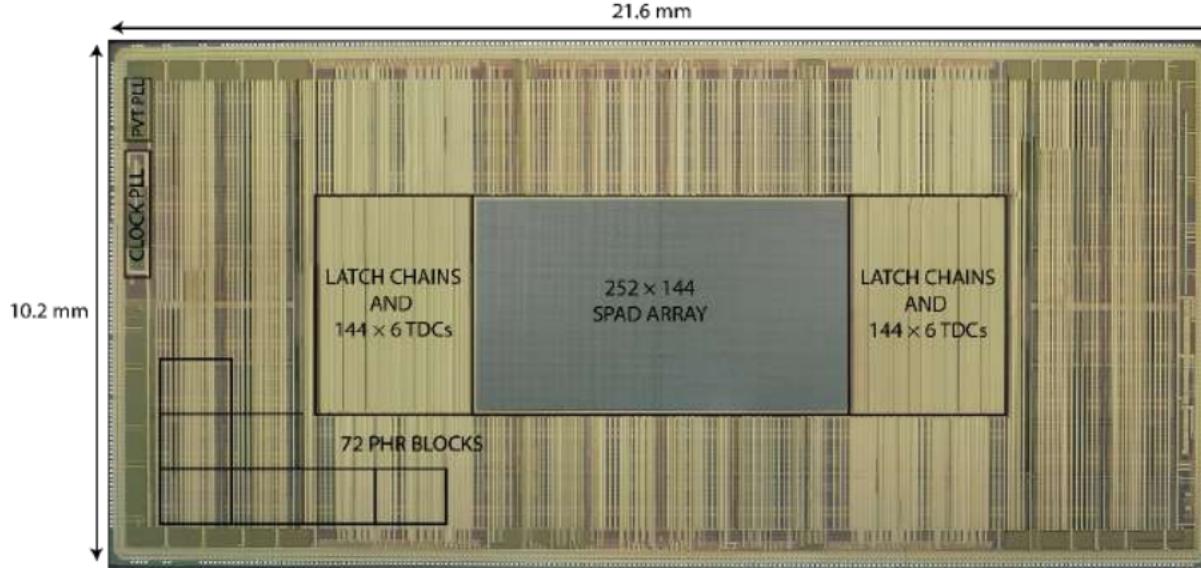
- DNL = +0.22/-1 LSB
- INL = +2.39/-2.6 LSB
- After calibration for clock transition:
- DNL = +0.6/-0.48 LSB
- INL = +0.89/-1.67 LSB



Example of on-chip processing



Implementation on 180nm CMOS



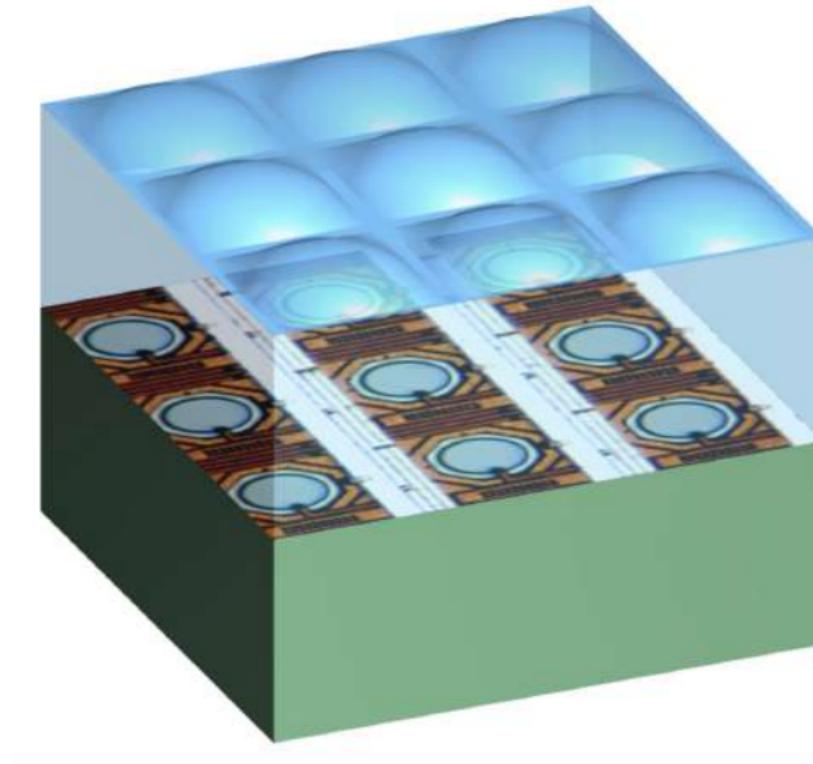
- 180nm CMOS
- 28% Fill factor (28.5 μ m pitch)
- 11.2 Gbit/s output data bandwidth

S. Lindner, C. Zhang et al., Symposium of VLSI, 2018
C. Zhang, S. Lindner et al., JSSC 2018

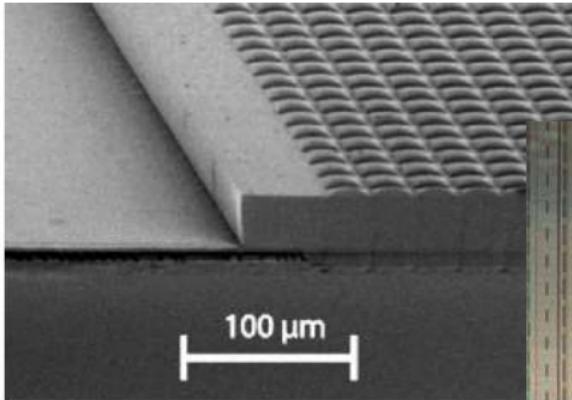
Small pixel perspectives

	Abbas, IEDM'16	Henderson, IEDM'10	Abbas, IISW'17	K. Morimoto & E. Charbon, Opex 2020		
Process technology	65/40nm 3D-BSI CMOS	90nm CMOS	130nm CIS		180nm CMOS	
Pixel pitch (μm)	7.83	5	3	2.2	3	4
Active diameter (μm)	-	2	1	1.2	2	3
Drawn fill factor (%)	45	12.5	14**	19.5*	32.3*	42.4*
Sensor resolution	128x120	3x3	4x4	4x4	4x4	4x4
Breakdown voltage (V)	12	10.3	15.8	32.35	23.6	22.1
Max. PDP (%)	27.5 ($V_{\text{ex}}=3\text{V}$)	36 ($V_{\text{ex}}=0.6\text{V}$)	15 ($V_{\text{ex}}=3.2\text{V}$)	10.3 ($V_{\text{ex}}=4\text{V}$)	17.3 ($V_{\text{ex}}=6\text{V}$)	33.5 ($V_{\text{ex}}=6\text{V}$)
Max. PDE (%)	12.4 ($V_{\text{ex}}=3\text{V}$)	4.5 ($V_{\text{ex}}=0.6\text{V}$)	2.1 ($V_{\text{ex}}=3.2\text{V}$)	2.0 ($V_{\text{ex}}=4\text{V}$)	5.6 ($V_{\text{ex}}=6\text{V}$)	14.2 ($V_{\text{ex}}=6\text{V}$)
Median DCR (cps)	11,000 ($V_{\text{ex}}=3\text{V}$)	250 ($V_{\text{ex}}=0.6\text{V}$)	150 ($V_{\text{ex}}=1\text{V}$)	751 ($V_{\text{ex}}=4\text{V}$)	1.6 ($V_{\text{ex}}=6\text{V}$)	2.5 ($V_{\text{ex}}=6\text{V}$)
Crosstalk (%)	-	<0.1 ($V_{\text{ex}}=0.6\text{V}$)	0.13-0.22 ($V_{\text{ex}}=1\text{V}$)	2.97 ($V_{\text{ex}}=4\text{V}$)	2.75 ($V_{\text{ex}}=6\text{V}$)	3.57 ($V_{\text{ex}}=6\text{V}$)
Afterpulsing probability (%)	-	-	0.18 ($V_{\text{ex}}=1\text{V}$)	<0.20 ($V_{\text{ex}}=4\text{V}$)	0.20 ($V_{\text{ex}}=6\text{V}$)	0.21 ($V_{\text{ex}}=6\text{V}$)
Timing jitter (ps)	136 ($V_{\text{ex}}=3\text{V}$)	107 ($V_{\text{ex}}=0.6\text{V}$)	107 ($V_{\text{ex}}=3\text{V}$)	72 ($V_{\text{ex}}=4\text{V}$)	70 ($V_{\text{ex}}=6\text{V}$)	88 ($V_{\text{ex}}=6\text{V}$)

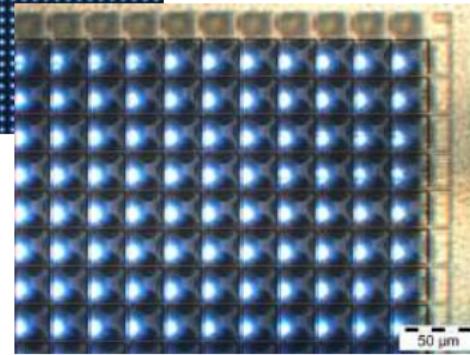
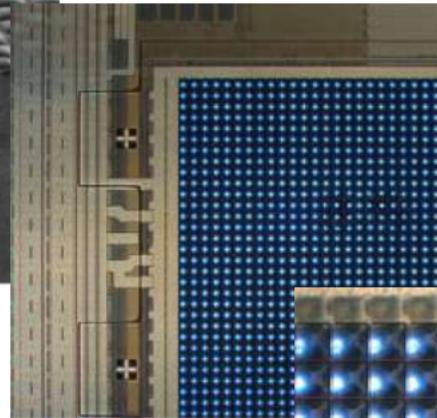
Fill factor recovery: microlenses



Fill factor recovery: microlenses

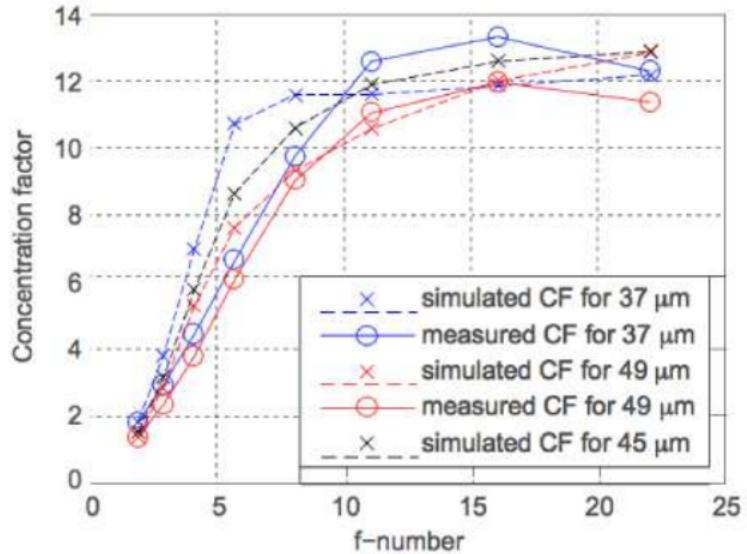


J. Mata Pavia et al., Optics Express 2014



C. Zhang et al., JSSC 2018

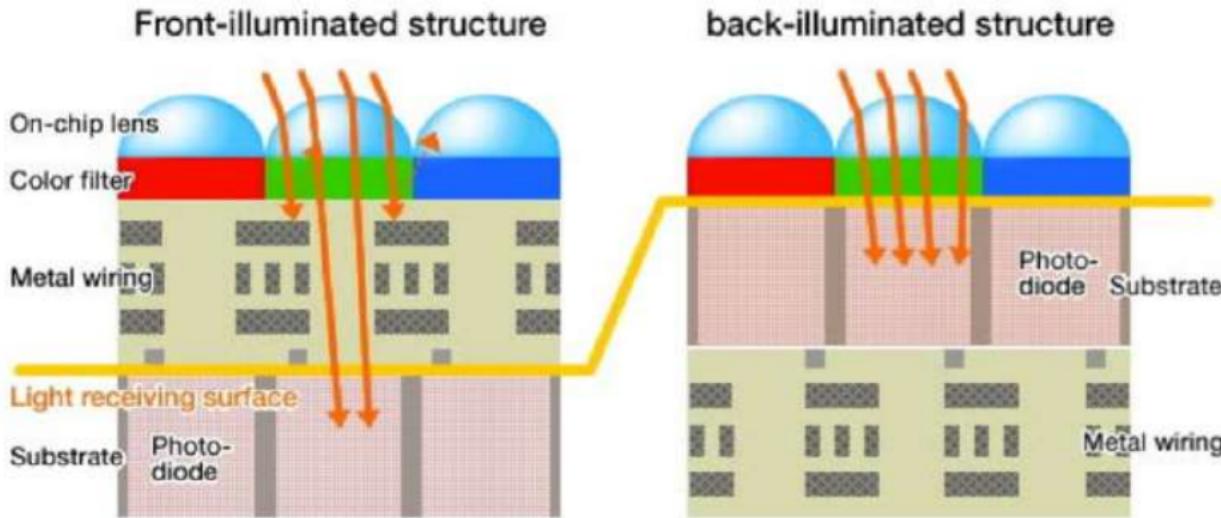
Fill factor recovery: microlenses



J. Mata Pavia et al., *Optics Express* 2014

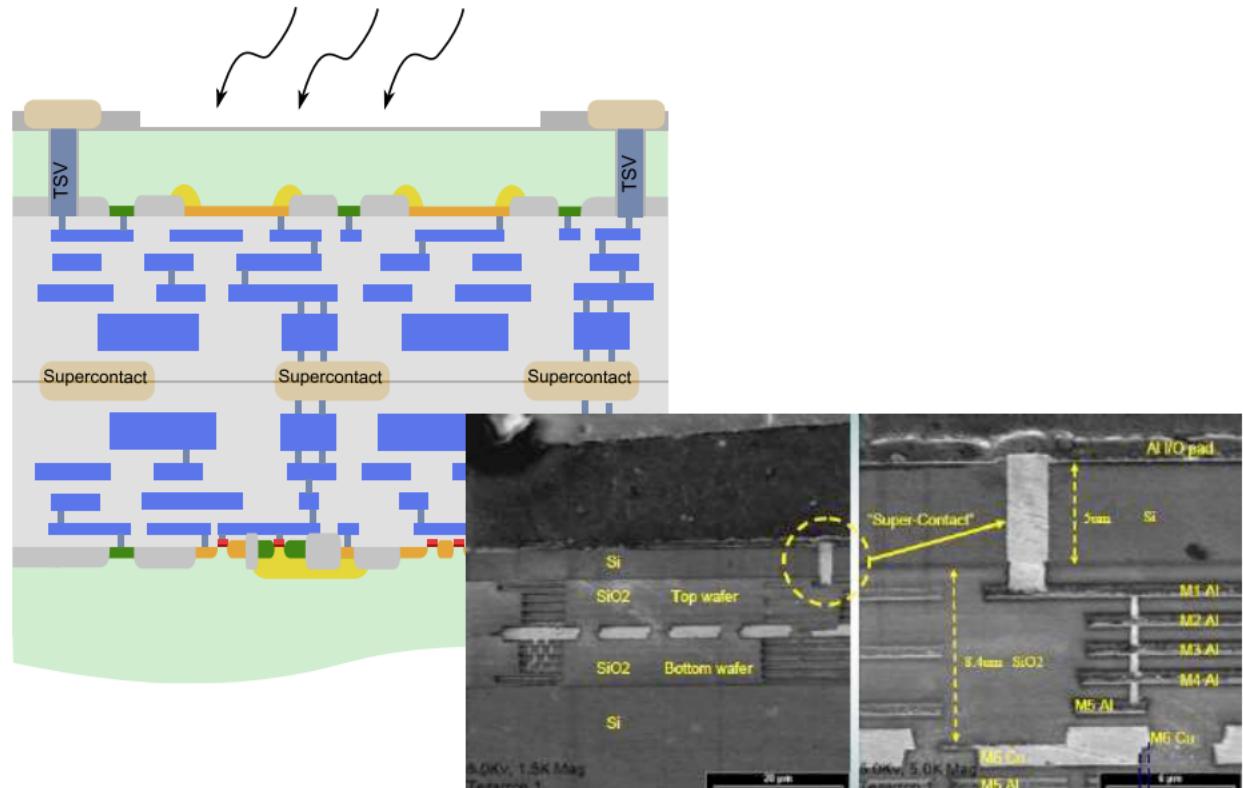
3D Integration

3D Integration: FSI vs. BSI



Source: Sony

3D Integration: Flip-Chip



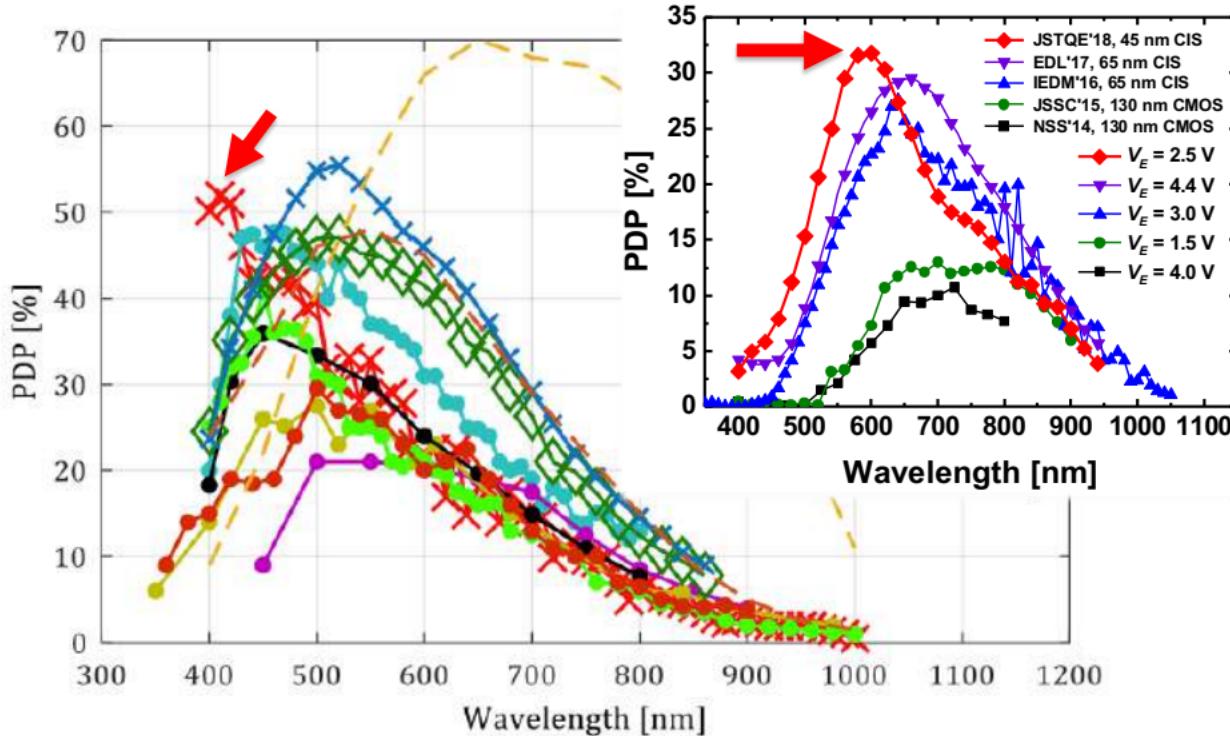
2D or not 2D: this is the question

A full camera needs 10'000 SiPM. There shall be several cameras.

- **2D**
 - + lower costs
 - - larger SPADs and simple electronics per SPAD
- **3D**
 - + different tier for SiPM and processing electronics
 - + better fill factor and therefore better overall sensitivity
 - + allows to use smaller SPADs
 - + more space for more processing electronics
 - - higher costs

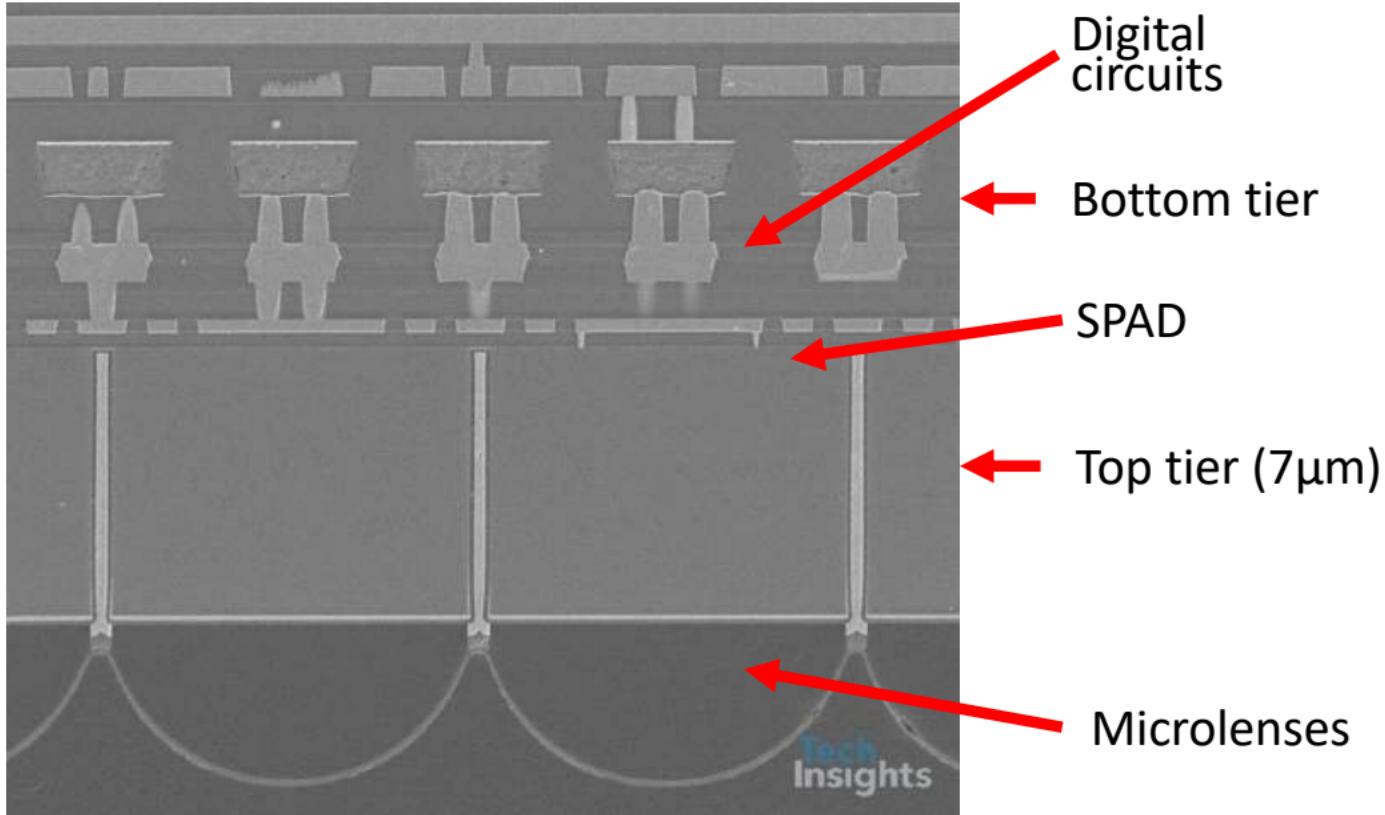
SPAD 3D integration evolution

M.-J. Lee et al., Jpn. J. Appl. Phys'18

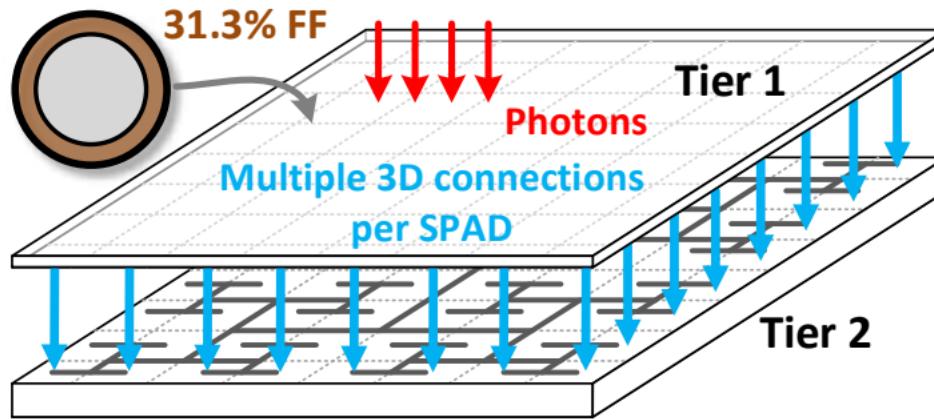


C. Veerappan & E. Charbon, TED 2016

Apple's SPAD 3D integration

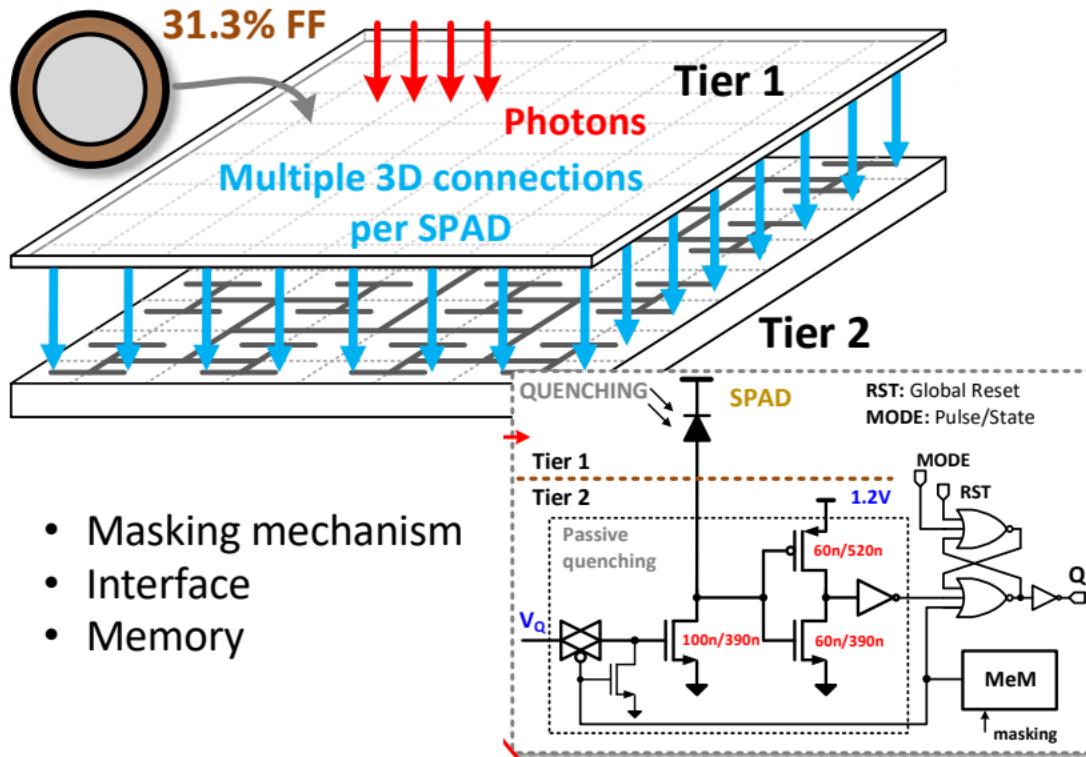


BSI + 3D-stacking

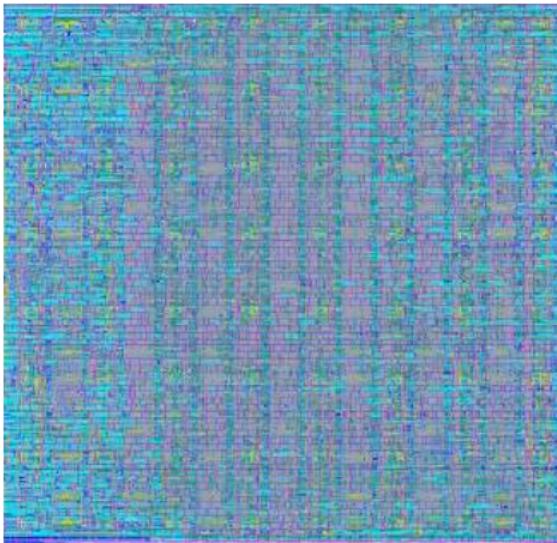


- Tier 1: SPADs + microlenses
- Tier 2: quenching, recharge, TDCs, multi-core, memories, communication unit, I/O

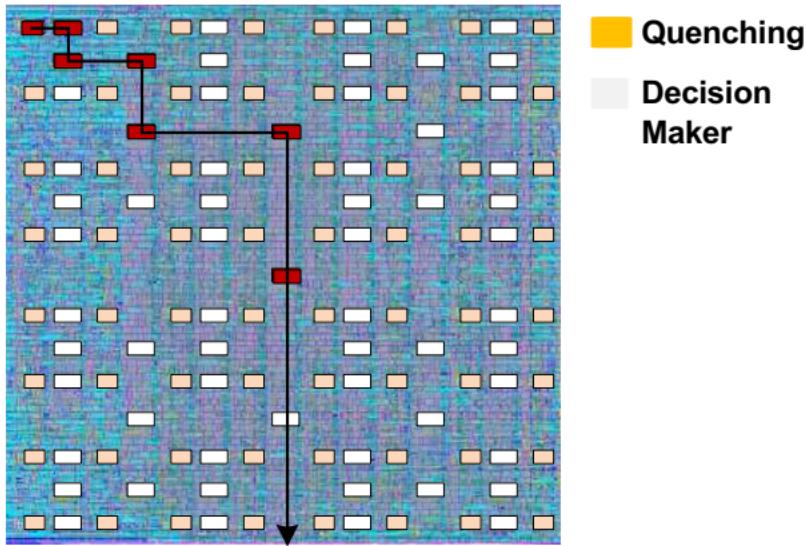
BSI + 3D-stacking



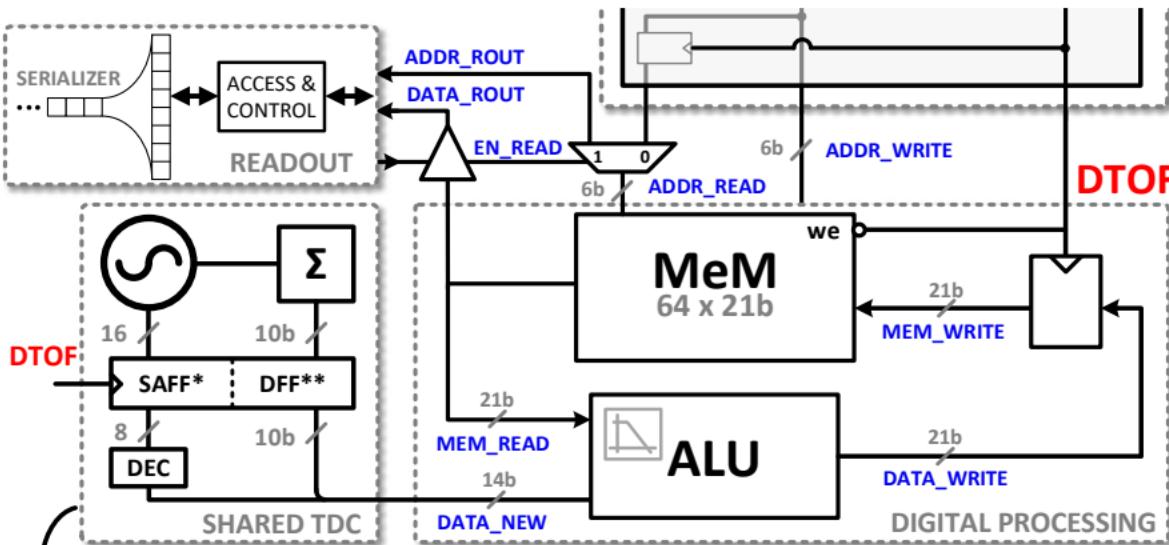
Bottom-tier electronics



Bottom-tier electronics

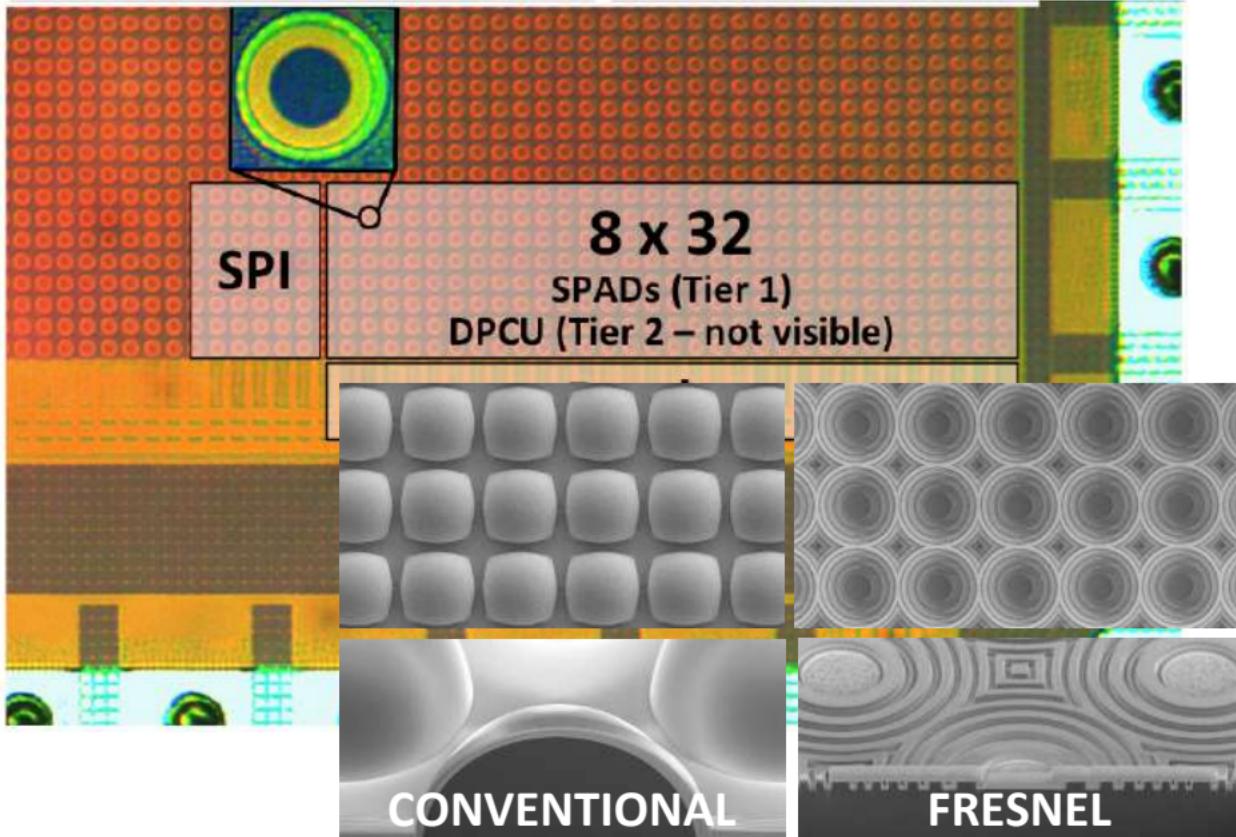


Bottom-tier electronics

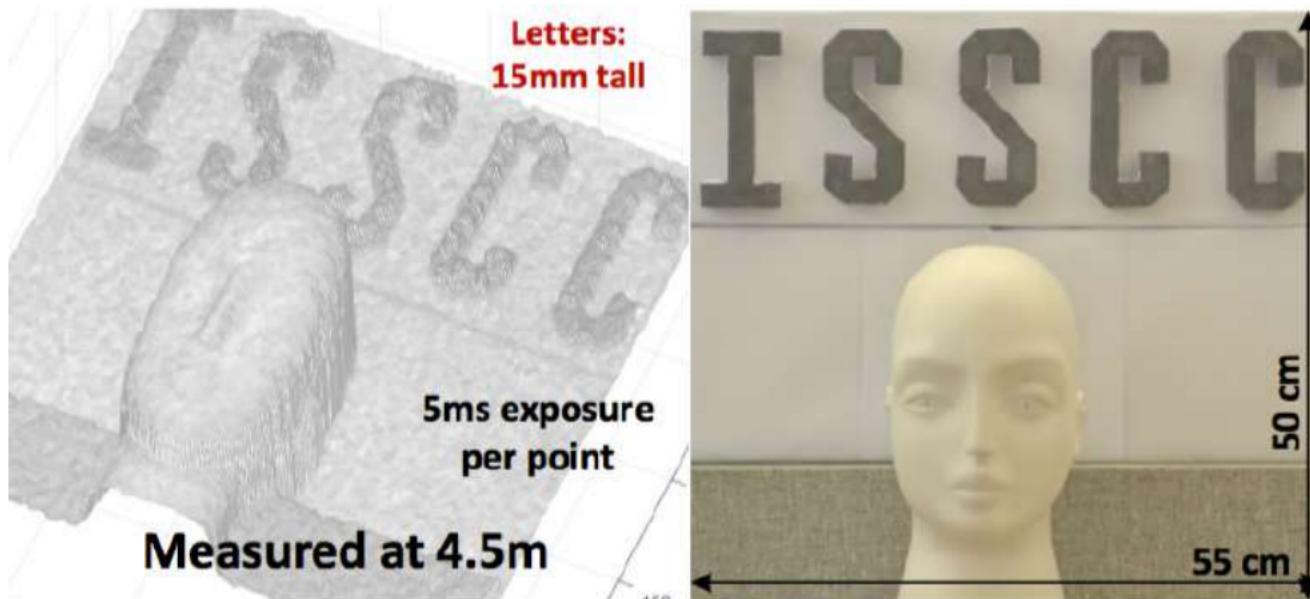


A.R. Ximenes, P.Padmanabhan *et al.*, ISSCC, 2018

3D-stacked chip micrograph

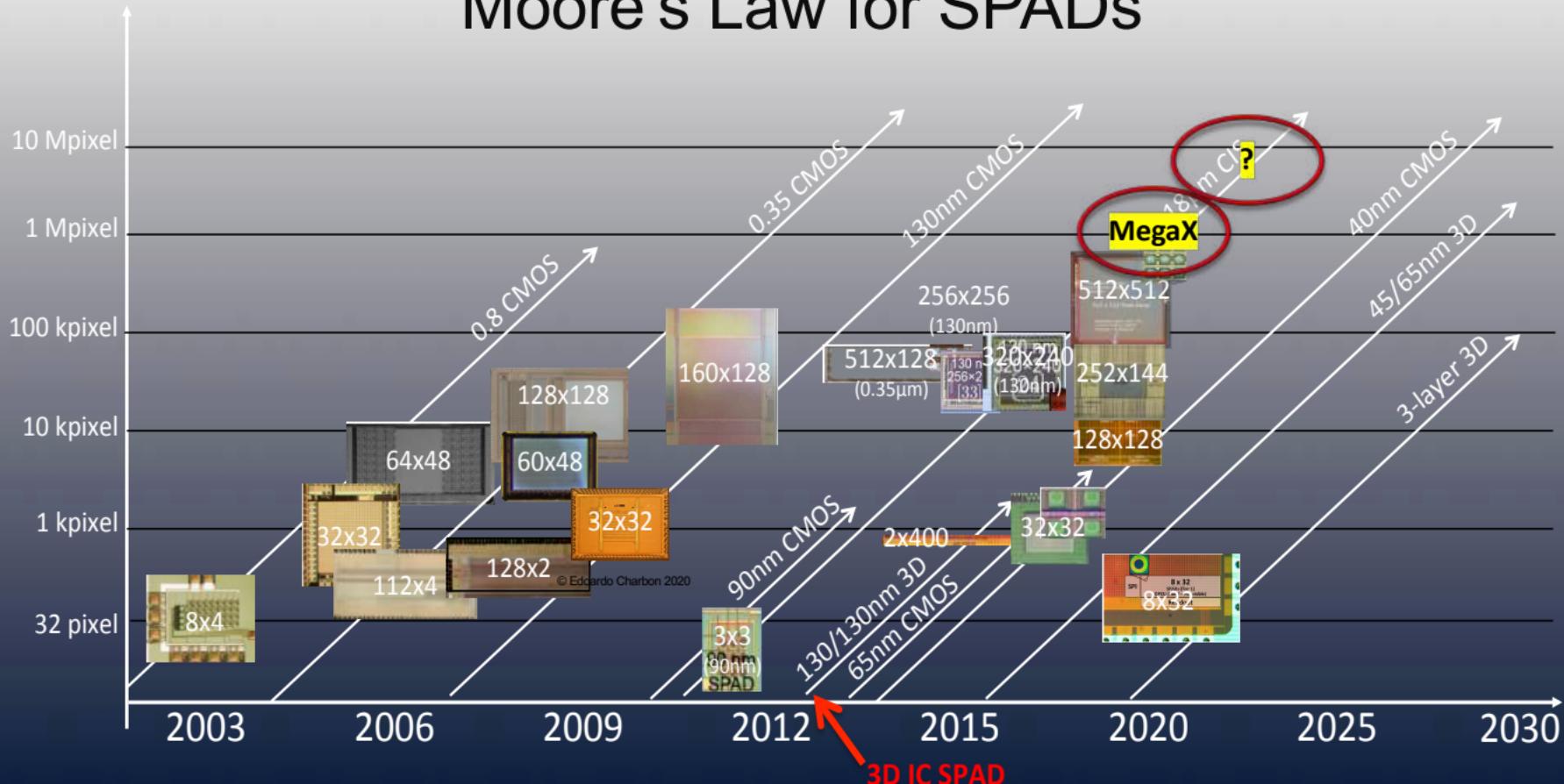


256x256 3D image reconstruction



A.R. Ximenes, P.Padmanabhan *et al.*, ISSCC, 2018

Moore's Law for SPADs



Conclusions

Take-home messages

- CTA has to keep data volume and power low!
- Proposed techniques in DiPC
 - Keeping signals digital to avoid unnecessary conversions
 - Compute time stamps
 - More advanced digital processing
- Modularity is an important ingredient to large photonic systems and

Thank You

<http://aqua.epfl.ch>

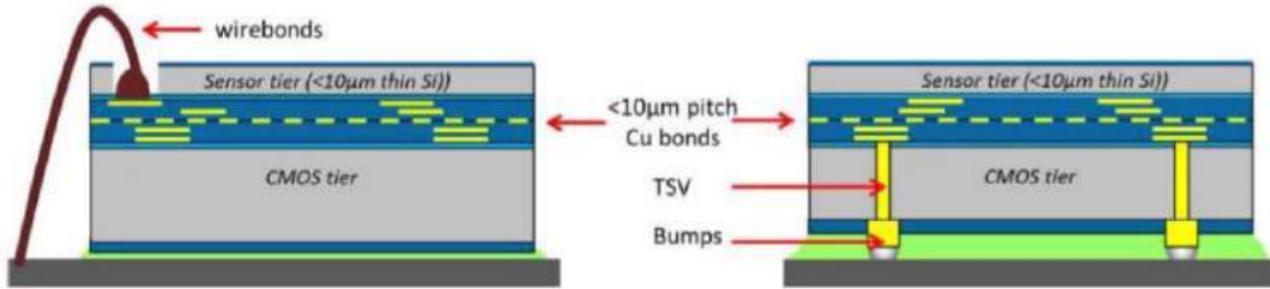
1st International SPAD Workshop (2018) 2nd edition: Edinburgh (2020)



SPADs are “hot”...Les Diablerets, CH, Feb 2018 <https://issw.epfl.ch/>

Next edition: 2022, in an undisclosed location

Completed Polis Process



Demonstrator 1 : 2-tiers 3D assembly with the same CMOS technology for the two tier (Existing imager technology).

Demonstrator 2 : 2-tiers 3D assembly an imager tier and a CMOS 40nm technology (with breakable low-k materials). it will include TSVs.