FCC – Vertex detectors in Extra Dimensions

Ronald Lipton

The Future from the Past point of view

- In accessing the prospects for a collider >20 years away it is interesting to look back at “future” prospects from ~40 years ago.
  Lederman, Huson, Schwitters – Snowmass 1982:

state of the art which depends on the properties of BBQ, gas chambers, liquid argon, lead glass, etc.

The conclusion is that things have only gotten worse since 1973.

II. Integration Time - Tracking

What are the implications of long integration times? We are facing collision energies so high that the charged and neutral multiplicities, $\bar{M}$ average about 60 particles near 1 TeV. These typical

increasing pervasiveness of calorimeters which have become indispensable devices for measurement of

IV. Current State of the Art

There is ample data from 1982 experiments that support this pessimism. Charm was discovered in 1975.

The conclusion (partly political) – can’t do physics at 10^{33}.
Silicon-based technologies developed in the ‘80s broke the paradigm on which LHS based their arguments, revolutionizing tracking detector spatial and time resolutions. Will there be another, comparable revolution?

Evolution and Revolution

I will not try to predict the next silicon-style revolution, but we can extrapolate trends in the semiconductor industry and current directions of detector R&D. There are also clear trends in detector development:

- Fast timing (10's of ps or less) – LGAD
- Position resolution (micron level) – Pixel (3D integration)
- Integration of intelligence, triggering
- Fast, efficient data transmission. – Optical systems->Wireless
- Radiation hardness – Substrate engineering, thin devices, deep submicron electronics
- Low system mass, low power – CO2 cooling, fiber and foam based supports.

2D → 3D → 4D and beyond

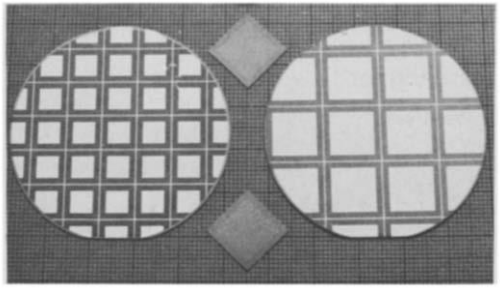
2D- Adapt planar silicon technology to diode sensors (Kemmer…)

- Microplex readout chip (Parker…)

3D – Development of pixel detectors utilizing bump bonding technology (1989…)

The fourth dimension is just emerging – time resolution aimed at tracking rather than bunch separation with picosecond - level resolution

We can also consider adding a fifth+ dimension – track angle by maximizing utilization of the information in our detectors



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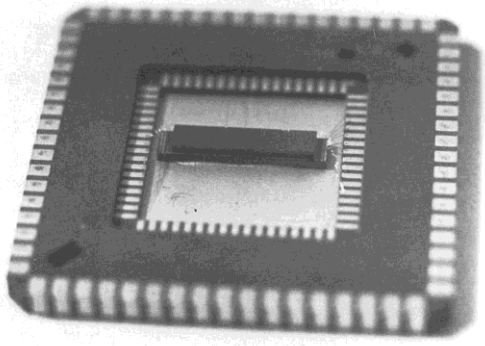
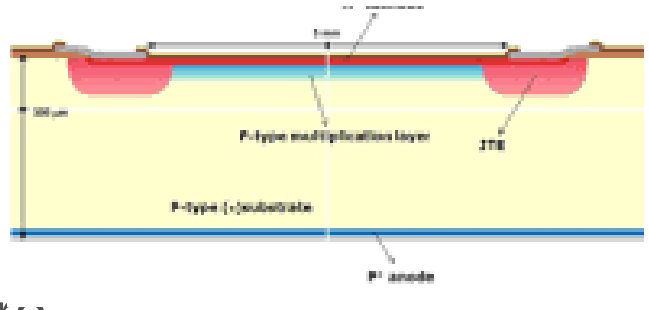
4. Conclusion

Using the planar process it is possible to fabricate
Si radiation detectors of extremely low reverse



ystems workstations with additional multi- Table 1



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Beyond Planar Technologies

The silicon substrate itself can be engineered to achieve the desired characteristics.

The first steps beyond planar technology were taken by Sherwood Parker with rad hard 3D/active edge sensors.

- Deep trenches into the silicon bulk

Avalanche Diodes use fields that penetrate into the bulk

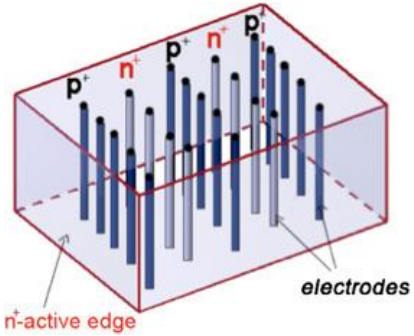
- SPADs, SIPMs, LGADs …

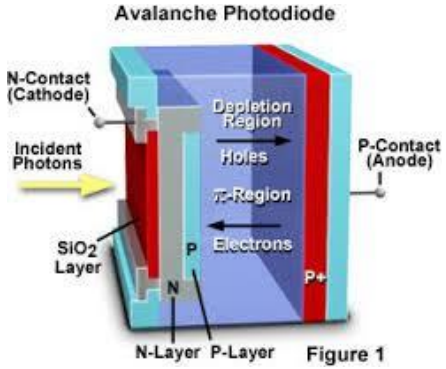
Epitaxial silicon

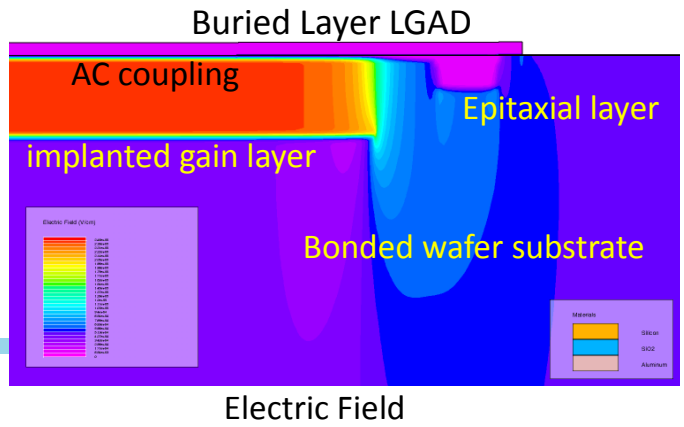
- CMOS MAPS built on an epitaxial layer
- Epitaxy can be “graded” to produce the needed dopant profile, buried layers

Wafer bonding

- Bonding of silicon wafers with different characteristics to achieve the required field profiles.







Costs of Information

Silicon strips provide us 2D (X,Z) information

- Large sensors, could be read out at the edges, easier cooling, larger capacitance

Hybrid silicon pixels provide 3D (X,Y,Z) information

- Bump bonded electronics, smaller capacitance, dimensions limited by CMOS reticule

LGADs, small pixels add timing (X,Y,Z,t) information

- Low fill factors (AC), complex fabrication, radiation hardness, complex electronics

3D integrated small pixels with pulse shape can add angle measurement (X, Y, Z, t, θ_x, θ_y)

- Complex signal and electronics, limited dimensions (CMOS), power, thick sensor

Speed and Power

We cannot get around the physics limitations

To achieve ~20 ps resolution we need:

- Low C_L – small pixels, low interconnect cap
- Large signal (LGAD ~ x10-20)
- Large g_m ~ I_{drain} ~ power
- Uniform pulse shape, time walk correction
- Consideration of charge deposit fluctuations – multiple samples, optimum sensor volume

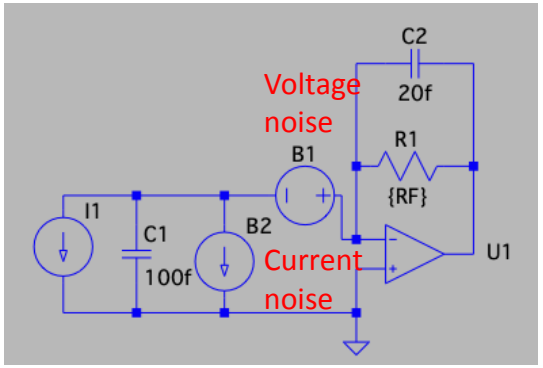
Time resolution

$$\sigma_t \sim \frac{C_L}{\sqrt{g_m t_a}} \frac{\sqrt{t_a^2 + t_d^2}}{Signal}$$

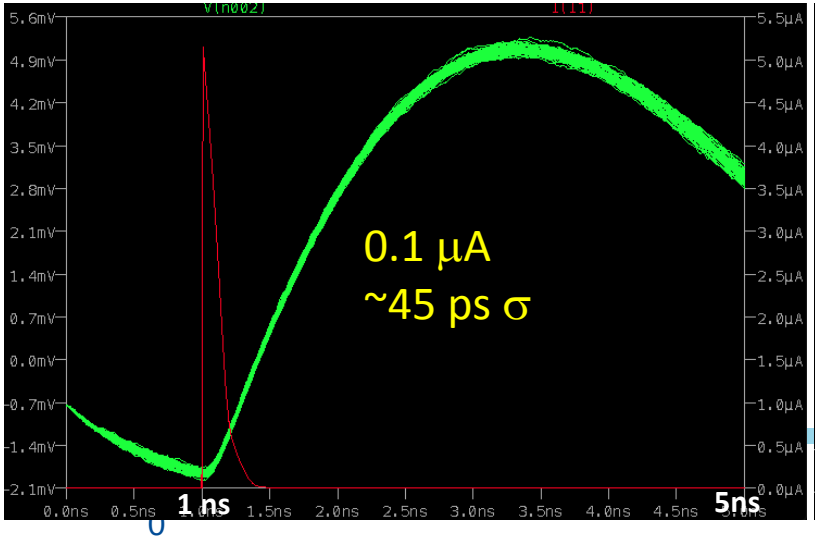
C_L – load capacitance

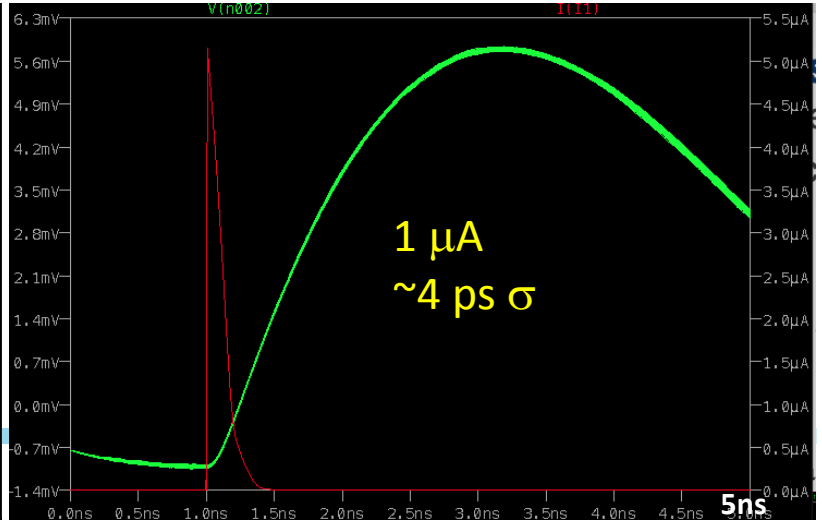
$t_{a,d}$ – amp, det rise time

g_m – input transductance



Simple Preamp noise model - input (red) and outputs (green) for .1μA and 1 μA transistor currents, 100ff Load No Landau fluctuations





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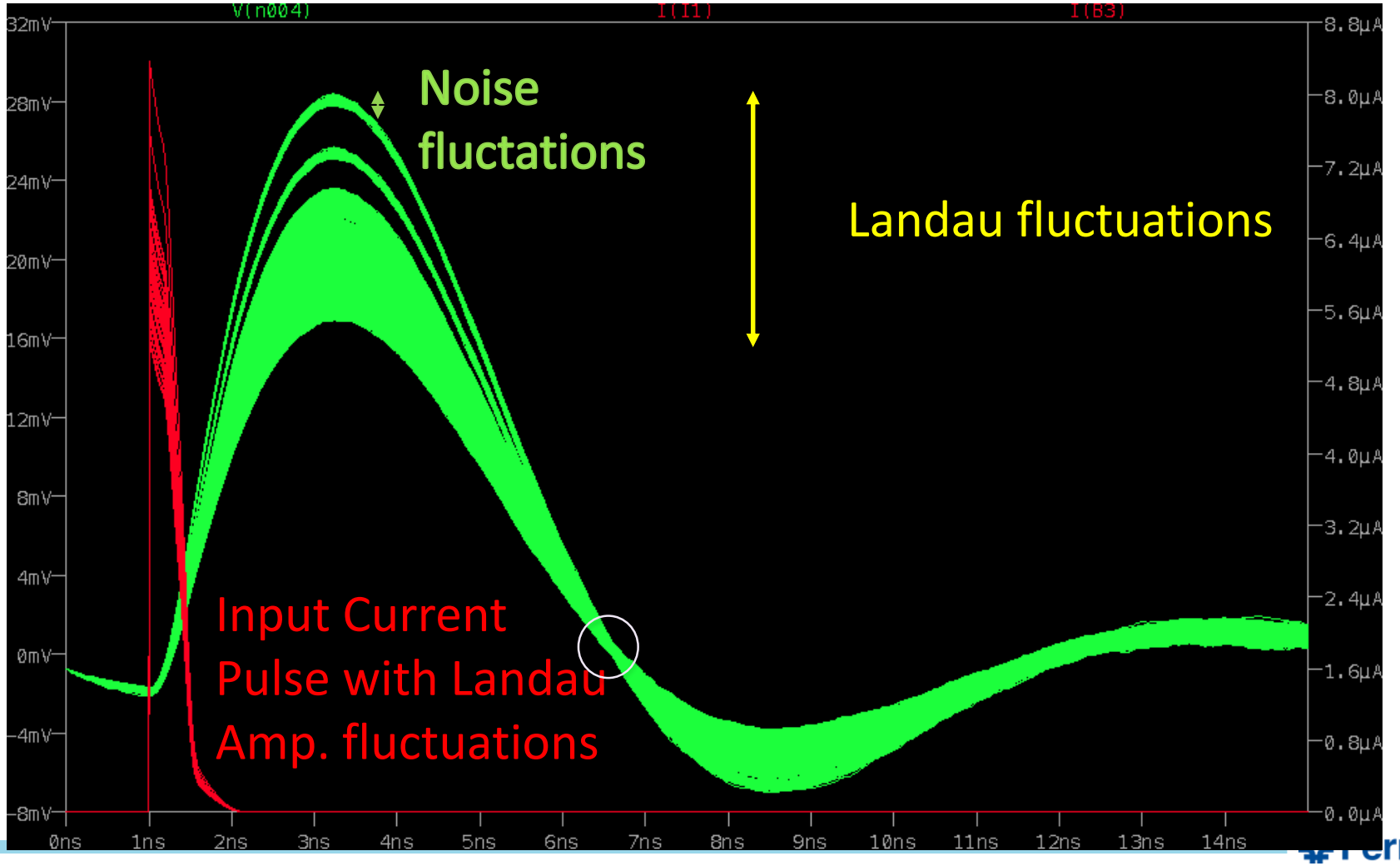
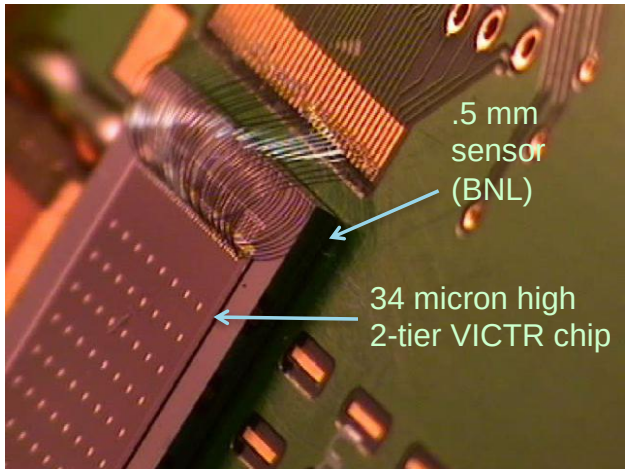
With Landau Fluctuations

- 50 micron thick sensor
- Illustrates time walk corrections needed



Requirements and Tools



We require detectors/readout that are:

- Radiation hard
- Have small pixels (~25 micron for vertex)
- Good time resolution (~20 ps)
- Ability to correlate and filter hits
- Low mass, low to moderate power
- Provide maximum event information with reasonable power

We have developed a toolbox we can use to optimize future detectors

- Sensor design and simulation (TCAD)
- Wafer engineering (epitaxy, wafer bonding, controlled doping, deep etching, defect engineering)
- Internal amplification of signals (LGADs, SPADs, …)
- Electronics and sensor design for rad. hardness
- Dense, multilayer stacking of sensors and electronics (3D)

More sophisticated approaches to tracking

There have been substantial developments in tracking, 3D electronics fast timing and device engineering that should enable MUCH more sophisticated track pulse shape discrimination.

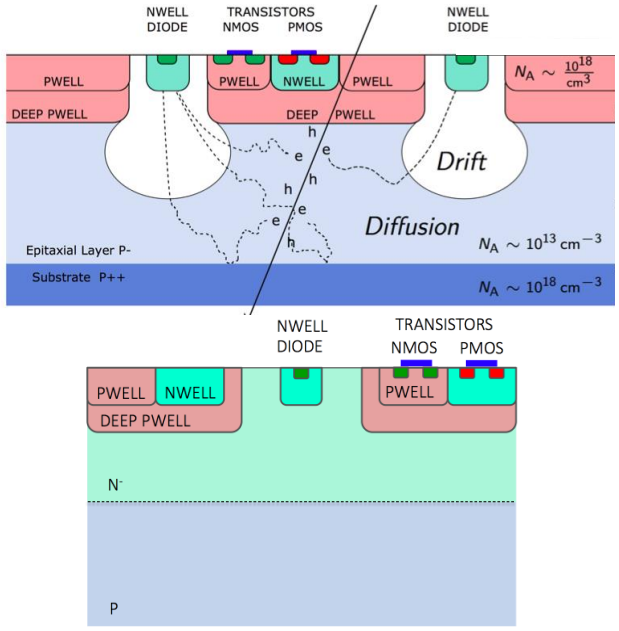
- LGADs to provide internal amplification and fast timing
  - AC LGADs add position resolution and fill factor
- Substrate engineering to manipulate charge motion within a detector
- MAPs for low cost, low mass fine pixel devices.
- 3D electronics to provide low capacitance small pixels with sophisticated processing
  - Integrated angle and timing measurement
  - Can supplement LGADs, MAPS and add local processing capabilities

CMOS MAPS

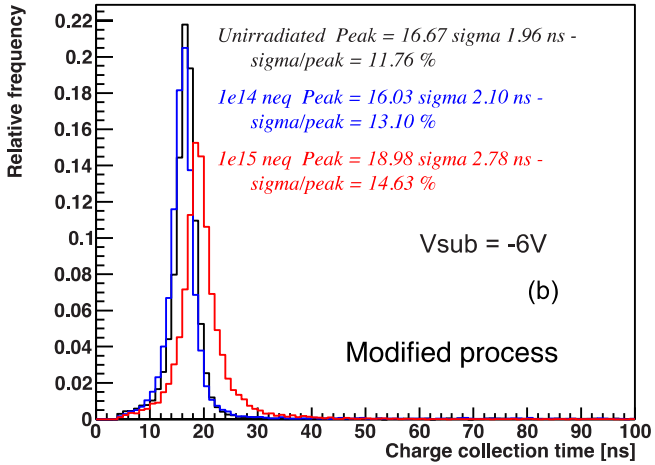
Detector is integrated into the CMOS chip, with the epitaxial layer used as sensor.

- Inexpensive, can be thinned
- Original design was not rad-hard, slow (used diffusion)
- New, depleted designs are much better
  - Deep n- design improves charge collection, rad tolerance by expanding drift region
  - Still not fast enough (rise time ~3-10x silicon diode), big dispersion – uniformity of pulse shape
  - Geometry is awkward for charge collection
- Limited space for on-chip processing

This is an important option with real prospects for development. Continued collaboration with foundries is essential.



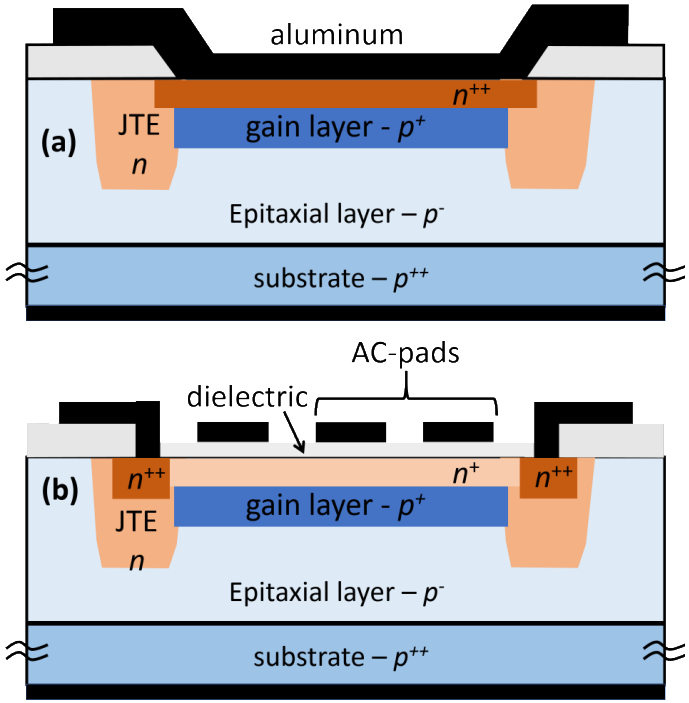
H. Pernegger *et al* 2017 *JINST* **12** P06008



LGADs / AC LGADs

Low gain avalanche diodes now being used for timing layers for CMS and ATLAS have excellent timing capability. But:

- Current versions must have large pixels large due to the areas needed for HV edge termination
- They are not very radiation hard due to low density implants



Gabriele Giacomini et al

AC-LGADs solve the pixel size problem by adding resistive and capacitive layers and moving the edge terminations from the pixels to the edge of the device.

- Must still be bump or 3D bonded to the readout electronics
- Small pixels need lots of power for time resolution

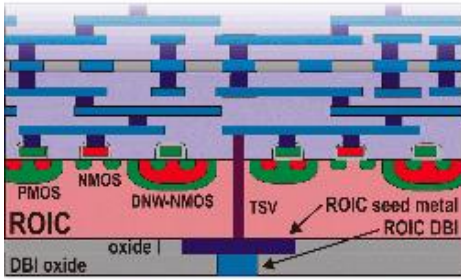
Buried gain implants can increase gain layer density and improve radiation hardness. R&D is proceeding on these areas at FNAL/BNL.

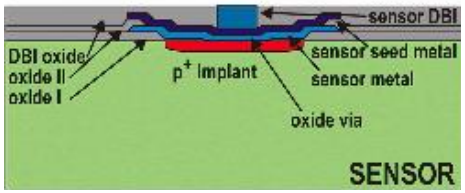
3D Integration (NOT 3D sensors)

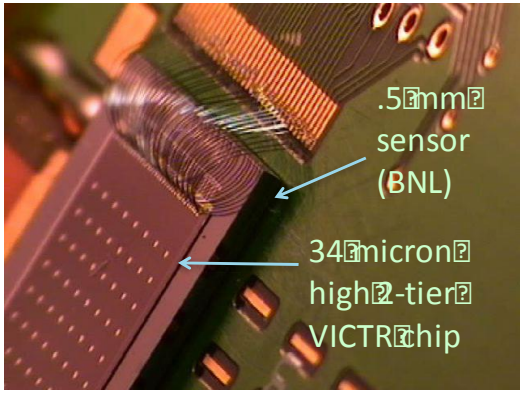
A three-dimensional integrated circuit (3D-IC) structure is composed of two or more layers of active electronic components using horizontal intra-tier and vertical inter-tier connectivity (TSVs). We pioneered this for HEP circa 2010-12.

- Very fine pitch (~3 micron)
- Rad hard
- Separate optimization of sensors and electronics
  - Sensor optimized for speed and resolution (LGAD or CMOS)
- Multiple layers of electronics would allow processing of fields of pixels – important for angle and charge deposition extraction

Can be combined with MAPS, LGADs … for optimal combined detector system with complex processing.







Current Pulse Based Detectors

The current generation of detectors typically measures total charge, and perhaps arrival time, and pulse width.

- There is much more information available during charge drift if thickness>pixel pitch

The current pulse in each electrode reflects charge motion deep in the detector

- Can use the current pulse to measure track angle, depth of charge deposition
- Pixels *that do not collect* charge have information
- Depends sensitively on the "weighting field"

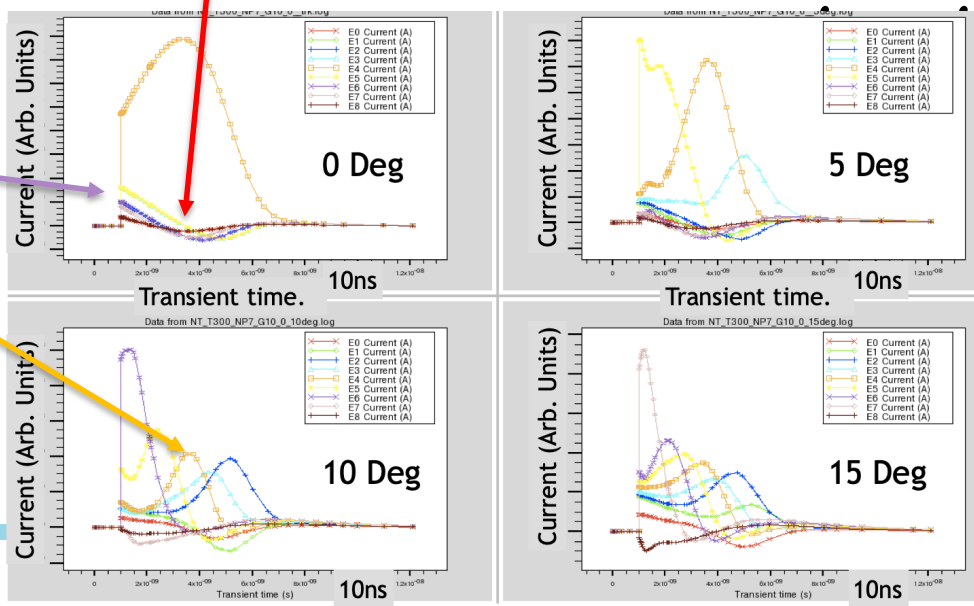
If we can utilize this information we can measure:

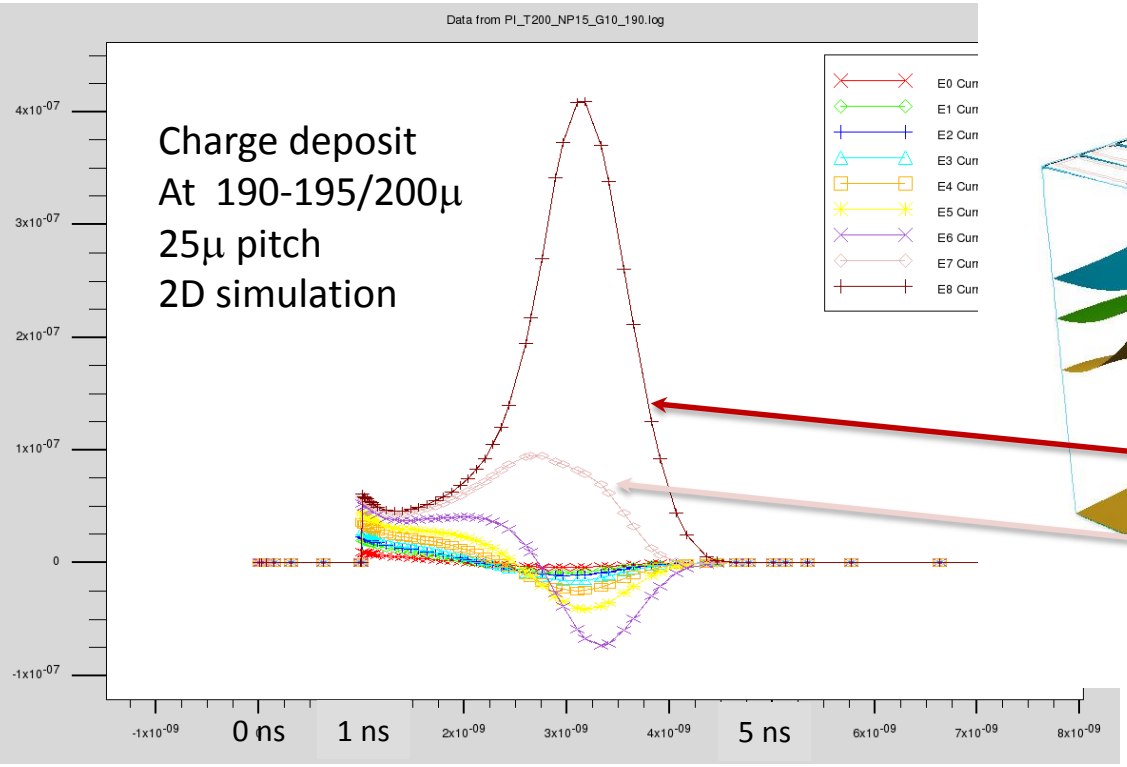
- time from initial rise,
- Angles from the pattern of currents in central and neighbor pixels.

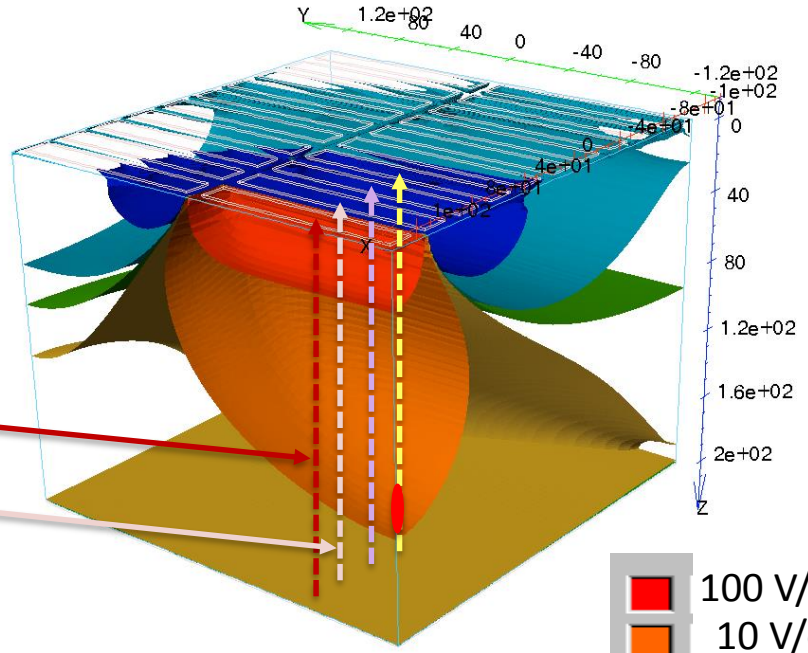
6D – X, Y, Z, Time , θ_x, θ_y

Remember – this is 20-30 years from now

TCAD Simulations $i = -q\vec{E}_w \times \vec{v}$

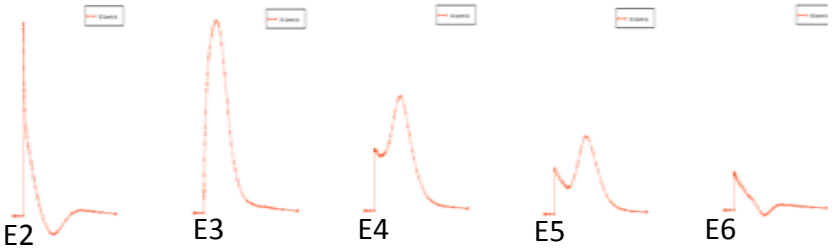


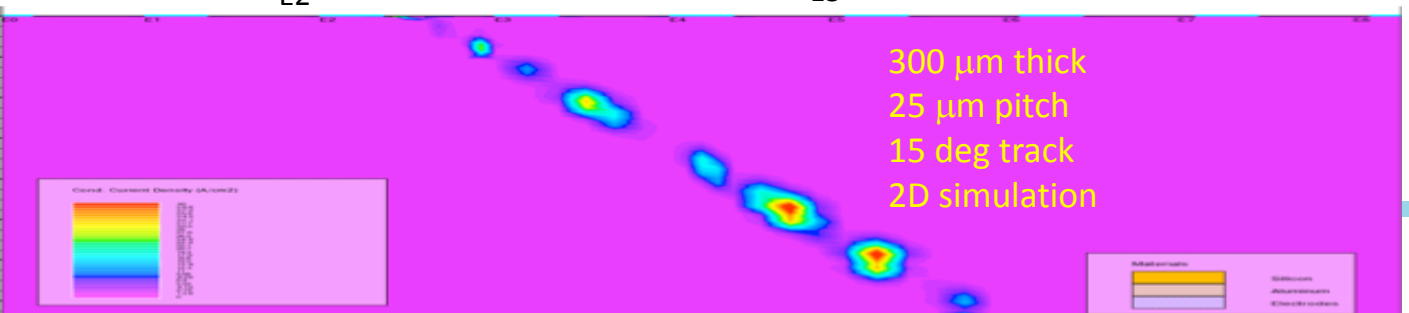




Weighting field for
25 x 125 x 200
micron Pixel array

Angled Track





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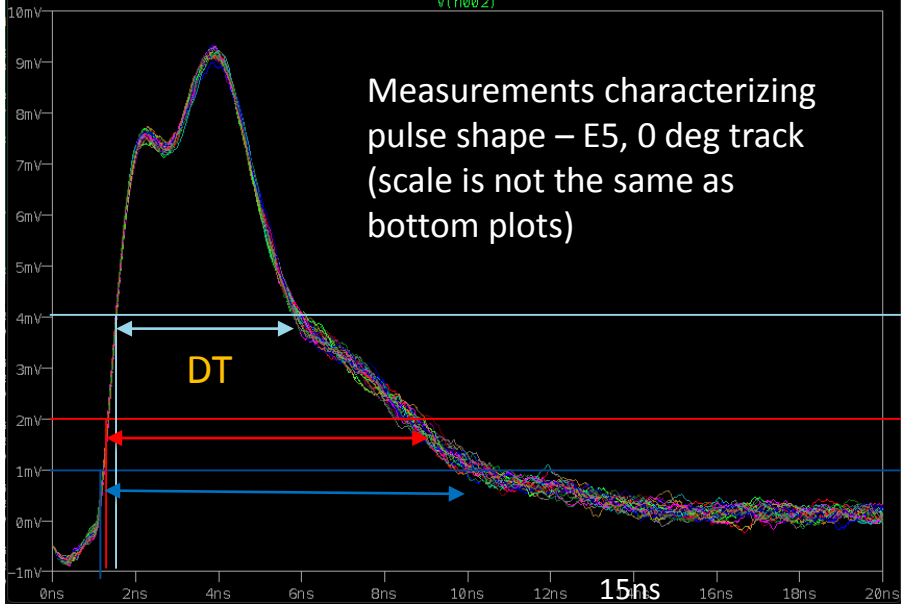
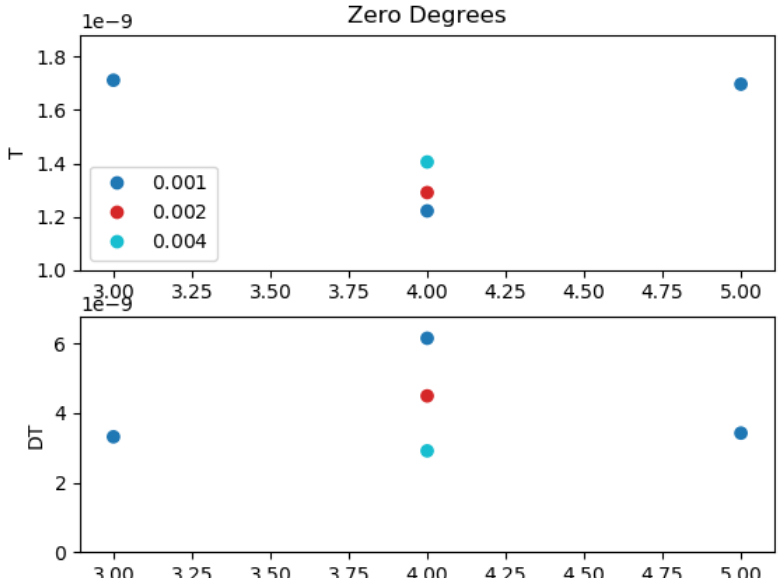
Small Pixel Study.

Assume each 25 μm pixel has 3 discriminator levels – measure start time and total width

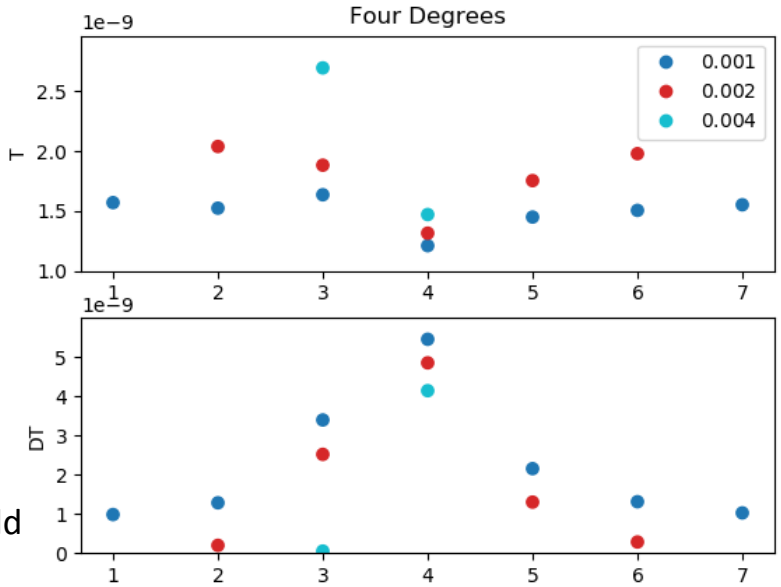
- Pulses are measured after preamplifier shaping
- Neighbors enabled by large central signal
- Complex resulting pulse patterns.



Direct impact on central Pixel – little charge spread to other electrodes

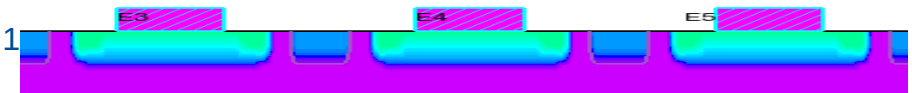


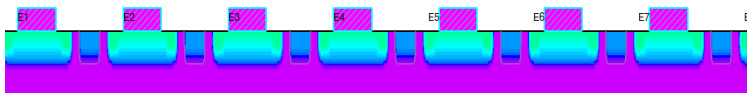
More electrodes now have signal
DT pattern related to track direction



Start time

Time over threshold

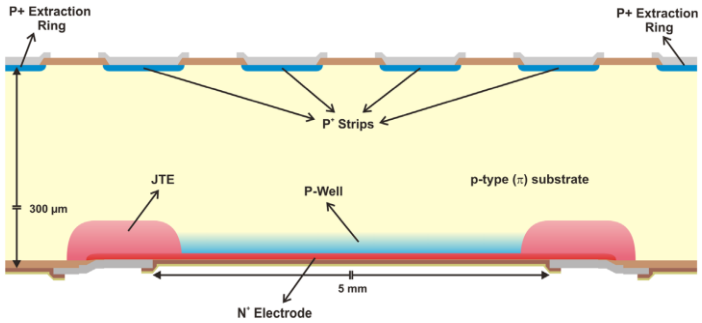


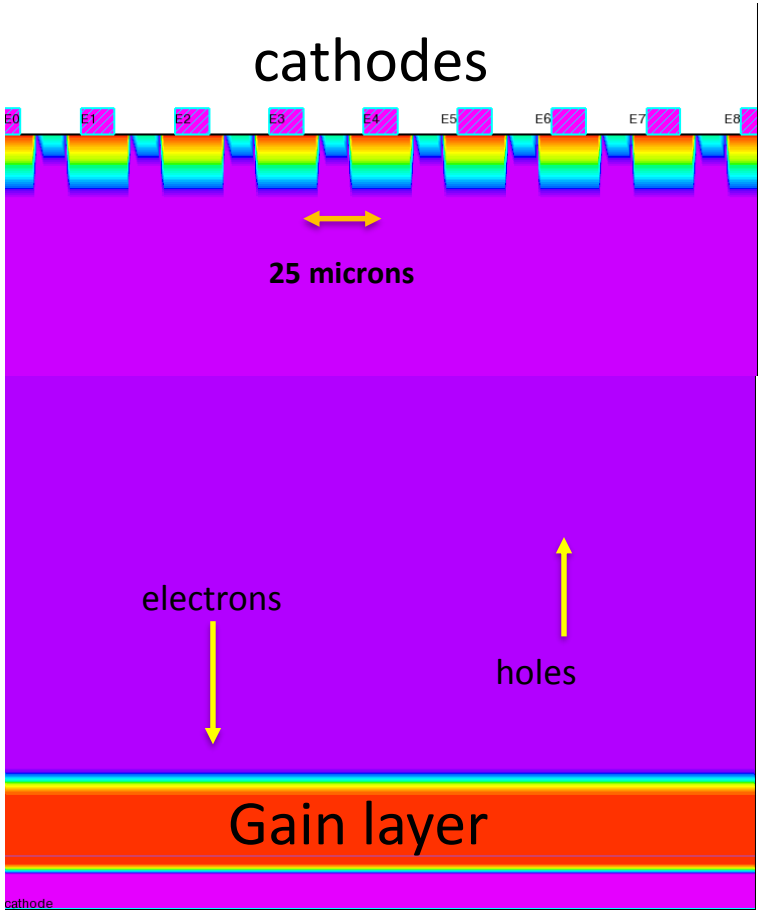


Double Sided (inverse) LGAD – Example of combining Technologies

Low Gain Avalanche Diode with fine pixels on the hole-collecting side (G. Pellegrini et al …)

- Anode can provide timing with coarse pitch
  - Lower total power and complexity
- Cathode subdivided into small pixels
  - Records “primary” hole collection, then holes from gain region – double peak that reflects charge deposition pattern
  - Lower power due to large signal from the gain layer
- Resulting current pattern can be used to measure angle and position.
- A thicker detector can be optimized to measure angle or charge deposit location at some sacrifice to time resolution





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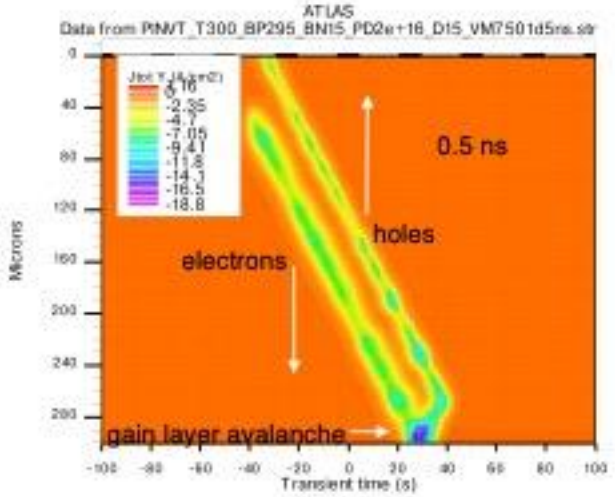
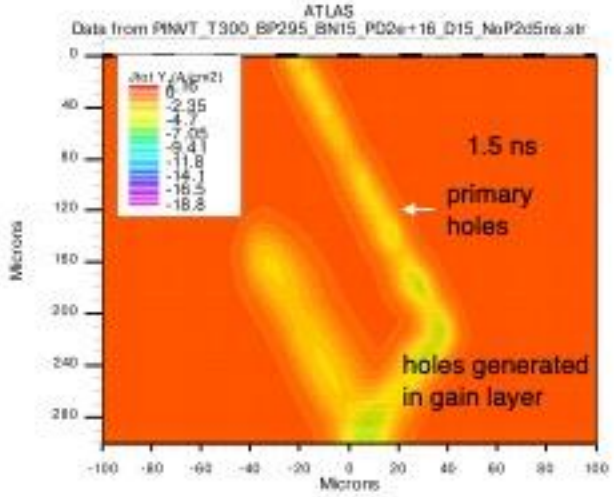
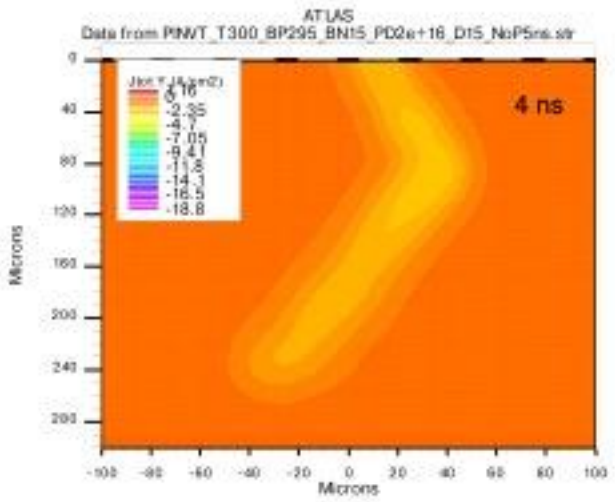
Double Sided LGAD Simulation

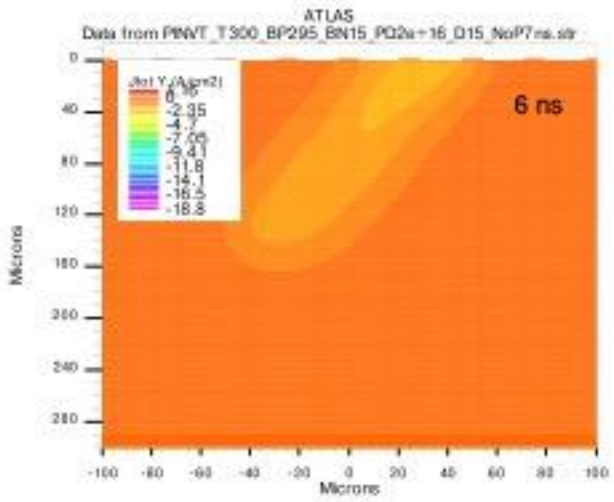
Use anode for timing, cathodes for pulse shape discrimination. Essentially a silicon TPC with gain. Time scale ~ 10 ns

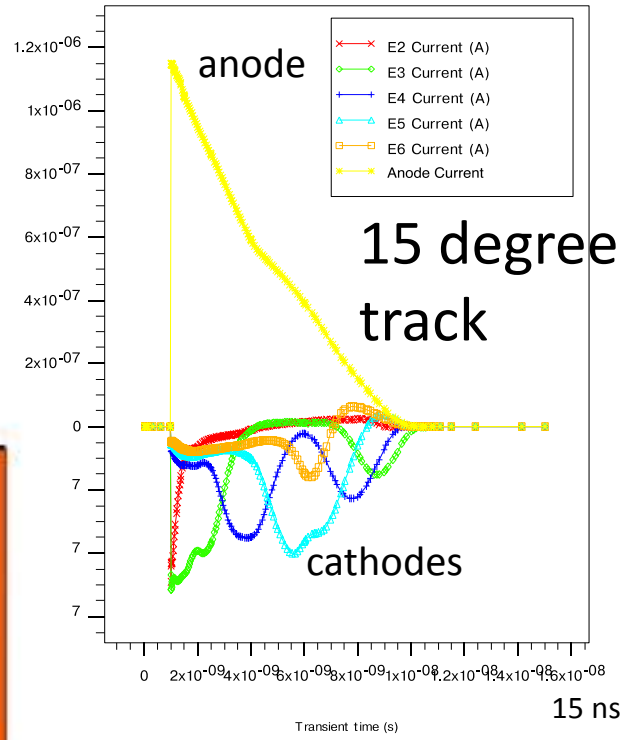
15 degree track detector internal current distributions



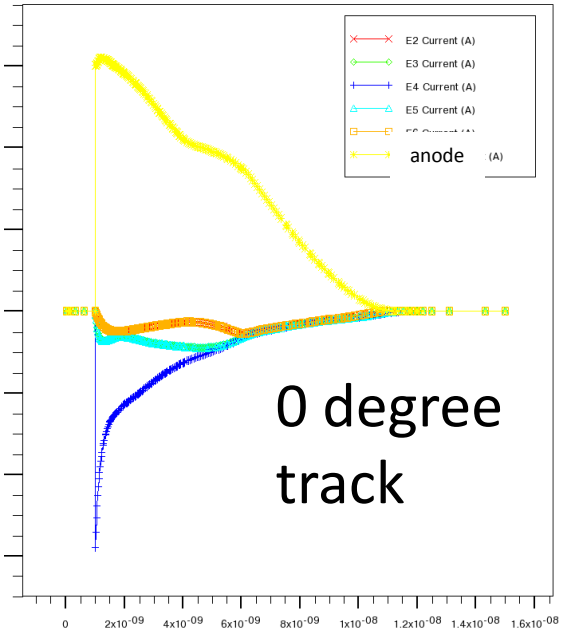








15 ns

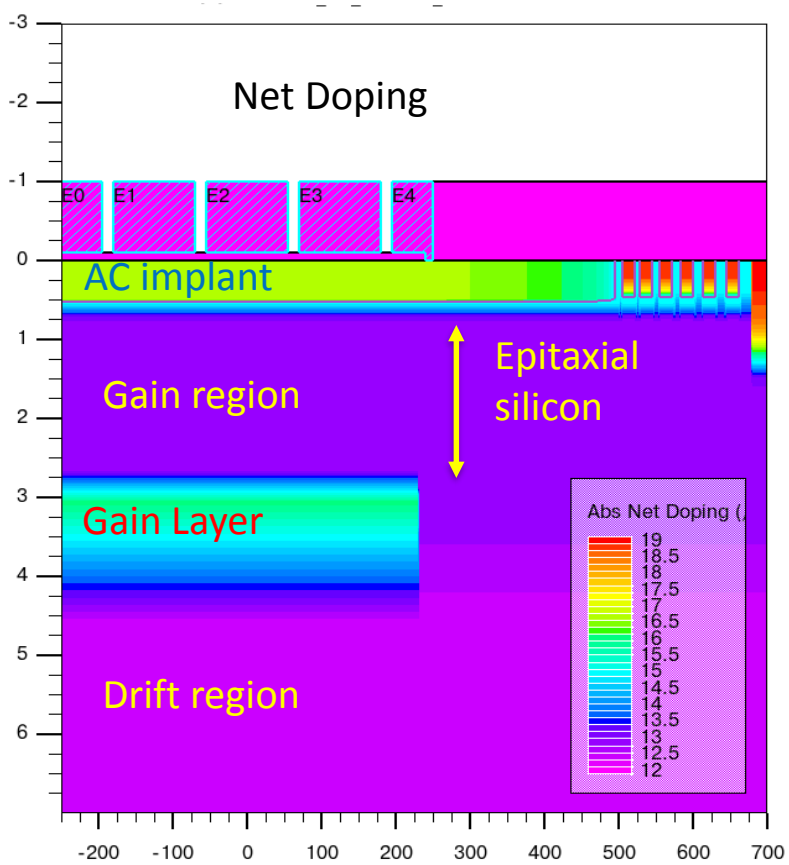


Buried layer LGAD

We can combine technologies to optimize the performance of LGADs. We (FNAL, BNL, Cactus Inc) are prototyping a device

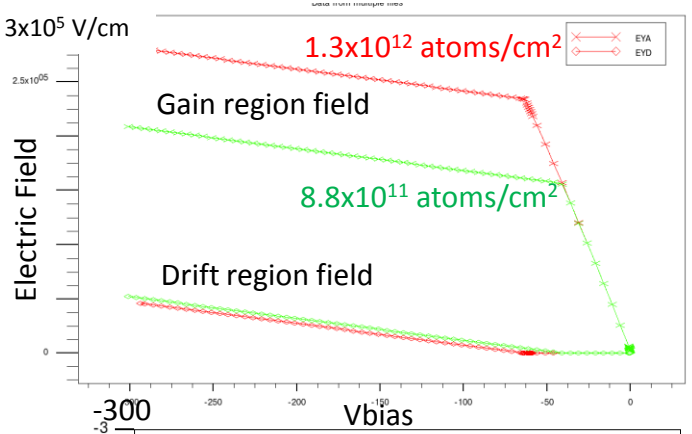
- 50 μ drift region FZ wafer Si-Si bonded to the substrate.
- Patterned gain layer implant – removes need for junction termination extension
- 3-4 μ epitaxial gain region over gain layer
- AC coupling top layer

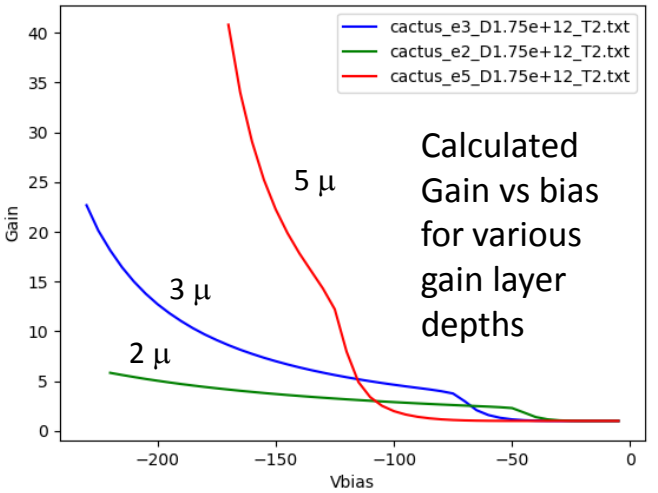
This design allows independent control of the depth of the gain layer; a thin, high density gain layer implant.



Engineering the Substrate – Buried layers, epitaxy

By engineering the substrate we can design the buried layer LGAD for specific gain, operating voltage, drift field





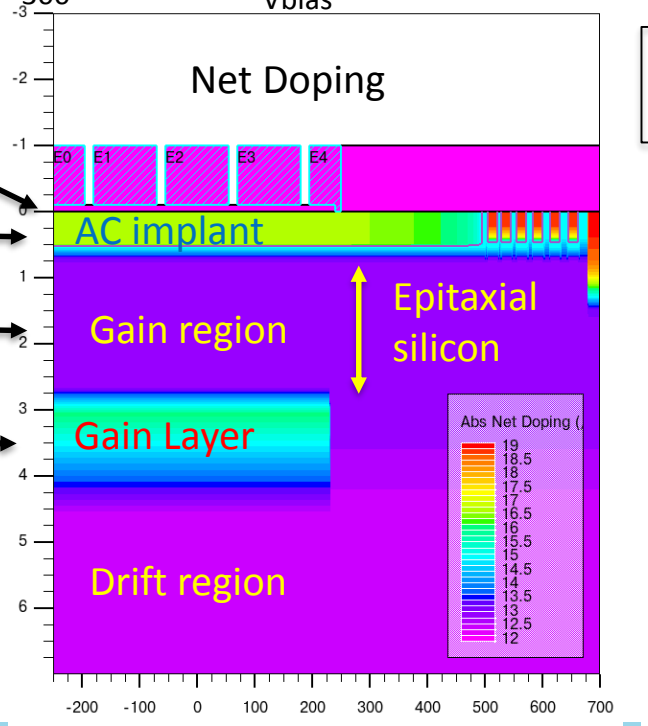
AC oxide – RC time, coupling

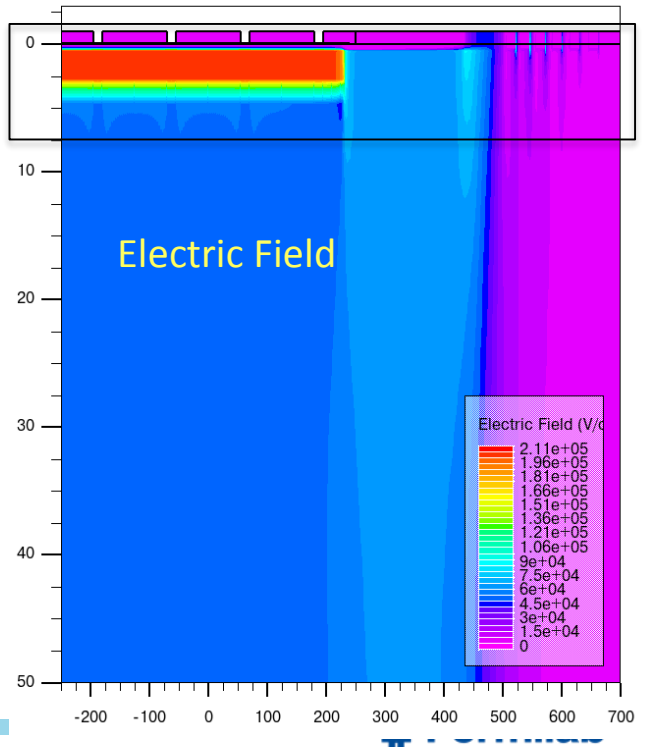
AC layer doping – charge sharing

Gain region – Gain characteristic ~ thickness

Buried gain layer (implanted)

- Total dopant – ratio of drift to avalanche field
- Dopant density – radiation hardness





Summary

Silicon technology has, in the past 40 years, revolutionized experiment particle physics capabilities.

This is continuing with developments of 3D, active edge sensors, LGADs, 3D sensor-electronics integration, CMOS MAPS and process integration

This has gone on for 40 years, and it is a good bet that FCC technologies will grow from current seeds.

"If you can look into the seeds of time, and say which grain will grow and which will not, speak then unto me.

William Shakespeare - Act I, Scene iii of Macbeth (Banquo to the witches)

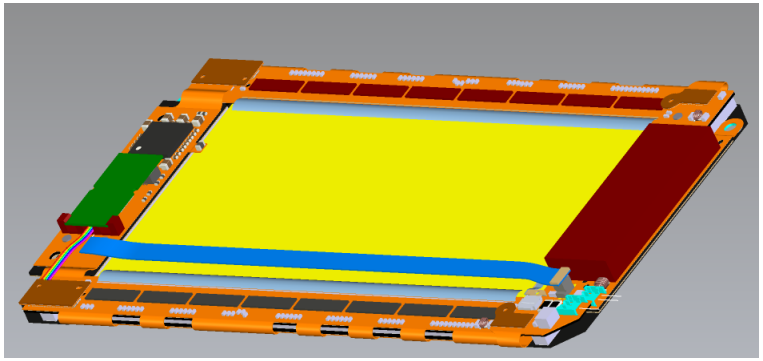
Charge Pattern Measurement and Inter-Detector Communication

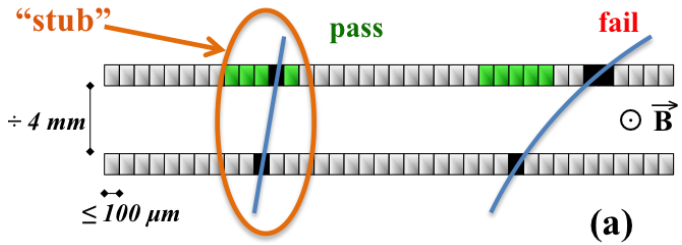
Angles can be measured by correlating hits between adjacent sensors. This is the approach used for the CMS track trigger.
The PS module uses short and long strips and is essentially a 1D problem. Pixels are 2D and there is the additional complexity of encoding and decoding transmitted hit positions on the target sensor IC to get hit information where it needs to be for position correlation. This data transmission and sorting will add power and complexity.

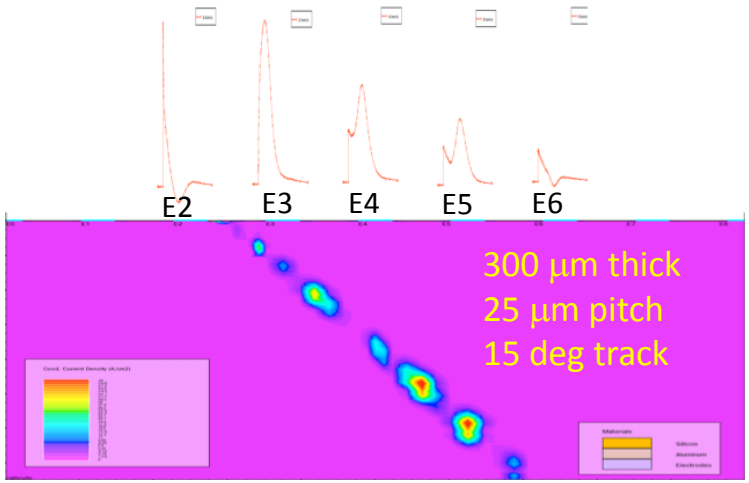
- We should try to do as much as possible local on-detector

A local (one-sensor) track angle filter could be very valuable.

- Given that we already are contemplating small pixels we can estimate angle and charge pattern if the readout pitch/detector thickness is small (~x10)

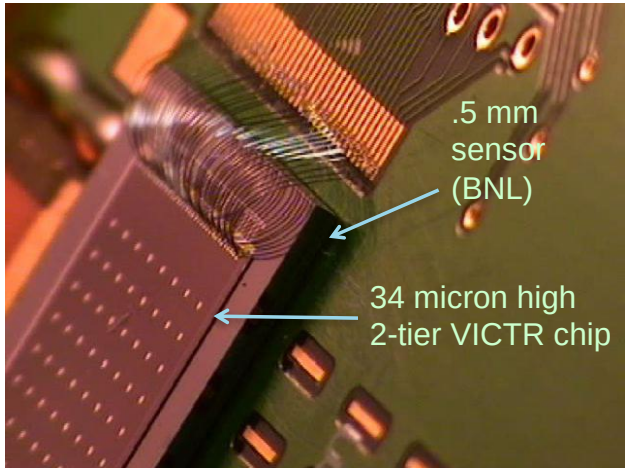


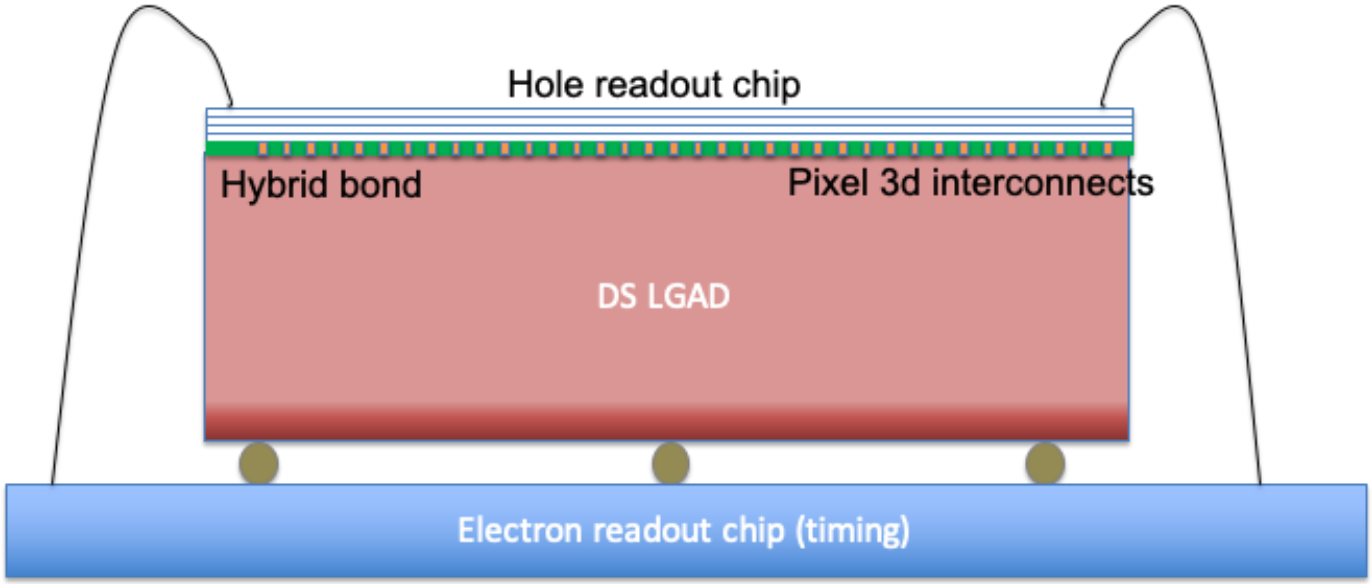




Implementation

- 3D Assembly with electron and hole ROICs
- This is similar to VICTR from the 2012 3D run





Using Current Pulse Shapes

3D allows for small pixels with small associated load capacitance. Small pixels with ~25x smaller capacitance should have similar timing performance to LGADs.

- Should be more radiation hard, but more power with denser electronics

The current pulse shape reflects charge motion deep in the detector

- Can use the current pulse to measure track angle, depth of charge deposition

Jitter

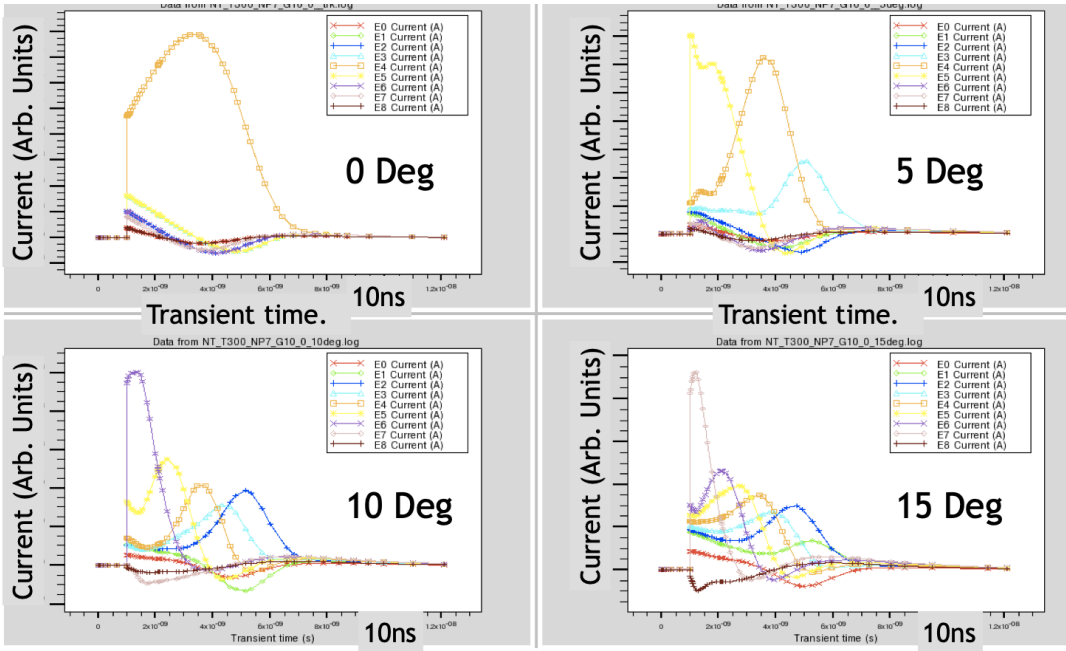
$$\sigma_t \sim \sigma_{noise}\left(\frac{\partial V}{\partial t}\right) \sim t_r\left(\frac{Noise}{Signal}\right)$$

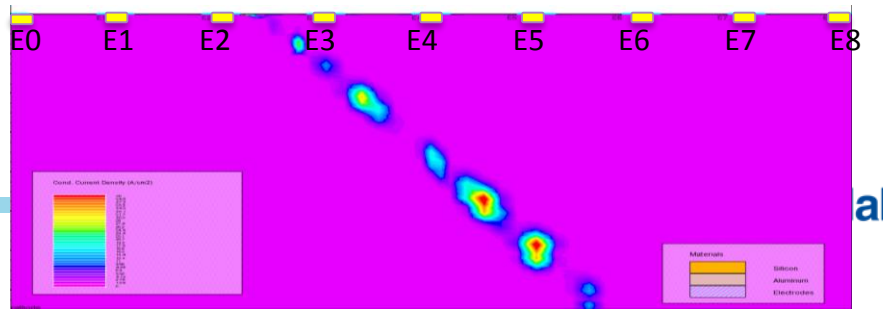
Front end noise

$$\sigma_n^2 = \frac{C_L^2(4ktA)}{g_m t_a}$$

Time resolution

$$\sigma_t \sim \frac{C_L}{\sqrt{g_m t_a}} \frac{\sqrt{t_a^2 + t_d^2}}{Signal}$$





2.5D & Chiplets

Known good die can be combined on an active or passive interposer, with or without TSVs

- Interconnect on silicon substrate
- Depends on microbump arrays
- Build complex assemblies with specialized ASICs
- A better way to implement
  - Front end amplification
  - Optical data transfer
  - Power conversion
  - Data concentration and filtering
  - Trigger generation
- A possibly more elegant solution for i.e. the CMS PS module (3 chip-on-flex hybrids)