DEPFET pixel sensors: Belle II and Beyond

▷ PXD at Belle II
  ▷ Construction, performance, and lessons learned

▷ Outlook – the way forward

DEPFET PXD Collaboration
and the
team at the Semiconductor Laboratory of the Max Planck Society
Higher luminosity, KEKB $\rightarrow$ SuperKEKB
- Higher event rate, higher background, higher radiation damage ...
- See Leo’s talk from Tuesday afternoon

Detector upgrade $\rightarrow$ Belle II
- New PID components, upgraded CDC ...
- New VXD: 4 layers DSSD + 2 DEPFET pixel layers
### Belle II PXD

<table>
<thead>
<tr>
<th></th>
<th>L1</th>
<th>L2</th>
</tr>
</thead>
<tbody>
<tr>
<td># ladders (modules)</td>
<td>8 (16)</td>
<td>12 (24)</td>
</tr>
<tr>
<td>Distance from IP (cm)</td>
<td>1.4</td>
<td>2.2</td>
</tr>
<tr>
<td>Thickness (μm)</td>
<td>75</td>
<td>75</td>
</tr>
<tr>
<td># pixels/module</td>
<td>768x250</td>
<td>768x250</td>
</tr>
<tr>
<td># of address and r/o lines</td>
<td>192x1000</td>
<td>192x1000</td>
</tr>
<tr>
<td>Total no. of pixels</td>
<td>3.072x10^6</td>
<td>4.608x10^6</td>
</tr>
<tr>
<td>Pixel size (μm^2)</td>
<td>55x50</td>
<td>70x50</td>
</tr>
<tr>
<td></td>
<td>60x50</td>
<td>85x50</td>
</tr>
<tr>
<td>Frame/row rate</td>
<td>50kHz/10MHz</td>
<td>50kHz/10MHz</td>
</tr>
<tr>
<td>Sensitive Area (mm^2)</td>
<td>44.8x12.5</td>
<td>61.44x12.5</td>
</tr>
</tbody>
</table>
the DEPFET all-silicon module

DCDB (Drain Current Digitizer)
Amplification and digitization
- UMC 180 nm
- 256 input channels
- 8-bit ADC per channel

DHPT (Data Handling Processor)
First data compression
- TSMC 65 nm
- CM and pedestal correction
- Data reduction (zero suppression)
- Drives data link

SwitcherB
- AMS/IBM HVCMOS 180 nm
- Gate and Clear signal
- 32x2 channels

Pixel array operated in „rolling shutter“ mode, 20µs/f
- Only 4/768 rows active a time → low power in active area
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x-ray picture of fully assembled module
0.21% of $X_0$
how to make thin DEPFETS

- thickness of the sensitive area is an almost free parameter
- full DEPFET technology in thin area
- thin area supported by a monolithically integrated silicon frame
Flip Chip of ASICs (~240°C):

- Bumped ASICs have the same solder balls (SnAg)
  - DHP bumping at TSMC, DCD bumping via Europractice
  - SWB bumping on chip level
- Flip Chip of PXD modules on custom made support plates

SMD placement (~200°C):

- Passive components (termination resistors, decoupling caps)
- Dispense solder paste, pick, place and reflow

Kapton attachment (~170°C), wire bonding:

- Solder paste printing on kapton,
- Wire-bond, wedge-wedge, 32 µm Al bond wires
module 0
71 modules attached to pre-tested kapton cables
- Module assembly yield ~97% (after rework of a 8 modules)
- ~56% contingency

collaborative effort (Bonn, Göttingen, HLL, MPP, IFIC Valencia)
- script based, automated procedure
- optimize/confirm ASIC and DEPFET parameters
  - linear response of the ADC, pedestal compression
  - Off-module link of DHP
- charge collection (DEPFET voltages: Drift, HV, Clear-Off)

Damage and repair after testing
- 2 x kapton cables revealed shorts (modules ok after kapton exchange)
- 1 x module: mechanically damaged (can not be depleted)
- 2 x modules: SwitcherB damaged at test

After characterization: Sr90 spectrum (Bonn Uni)

- 291 unresponsive single pixels
- 251 noisy pixels
- 99.85% active pixels
ladder assembly and installation

- Join two modules to a ladder → “ladder gluing”
  - v-grooves for small ceramic inserts on the back side → Reinforcement of the joint
- **Yield issue**: out of 17 assembled ladders, 5 were lost due to damage at assembly
  - Resolved by now
- **Install de-scoped PXD** to meet the schedule for the start of data taking (March 2019)
  - Full L1 (8 ladders) and 2/12 ladders in L2
- **Completion of PXD (“PXD2”)** early 2022 with new modules
PXD in operation in Belle II since March 2019 with good performance

First application of DEPFET sensors in HEP!

S/N between 40 and 50, stable over time and with good homogeneity

Narrow and stable pedestals and noise

Impact parameter resolution close to expectations

data: $\sigma(d_0) = 14.2 \, \mu m \leftrightarrow 12.5 \, \mu m$: simulation
Damage due to beam losses/incidents

- Origin of beam losses not completely clear (beam-dust events? machine glitches?)
- Resulted in collimator damage, quench of the QCS magnet system ...
- Huge instant radiation dose of about 300 rad in \(~40 \mu s\) in the PXD
  - Permanent damage of entire rows \(\rightarrow\) "dead", inefficient regions
  - Overall efficiency loss \(~2.5\%\) at the moment
- Origin of PXD damage traced back to SEE in the Switcher HV-CMOS chip
  - Reproduced at MAMI accelerator in Mainz
    - Electron pencil beam scanned over DEPFET array and Switcher chip

Mitigation (from PXD side)

- Accelerate beam abort signal and power-down of modules
- Root cause in the switcher chip understood (needs schematic change and final verification, though)
Backplane (HV, depletion) is increasing from tens of µA to >1mA
- Most affected modules are currently in +x direction
- This is where the background is 2x higher ...

Module performance not affected, noise and signal stable
- Also negligible contribution to overall power consumption

Issue: the power supply system is not designed to supply that high current and needs upgrade
- Details are currently being discussed

Root cause is at the moment under investigation
- Combination of radiation effects and module/sensor properties (?)

Dedicated electron and photon irradiation campaigns of representative smaller DEPFET arrays are scheduled

Meanwhile: operation in Belle II and construction of PXD2 continues
Improvements: back to the basics

\[ g_q = \frac{dl_D}{dQ} = \frac{g_m}{C_{ox}} \quad \rightarrow \quad g_q \sim \frac{1}{L^{1/2}} \quad g_q \sim \frac{1}{W^{1/2}} \quad g_q \sim t_{ox}^{1/2} \quad g_q \sim I_D^{1/2} \]

(Ideal transistor theory - neglecting short channel effects)

\( g_q \) for of the latest DEPFET generation (large Belle II sensors): \(~0.5\) nA/e
improving $g_q$

- Better $g_q$ by reducing $L$ (obvious)
  - Limitation by avalanche generation at Drain
  - Higher noise, S/N

- Next generation of DEPFETs (A. Bähr)
  - Shaping of drain implant to reduce el. field

- Possible improvement (simulation)
  - 500 pA/e$-$ → 2000 pA/e$-$ (L~1µm)

- Test project for next generation DEPFETs scheduled
  - Various L, implant parameters, improving litho ...
  - DEPFETs with “SuperGq” under way

- Driving application is spectroscopy
  - Fast read-out with sub-electron noise
opportunities – simple scaling

- Better $g_q$ means in tracking applications
  - Higher MIP signal $\rightarrow$ thinner sensitive area
  - Smaller bias current $\rightarrow$ less power in pixel area
  - Thinner gate isolator $\rightarrow$ higher radiation tolerance

- Effect of TID on DEPFET operation $\rightarrow$ threshold voltage shift of the external gate
  - Has to be compensated, i.e. $V_{\text{gate}}$ (and Clear_gate) need adjustment with increasing TID
  - In principle no problem, performance of the sensors changes only marginally

\[ g_q \sim I^\frac{1}{2} \]

As an example:
- Reduce $L$ and $t_{ox}$ by 2x $\rightarrow$ $g_q$ is 2x better
- At the same time $\Delta V_{th}$ is 4x better

\[ g_q \sim \sqrt{\frac{t_{ox}}{L^3}}, \quad \Delta V_{th} \sim t_{ox}^2 \]
Speed Considerations

- DEPFET sensor is operated in rolling shutter mode (row wise read-clear ...)
  - Minimize power consumption in sensitive area
    - ~0.5 W (1000 pixels on) in sensitive area
    - ~1 W for the Switchers
    - ~7.5 W at end-of-stave (mostly ADCs of DCD)

- The price to pay is speed
  - PXD has 192 gate lines (four-fold), read in 20μs → ~100 ns for read-clear cycle

- Speed improvement possible with faster processing for each row (“gate”)
  - ASIC related limitations → faster ADCs possible (parallel processing), also reduction of bits (binary?)
    - Currently we have 8 bits → better resolution than just binary read-out
  - Settling time of signals on matrix → faster switcher & reduce RC constants on matrix (metal system)

- Overall, in this configuration, an improvement of **more than 2x or 3x not realistic**

- Is this the end? Or can we change something on the module?
The basic idea – stick to the proven all-silicon module

PXD
- 1000 DCD channels
- 192 SWB channels

90° turn: 3x speed
- 3072 DCD channels
- 62 SWB channels

Another 2x possible with faster DCD \(\Rightarrow\) \(\sim\)3\(\mu\)s per frame in reach
What do we need for this?

- Improve DEPFET pixel cell
  - Higher \( g_q \) ....

- Improvement of the metal system on the module
  - technology development planarization (started)
  - 3\textsuperscript{rd} Alu layer on module
  - Possibly 2\textsuperscript{nd} Cu layer

- New ASICs \( \Rightarrow \) go for the best available technology – profit from huge micro-electronics industry
  - DCD: smaller, more channels, less ADC bits, faster, driving capability .... \( \Rightarrow \) has to be slim, thin, small bump pitch ...
  - SWB: improved driving capabilities, more channels .. \( \Rightarrow \) has to be thin, small bumps (material)
  - module controller chip (off-module driver, sequencer ..) and voltage regulators

- Assembly
  - Basically business as usual, bit of R&D for flip chipping of thin ASICs to balcony and thin sensitive region
  - Technology is under control

- ... we are not starting from scratch! One important part already quite advanced ...
Micro-channel cooling

A spin-off of SOI approach: thinned all-silicon module with integrated cooling

- idea: integrate channels into handle wafer beneath the ASICs
- channels etched before wafer bonding → cavity SOI (C-SOI)
- full processing on C-SOI, thinning of sensitive area
- micro-channels accessible only after cutting

Small team within DEPFET PXD: Bonn, HLL, IFIC

2nd iteration already, see other talks on this
In Summary

- Belle II PXD: the first full vertex detector based on DEPFETs!
  - Overall performance of the modules meets the requirements at SuperKEKB
  - There were a few surprises, many lessons learned
    - One of the most important ones: have to make the system more user friendly!

- New DEPFETs with improved properties are in the pipeline
  - Higher amplification \( (g_q) \) → thinner sensors with excellent S/N
  - More radiation tolerant
    - Thinner gate dielectrics

- Changing the read-out direction together with the design of new read-out and steering ASICs is the obvious way to increase the frame rate

- Deployment of micro-channel cooling opens the way to an highly integrated module with much better performance and minimal material budget

- Finally: a module is not necessarily square or flat ...
Backup
Design of current PXD modules with moderate changes

- Balcony wider for DCDs: 5 mm
- Thinner sensitive area: 50 µm and 30 µm
- Frame in standard thickness 450 µm (was 525 µm for PXD)
- Copper 100% on balcony and 10% in sensitive area: 5µm
- 10k bumps on balcony
- DCDs thinned to 100 µm and 50 µm
- “Sub-millimeter channels” in balcony with H2O
First prototypes with integrated resistive heaters

- DRIE etching of handle wafer
- CSOI wafer with integrated resistors
- Module after cutting
- Detail: inlet for the cooling fluid

~350 µm
Next steps

Improve fluidics, temperature homogeneity, flip-chip to micro-channel area .... More to come, stay tuned
In-plane supply of the cooling liquid

- 3D printed adapters also for mechanical support
- Self-aligned to channel openings
- Initial simple approach: „gluing“
Low flow rate (~1l/h) and low pressure (<1bar) are enough to remove the heat generated in the front end.

Maximum power dissipation for a ΔT of 10 K as a function of the flow rate:
- Temperature stable up to a power density of 25 W/cm²
- To remove 22W at the end of stave 3l/h are needed for a ΔT of 10K
- Still low pressure: up to 1.5 bar
- Good agreement with the FE simulation within an error of 10%