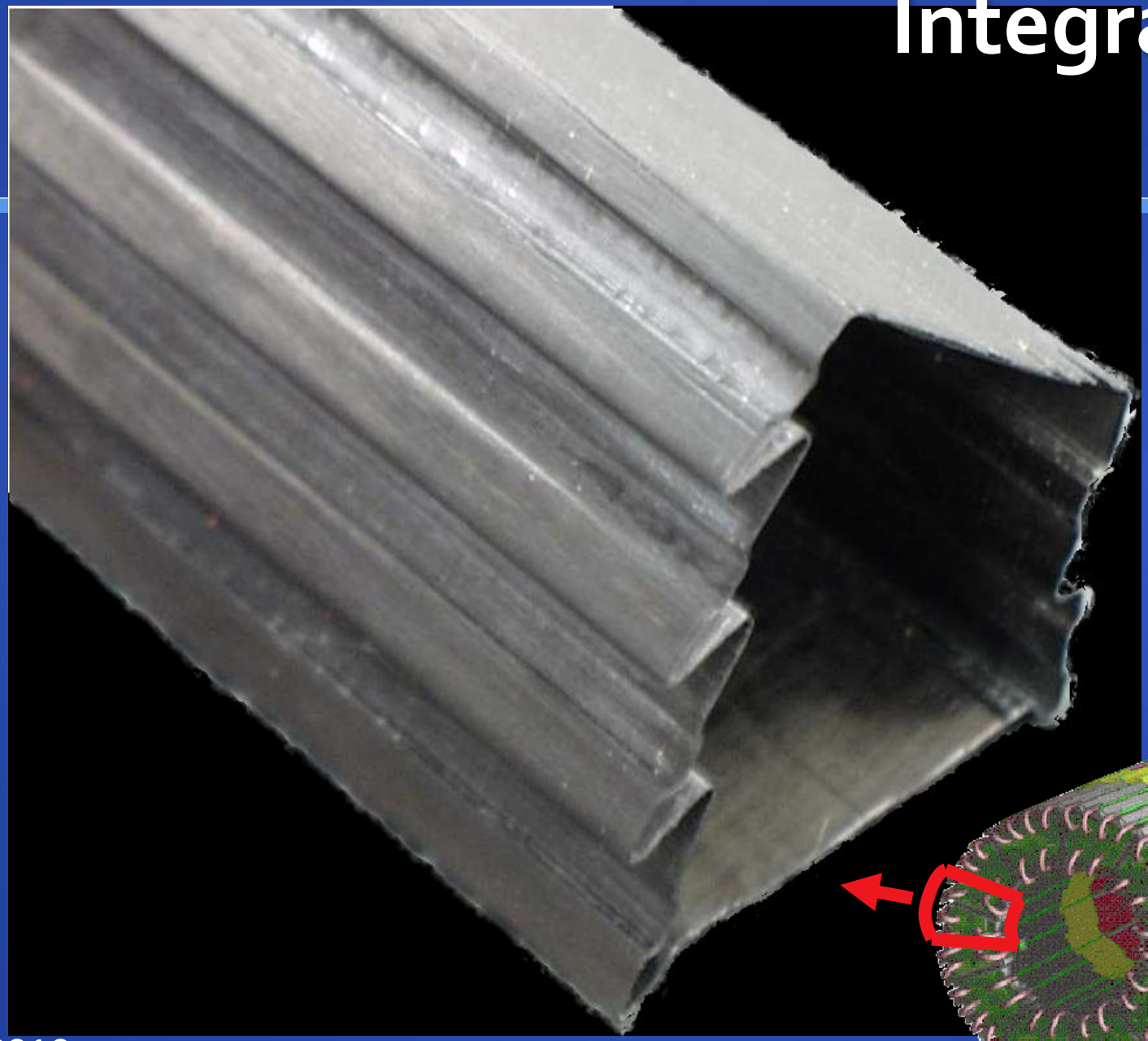
Material budget and power dissipation in Alice SPD and NA62 Gigatracker.

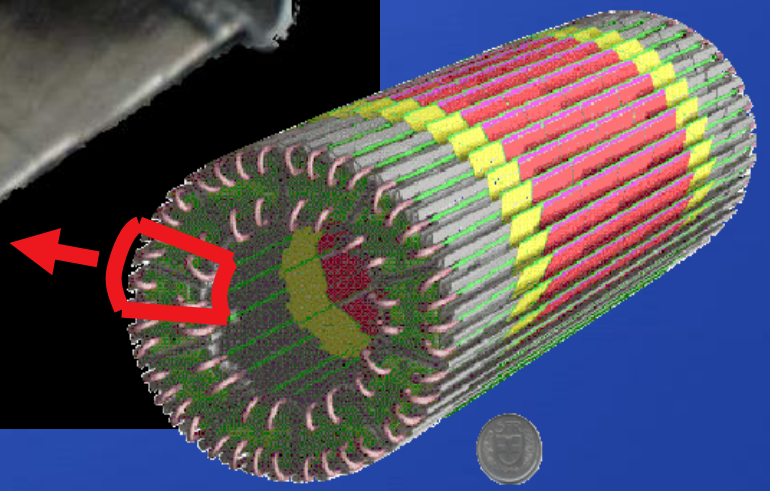
presented by A. Kluge
CLIC CDR WG4
CERN/PH-ESE
May 6, 2010

Outline

- ALICE SPD
  - material
  - power consumption
- GigaTracker
  - material
  - power consumption
- Summary

Integration





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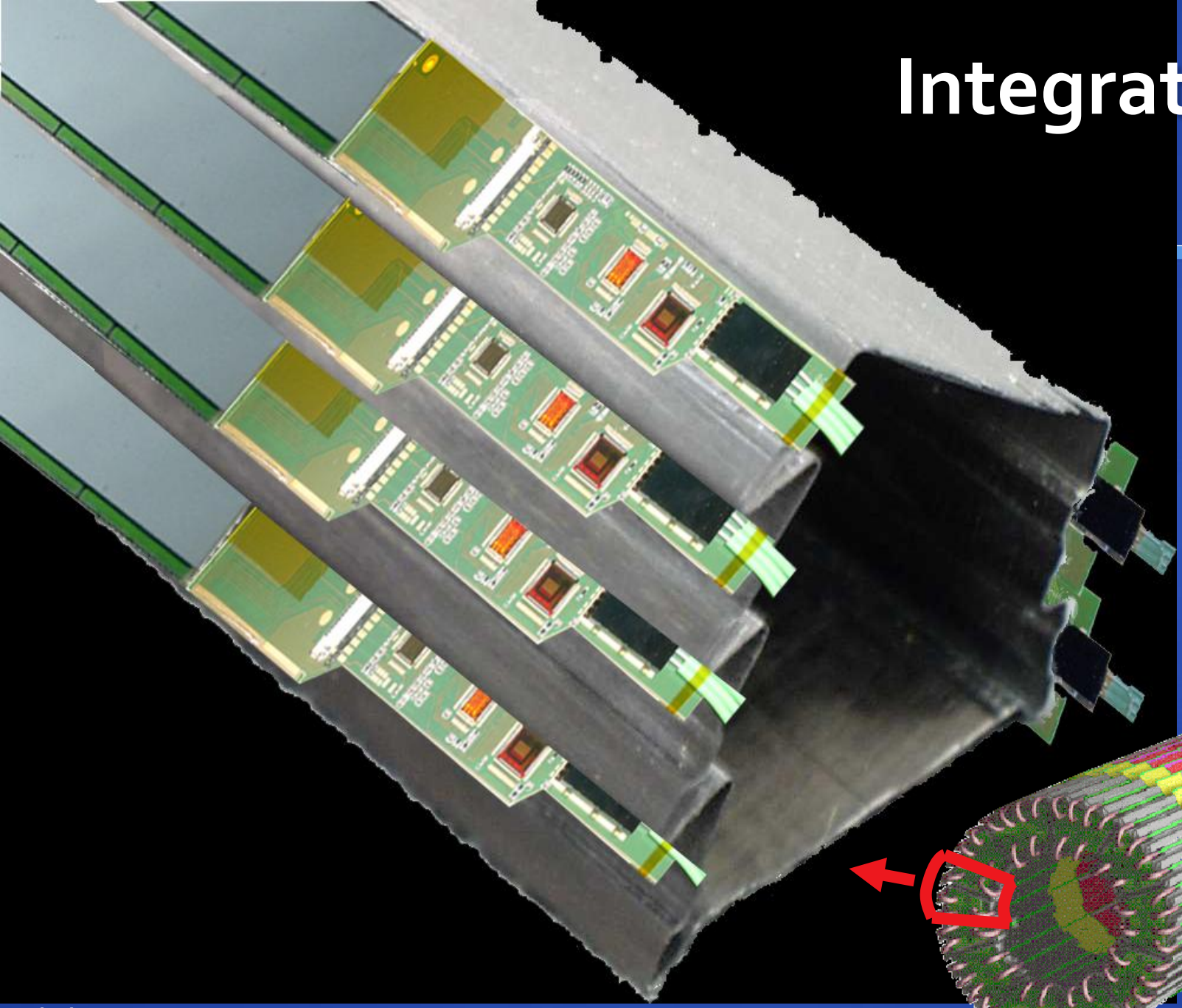
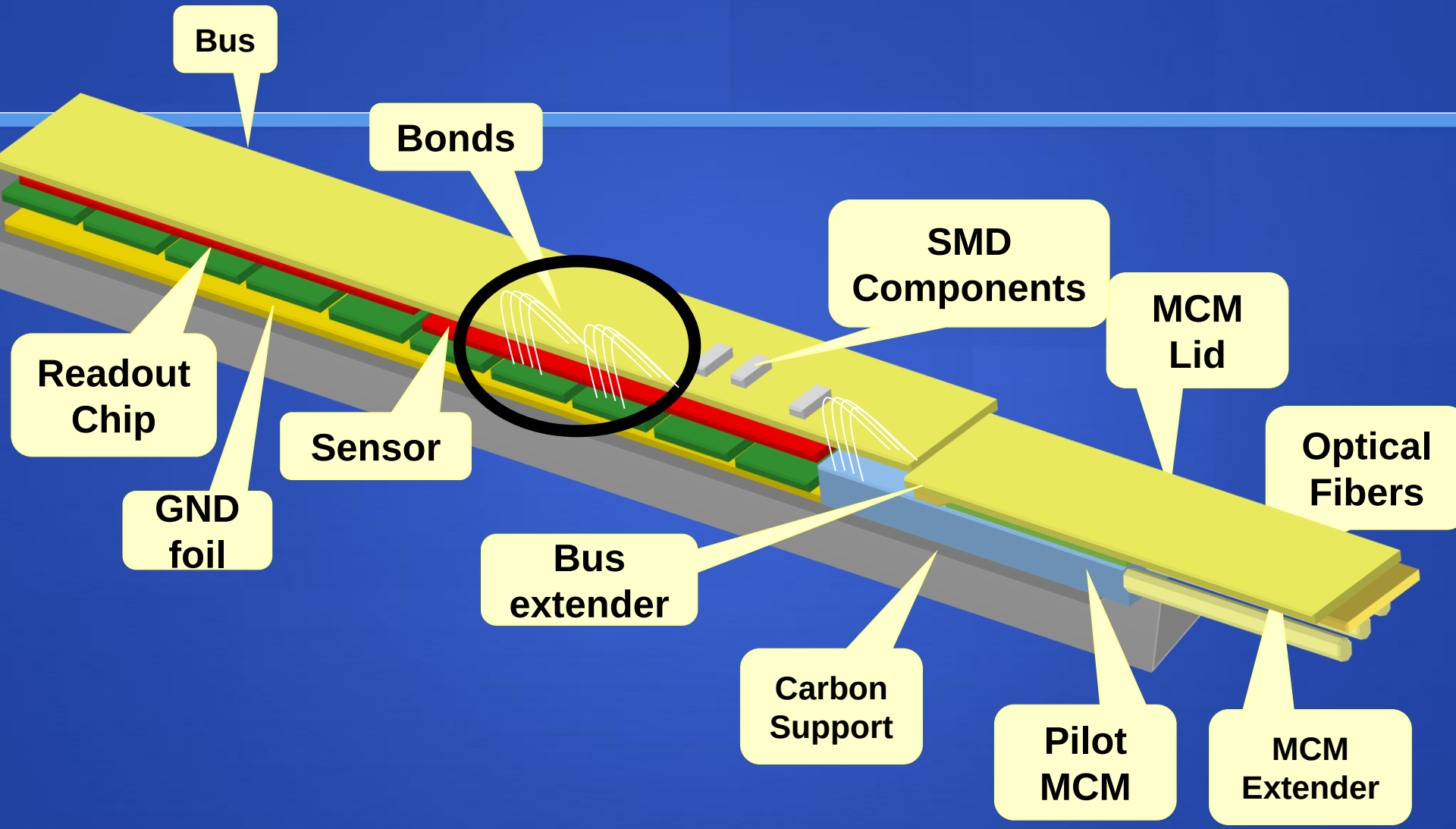


Electronics integration



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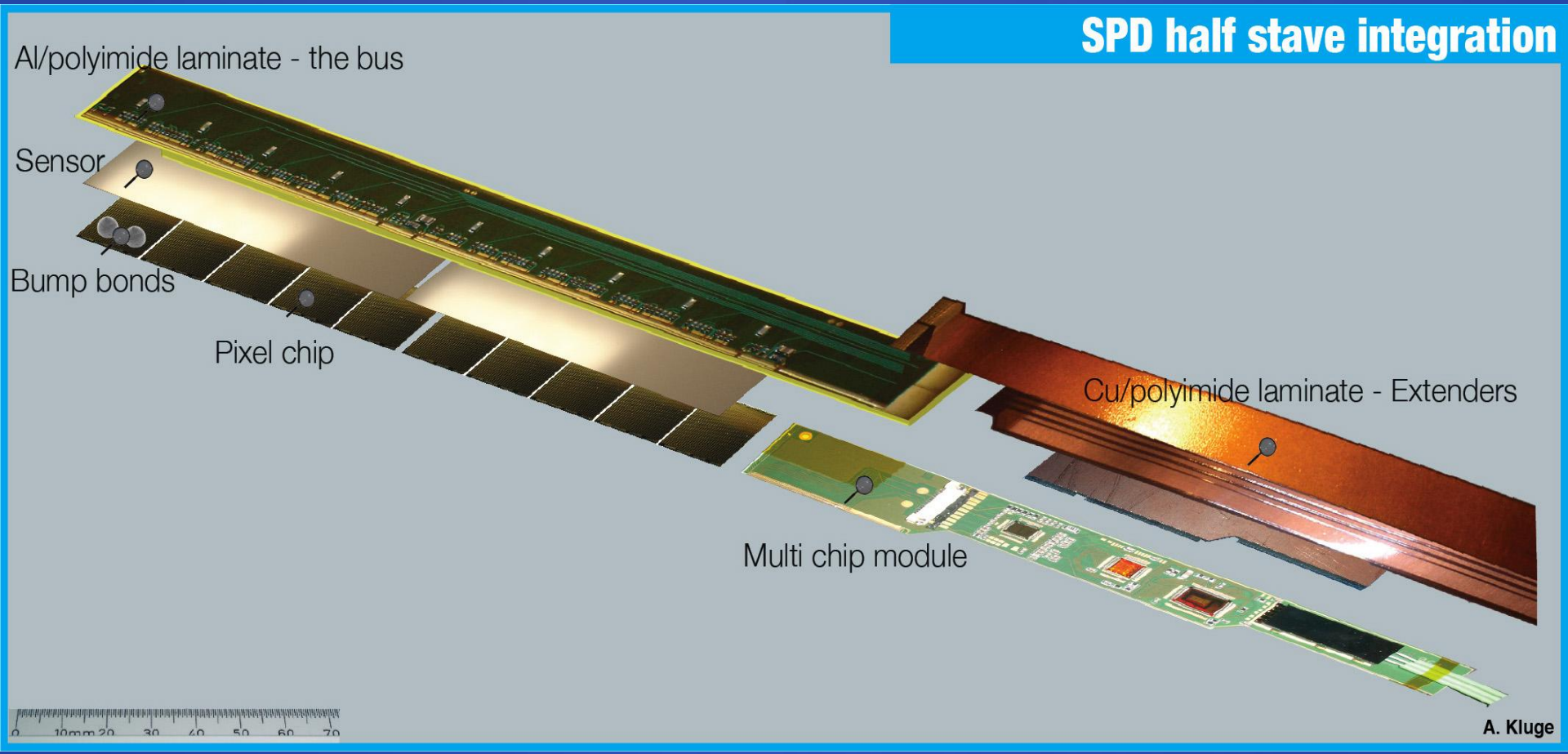

Material budget of one ALICE SPD layer

SPD Element	Thickness μm	% X_0
Al Bus		
Kapton	60	0.021
Al power	100	0.112
Al signals [50% of total surface]	17.5	0.020
Glue Epoxy	70	0.016
SMD components	16.4	0.173
Total bus		**0.341**
Other Components		
Pixel chip	150	0.160
Sensor	200	0.214
Bump bonds Sn 60%+Pb 40%	0.18+0.12	0.004
Grounding Foil-Kapton/Al	50+10	0.029
Glue Epoxy/thermal grease	200	0.049
Carbon fiber	200	0.106
Total components		**0.561**
Total bus and components		**0.903**

Material budget of one ALICE SPD layer

Star Low Mass Carrier (Mimosa5) illustration from Marco

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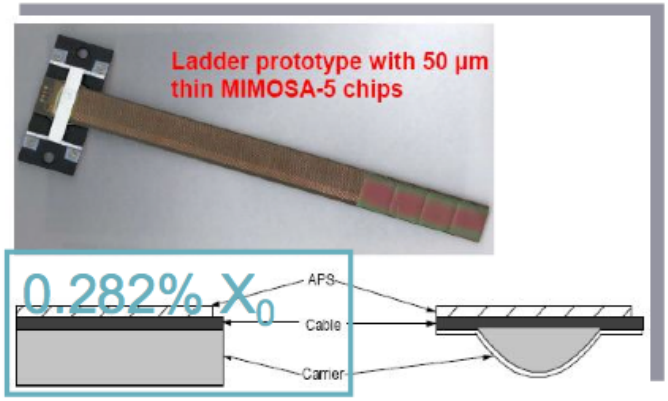


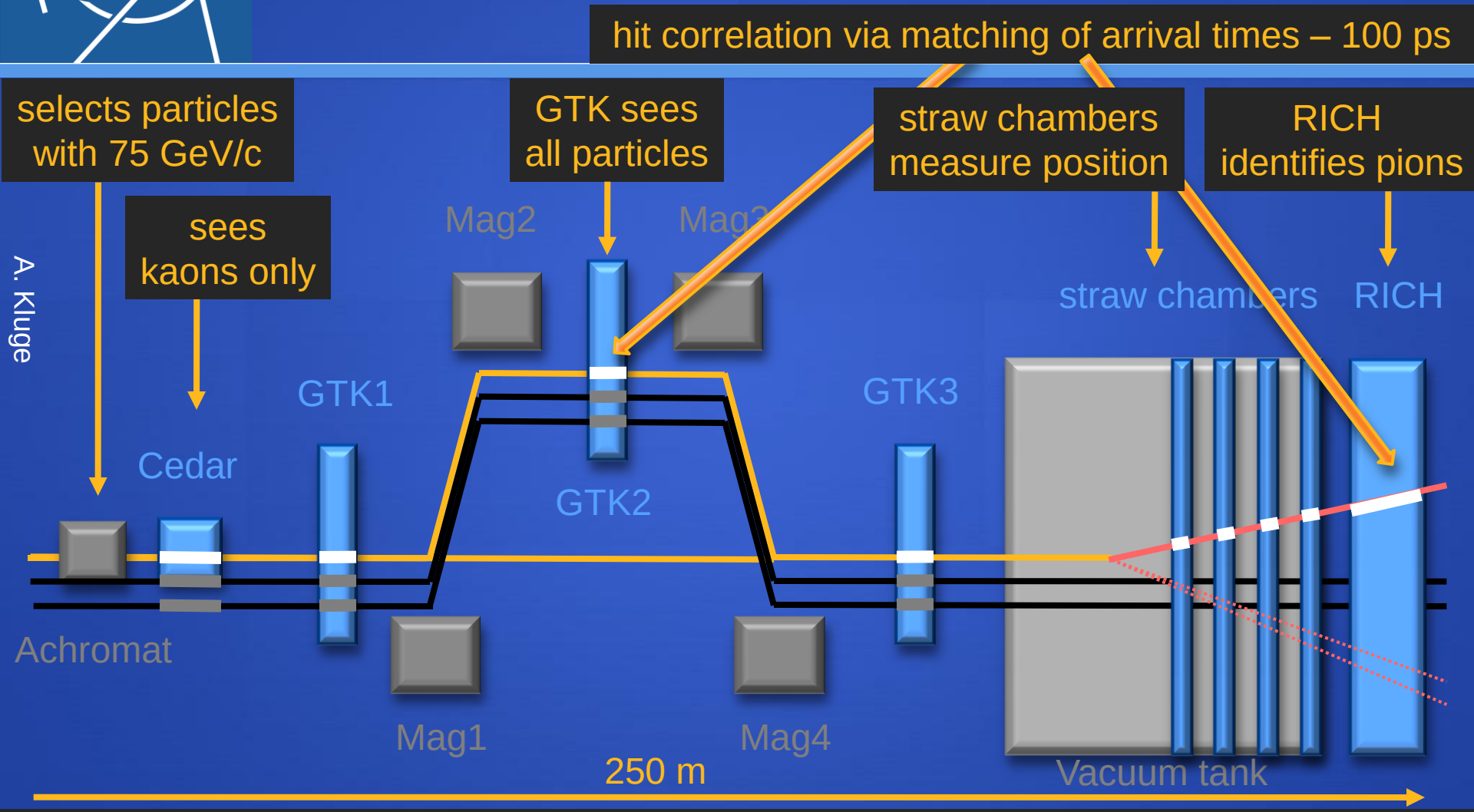
3.2 m RVC+50 m CFC (=0.11%X_0);

Component	Thickness (% X_0)
50 m Chip	0.054
Adhesive	0.014
Kapton Cable	0.090
Adhesive	0.014
Carrier	0.110
Total	0.282

Power consumption

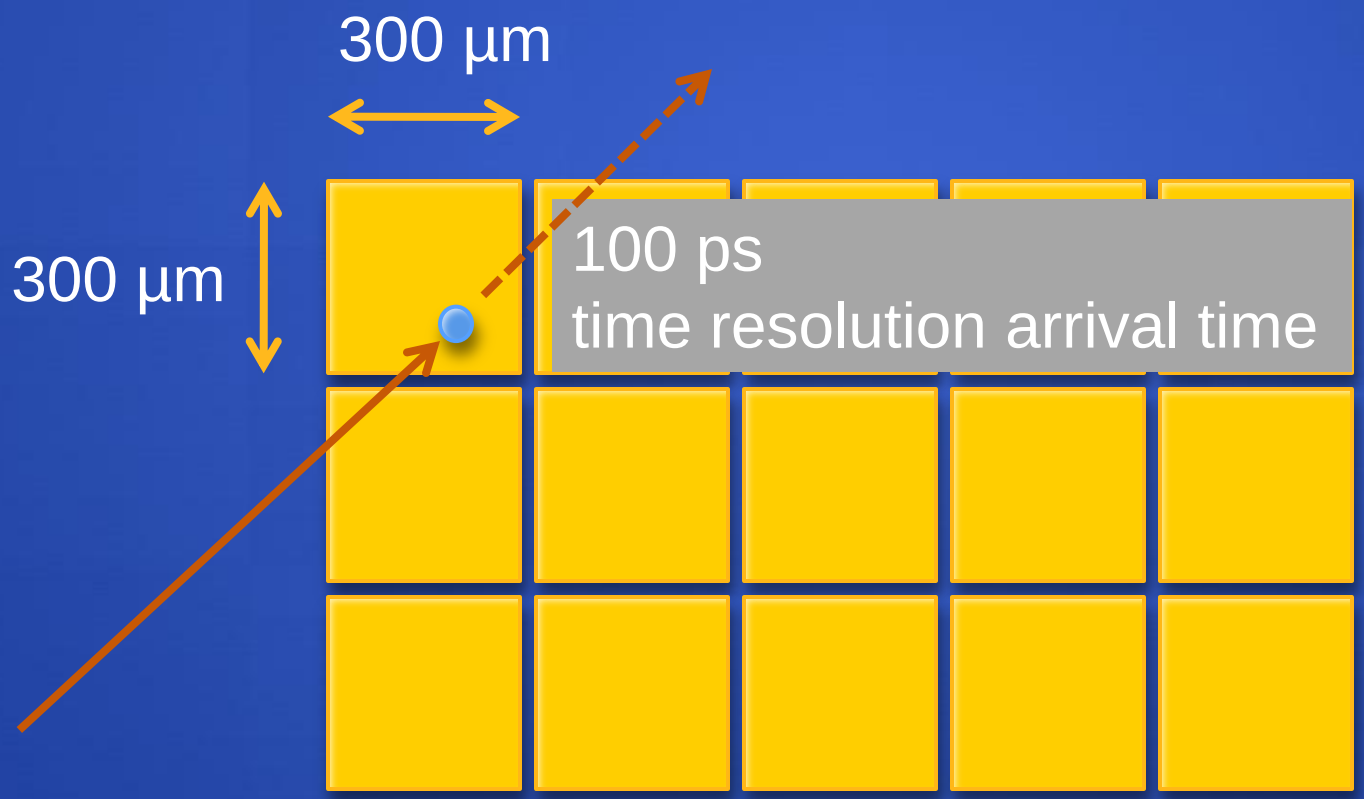
- Analog: 1.6 V * 560 mA = 0.9 W
- Digital: 1.6 V * 400 mA = 0.64W
- ASIC size = 15 * 14 mm^2 = 210 mm^2
- Active pixel area = 13.6 x 12.8 mm^2 = 174 mm^2
- Power consumption (ASIC/Active) = 0.7 W / cm^2 / 0.9 W / cm^2

Experimental setup- NA62



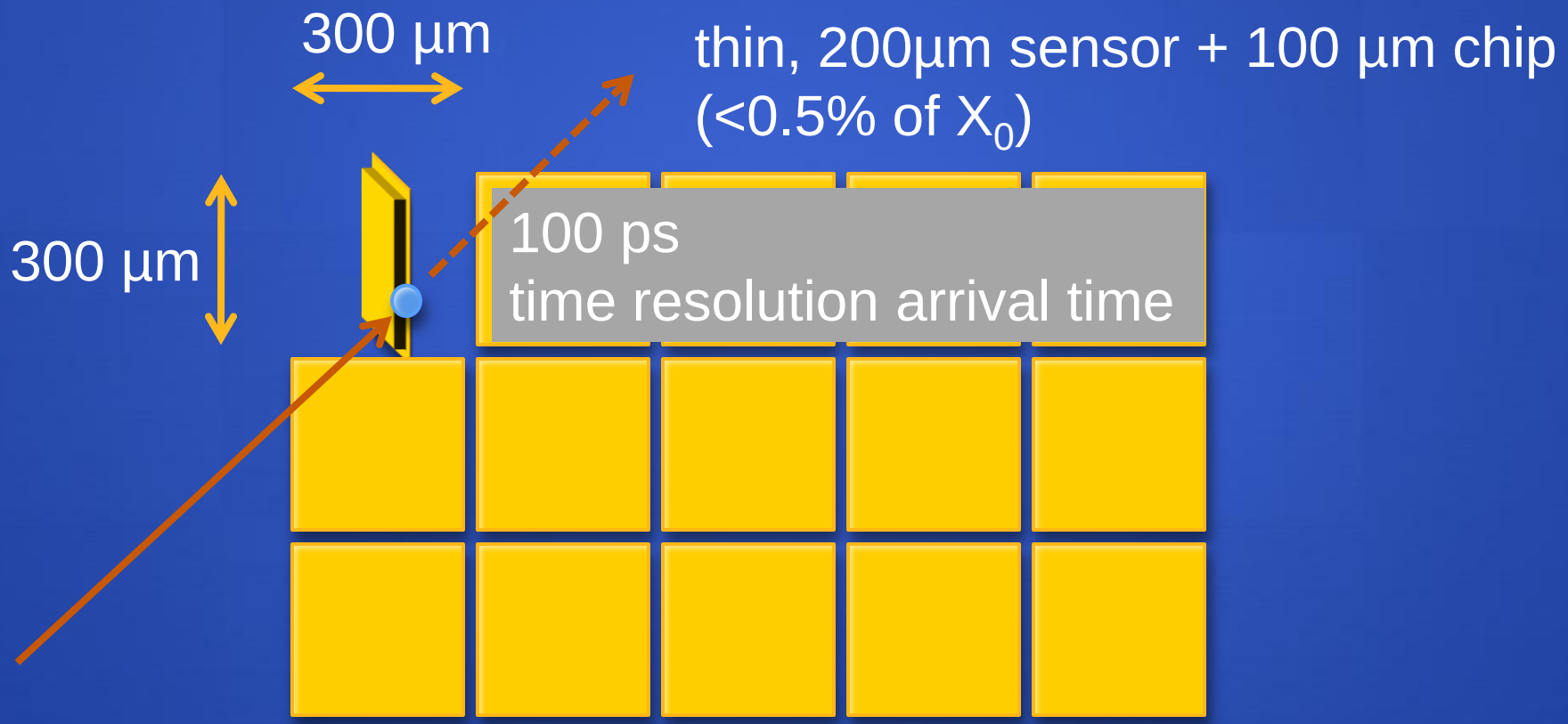
beam: hadrons, only 6% kaons-> only 20% decay in the vacuum tank into a pion and 2 neutrinos -> out of which only 10^{-11} decays are of interest

Experimental setup: GTK specifications



800 MHz particle rate

Experimental setup: GTK specifications



Beam & detector configuration

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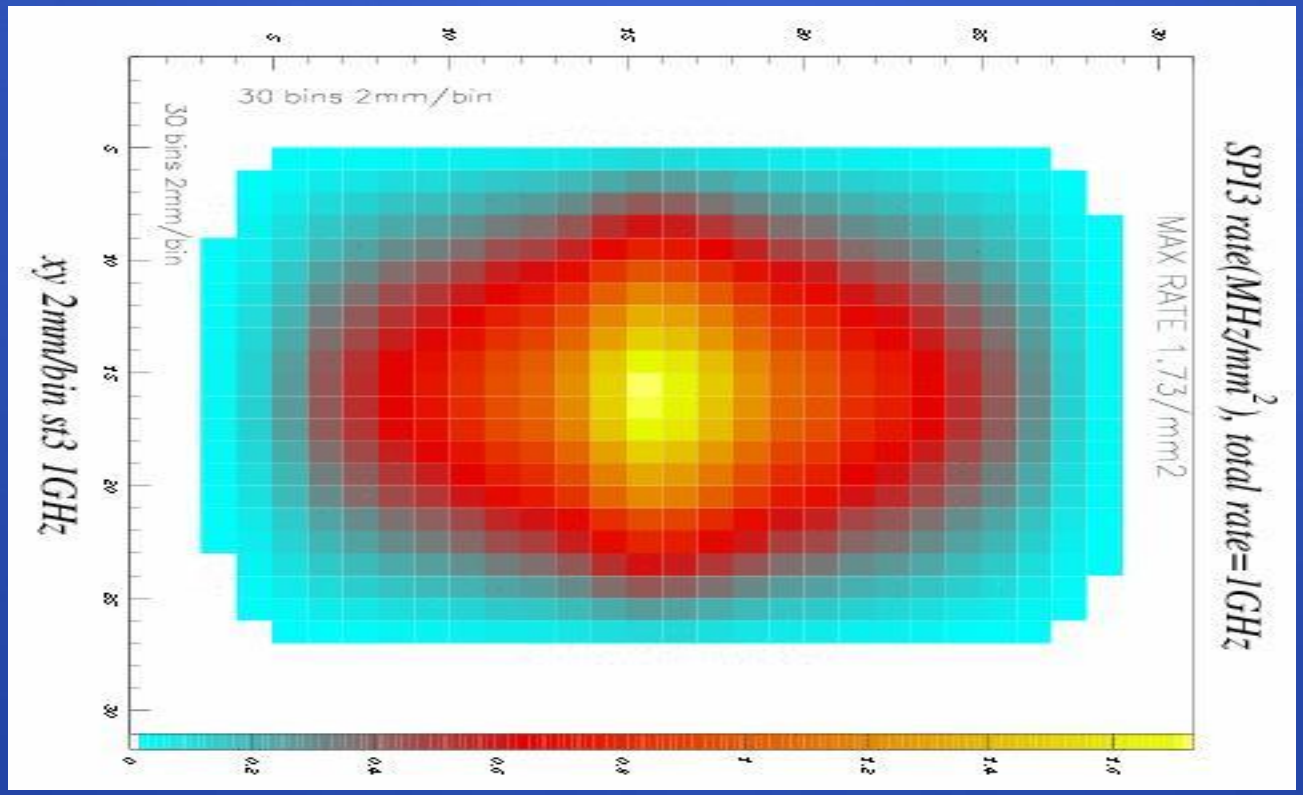
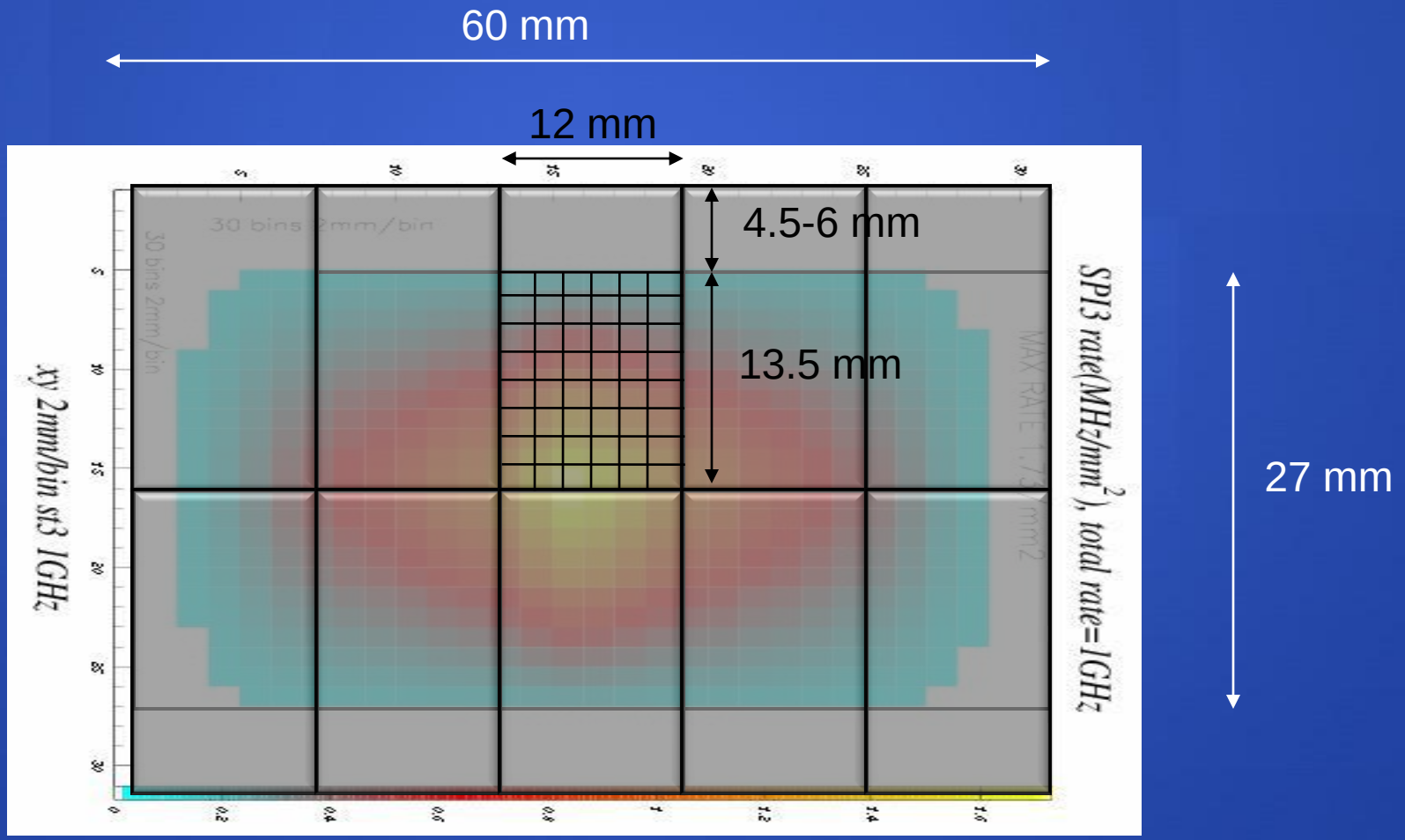
Beam profile

60 mm



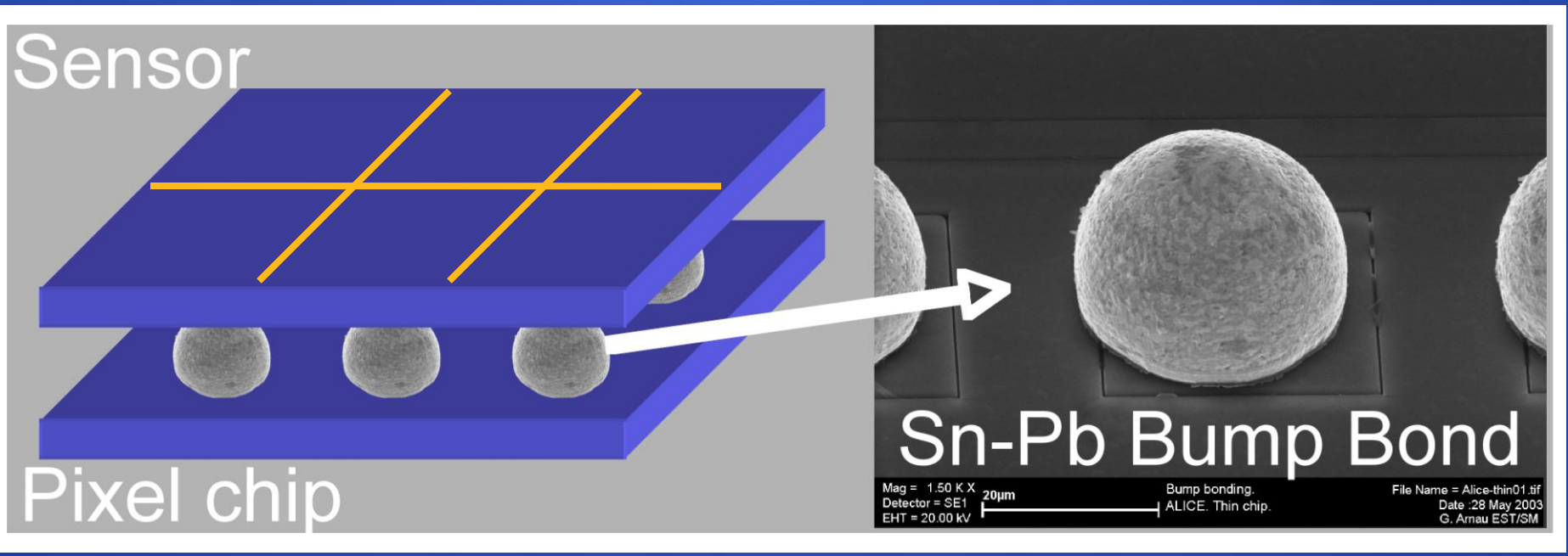
27 mm

ASIC covering beam

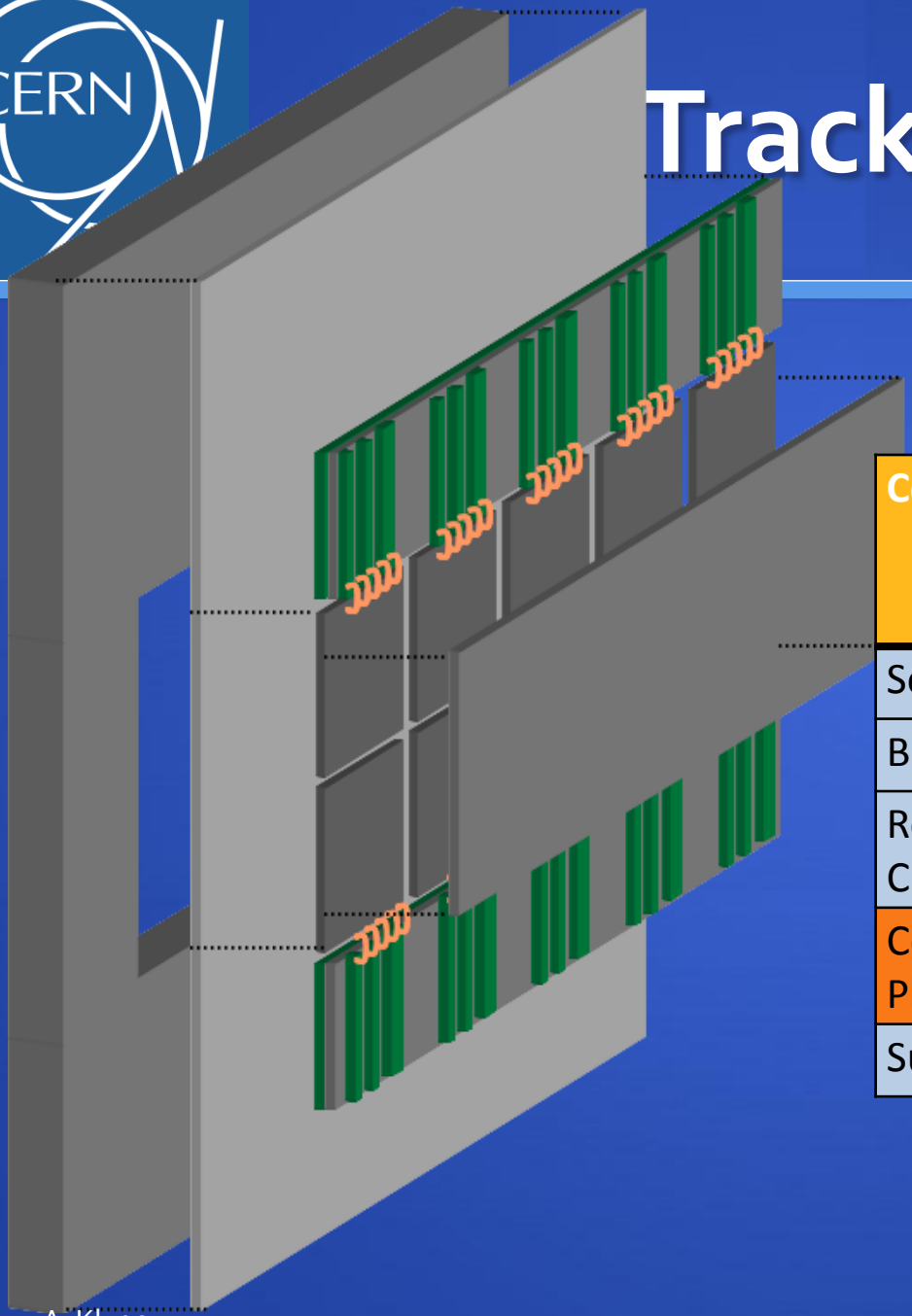


45 rows times 40 columns per chip = 1800 pixels per chip

Hybrid pixel detector



Tracker setup



Component	Material	Thickness [µm]	X0 [%]
Sensor	Si	200	0.21
Bump Bonds	Pb-Sn	~25	0.001
Readout Chip	Si	100	0.11
Cooling Plate	Si	~150	~0.15
Sum			~0.47

The electronics specification

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General: System Specifications

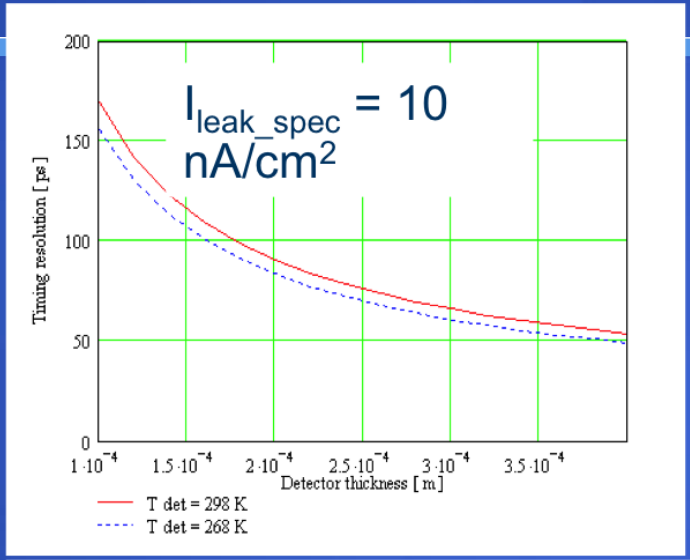
Number of pixels per chip	1800 = 45 x 40
Size of pixels	300 µm x 300 µm
Active area per chip	12 mm x 13.5 mm = 162 mm^2
Chip design time resolution	100 ps (rms)
Thickness of sensor	200 µm
Type of sensor	p in n
Thickness of read-out chip	100 µm
Dynamic input range	5000 – 60000 electrons

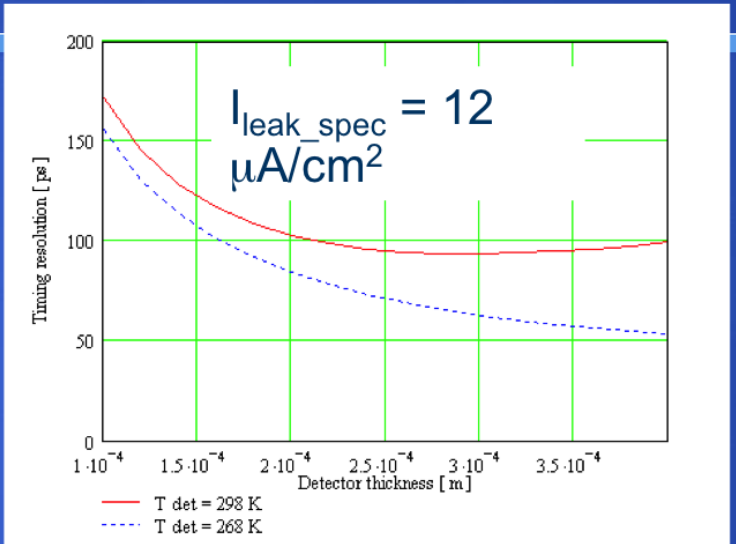
General: System Specifications

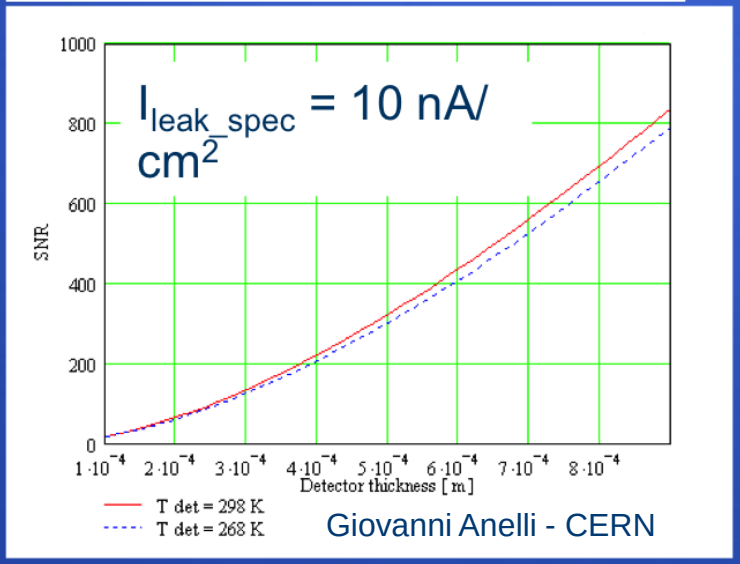
Design particle rate per chip	130 MHz
Rate of center pixel	140 kHz
Rate of center column	~ 3.3 MHz or 0.82 MHz/mm^2
Average rate per pixel	73 kHz
Maximum dead time	1 % (2 % in beam center)
Data transfer rate per chip	6 Gbit/s
Total dose in 1 year	~ 10^5 Gy
Neutron flux in 100 days	2 x 10^{14} 1 MeV neutron equivalent cm^{-2}
Material budget/power	0.5 % X_0 per station / <2W/cm^{-2}

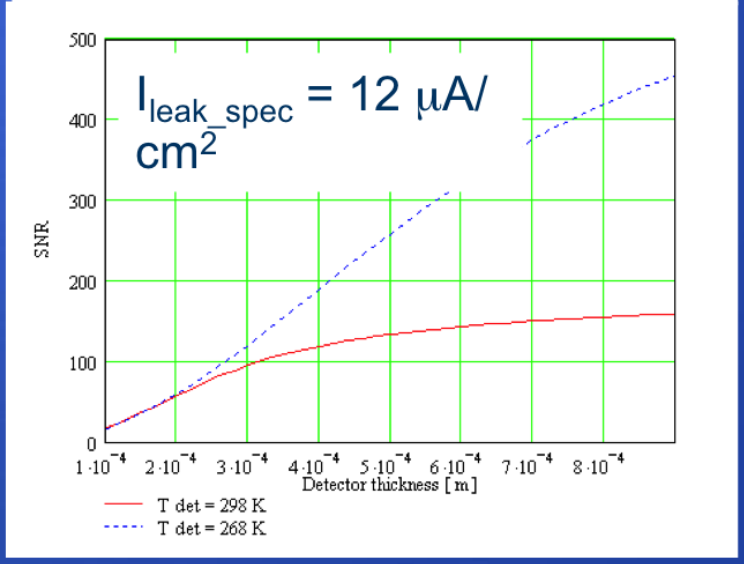
Sensor thickness optimisation

- Max power dissipation: 1.2 W/cm^2
- Only 30% of the power per pixel goes into the input transistor



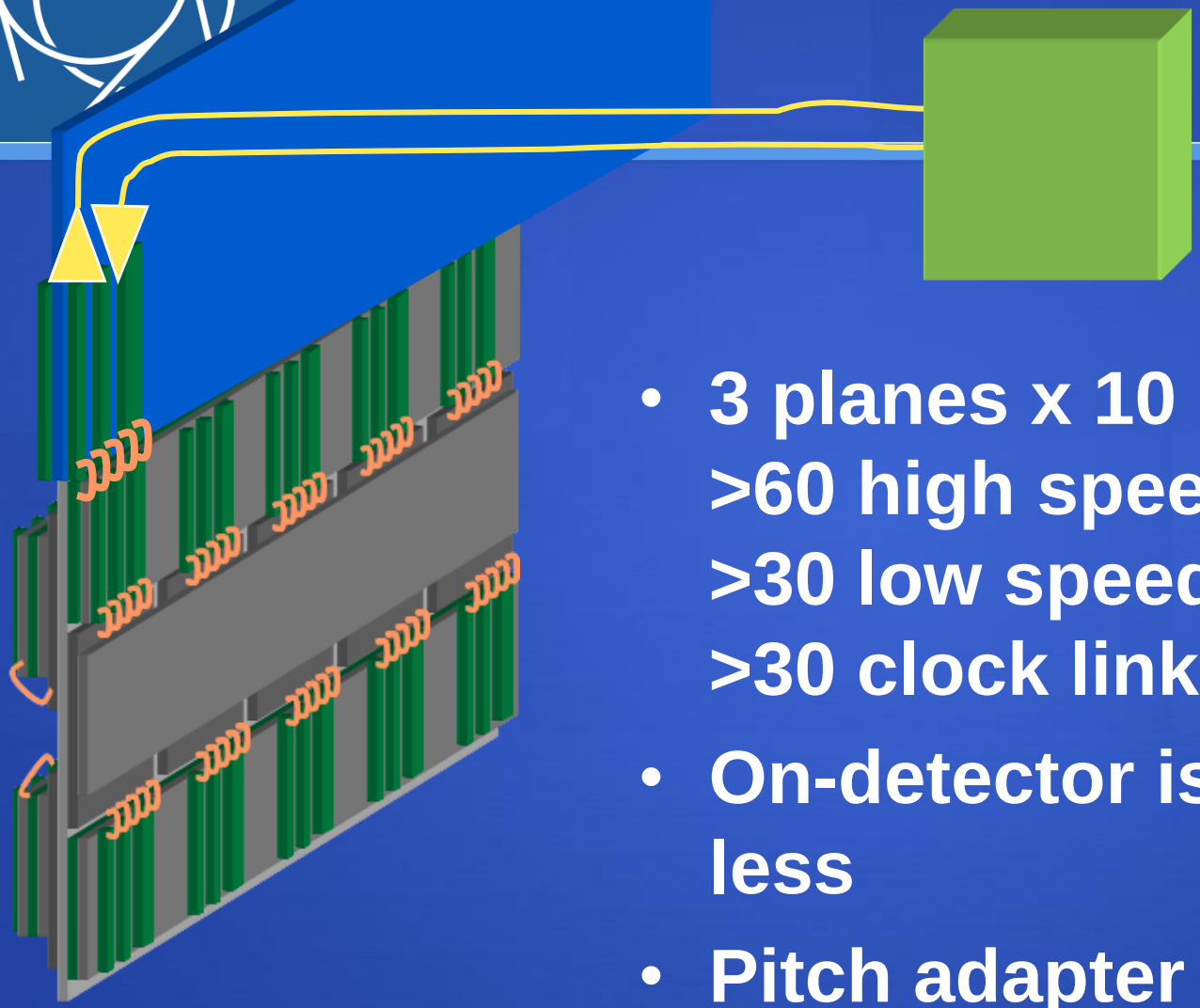






Giovanni Anelli - CERN

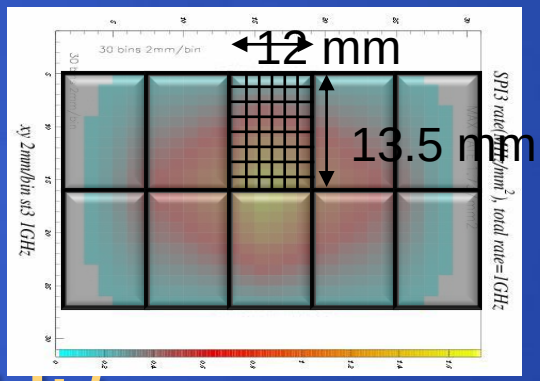
Read out



- 3 planes x 10 chips:
  >60 high speed links +
  >30 low speed links+
  >30 clock links
- On-detector is trigger-less
- Pitch adapter & multi gigabit serial links

Data rate

- Rate of center column = chip design rate:
  3.3 MHz/column
  ~ 82 MHz/cm²
  - => avg rate 73 kHz/pixel
  - => 132 MHz/chip



- => 132 MHz/chip * ~ 32 bit = ~4.2 Gbit/s

  - => max rate in beam center 140 kHz/pixel

  - Example data word (11 bit address, 5 bit fine time, (5 bit fine time trailing), 11 bit coarse time

The ASIC architecture

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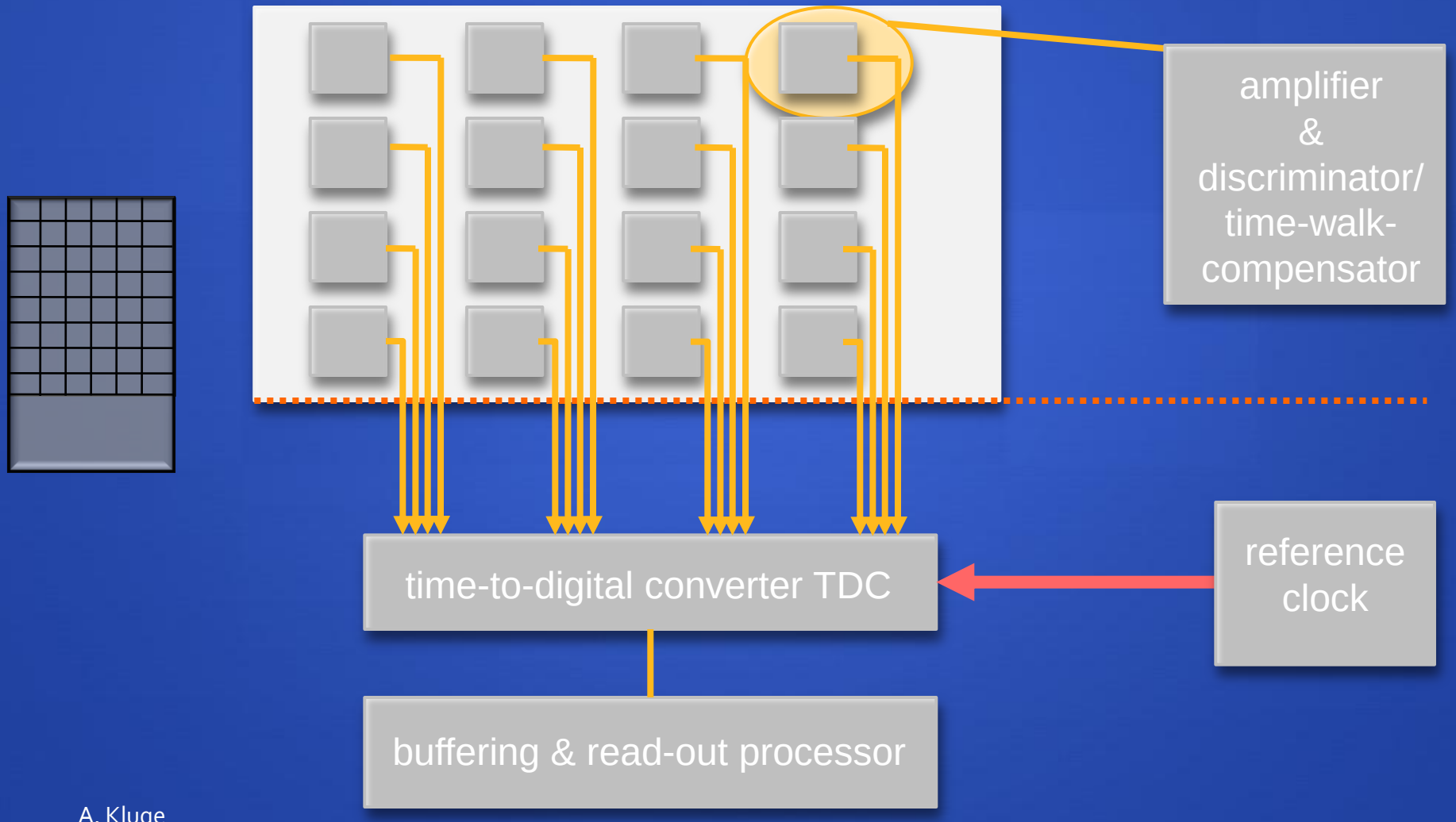
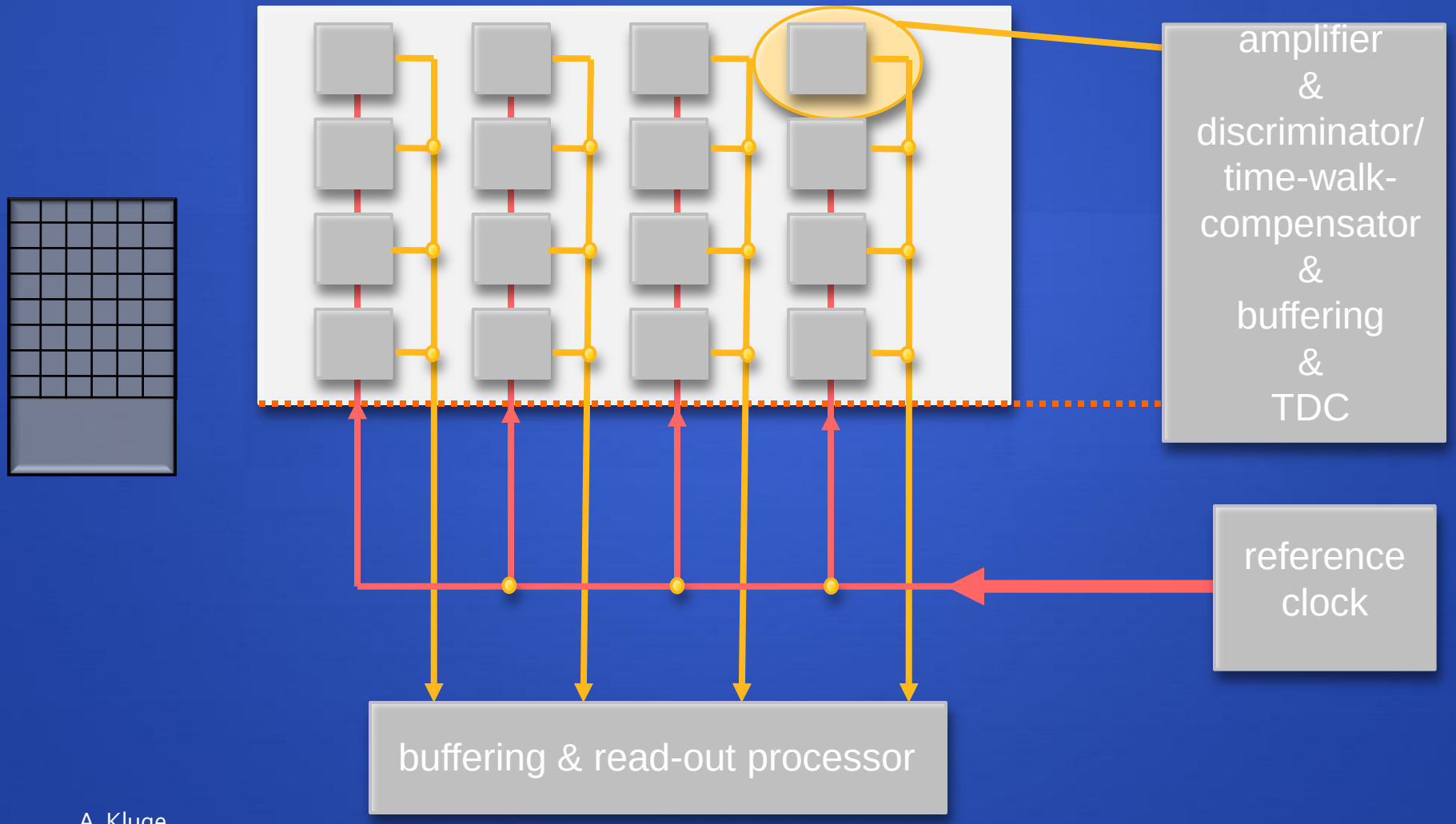
Jitter-free pixel signal to TDC in EOC



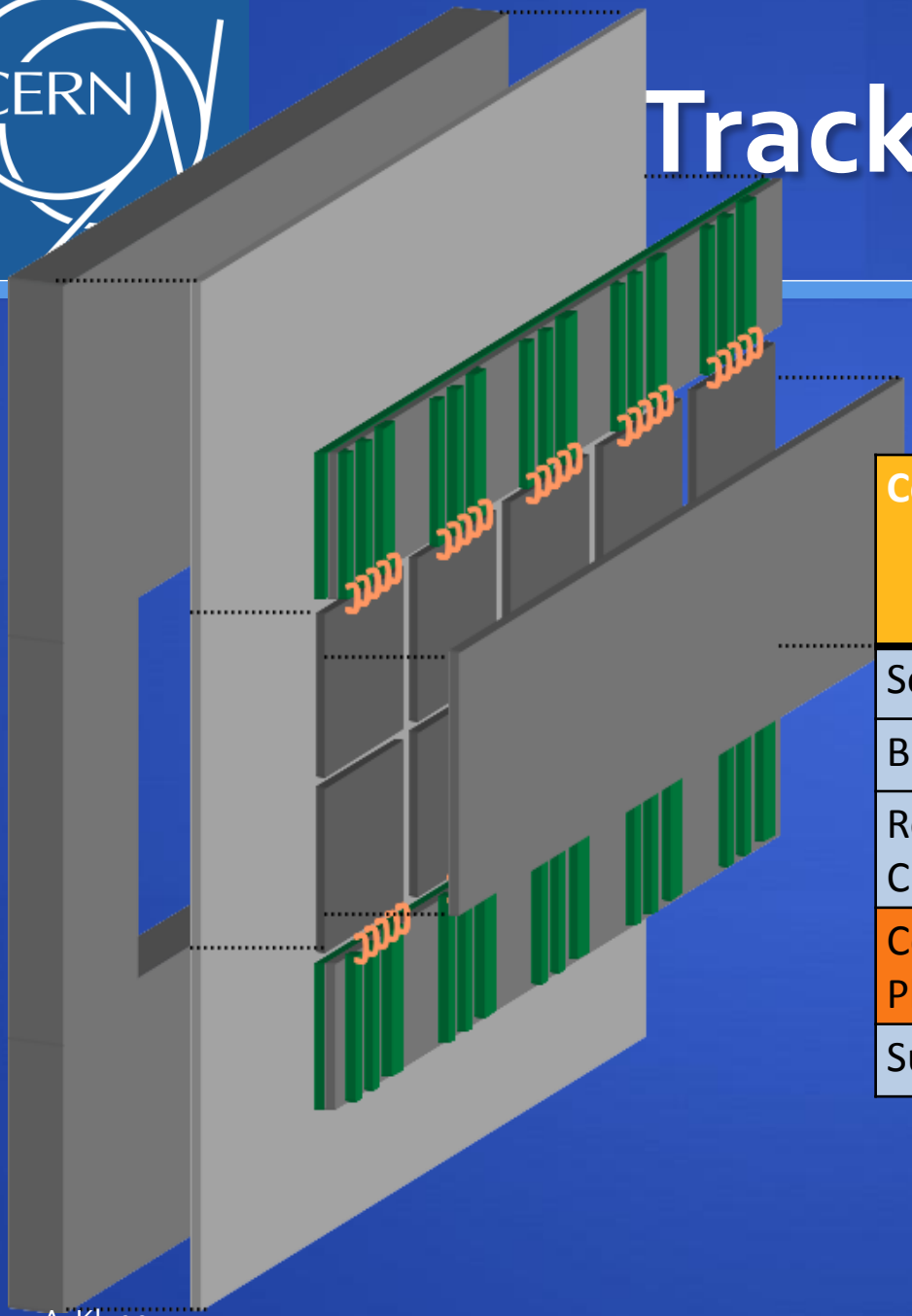
Precise clock signal to all pixels



GTK cooling & electro-mechanical integration

Vito Carassiti, Alessandro Mapelli, Michel Morel,Georg Nüssle

Tracker setup



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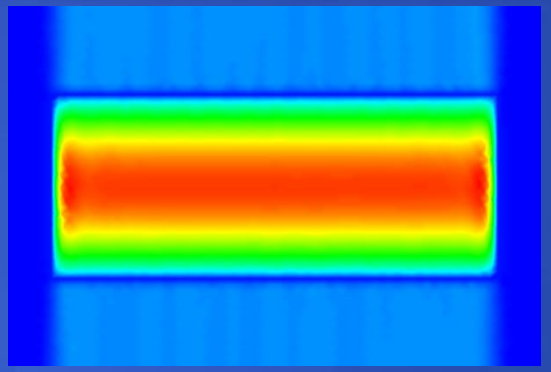
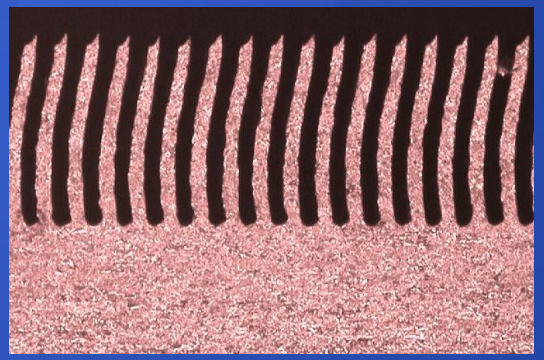
Cooling systems under investigation

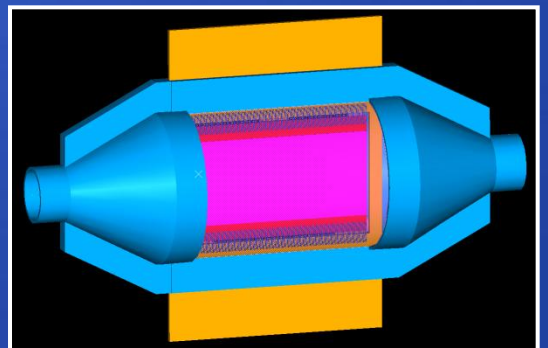
- carbon plate, conductive cooling



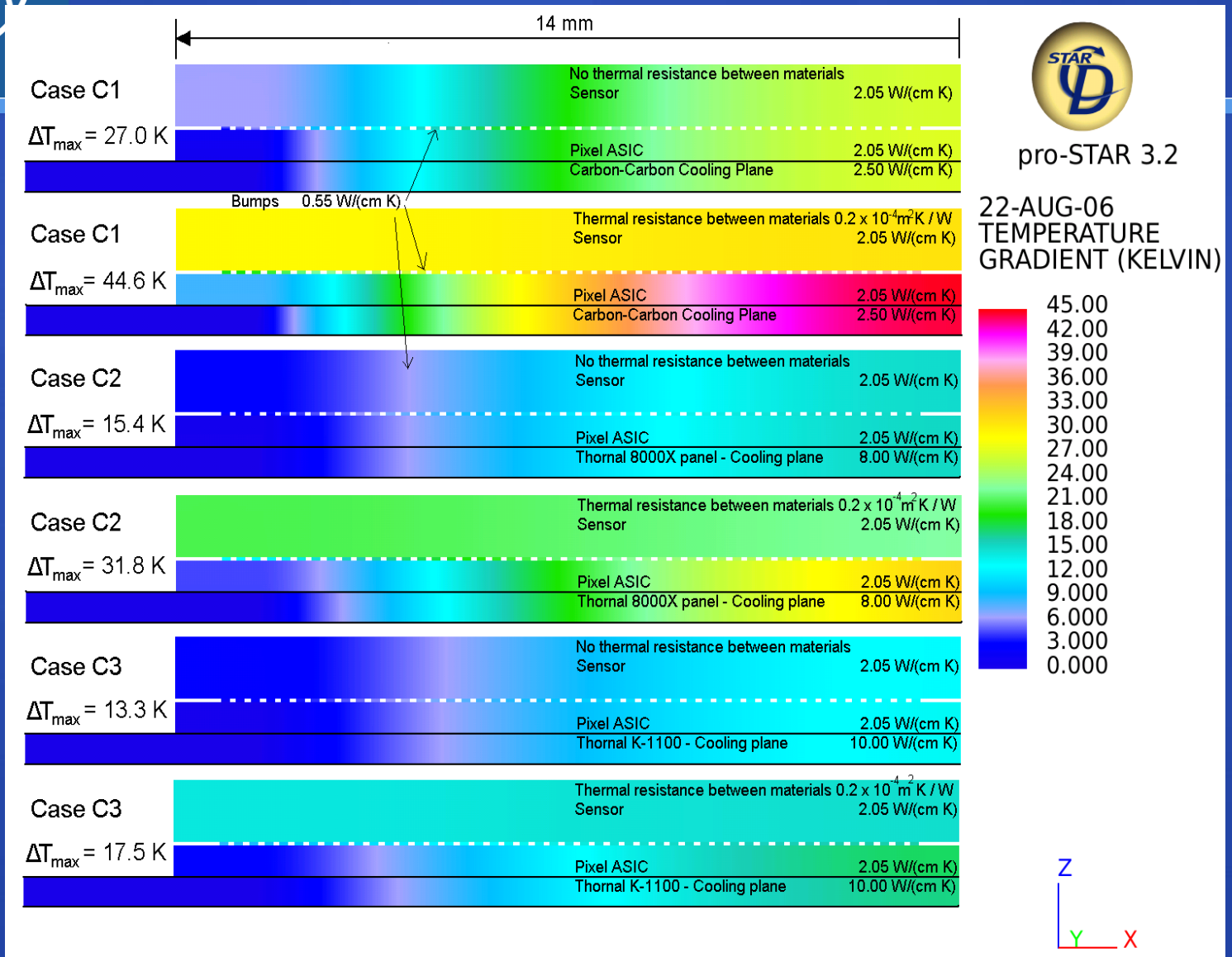
- micro channels



- convective cooling in a vessel

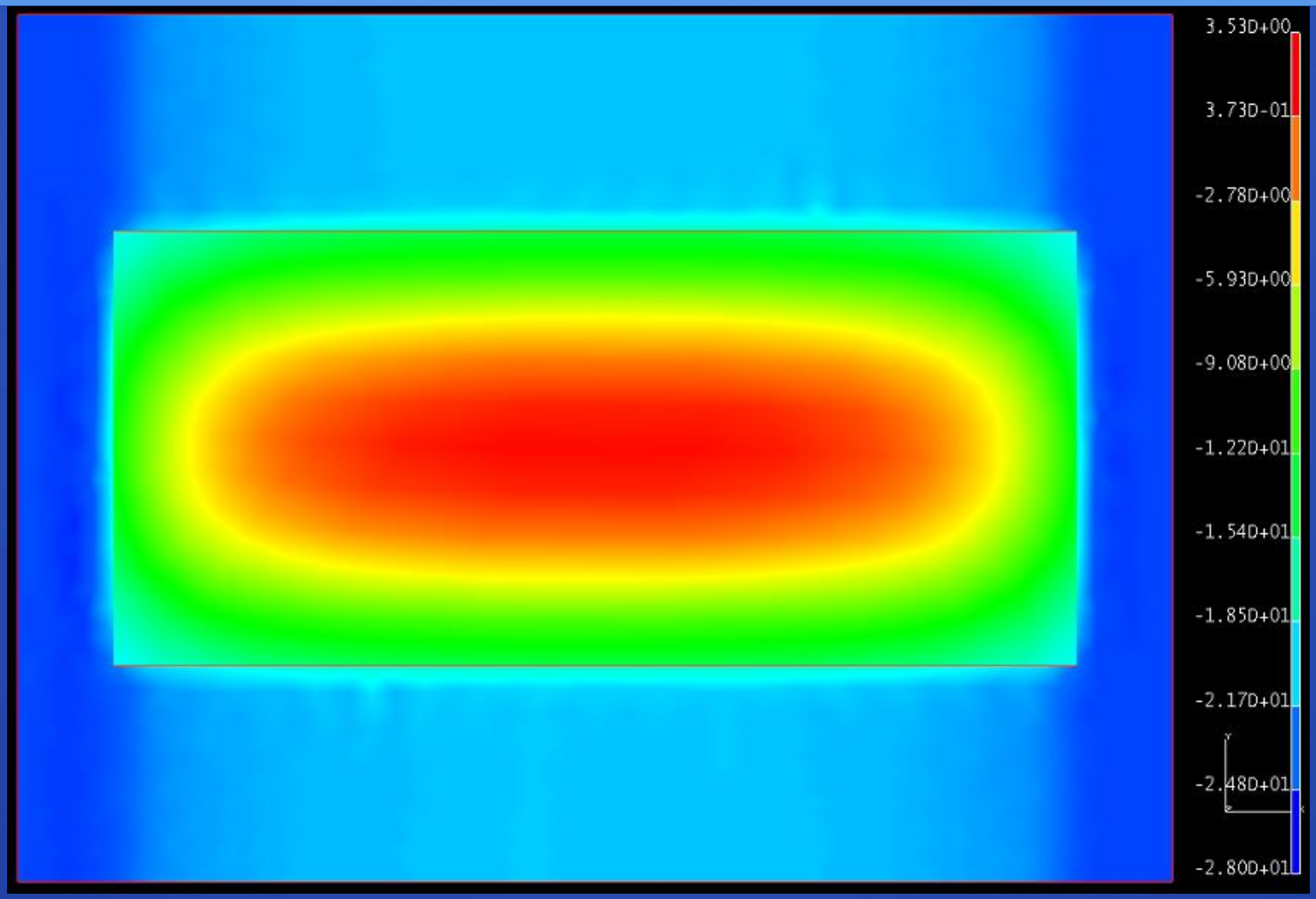


Thermal drop: ideal contact between materials (Thomas Kuhn)

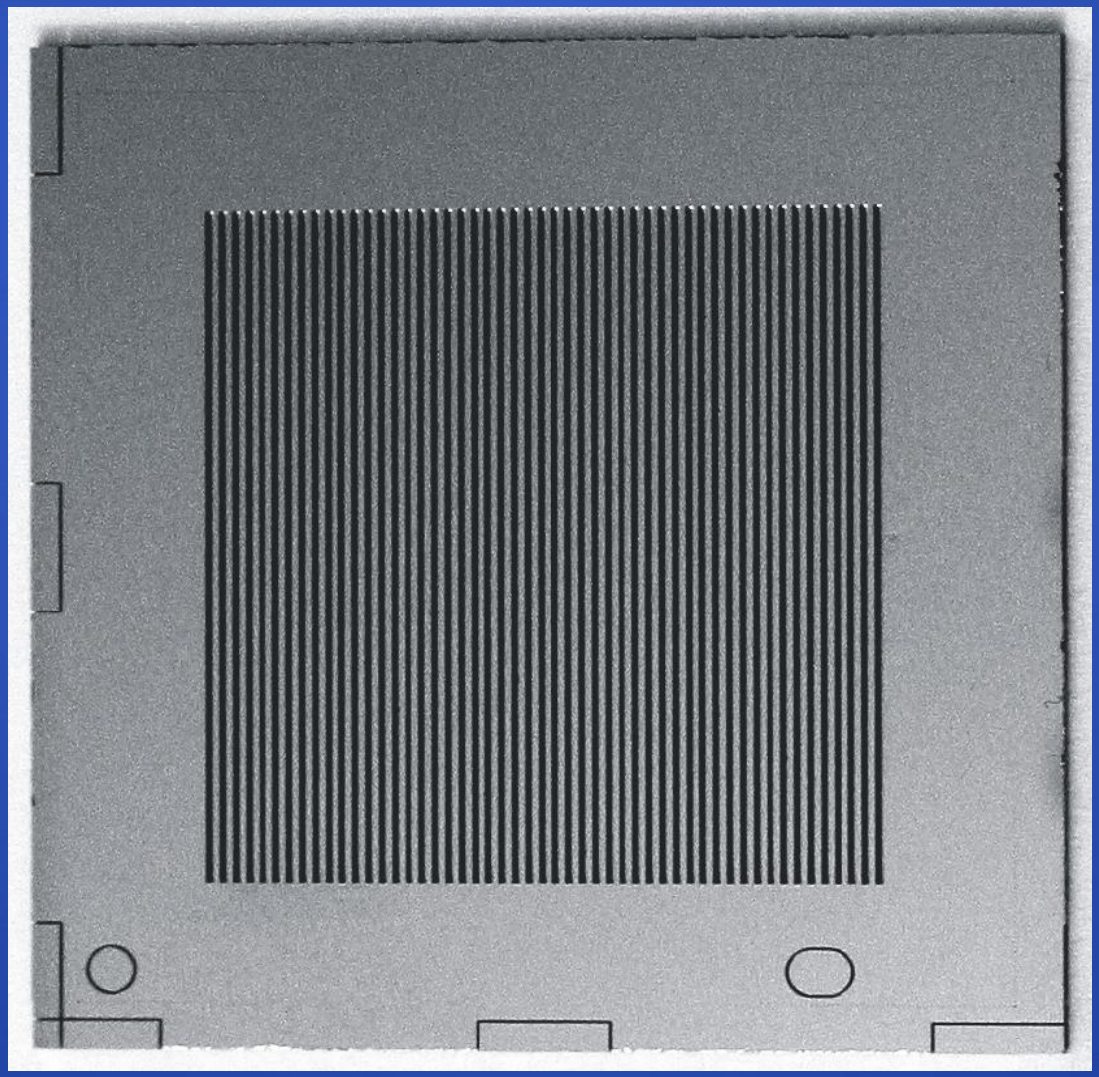


https://edms.cern.ch/document/761753/1

Temperature distribution

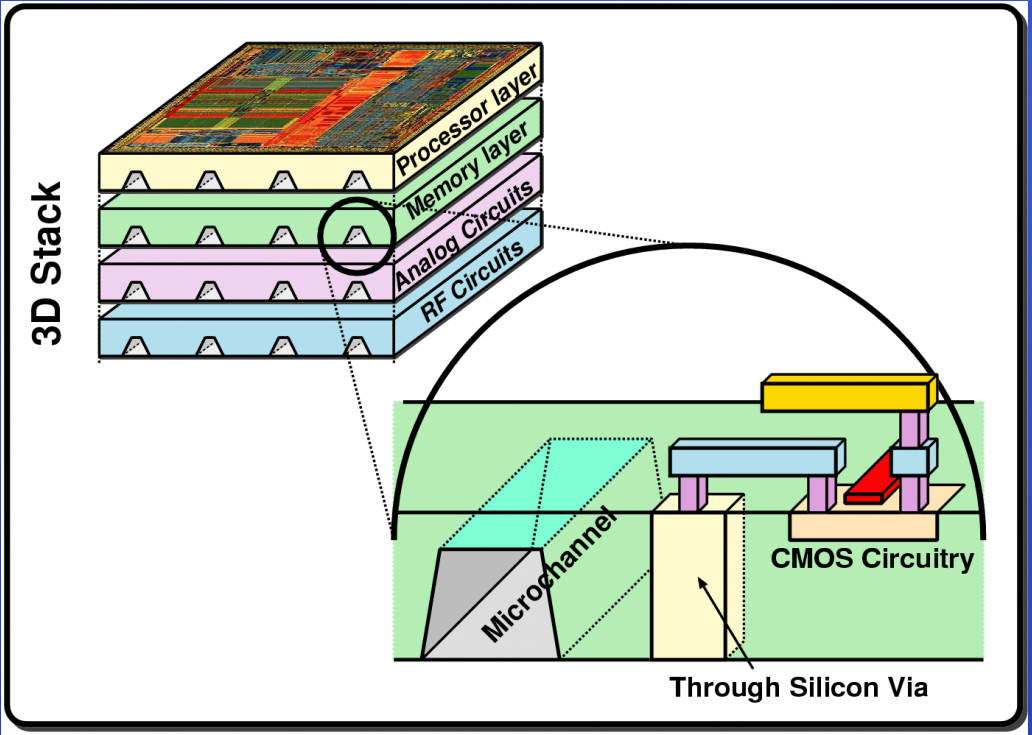


Microchannel cooling

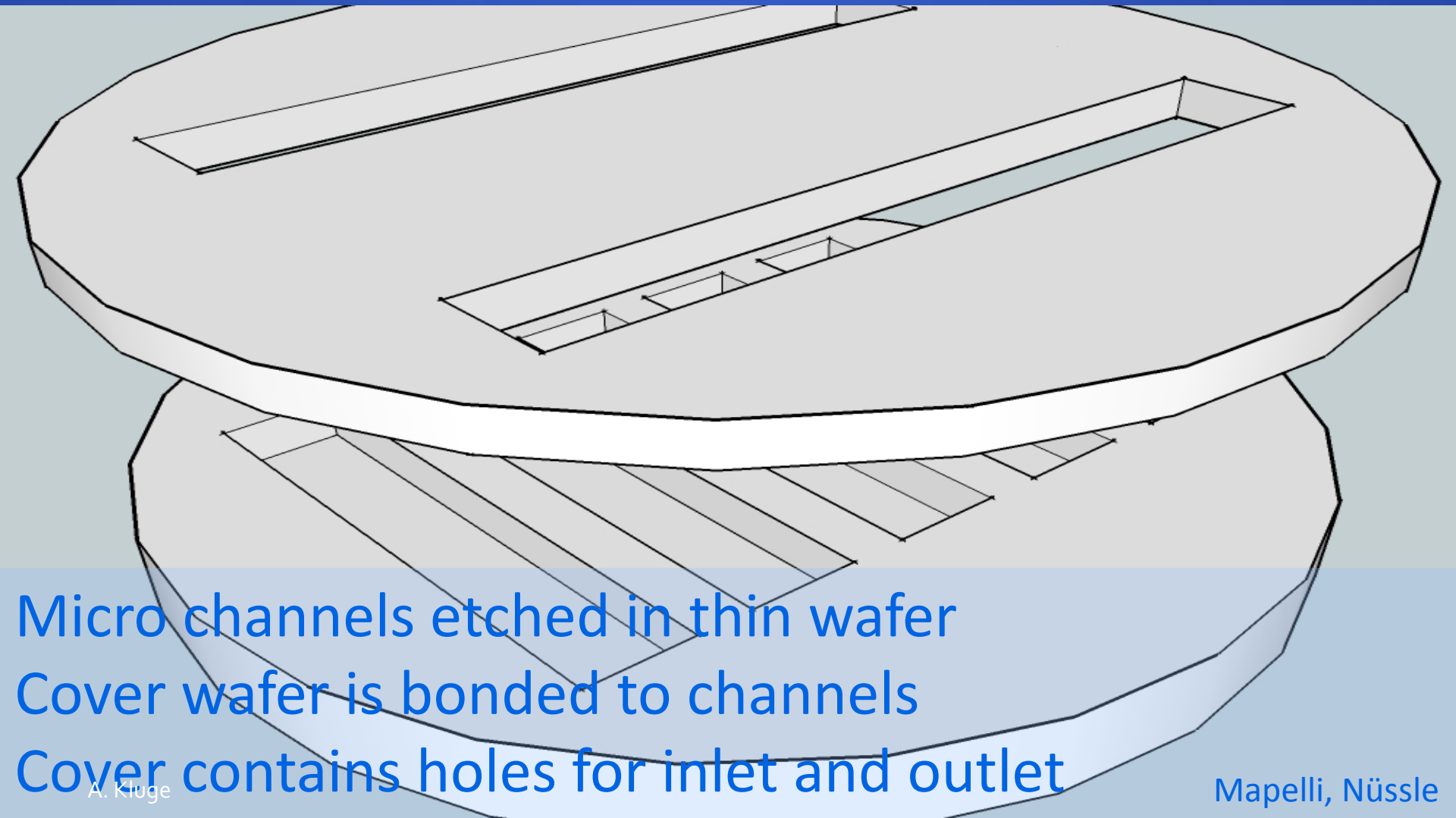


3D integrated ASIC cooling

- EFPL Lausanne, Prof. Thome



Production principle

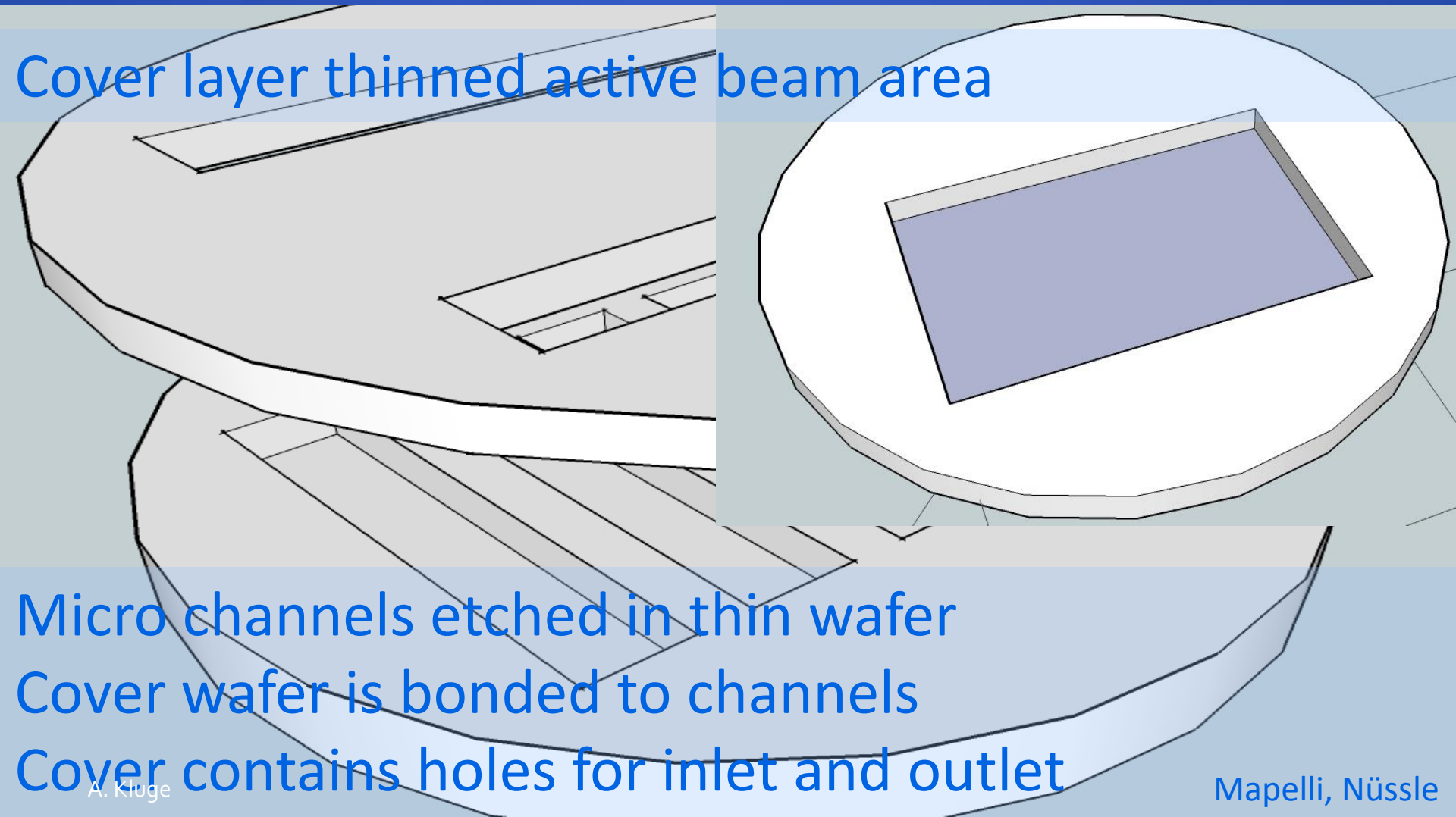


Micro channels etched in thin wafer
Cover wafer is bonded to channels
Cover contains holes for inlet and outlet

Mapelli, Nüssle

Production principle

Cover layer thinned active beam area



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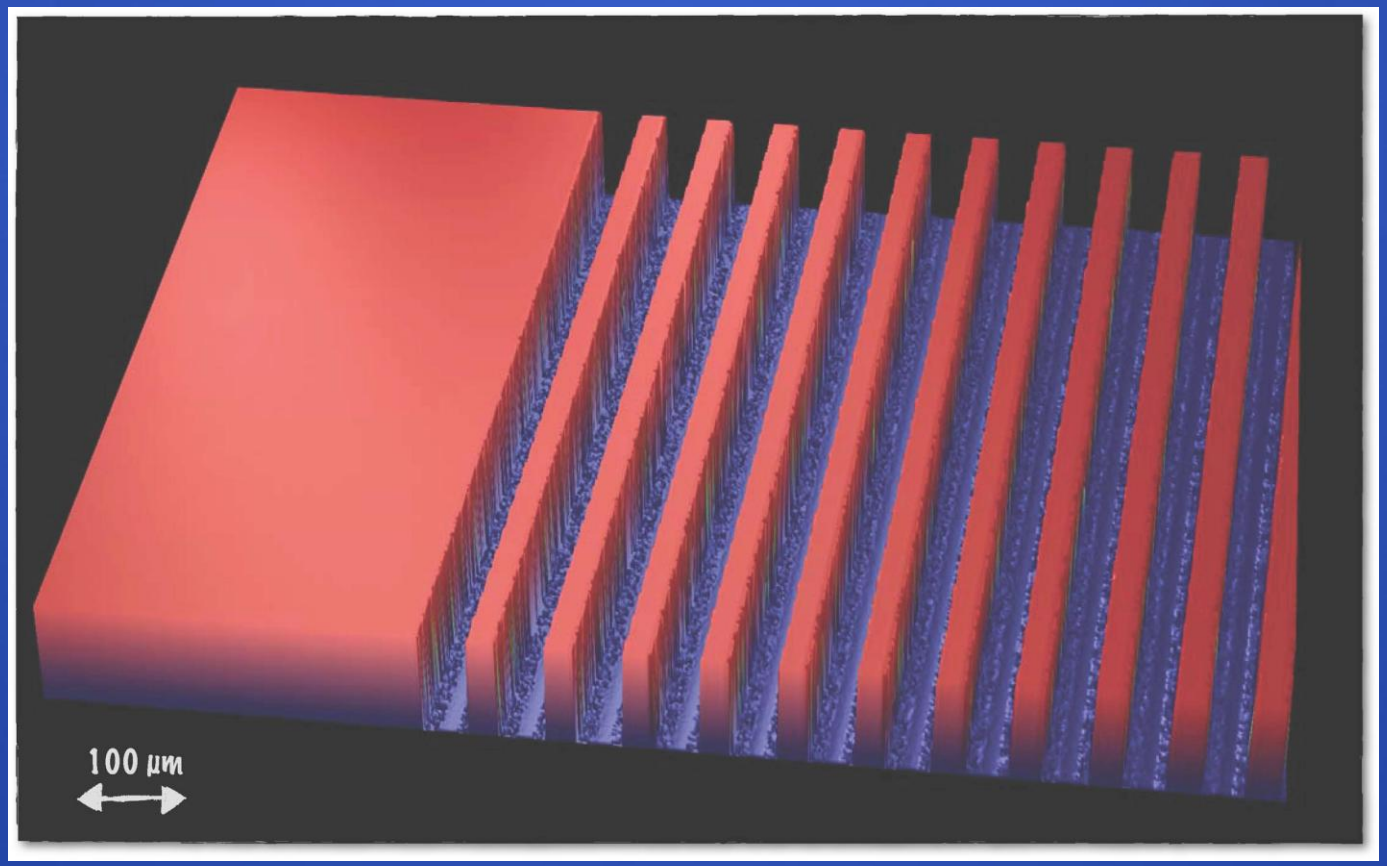
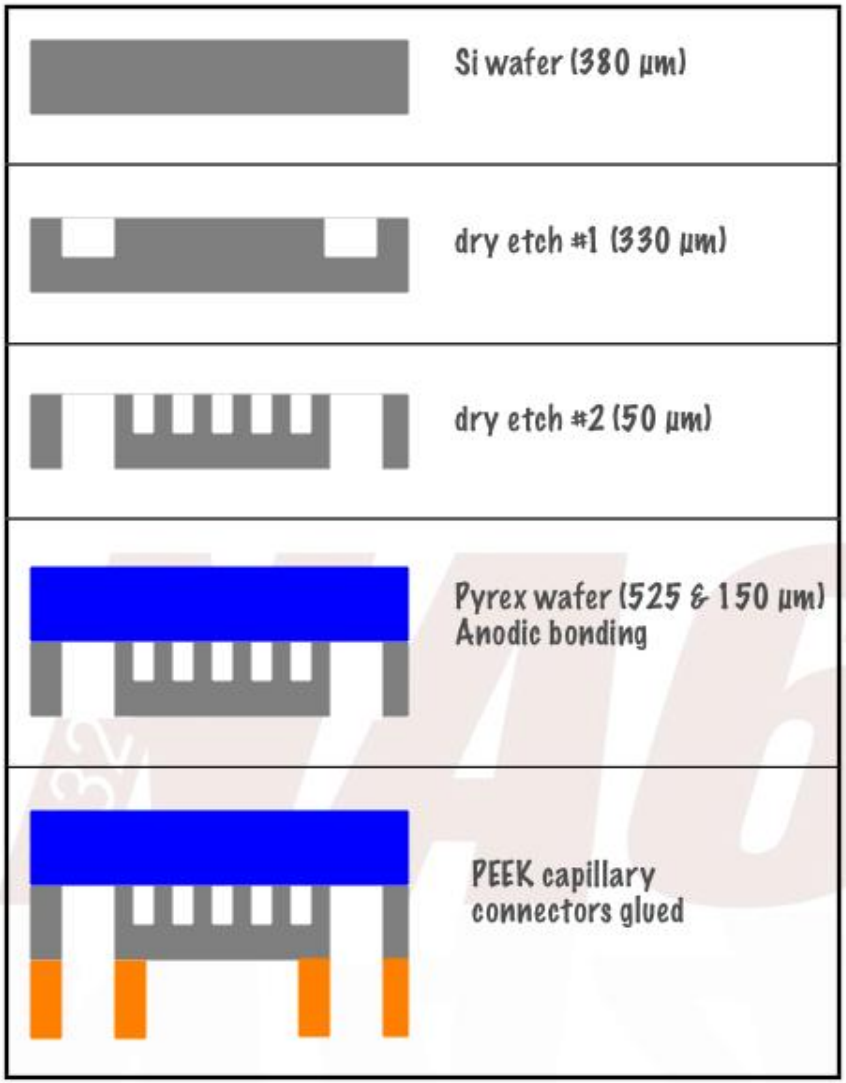
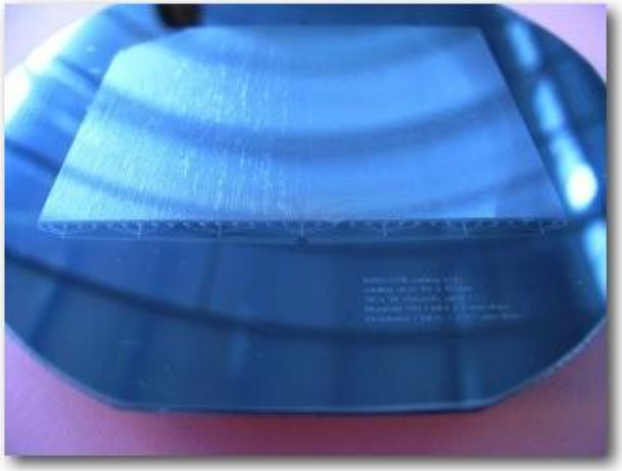
Mapelli, Nüssle


CMI TEST 21279

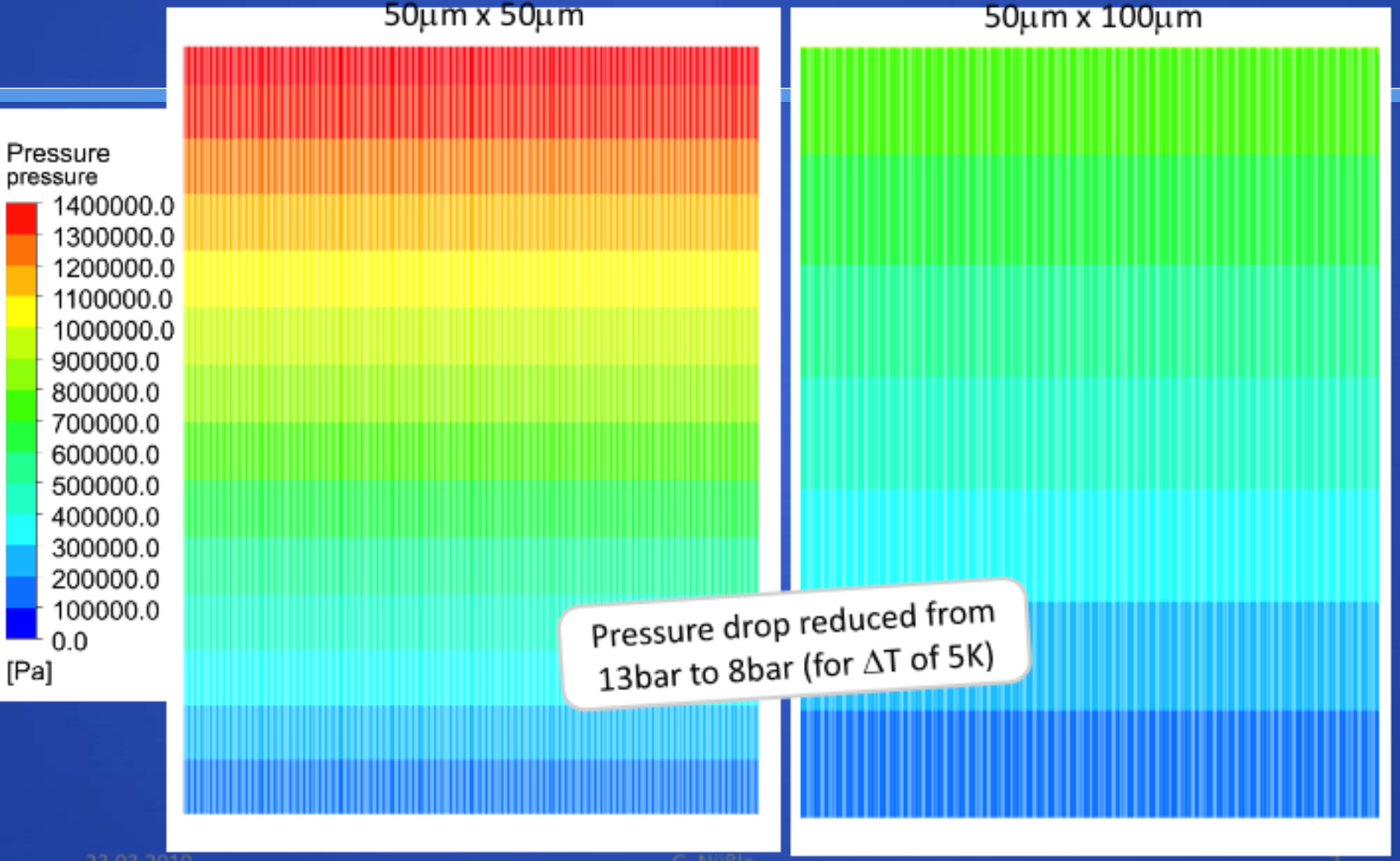

100 µm

CERN / EPFL process - proto 3



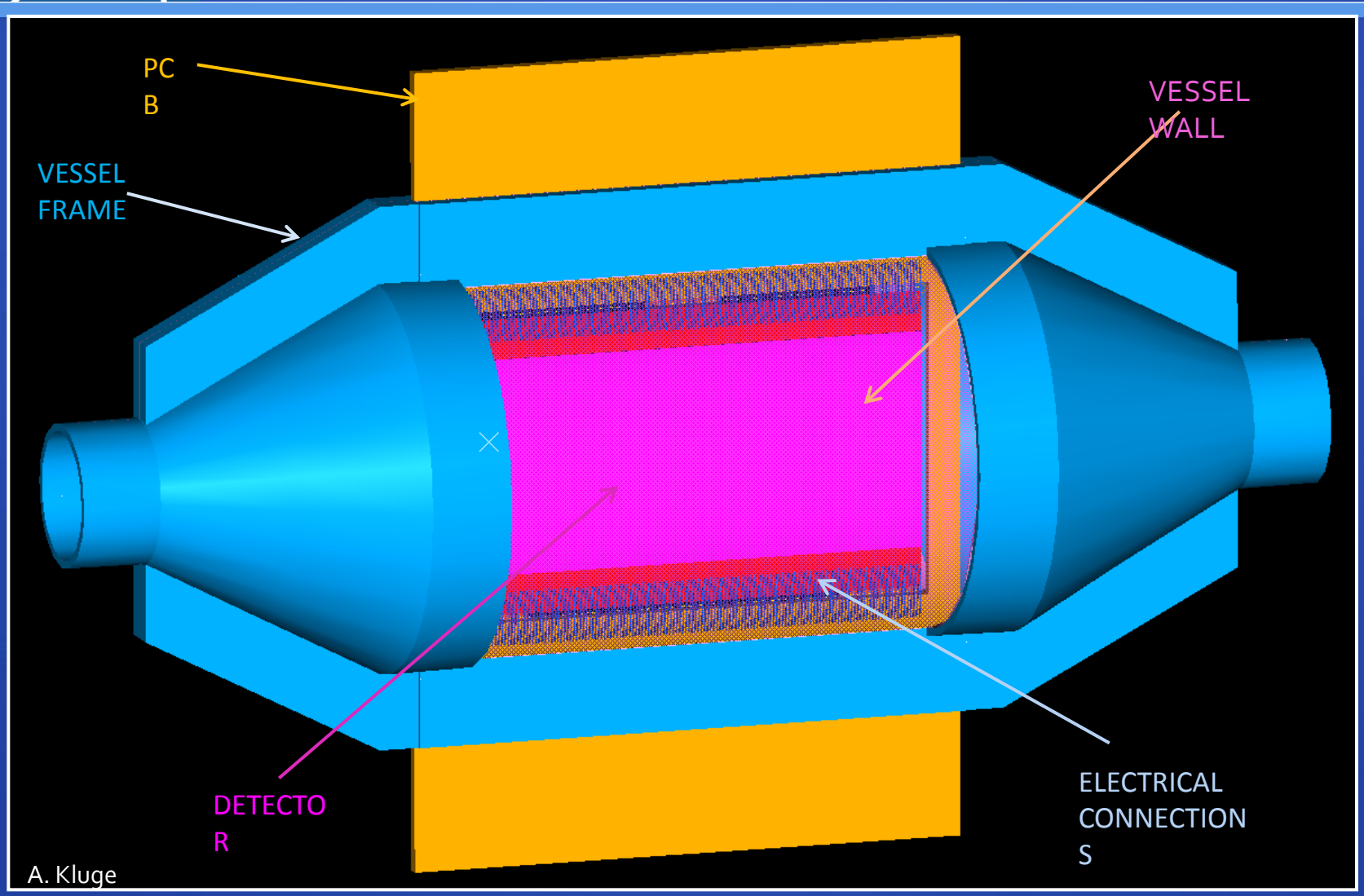


Micro Channel Design – CFD Simulation for different cross sections



Cooling vessel

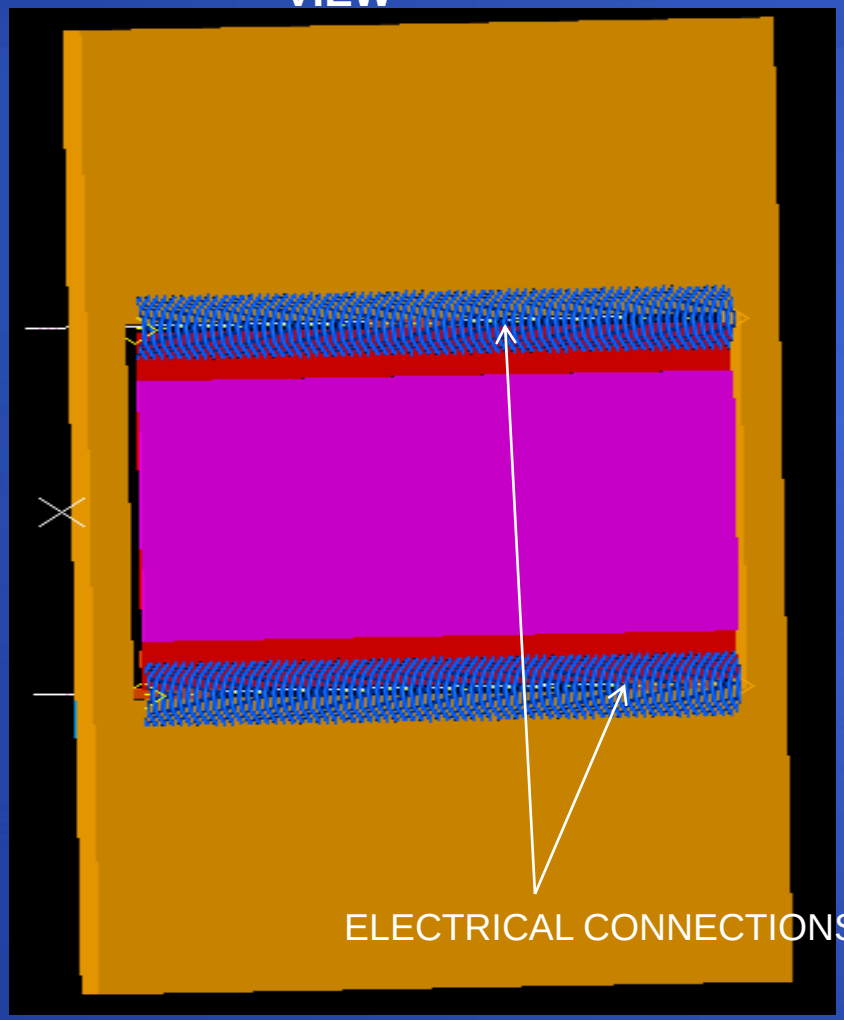
Cooling vessel



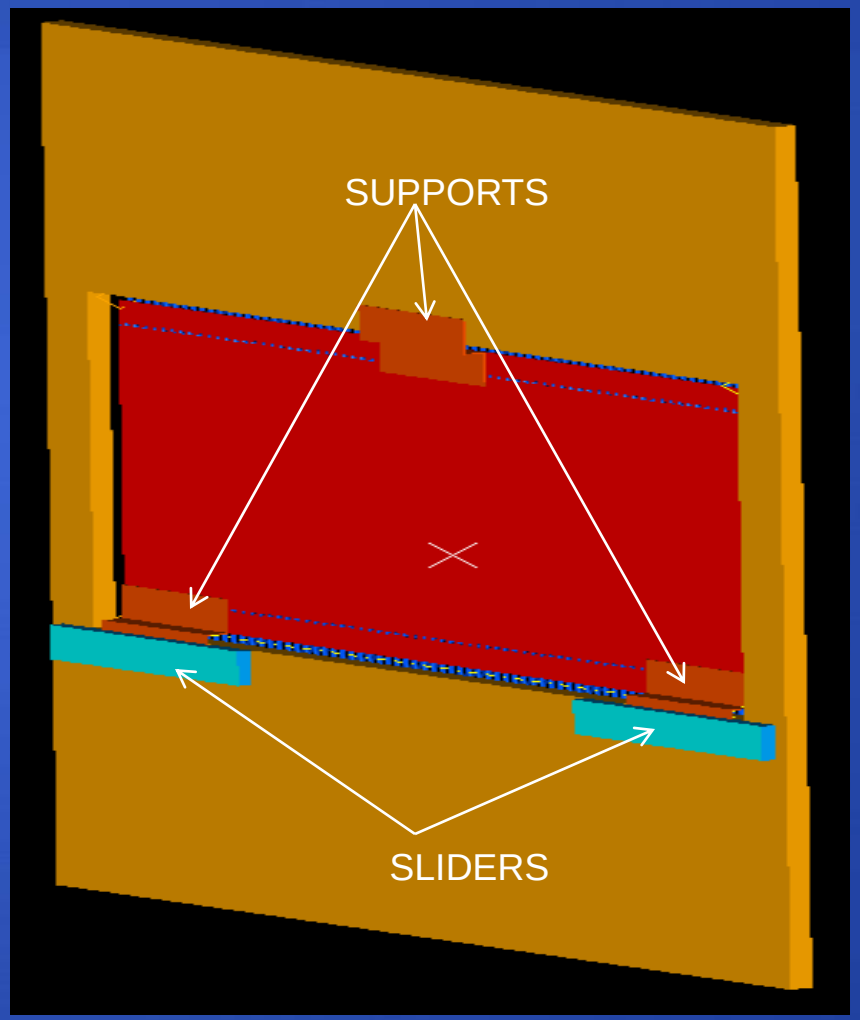
A. Kluge

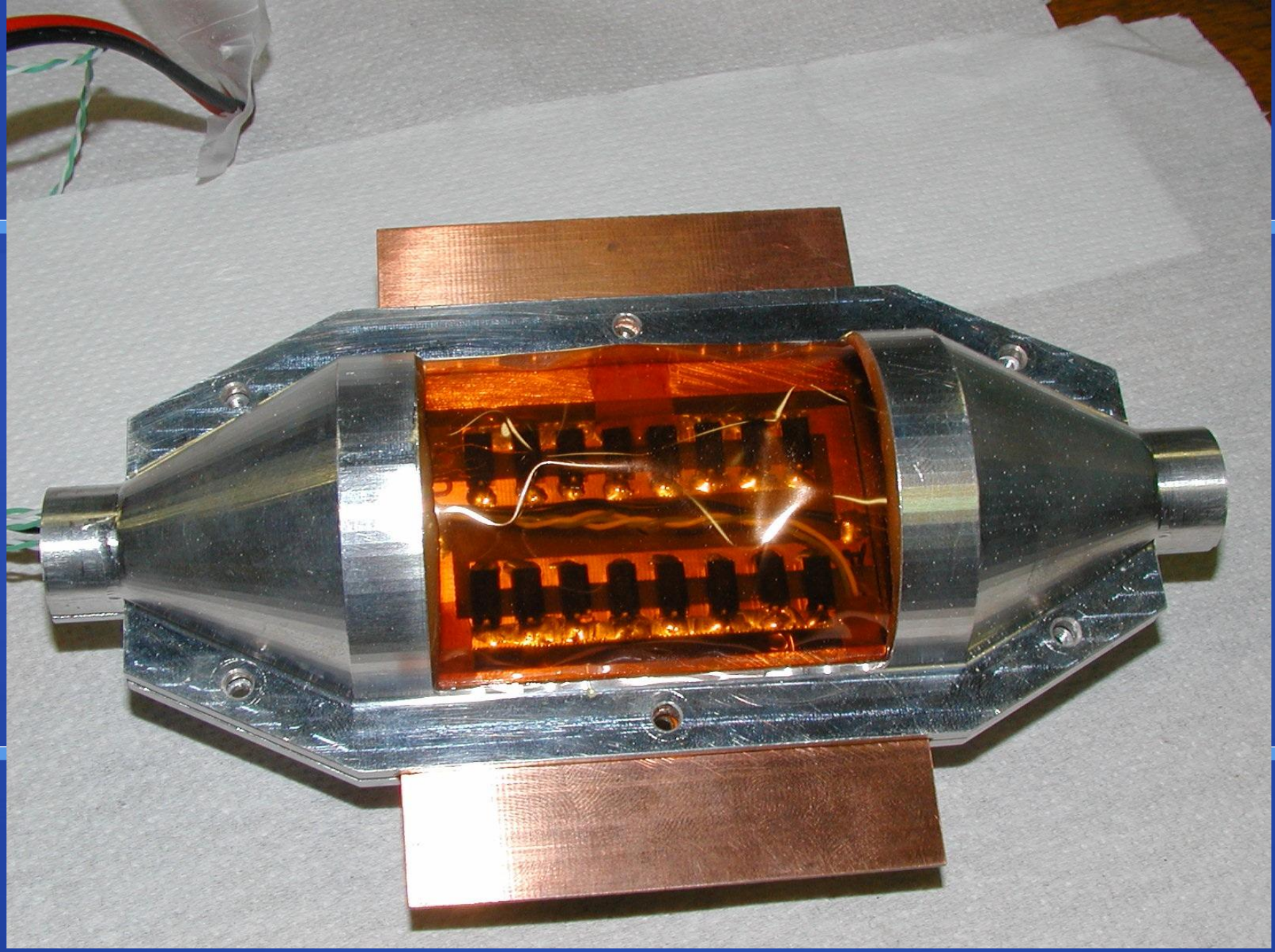
DETECTOR – PCB ASSEMBLY

FRONT VIEW



BACK VIEW





Summary

- ALICE SPD & NA62 GTK are LHC-type hybrid pixel detectors
- Analog consumes significant power because of timing response (25ns / 3 ns)
- Material budget: 1% -> 0.45 %
- Micro-channel cooling: GTK first application in HEP

data rate & can pulsing be done

- can power pulsing be done or is the read-out rate too high?
- occupancy: 10 (-50) hits /mm²/312 bx
- assume chip of: 10 mm x 10 mm and pixel size of 50 µm x 50 µm => 200 x 200 pixel = 40000 pixels = 16 bit address
  time stamping 1 bx out of 312 = 9 bit
  occupancy => 10 hits/mm² * 100 mm² / 40000= 1000 / 40000= 2.5%
- No trigger: Chip Data rate/ 312 bx => 1000 hits * 32 bit = 32000 bit
  32 kbit/20ms = 1.6 Mbit/s
  32 kbit/312 bx= 200 Gbit/s
- No trigger: Data rate /cm² = 1.6 Mbit/s continous