# RD50-MPW2 active pixel matrix measurements

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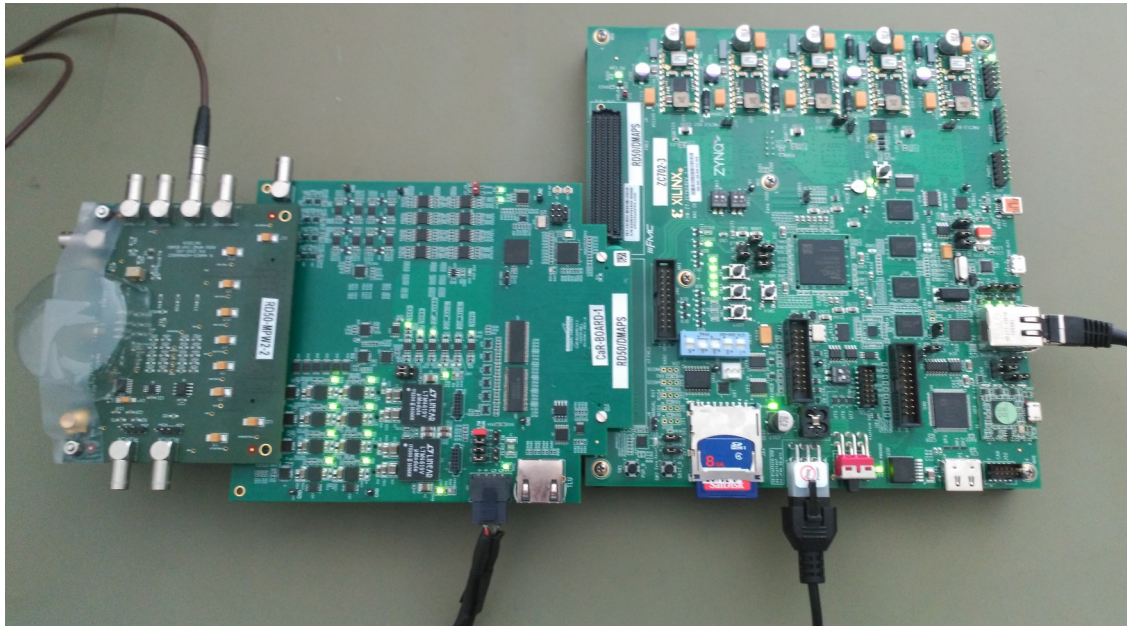
# RD50-MPW2 active pixel matrix measurements setup

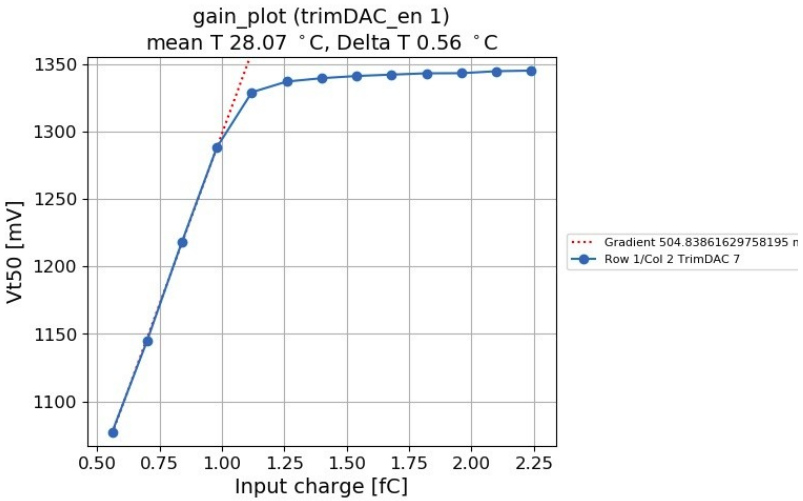
- Two RD50-MPW2 chip boards used:
  - RD50-MPW2-2: RD50-MPW2 W10 device bonded (1.9 kΩ·cm). Gain/noise with HV applied to active matrix.
  - RD50-MPW2-3: RD50-MPW2 W14 device bonded (> 2 kΩ·cm). Gain/noise with HV applied to active matrix.
- FMC CaR board, ZC702 board and own firmware/software used.
  - VHDL blocks for RD50-MPW2 stream data generation, analog buffer control, test pulse generation and comparator pulse readout.
  - Linux running in Zynq ARM (from SD card).
  - Python scripts and UIO driver/I2C driver for controlling the system.

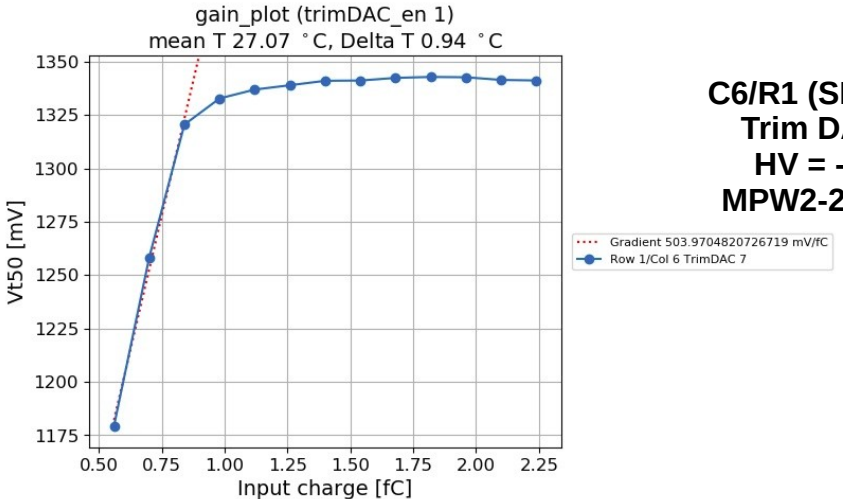


# RD50-MPW2 gain measurements

- Measurement details: **RD50-MPW2 W10 and W14 comparison.**
  - 400 test pulses generated (100 us of width and 1 ms of period). Amplitude 200 mV to 800 mV. **Input charge.**
  - Two types of pixels measured: **C2/R1 (CR pixel) and C6/R1 (SR pixel)**.
  - Nominal values of bias voltage registers. BL 900 mV. TH variation adjusted to pixel (2 mV step).
  - TrimDAC enabled and programmed to 7. **HV = -60 V.**

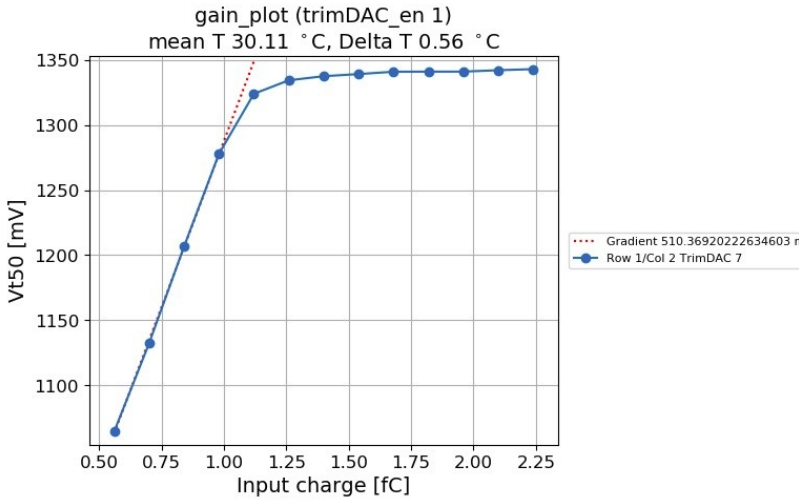
**C2/R1 (CR pixel) Trim DAC 7. HV = -60 V. MPW2-2 (W10).**

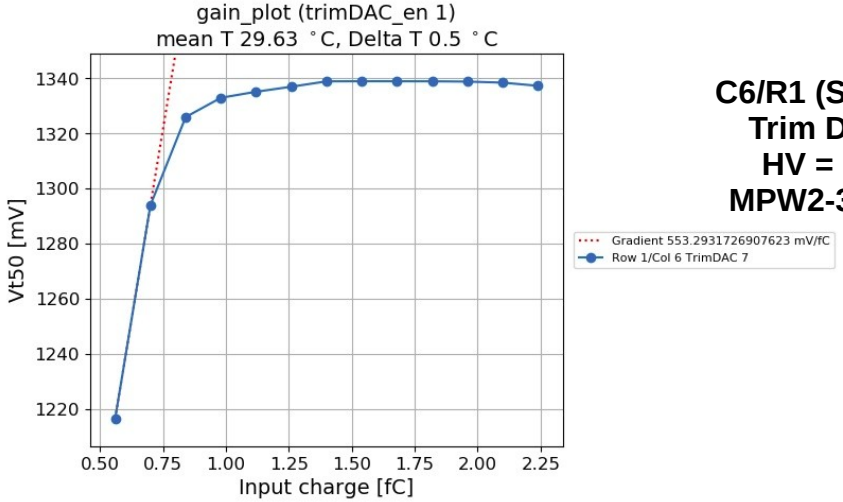



**C6/R1 (SR pixel). Trim DAC 7. HV = -60 V. MPW2-2 (W10).**

**C2/R1 (CR pixel) Trim DAC 7. HV = -60 V. MPW2-3 (W14).**



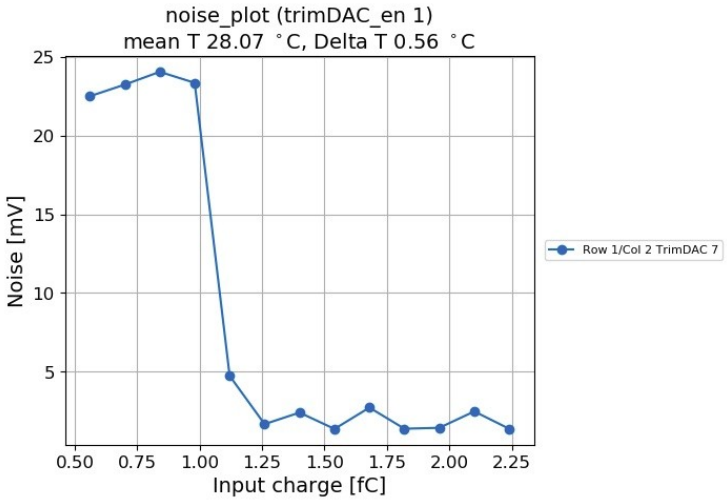



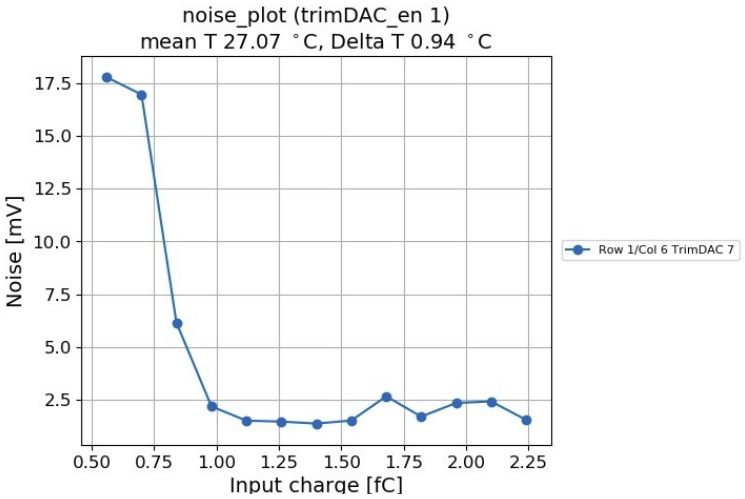

**C6/R1 (SR pixel). Trim DAC 7. HV = -60 V. MPW2-3 (W14).**

# RD50-MPW2 noise measurements

- Measurement details: **RD50-MPW2 W10 and W14 comparison.**
  - 400 test pulses generated (100 us of width and 1 ms of period). Amplitude 200 mV to 800 mV. **Input charge.**
  - Two types of pixels measured: **C2/R1 (CR pixel) and C6/R1 (SR pixel).**
  - Nominal values of bias voltage registers. BL 900 mV. TH variation adjusted to pixel (2 mV step).
  - TrimDAC enabled and programmed to 7. **HV = -60 V.**

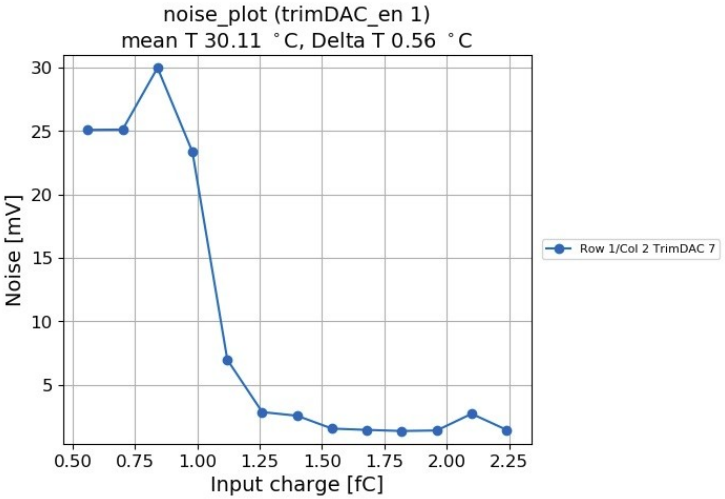
**C2/R1 (CR pixel). Trim DAC 7. HV = -60 V. MPW2-2 (W10).**

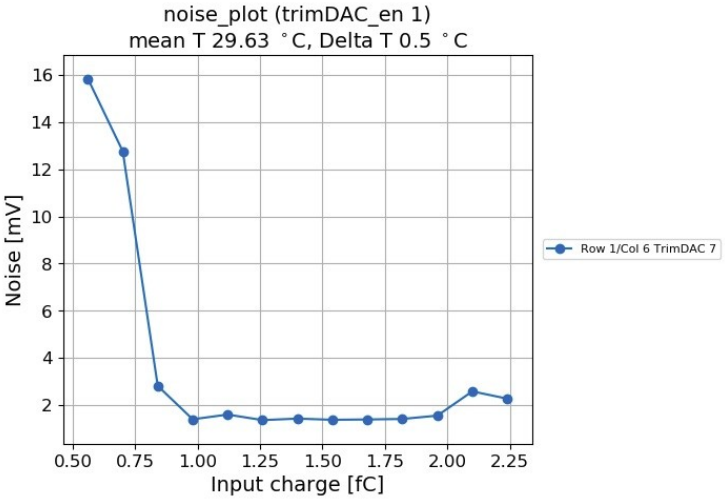



**C6/R1 (SR pixel). Trim DAC 7. HV = -60 V. MPW2-2 (W10).**

**C2/R1 (CR pixel). Trim DAC 7. HV = -60 V. MPW2-3 (W14).**

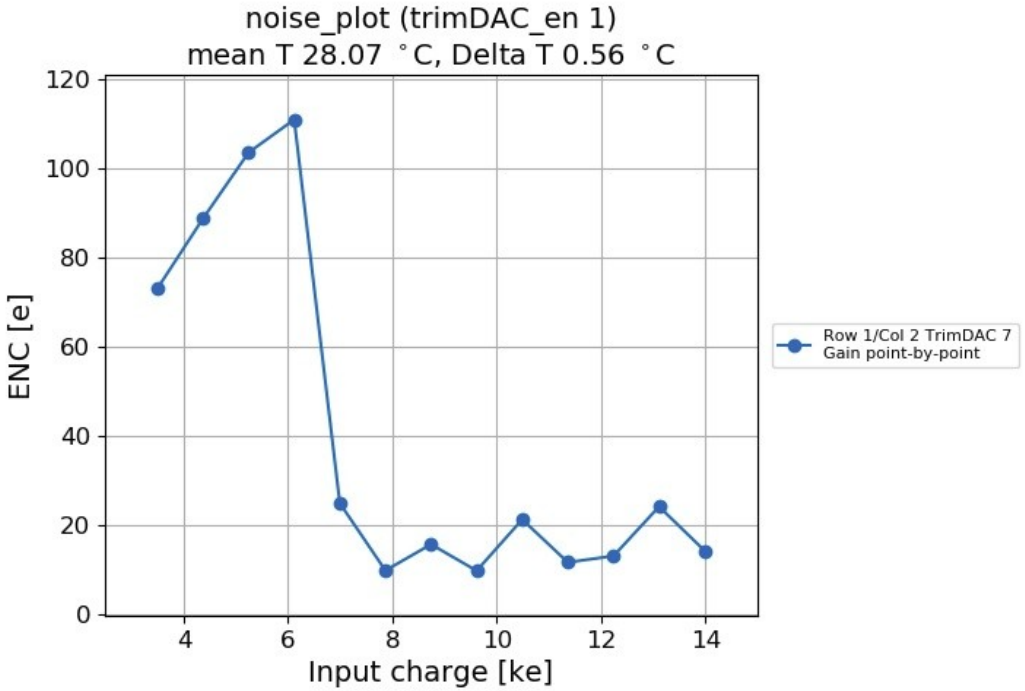


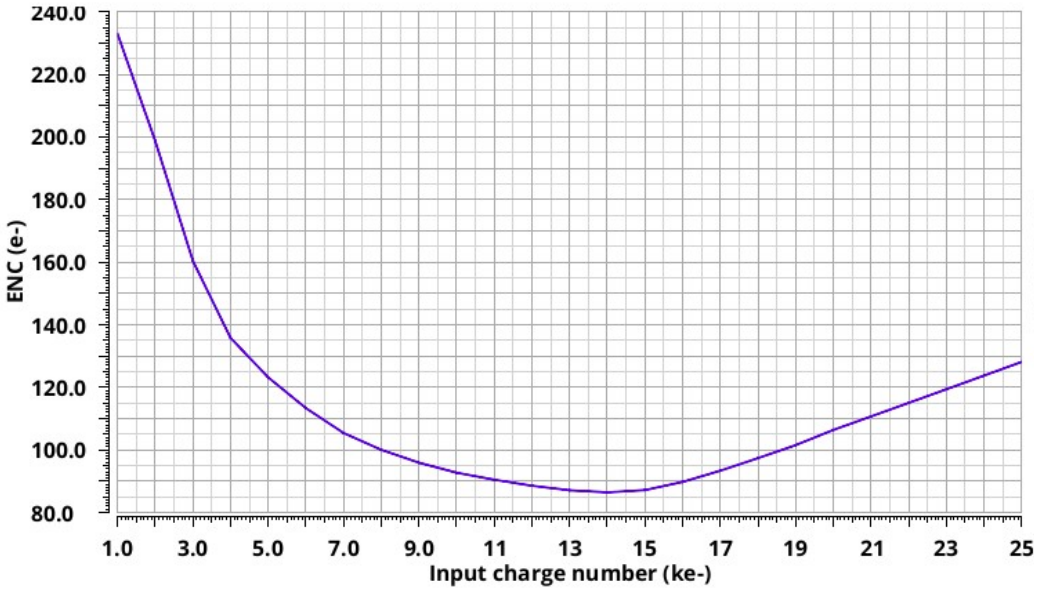

**C6/R1 (SR pixel). Trim DAC 7. HV = -60 V. MPW2-3 (W14).**

# RD50-MPW2 noise measurements

- **Noise referred to input of CSA**: from standard noise measurements (**MPW2-2, W10**).
  - Two types of pixels measured: **C2/R1 (CR pixel)** and C6/R1 (SR pixel)**.**
  - Divide noise by gain of CSA (calculated point-by-point as mV/fC) and show data in e instead of fC to compare with simulation results.
  - Simulation results for charge injected through pixel (Cpixel with HV -60 V) and measured results for charge injected through calibration circuit (Cinj) with HV applied (Cpixel with HV -60 V).
  - Same order of magnitude and noise behaviour.



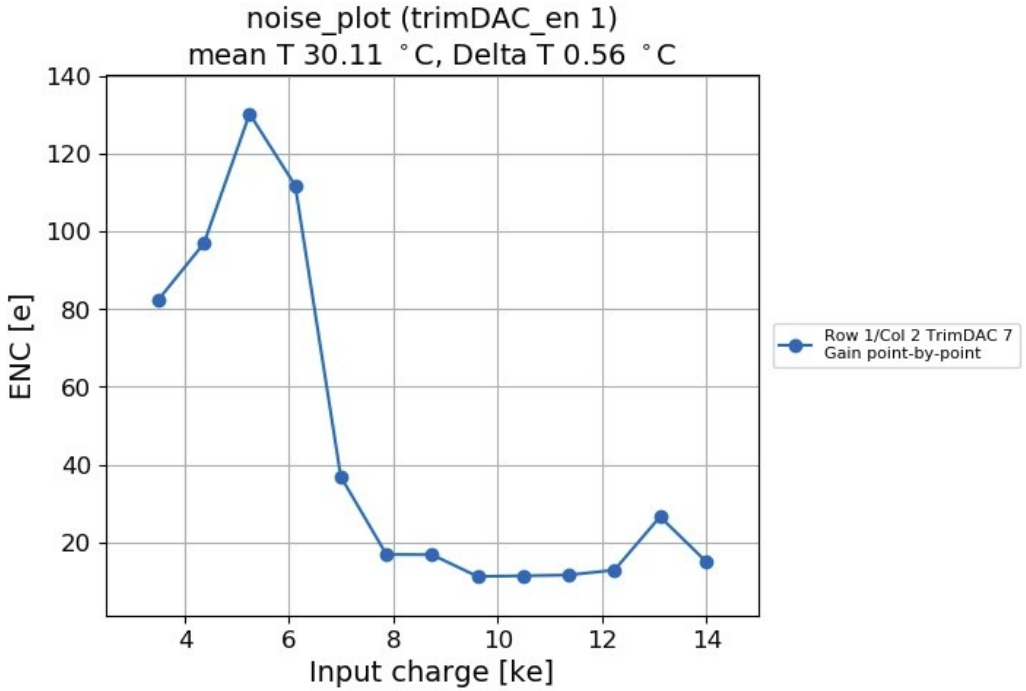

**C2/R1 (CR pixel). Trim DAC 7. HV = -60 V. MPW2-2 (W10).**



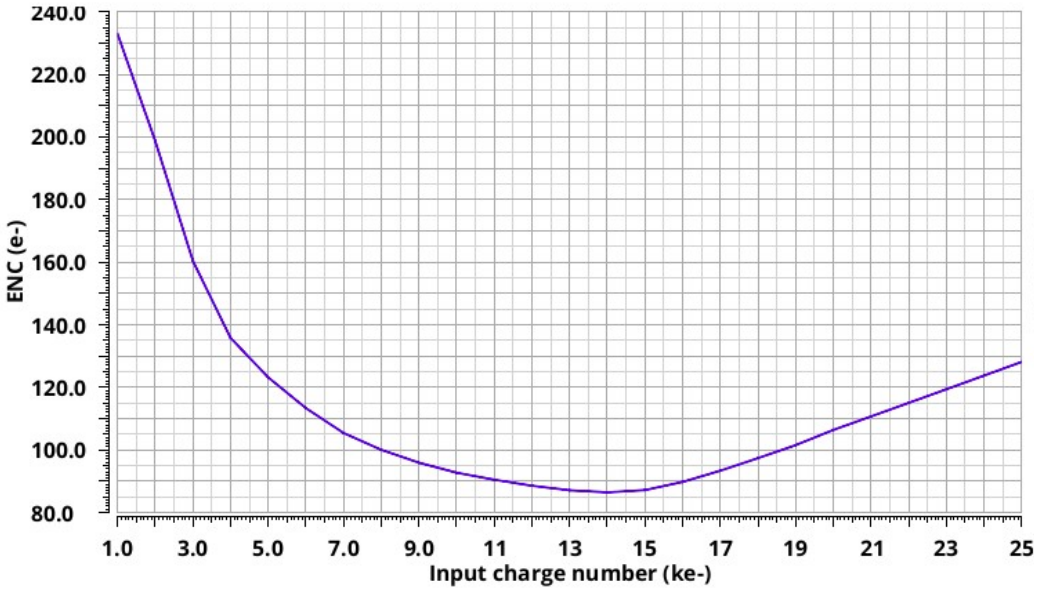

**Simulation results for a CR pixel with injected charge through pixel (HV -60 V).**

# RD50-MPW2 noise measurements

- **Noise referred to input of CSA**: from standard noise measurements (**MPW2-3, W14**).
  - Two types of pixels measured: **C2/R1 (CR pixel)** and C6/R1 (SR pixel)**.**
  - Divide noise by gain of CSA (calculated point-by-point as mV/fC) and show data in e instead of fC to compare with simulation results.
  - Simulation results for charge injected through pixel (Cpixel with HV -60 V) and measured results for charge injected through calibration circuit (Cinj) with HV applied (Cpixel with HV -60 V).
  - Same order of magnitude and noise behaviour.



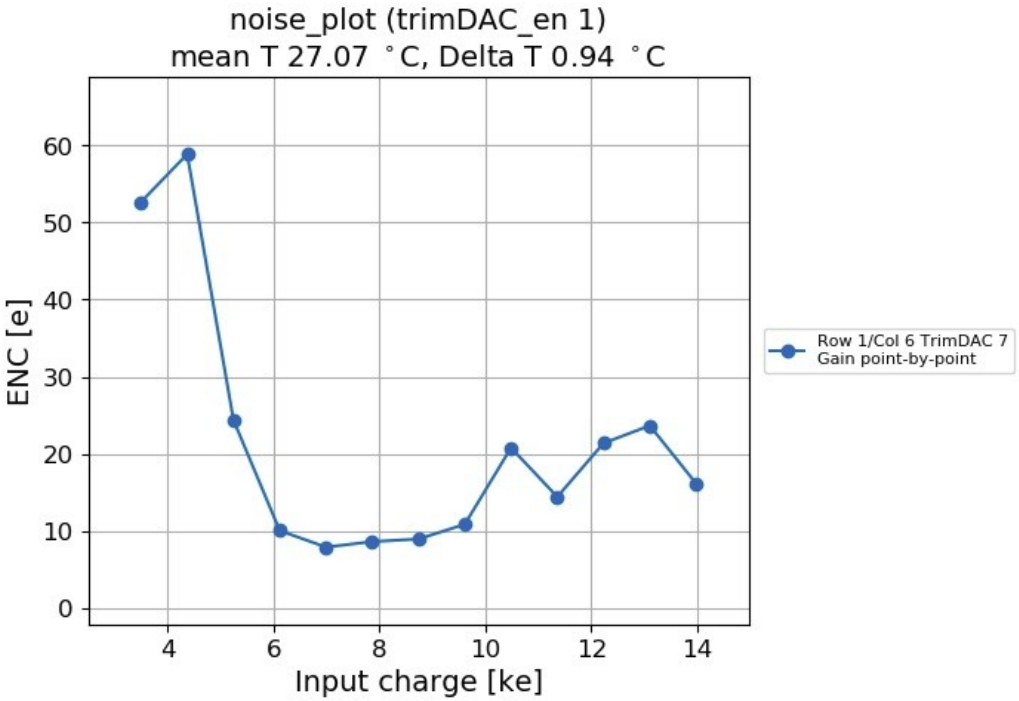

**C2/R1 (CR pixel). Trim DAC 7. HV = -60 V. MPW2-3 (W14).**



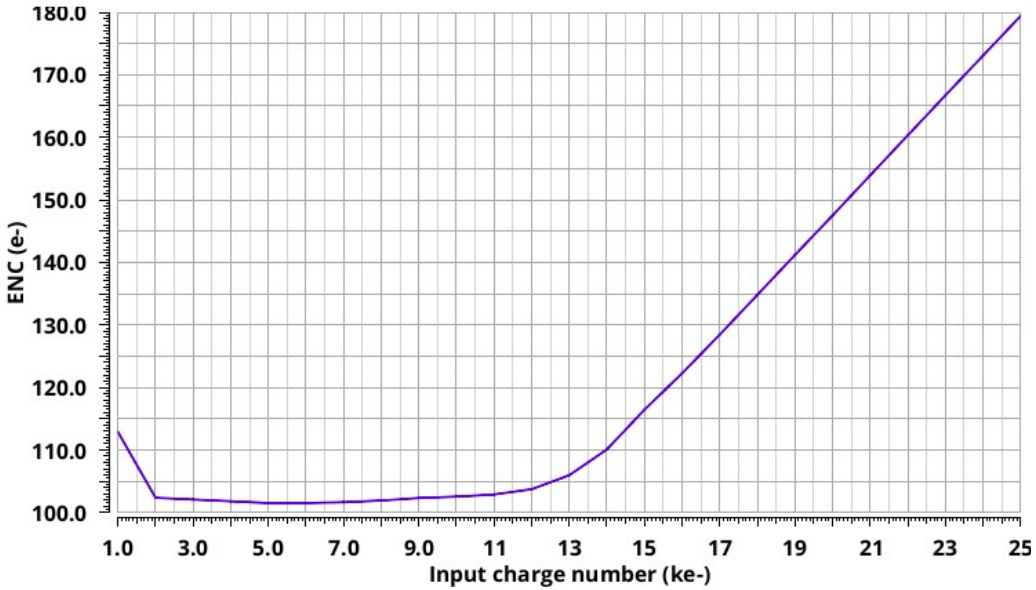

**Simulation results for a CR pixel with injected charge through pixel (HV -60 V).**

# RD50-MPW2 noise measurements

- **Noise referred to input of CSA**: from standard noise measurements (**MPW2-2, W10**).
  - Two types of pixels measured: C2/R1 (CR pixel) and **C6/R1 (SR pixel).**
  - Divide noise by gain of CSA (calculated point-by-point as mV/fC) and show data in e instead of fC to compare with simulation results.
  - Simulation results for charge injected through pixel (Cpixel with HV -60 V) and measured results for charge injected through calibration circuit (Cinj) with HV applied (Cpixel with HV -60 V).
  - Same order of magnitude but different noise behaviour.



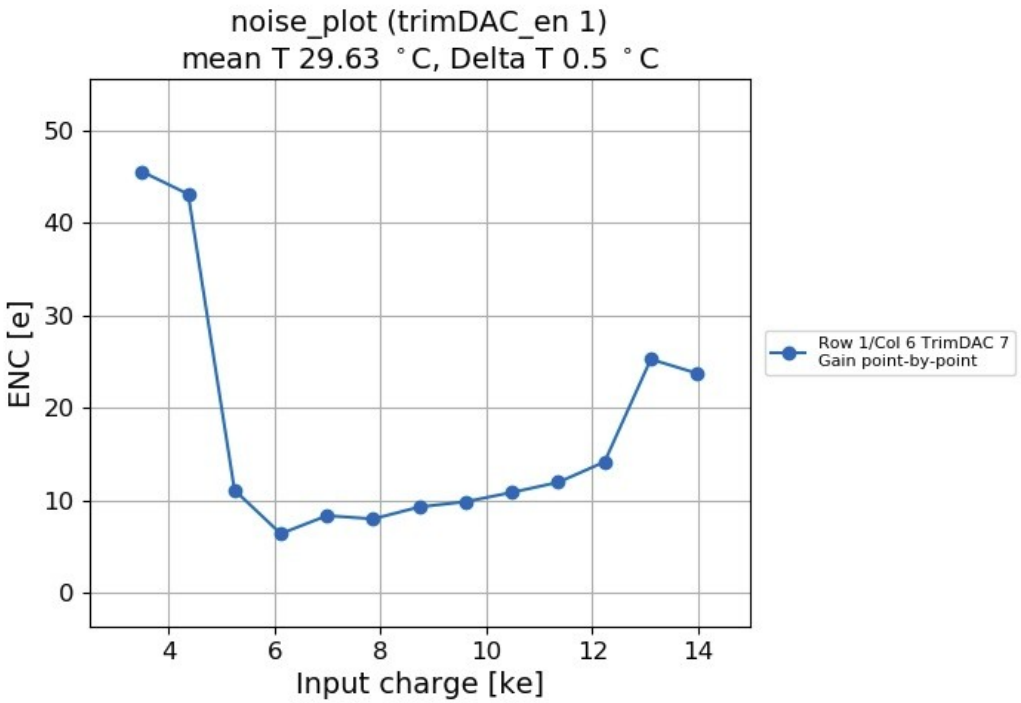

**C6/R1 (SR pixel). Trim DAC 7. HV = -60 V. MPW2-2 (W10).**



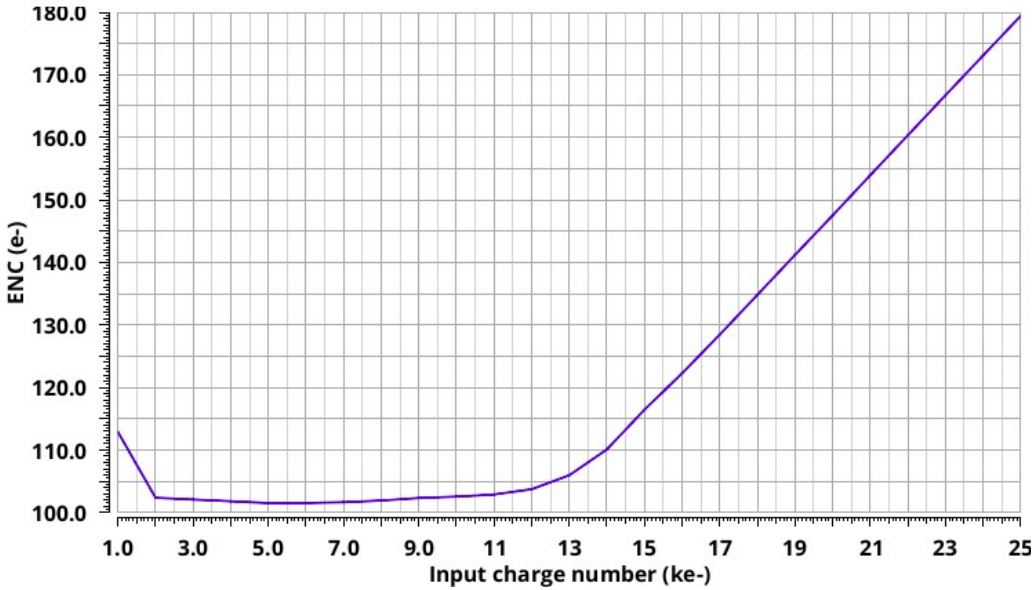

**Simulation results for a SR pixel with injected charge through pixel (HV -60 V).**

# RD50-MPW2 noise measurements

- **Noise referred to input of CSA**: from standard noise measurements (**MPW2-3, W14**).
  - Two types of pixels measured: C2/R1 (CR pixel) and **C6/R1 (SR pixel).**
  - Divide noise by gain of CSA (calculated point-by-point as mV/fC) and show data in e instead of fC to compare with simulation results.
  - Simulation results for charge injected through pixel (Cpixel with HV -60 V) and measured results for charge injected through calibration circuit (Cinj) with HV applied (Cpixel with HV -60 V).
  - Same order of magnitude but different noise behaviour.




**C6/R1 (SR pixel). Trim DAC 7. HV = -60 V. MPW2-3 (W14).**




**Simulation results for a SR pixel with injected charge through pixel (HV -60 V).**

# Next steps

- Follow agreed measurements of excel file.
  - Measurements with radioactive source.
  - Measurements with irradiated devices (neutron and TID).
- Continue with IV and CV measurements of test structures (non-irradiated and irradiated devices).
- Design of RD50-MPW3 slow control.
- ...

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