

CERN EP-ESE Electronics Seminars

Cryogenic Readout Electronics Systems for Liquid Argon TPCs in Neutrino Experiments

Shanshan Gao
On behalf of BNL CE Team
September 15, 2020

**BROOKHAVEN**
NATIONAL LABORATORY

a passion for discovery



U.S. DEPARTMENT OF
ENERGY

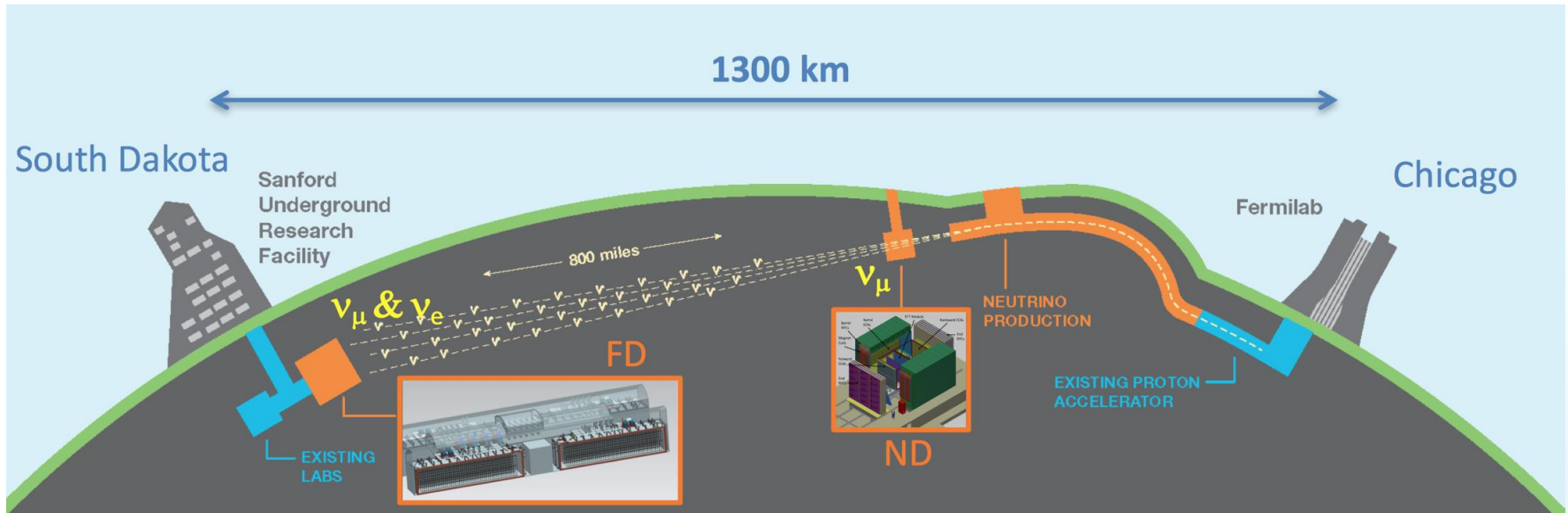
Office of
Science

Outline

- **Liquid Argon TPC in Neutrino Experiments**
 - **Cryogenic Readout Electronics (CE)**
 - Advantages
 - A Brief History
 - R&D on CMOS Cryogenic Electronics
 - **Cryogenic Readout Electronics Systems Applied in LArTPCs**
 - ProtoDUNE-SP
 - DUNE Far Detector
- } Long Baseline Neutrino Experiments**
- **Summary**

Only focus on single phase LAr TPC detector with wire electrode in neutrino experiments

Long Baseline Neutrino Program: LBNF/DUNE



An international flagship experiment to unlock the mysteries of neutrinos

Three major discovery areas



Origin of Matter

DUNE scientists will look at the differences in behavior between neutrinos and antineutrinos, aiming to find out whether neutrinos are the reason the universe is made of matter.



Unification of forces

DUNE's search for the signal of proton decay—a signal so rare it has never been seen—will move scientists closer to realizing Einstein's dream of a unified theory of matter and energy.

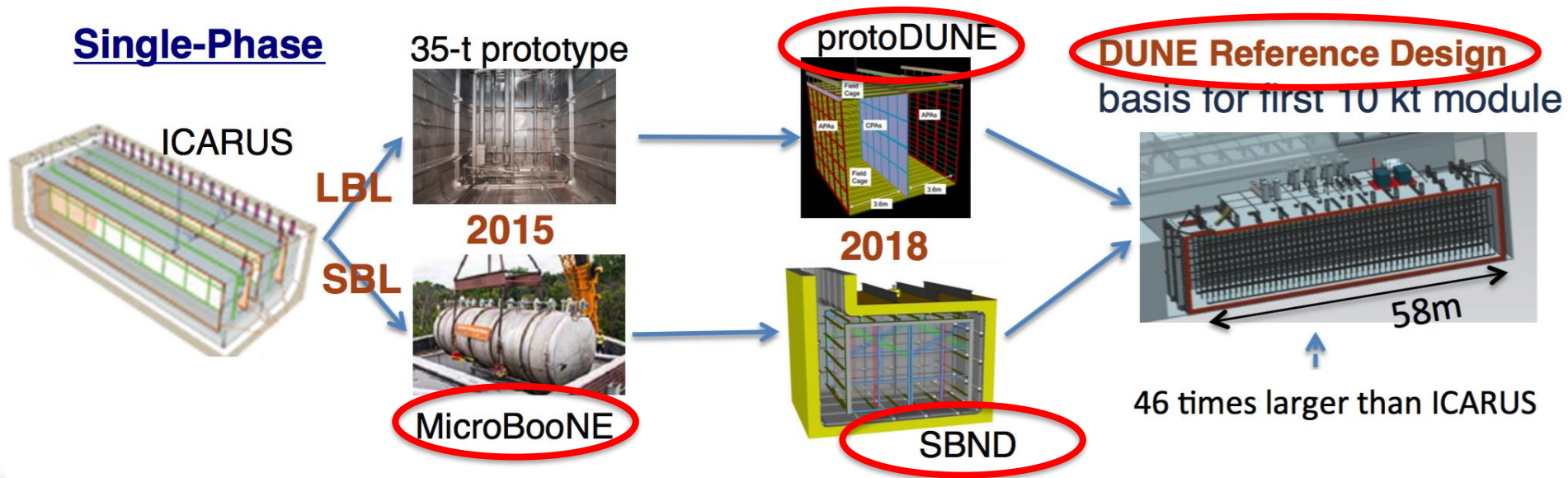


Black hole formation

DUNE will look for the gigantic streams of neutrinos emitted by exploding stars to watch the formation of neutron stars and black holes in real time, and learn more about these mysterious objects in space.

Development of LArTPC for Neutrino Experiments

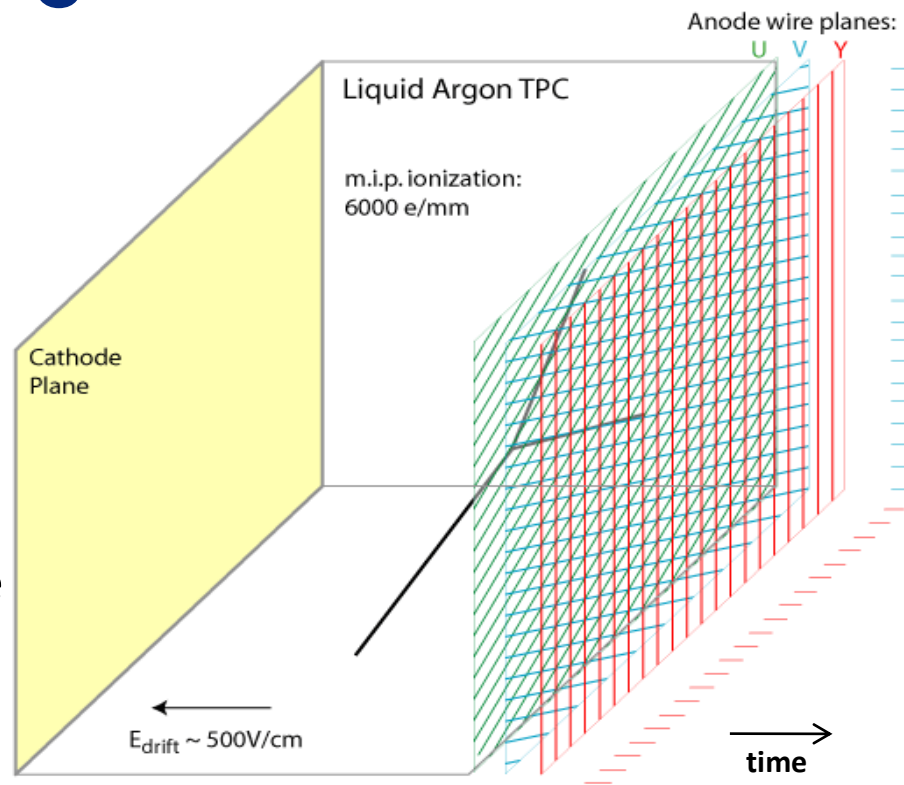
- BNL is **leading** TPC readout electronics **SYSTEM** design
 - Including MicroBooNE and SBND as part of the Short Baseline Neutrino Program



Note: Dual-Phase LArTPC is not included in this talk

Liquid Argon TPC

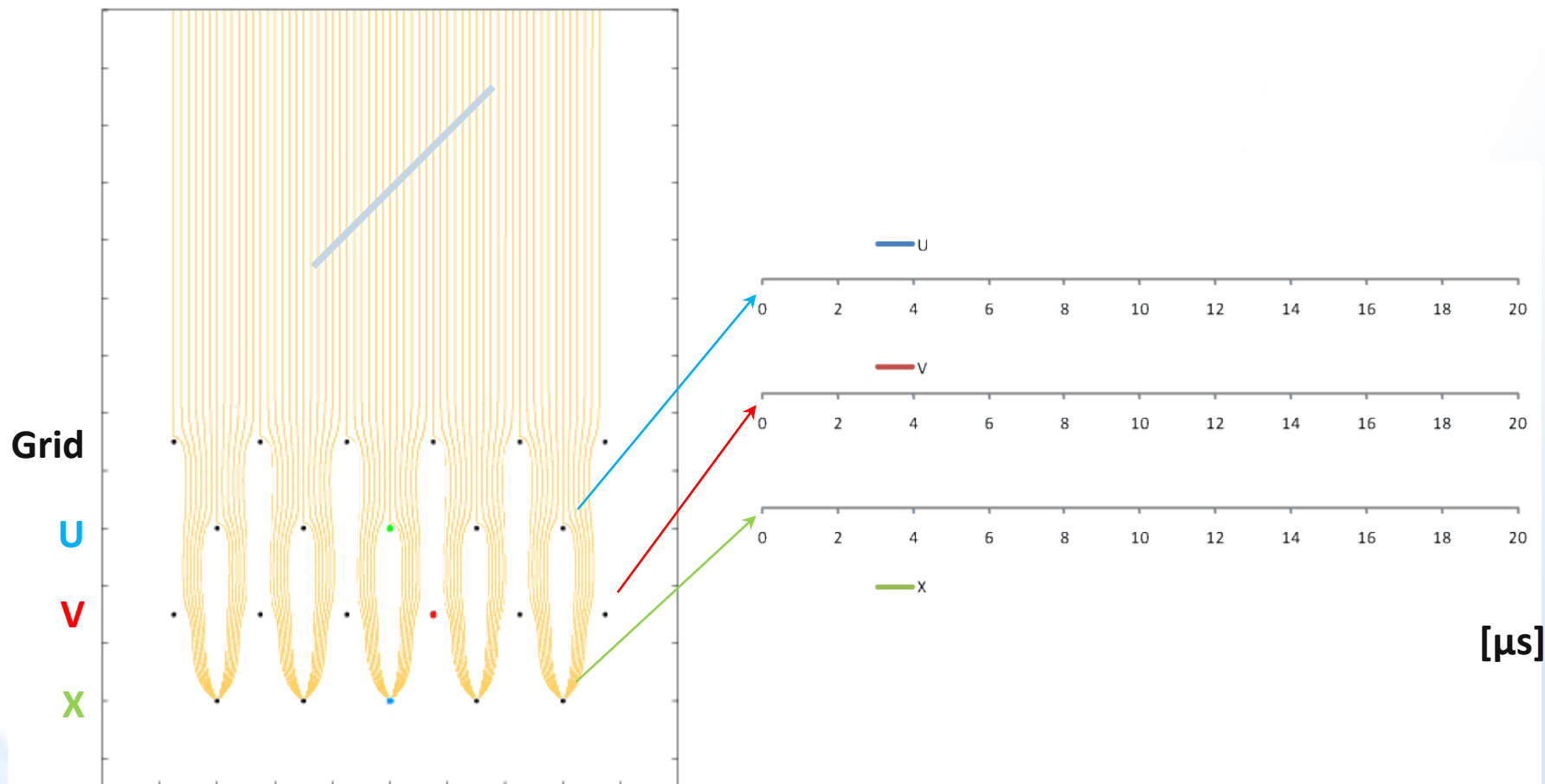
Charged particles passing through detector ionize the argon atoms, and the ionization electrons drift in the electric field to the anode wall on a timescale of milliseconds. The anode consists of layers of active wires forming a grid.



- 3 Wire Plane readout with Excellent Space and Energy resolution
- 3D-imaging: full event topology reconstruction
- Higher sensitivity to neutrino physics and for some of the proton decay channels (e.g. $p \rightarrow K\nu$)

NP04 (ProtoDUNE-SP) CERN Beam Test

Signal Formation: Induced Signals from a Track Segment



DUNE style wire arrangement: 3 instrumented wire planes + 1 grid plane
Raw current waveforms convolved with a $0.5\mu\text{s}$ gaussian to mimic diffusion

Signals in LAr TPC

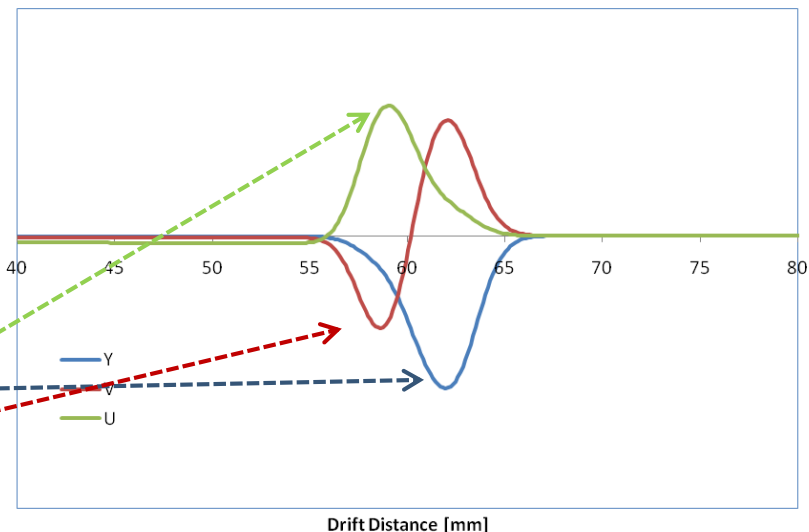
■ Charge signal is very small

- There is no electron amplification inside LAr
- A 3mm MIP track should create $210\text{keV/mm} \times 3\text{mm} / 23.6\text{eV/e} = 4.3\text{fC}$
- After a 1/3 initial recombination loss: $\sim 2.8\text{fC}$
- Assume the drift path to equal the charge life time, reducing the signal to $1/e \approx 0.368$
- The expected signal for 3mm wire spacing is then $\approx 1\text{fC} = 6250\text{ e}$, ... and for 5mm, $\approx 10^4\text{ e}$, for the “collection signal”
- The induction signals are smaller
- The time scale of TPC signals is determined by the **wire plane spacing** and **electron drift velocity**, ($\sim 1.5\text{ mm}/\mu\text{s}$ at 500 V/cm)

Noise Sensitive!

Induced Current Waveforms on 3 Sense Wire Planes

0° track, $0.6\mu\text{s}$ rms "diffusion", 3×3 cell



S:N requirement to “distinguish a Minimum Ionizing Particle (MIP) track cleanly from electronic noise everywhere within the drift volume.”

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 - DUNE Far Detector

} Long Baseline Neutrino Experiments
- Summary

Cryogenic Electronics is the Optimal solution for Noble LArTPCs

Cold electronics for “Giant” Liquid Argon Time Projection Chambers

1st International Workshop towards the Giant Liquid Argon Charge Imaging Experiment (GLA2010)

Veljko Radeka^{1*}, Hucheng Chen¹, Grzegorz Deptuch², Gianluigi De Geronimo¹, Francesco Lanni¹, Shaorui Li¹, Neena Nambiar¹, Sergio Rescia¹, Craig Thorn¹, Ray Yarema², Bo Yu¹

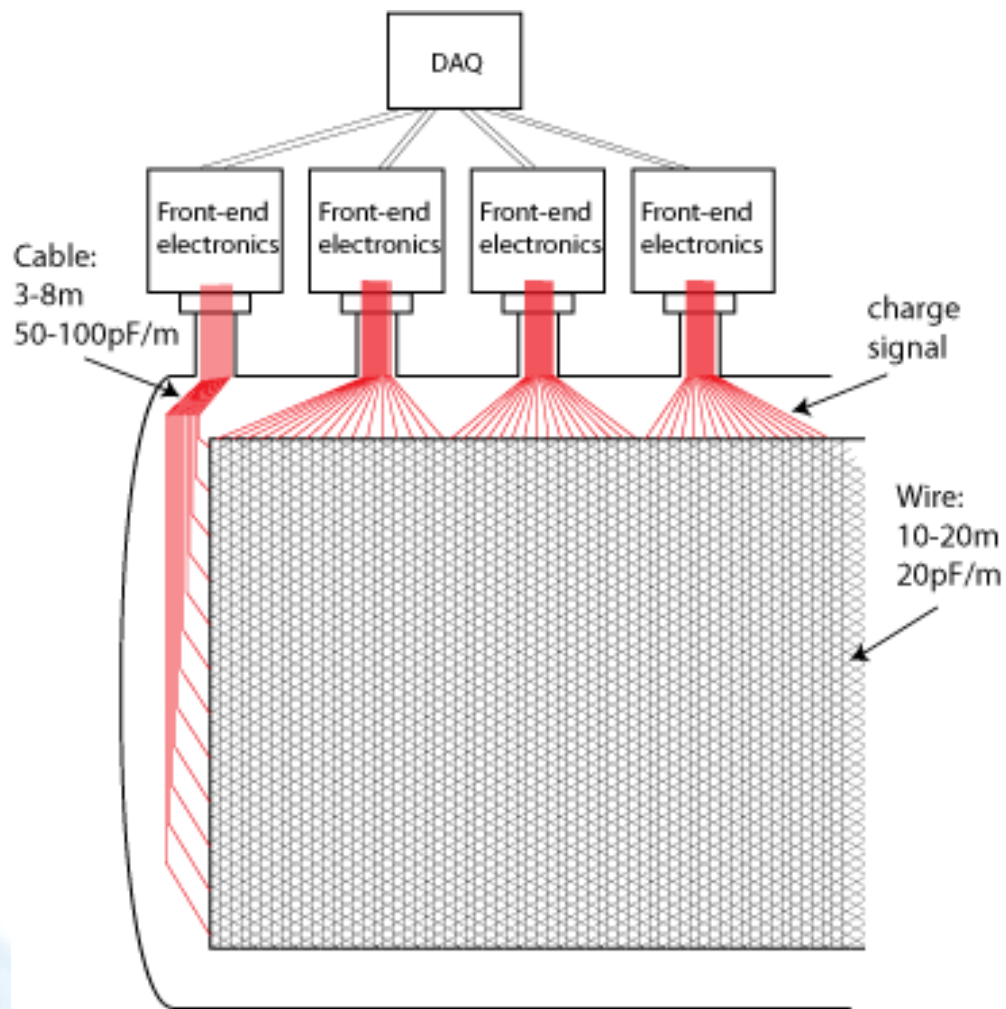
¹ Brookhaven National Laboratory, Upton, NY 11973-5000, USA

² Fermi National Laboratory,

*Correspondence, e-mail: radeka@bnl.gov

Abstract. The choice between cold and warm electronics (inside or outside the cryostat) in very large LAr TPCs (>5-10 ktons) is not an electronics issue, but it is rather a major cryostat design issue. This is because the location of the signal processing electronics has a direct and far reaching effect on the cryostat design, an indirect effect on the TPC electrode design (sense wire spacing, wire length and drift distance), and a significant effect on the TPC performance. All these factors weigh so overwhelmingly in favor of the cold electronics that it remains an optimal solution for very large TPCs. In this paper signal and noise considerations are summarized, the concept of the readout chain is described, and the guidelines for design of CMOS circuits for operation in liquid argon (at ~89 K) are discussed.

“Warm” Electronics



- A typical readout configuration with warm electronics: long cables connect the sense wires to the FEE, resulting in **high capacitance and large electronics noise**.
- To reduce the cable length, one has to implement cold feedthroughs below the liquid level, which **increases the cryostat complexity**.

“Warm” Electronics

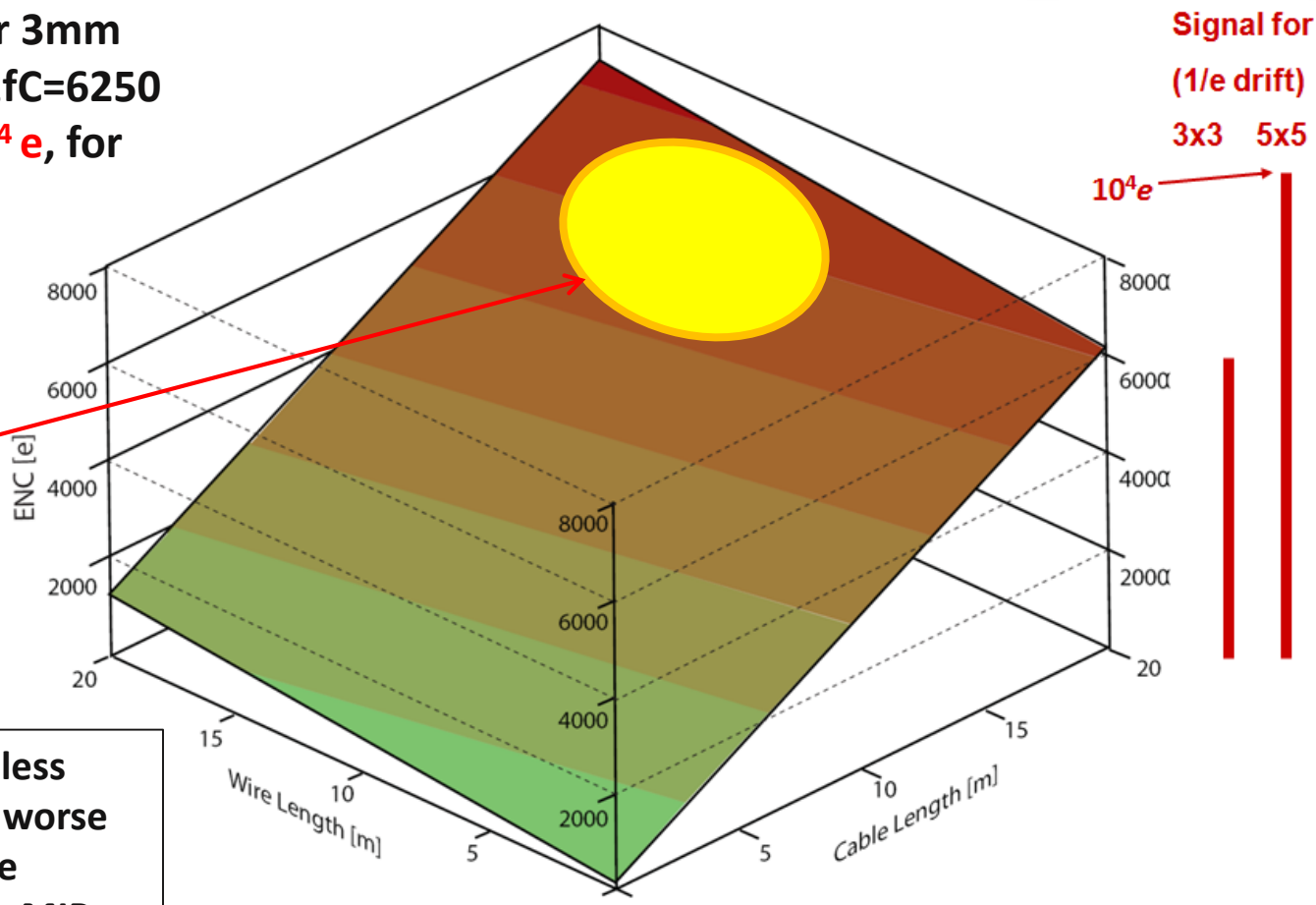
Noise (ENC) vs TPC Sense Wire and Signal Cable Length

MIP Signal for 3x3 and 5x5 mm Sense Wire Spacing

The expected signal for 3mm wire spacing is then $\approx 1fC=6250$ e, ... and for 5mm, $\approx 10^4$ e, for the “collection signal”

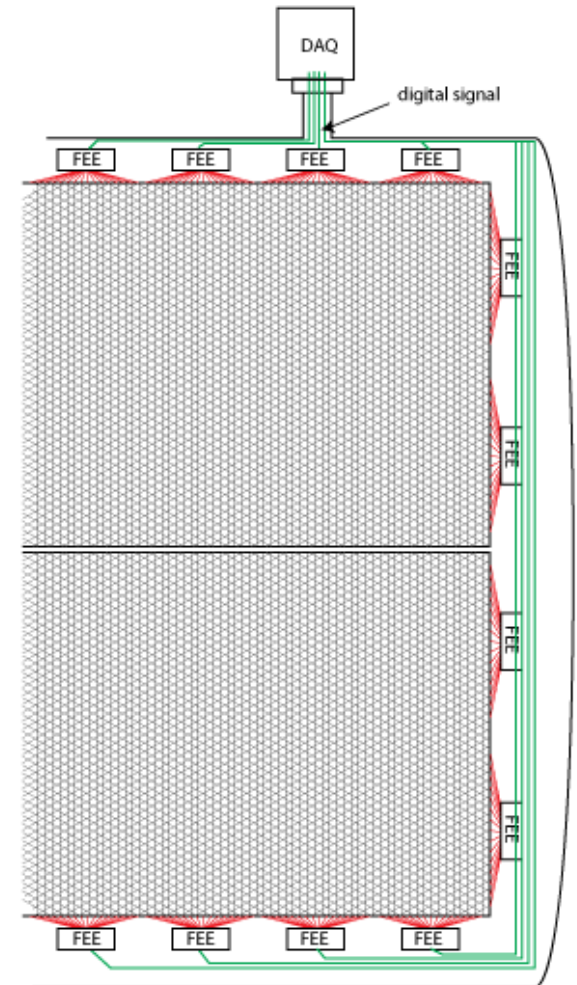
10kton DUNE LArTPC with warm electronics (300K)
ENC $\sim 6 \times 10^3$ e rms

DUNE: Total ENC shall be less than 1/9 of the expected worse case instantaneous charge arriving at the APA from a MIP.



Advantages of Cryogenic (“Cold”) Electronics

- Having front-end electronics in the cryostat, close to the wire electrodes yields **the best SNR. Noise is independent of the fiducial volume.**
- Highly multiplexed circuits with fewer digital output lines not only greatly reduce the number of cryostat penetrations, but also give the designers of both the TPC and the cryostat **the freedom to choose the optimum configurations**

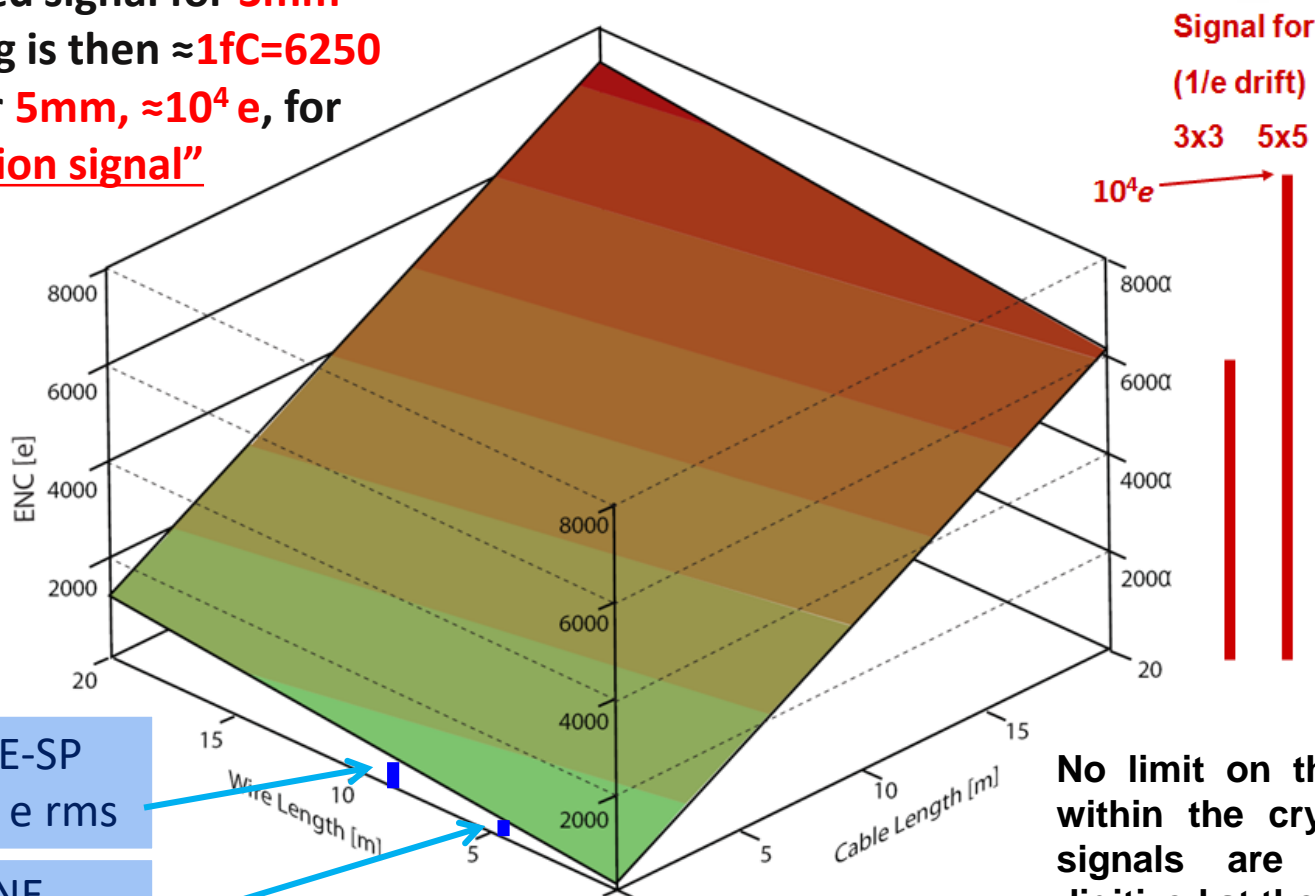


“Cold” Electronics as an Optimal Solution

Noise (ENC) vs TPC Sense Wire and Signal Cable Length

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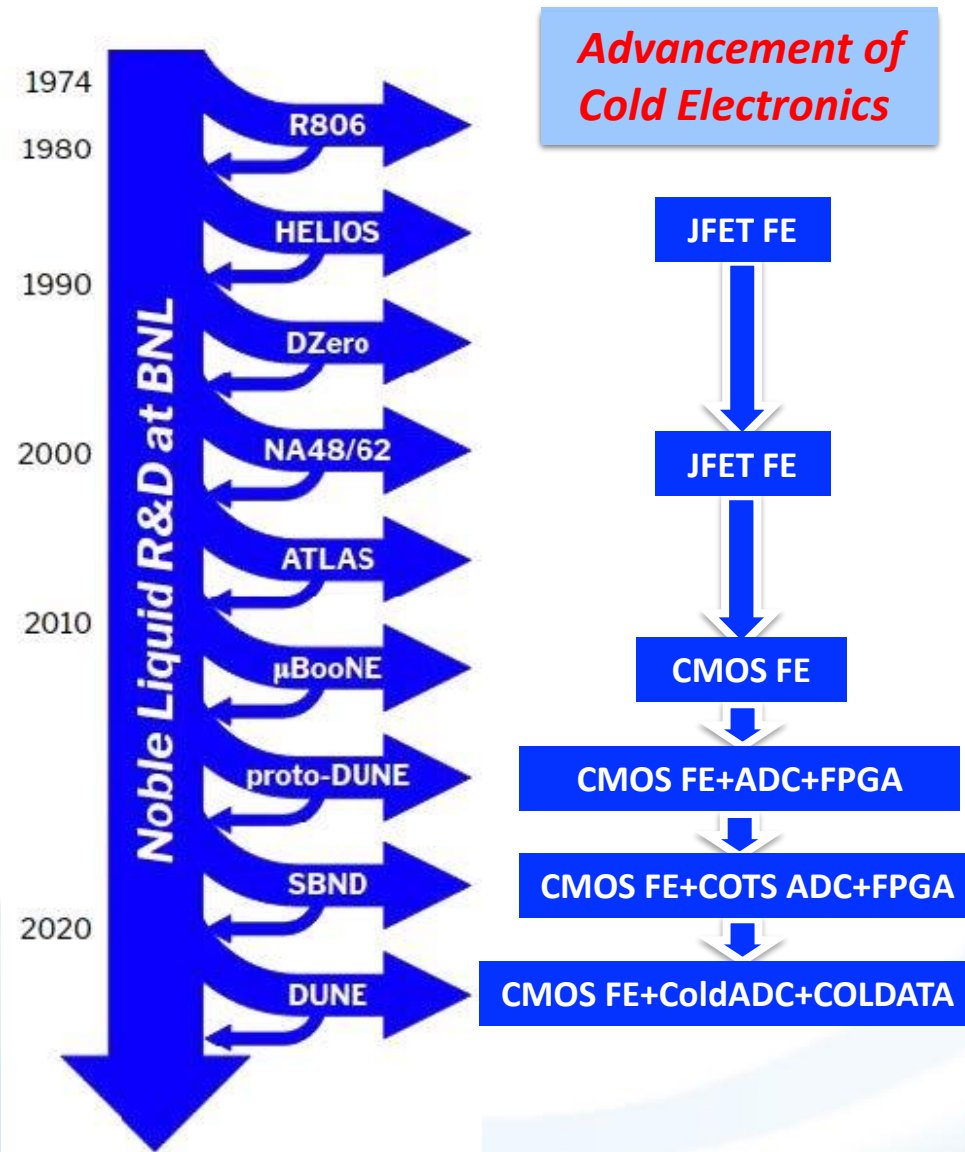


ProtoDUNE-SP
ENC ~ 600 e rms

MicroBooNE
ENC ~ 400 e rms

No limit on the cable length within the cryostat after the signals are amplified and digitized at the sense wires.

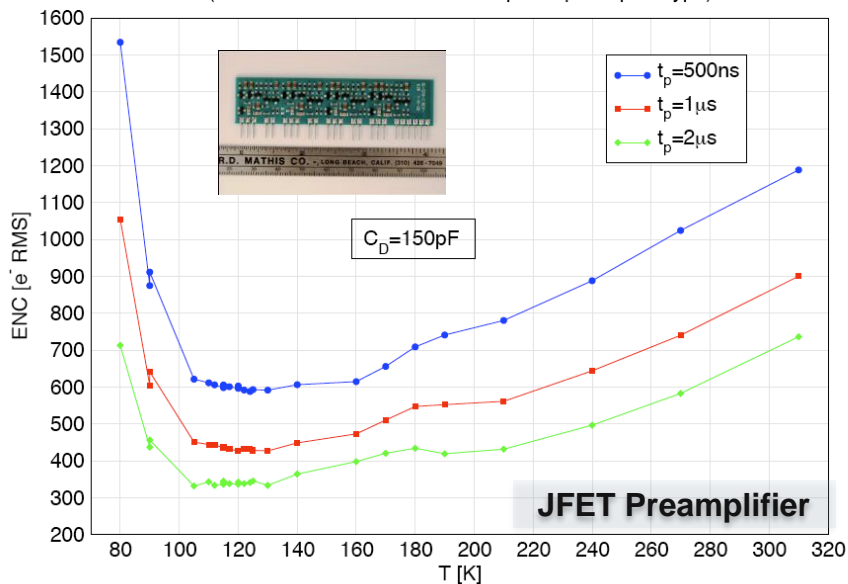
A Brief but Long History of CE Development



- BNL pioneered LAr based detector technology in 1974 ^[1]
- Physics/Engineering expertise which has made essential contributions to various programs, e.g. ATLAS, MicroBooNE
- Unique experience in cryogenic electronics and micro-electronics
- The R&D effort makes the experiments possible; the experiments, in turn, feed information back into the R&D process
- Cryogenic/Cold electronics development is making continuous advancement, from JFET to CMOS, from analog front-end to mixed signal ADC and FPGA
- ***A strong cold electronics team is built up as a core BNL competence, in close collaboration with other institutes, to realize various LAr TPC experiments***
- [1] W. Willis, V. Radeka, Nucl. Instr. Methods, 120 (1974) 221

From JFET to CMOS

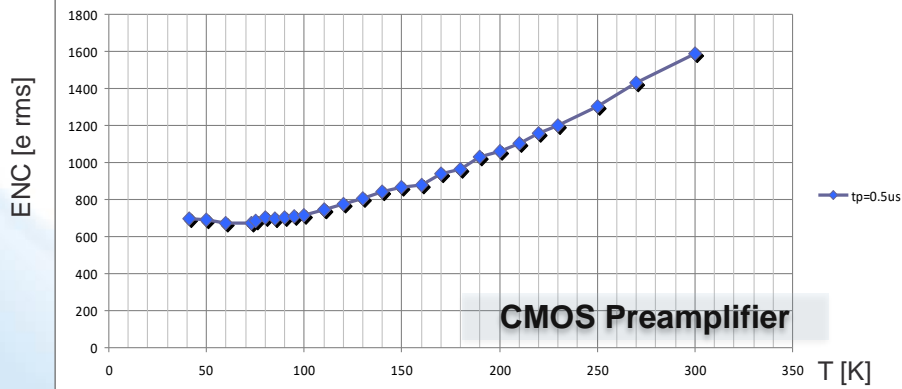
Equivalent Noise Charge vs. Temperature
(First Measurements on a Quad-preamplifier prototype)



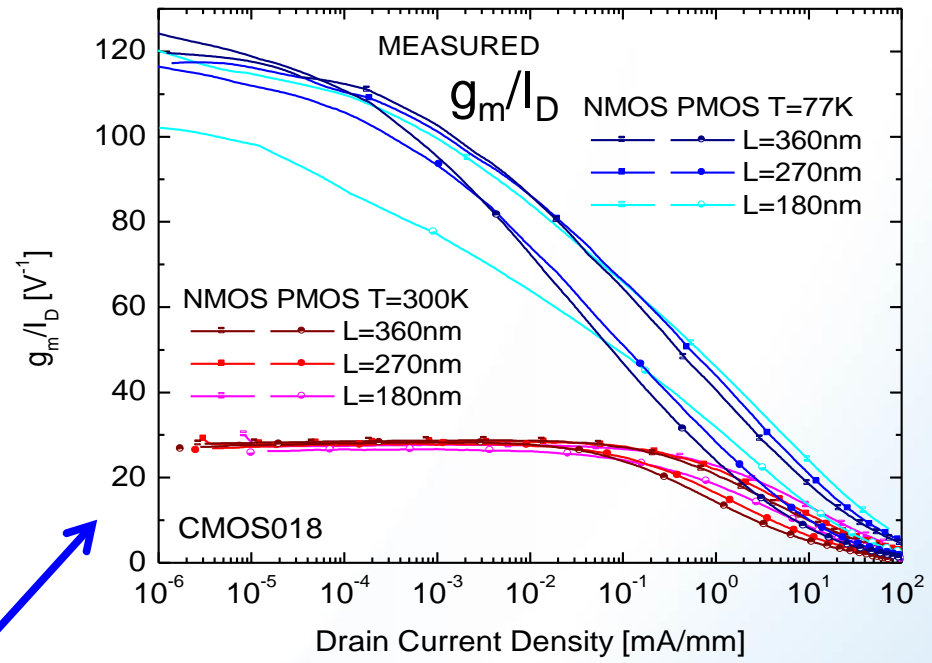
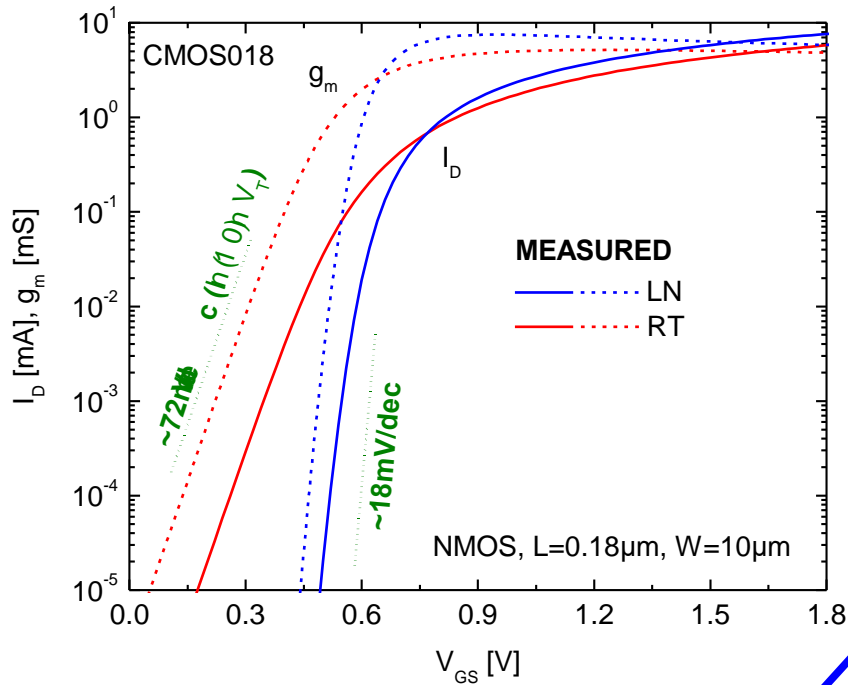
- JFET based preamplifier designed for MicroBooNE
 - Bulk mobility and transconductance increase as temperature decreases, carrier freeze out causes **ENC increasing when temperature lower than ~100K**

- CMOS technology – test result of an existing ASIC in $0.25 \mu\text{m}$ (*not designed for LAr*)
 - CMOS in LAr has **less than half the noise** as that at room temperature, higher mobility and higher transconductance/current ratio
 - R&D of CMOS cold electronics at BNL started in 2008

ENC vs. T (Cd=100pF, 0.5µs peaking time)



CMOS Characteristics in LAr



Transconductance/
drain current $\rightarrow \frac{g_m}{I_D} \rightarrow \frac{q}{nk_B T} = \begin{cases} \sim 30 \text{ at } T = 300K \\ \sim 116 \text{ at } T = 77K \end{cases}$

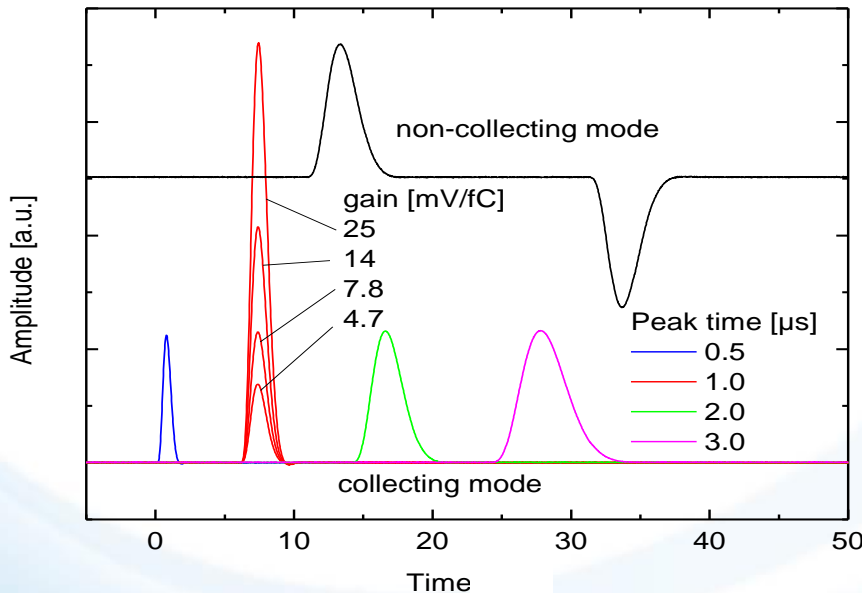
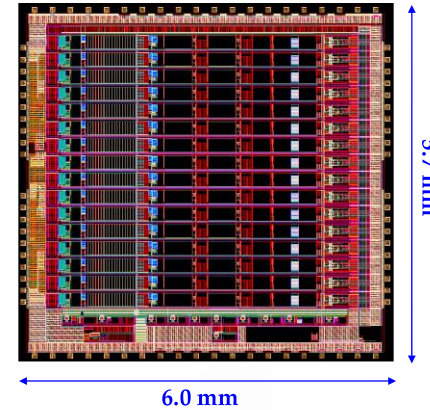
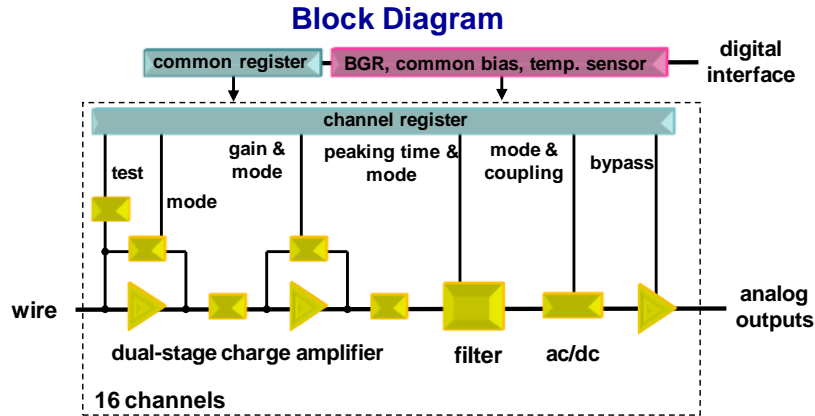
At 77-89K, charge carrier **mobility** in silicon increases and **thermal fluctuations decrease** with kT/e , resulting in a **higher gain, higher g_m/I_D , higher speed** and **lower noise**.

CMOS Reliability at Cryogenic Temperatures

- Studies of CMOS lifetime and reliability at 77 K have been conducted
 - "LAr TPC Electronics CMOS Lifetime at 300K and 77K and Reliability under Thermal Cycling," *IEEE Trans. on NSci*, 60, No: 6, Part: 2, p4737(2013)
- **Most of the major failure mechanisms** are strongly temperature dependent and **become negligible at cryogenic temperature**
 - Such as electro-migration, stress migration, time-dependent dielectric breakdown and negative-bias temperature instability
- The degradation (aging) due to channel Hot Carrier Effects (HCE)
 - **The only remaining mechanism** that may affect the lifetime of CMOS devices at cryogenic temperature
 - Lifetime due to HCE aging
 - **A limit defined by a chosen level of monotonic degradation**
 - Drain current, transconductance, threshold voltage etc.
 - The aging mechanism does **not** result in **sudden device failure**
 - The device "fails" if a chosen parameter gets out of the specified circuit design range
- The degradation mainly concerns NMOS devices
 - PMOS usually exhibits a lifetime much longer than NMOS.

LArASIC - Analog Front-End ASIC

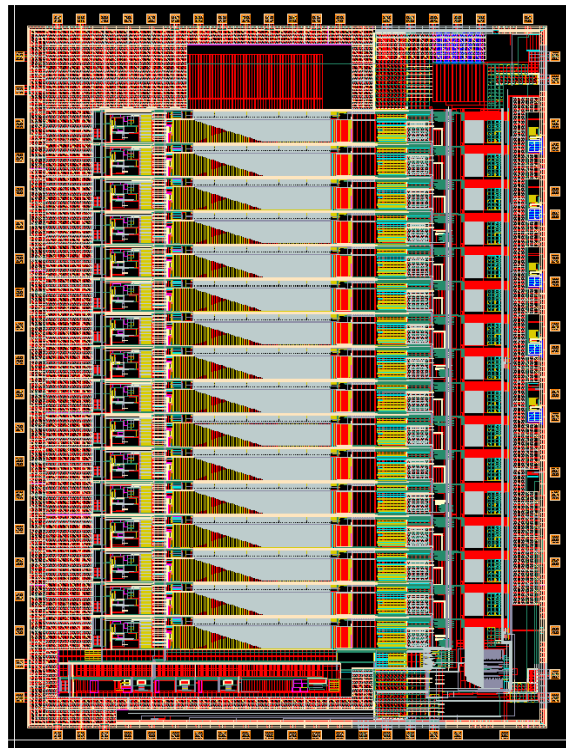
16x ch programmable charge amplifier working at 77-300K for neutrino experiments



- **P1/P2 Version (new features)**
 - Built-in 6-bit DAC for calibration
 - **Built-in analog monitoring output (P2)**
 - Higher bias current options (1nA / 5 nA)
 - Smart reset
 - Increase ESD protection on I/O
 - **Mitigate pole-zero cancellation (P2)**
 - Increase the buffer-off drive capability
- **P3 Version (new features)**
 - Address the baseline distortion
 - Remap the register for gain setting (set 14 mV/fC as default)
- **P4 Version (new features)**
 - Differential output to couple with ColdADC

Cold ADC ASIC for ProtoDUNE-SP

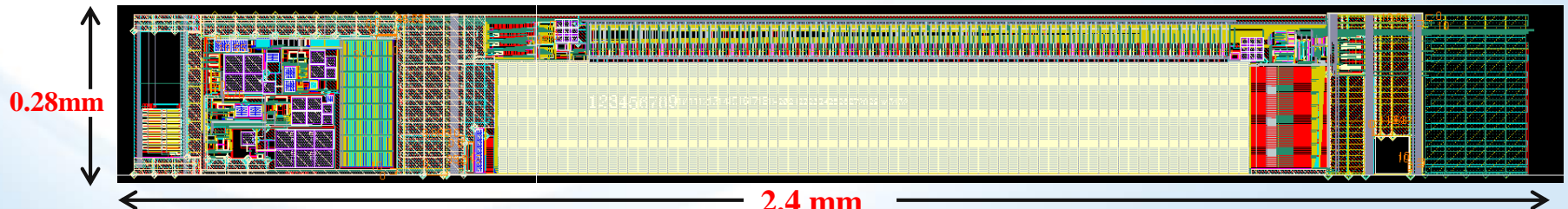
Development discontinued after ProtoDUNE-SP



6.1 mm

4.5 mm

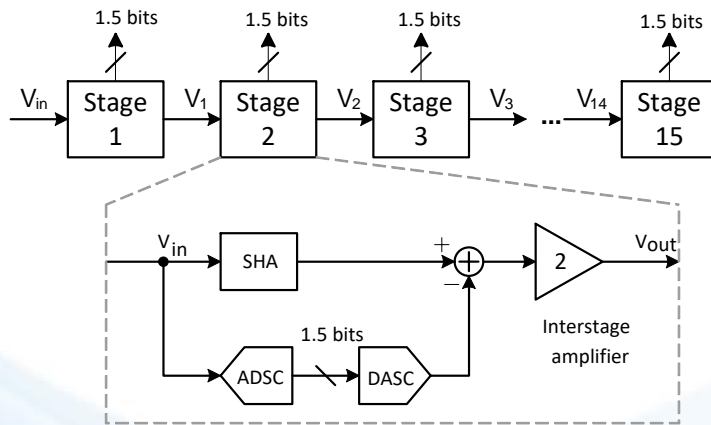
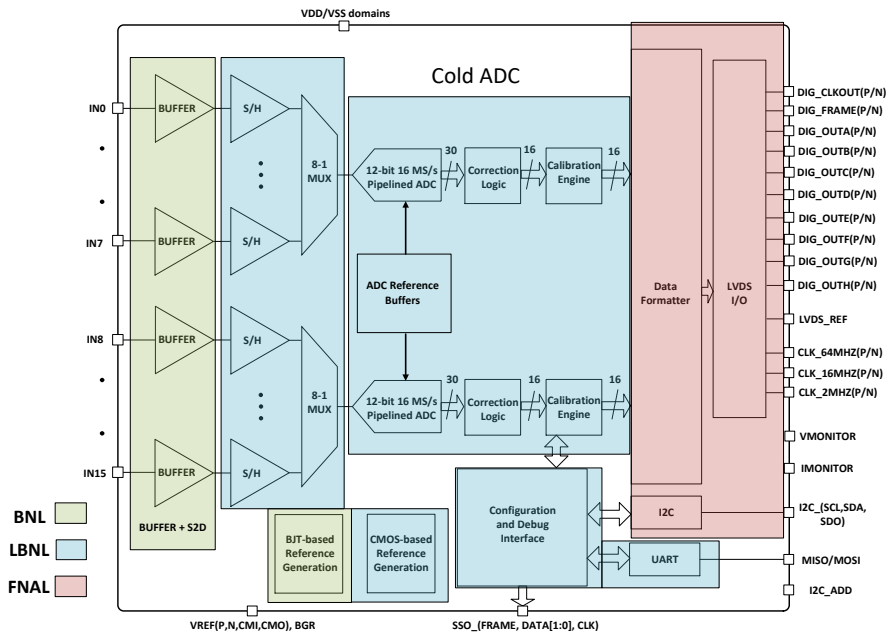
- 16 channels, programmable
- sample/hold
- 12-bit ADC at 2MS/s sampling rate
- current-mode domino architecture
- FIFO 192s bit wide x 32 bits deep
- multiplexer 8:1 or 16:1
- serializer 12:1
- adjustable offsets
- ~4.5 mW/ch.
- power-down modes
- ~ 300,000 MOSFETs
- designed for 77-300K operation
- designed for long lifetime
- tech. CMOS 180nm, 1.8 V, 6M, MIM, SBRES



0.28mm

2.4 mm

ColdADC ASIC for DUNE



ADC block diagram

- Designed by joint team from LBNL, FNAL, and BNL
- Cold ADC is a 16-channel, 12-bit, 2 MS/s Digitizer ASIC for the DUNE Far Detector
- Cold ADC uses a conservative, industry-standard design with digital self-calibration
- Besides functionality and reliability, design goal is low-noise and cryogenic operation
- Digital-On-Top Design Methodology
 - 65nm CMOS process, 9 metal stack
 - leverages existing FNAL cold models
 - facilitates potential future integration with COLDATA
 - Chip size: 6860 μm x 7610 μm
- P1 was fully characterized with few issues have been addressed in P2
- P2 is being characterized.

COLDATA ASIC for DUNE

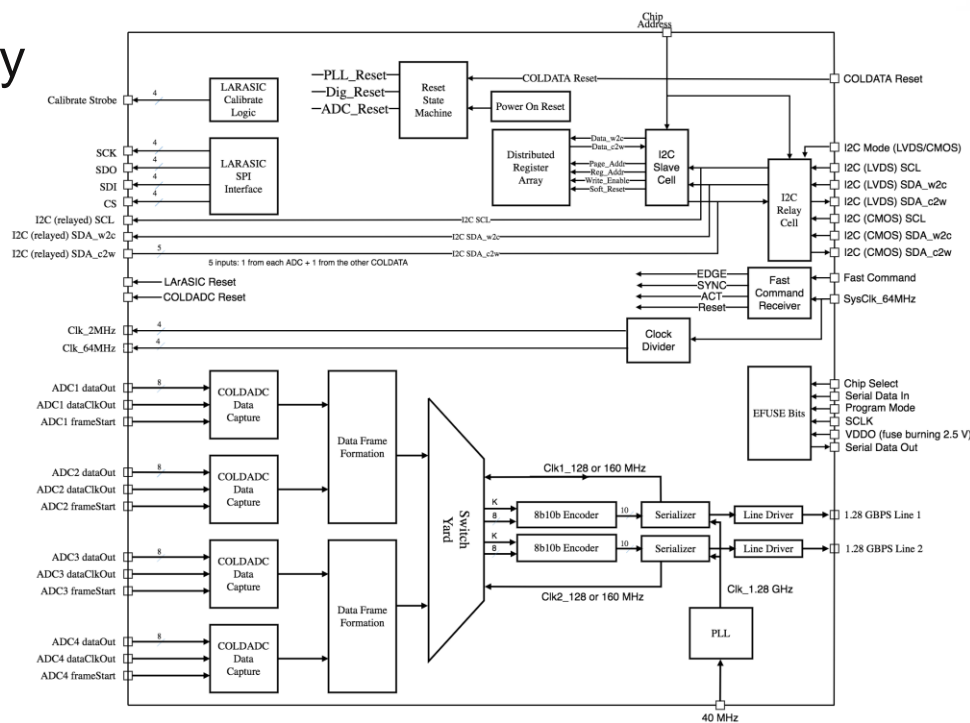
Digital-On-Top Design Methodology

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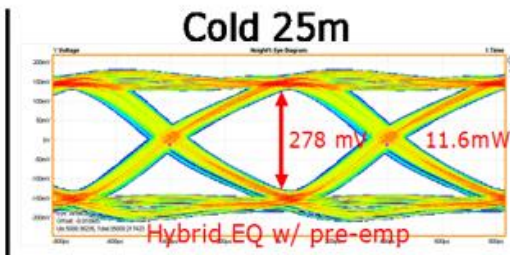
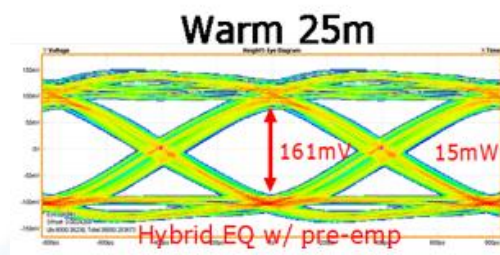
Functions

- Configure and control 4 COLDADCs and 4 LArASICs
- Accept data from 4 COLDADCs
- Format ADC data (truncate to 12 or 14 bits) & pack into an array of 8-bit words
- Combine packed arrays from pairs of ADCs into 2 output data frames
- Encode the output data using 8b10b
- Drive the output data to a WIB at 1.28 Gbps

- P2 was characterized
 - 2 minor known issues
 - 4 requests for modification
- P3 is being taped out

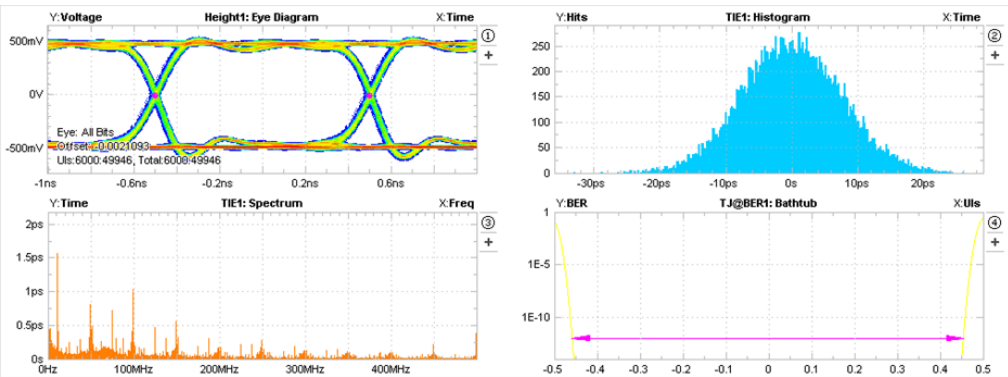


BER < 10⁻¹⁵

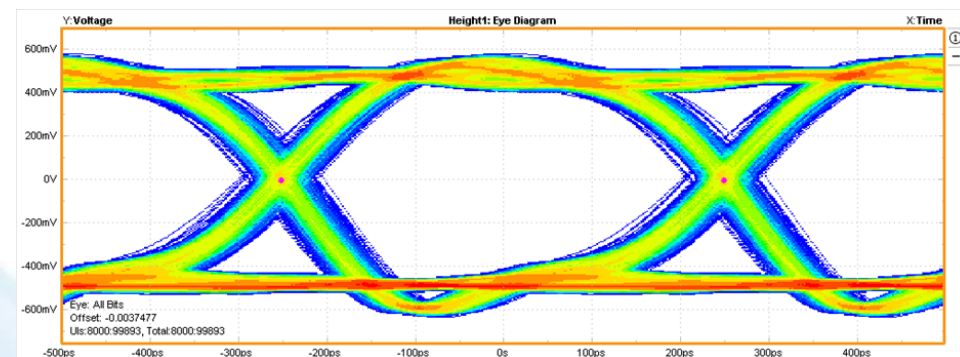


Line Driver eye diagram measurement result

Cold FPGA Qualified FPGA for Cold Operation



1Gb/s transceiver

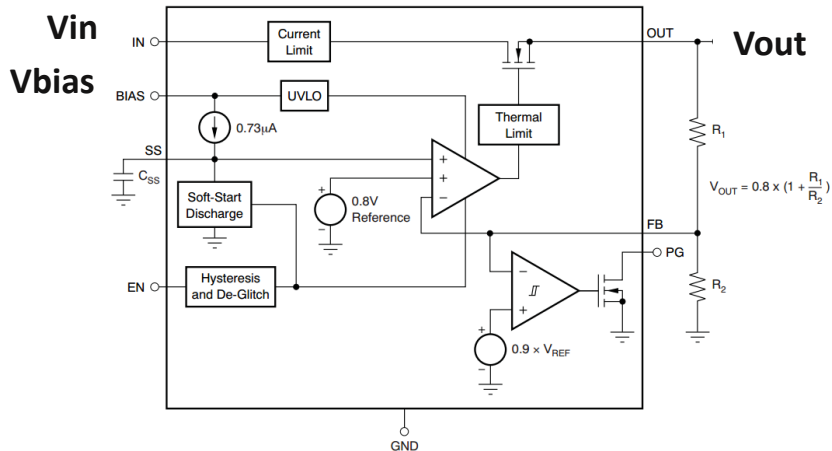


2Gb/s transceiver

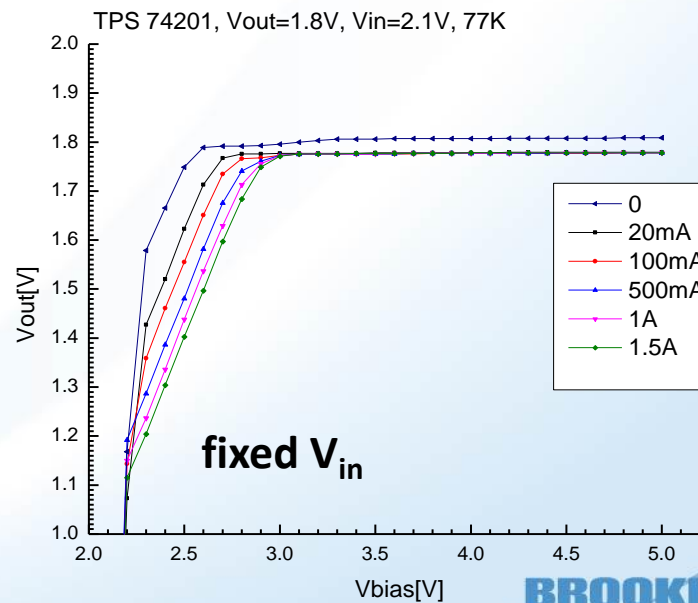
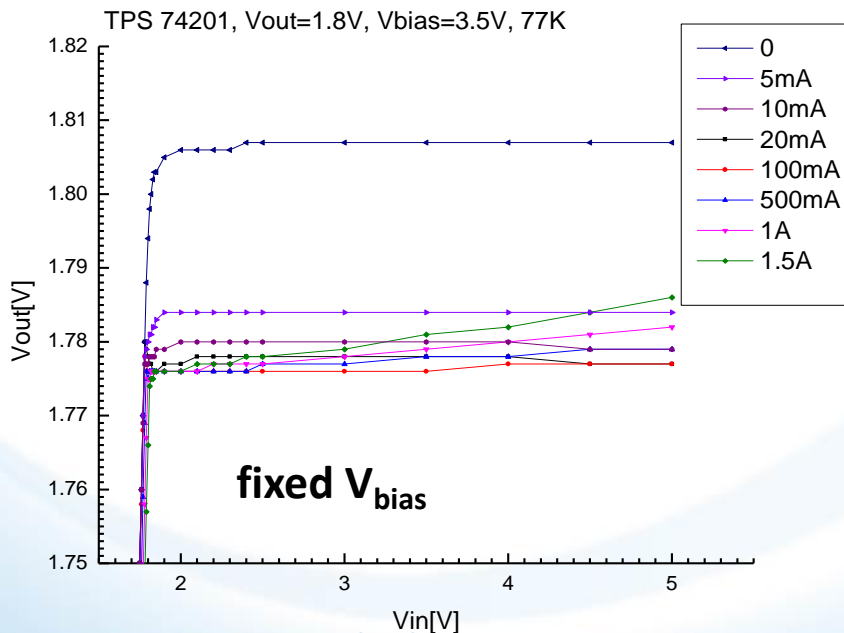
- Test of Cyclone IV GX Transceiver Starter Board in LN₂
 - Transceiver works well at both 1Gbit/s and 2Gbit/s
 - Height
 - 839mV @ 1Gbit/s
 - 823mV @ 2Gbit/s
 - Eye Width
 - 914ps @ 1Gbit/s
 - 357ps @ 2Gbit/s
 - On board SRAM works with BIST
 - 18-Mb SRAM from ISSI IS61VPS102418A-250TQL
 - Cyclone IV GX is running with Nios II processor and utilization of ~80% fabric resources

Cold Regulator Qualification

TI TPS74201



- TI TPS742xx voltage regulator family has been identified working well at cryogenic temperature recently
- 1.5A max I_{out} , 0.8V-3.6V adjustable V_{out} and separate V_{in} makes it an ideal candidate for all of the cold electronics chain



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ProtoDUNEs

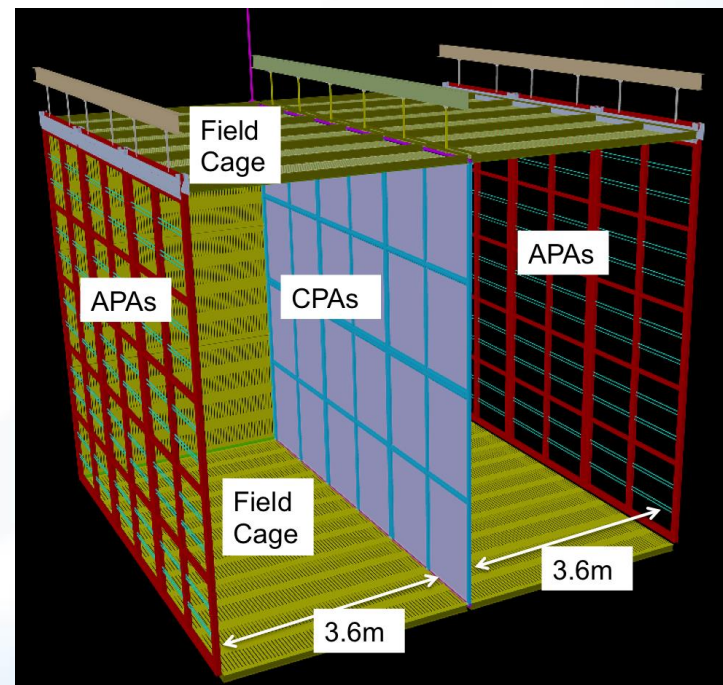
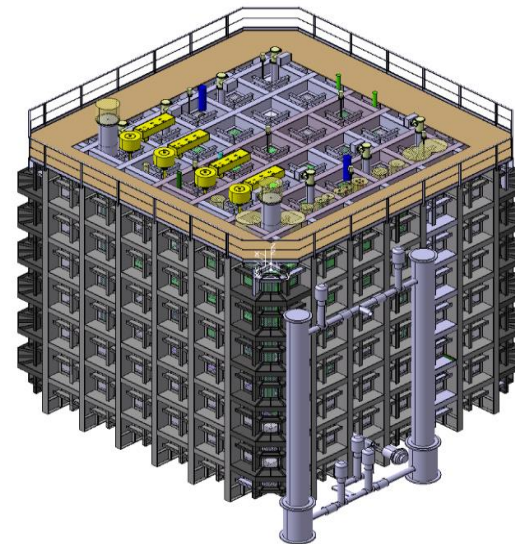
- ProtoDUNEs provide critical validation of technology, detector performance, and long-term stability



- BNL focused on **ProtoDUNE-SP Cold Electronics** R&D (both electrical and mechanical), production, installation and commissioning

ProtoDUNE-SP

- NP04 experiment at CERN
 - 400-ton fiducial LArTPC
 - Sit in H4 beam line
- Single-phase TPC prototype
 - 6 full-size APAs plus 3 CPAs
 - 2 x 3.6m drift regions
 - Total 15,360 TPC channels
 - Use full scale components of DUNE far detector module
 - RUN I has been completed in 2020
 - RUN II is planned ~2022
- A key test of:
 - Components
 - Construction methods
 - Installation procedures
 - Commissioning
 - Detector response to particles
 - Confirm modeling and simulation



Timeline

Sep. 2016

Jan 2017

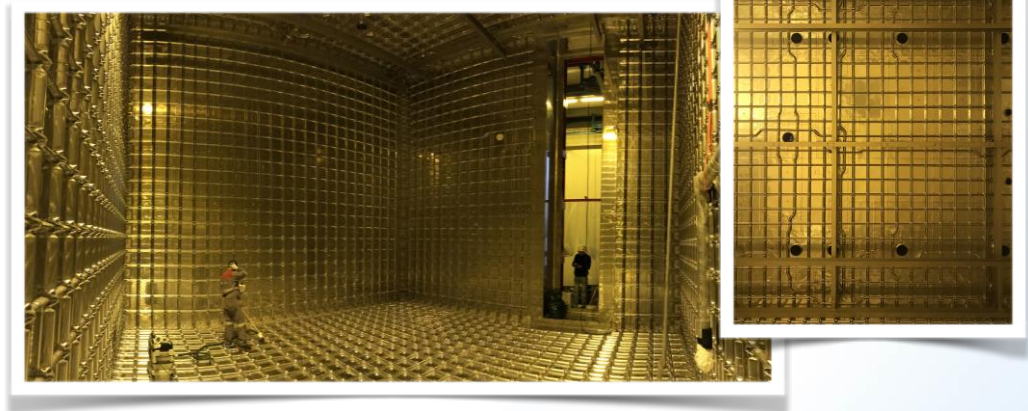
May 2017

Sep. 2017

Construction of the outer structure



Construction of the inner cryostat



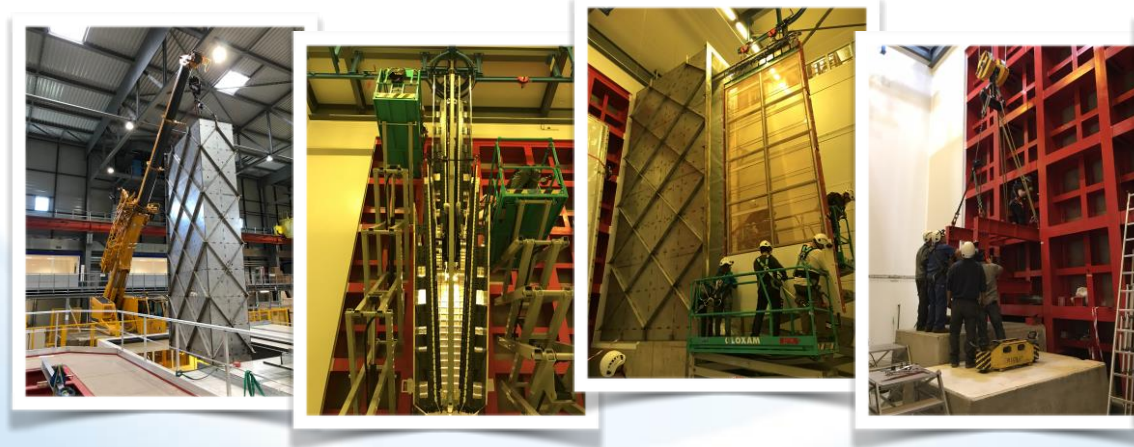
Sep. 2017

Jan 2018

May 2018

Sep. 2018

Test and installation of the TPC



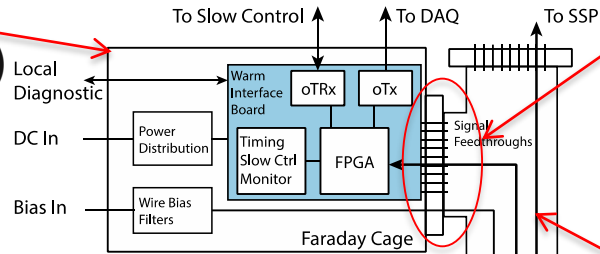
Purging cooling and filling

Beam ready



ProtoDUNE-SP Cold Electronics System

- Warm interface electronics
- Warm Interface Electronics Crate (6)
- Warm Interface Board (30)
- Power and Timing Card (6)
- Power and Timing Backplane (6)

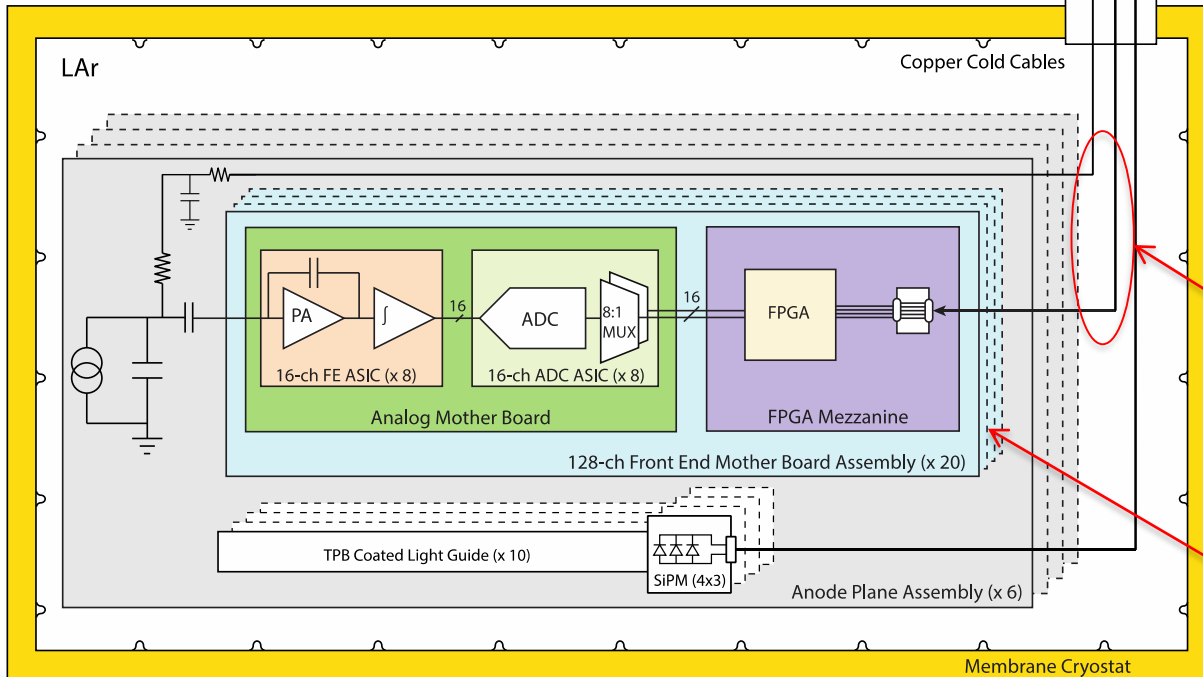


CE flange
Flange assembly with cable strain relief and flange PCB for cable/WIB connection (6)

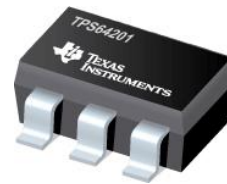
Signal feed-through
Tee pipe with 14" Conflat flanges and crossing tube cable (CTC) support (6)

Cold cable
LV and data cable (120+120) to FEMB and APA wire-bias SHV cable (48)

Front End Motherboard (FEMB) 128 channels of digitized wire readout enclosed in CE Box (120)



Cold Electronics R&D

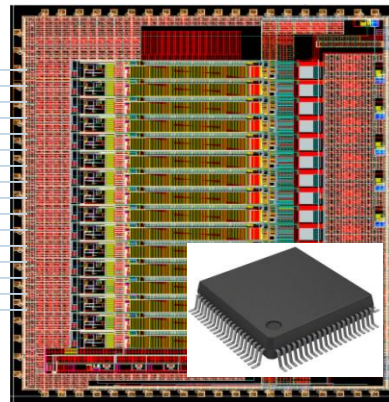
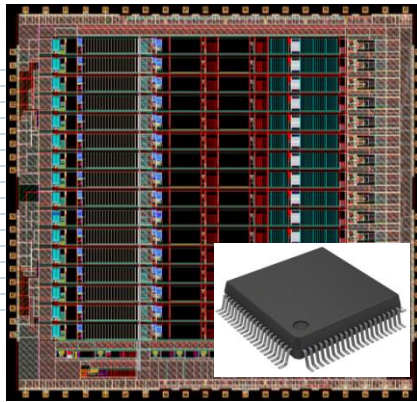


voltage regulation (COTS)
($< 100\text{mV}$ dropout)

Front end ASIC
 $\sim 5\text{mW}/\text{ch.}$

ADC ASIC
 $\sim 5\text{mW}/\text{ch.}$

FPGA (COTS)
 $\sim 8\text{mW}/\text{ch.}$

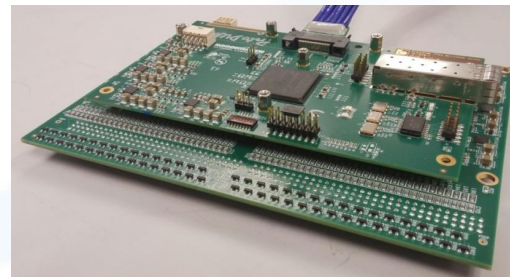


overall 128:4
multiplexing

1 x

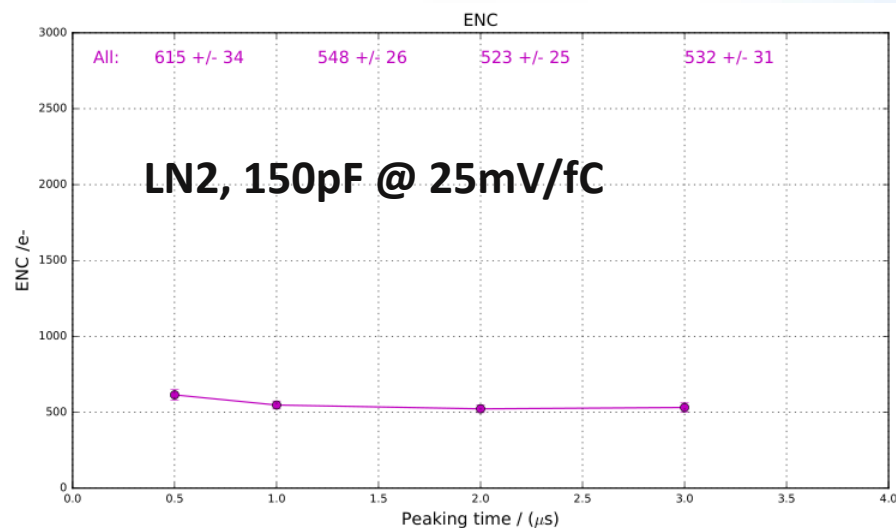
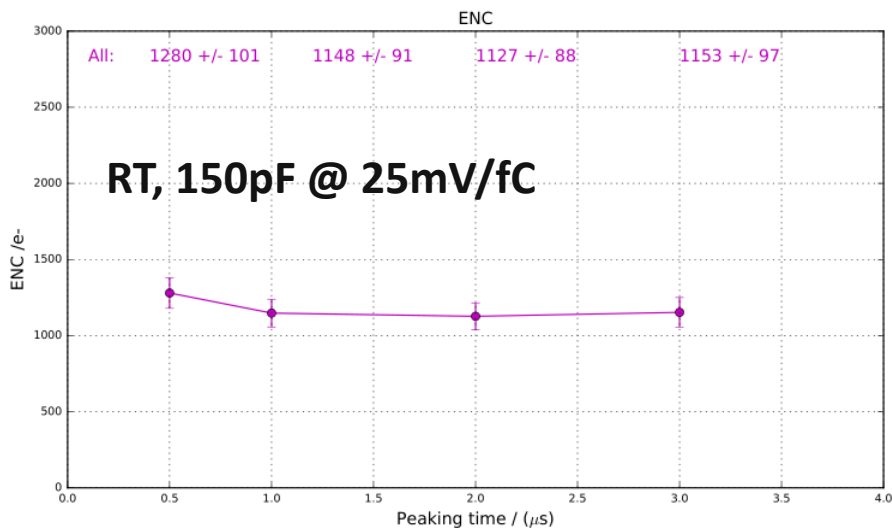
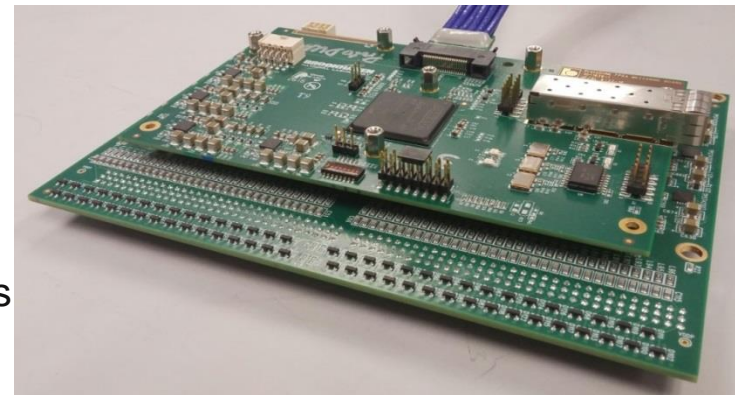
8 x

*R&D produced key components
to form a complete cold front-
end readout chain for LAr TPC
experiments*



Front End Mother Board (FEMB) Assembly

- 128 channels of digitized TPC wire readout
 - Analog Mother Board**
 - 8 LArASIC and 8 P1 ADC chips
 - FPGA Mezzanine**
 - Multiplexing and readout of digitized detector signals
 - 4x1Gb/s serial links to transmit 128 FE channels of data



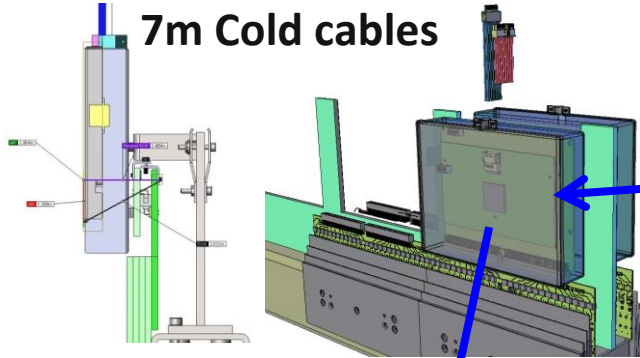
~1150e⁻ at RT and **~550e⁻ at LN2** @ 1us peaking time, 25mV/fC gain and 150pF C_d

Noise decreases significantly at cryogenic temperature

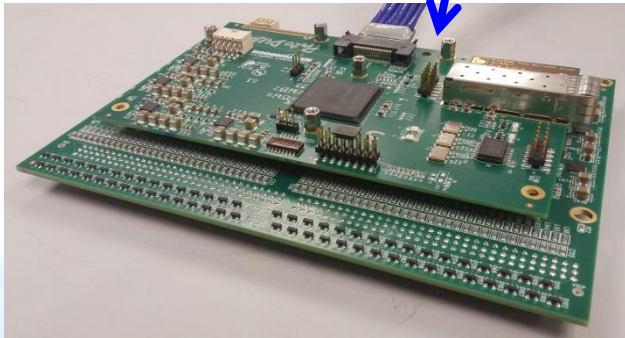
One WIEC for One APA Readout



7m Cold cables

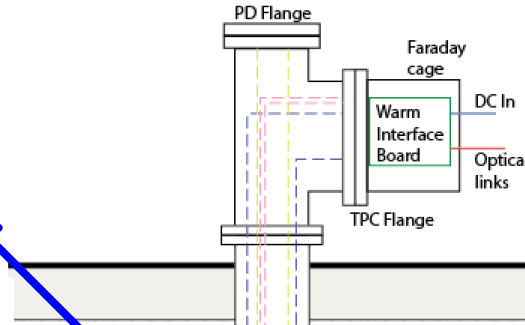


20 CE boxes on APA

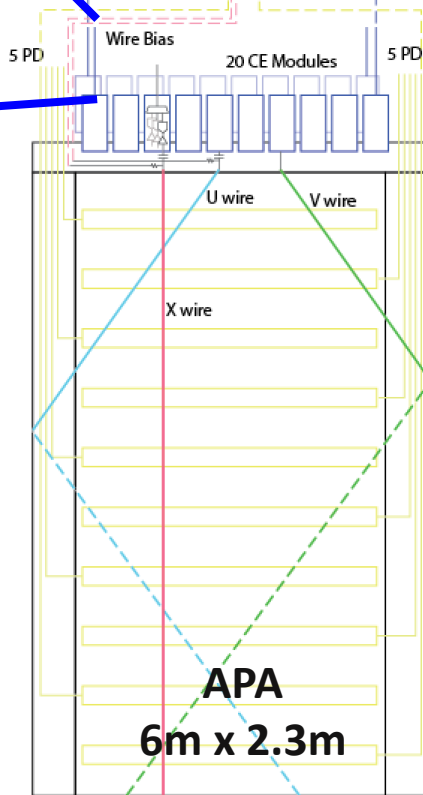
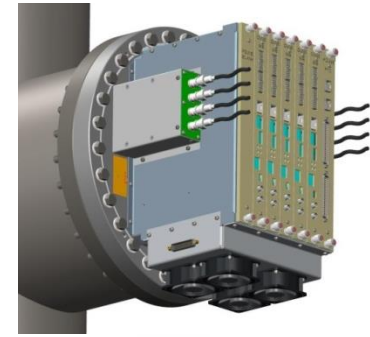


FEMB (inside CE box)

Cold Side

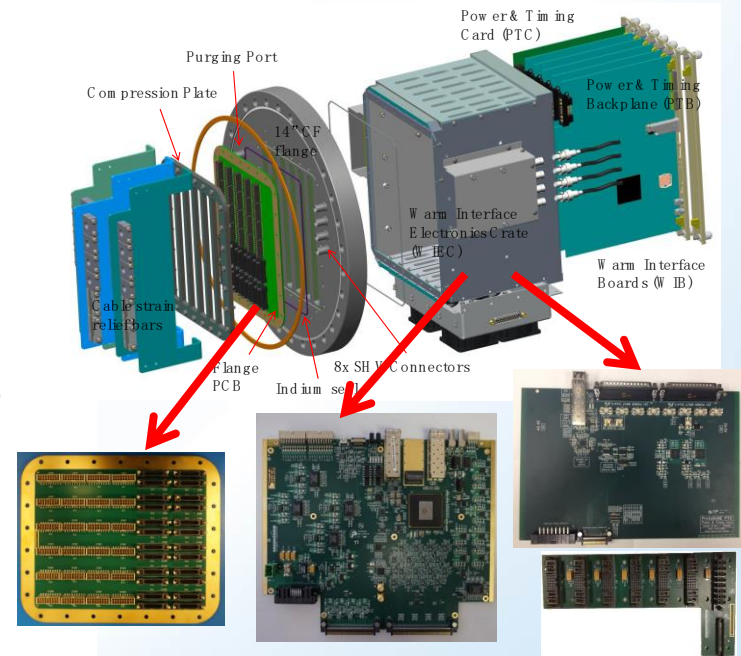


Signal Feed-through Assembly



APA

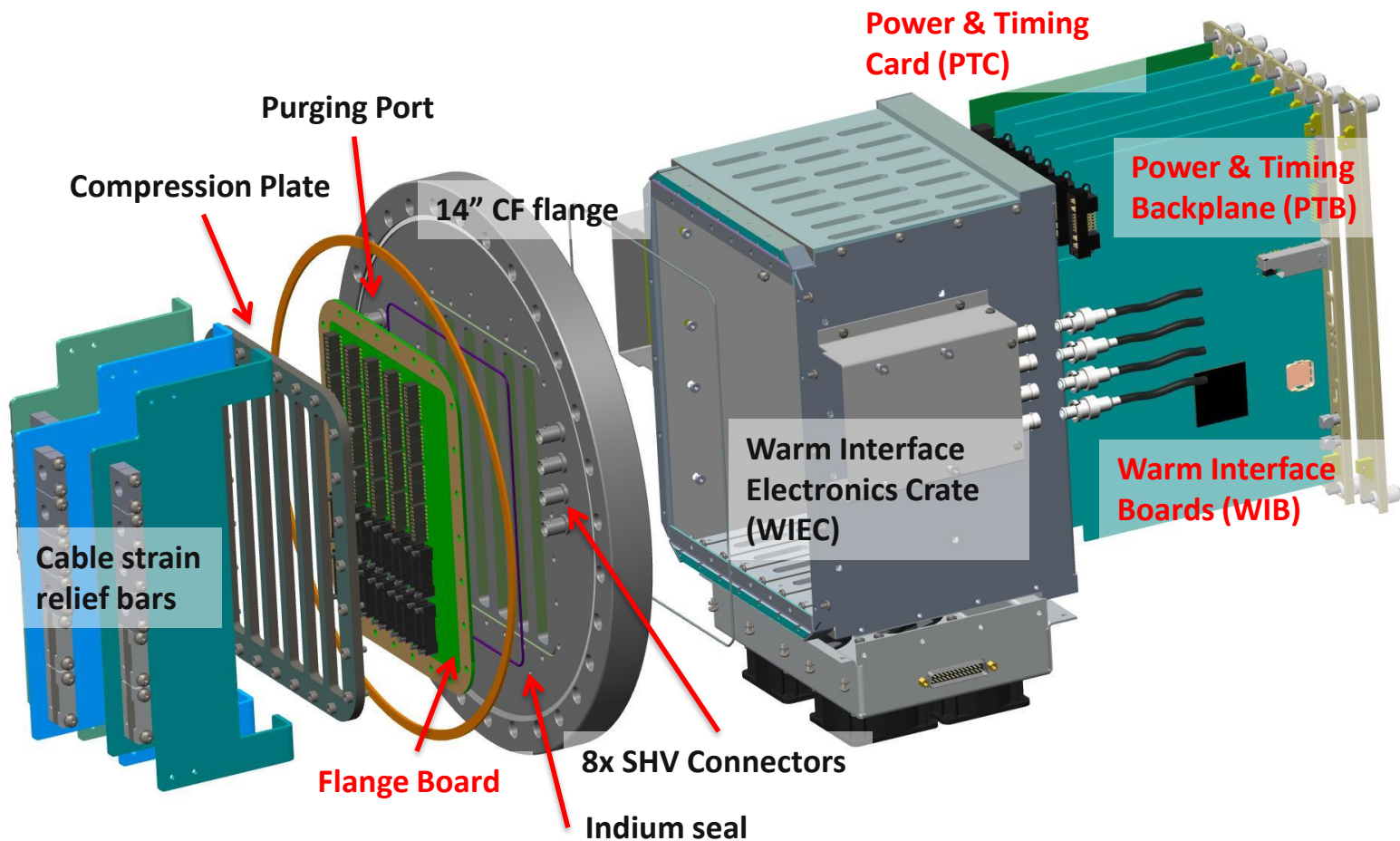
6m x 2.3m



Flange Board, WIB, PTC, PTB

Warm Side

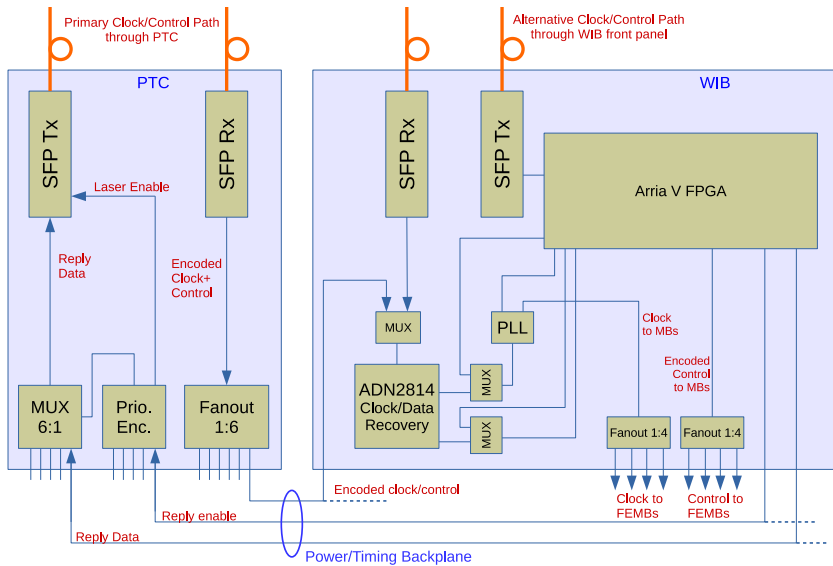
WIEC and Feed-through Assembly



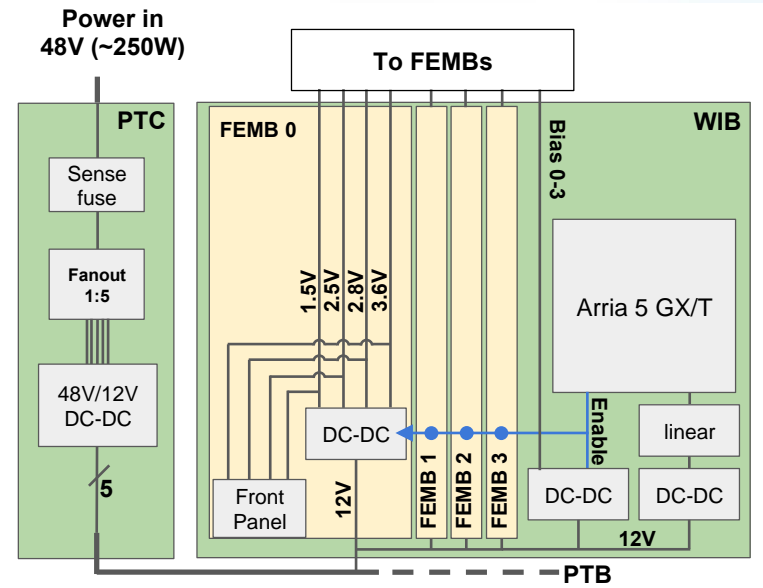
CE flange and WIEC are a single assembled unit

Warm Interface Electronics

- Interface Electronics between CE and DAQ
 - Receives the timing and control from the 50 MHz encoded system clock
 - Sends timing and control to FEMBs and receives high-speed TPC data over cold data cable and transmits it to the DAQ systems over optical fiber
 - Power supply distribution and monitoring
 - Data speed up to 10 Gb/s
 - Includes WIB (Warm Interface Board), PTB (Power Timing Backplane), PTC (Power Timing Card) and WIEC (Warm Interface Electronics Crate)



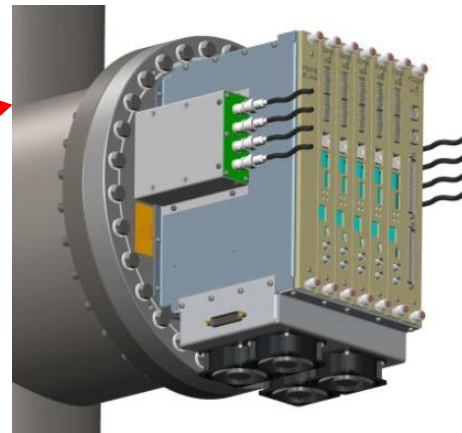
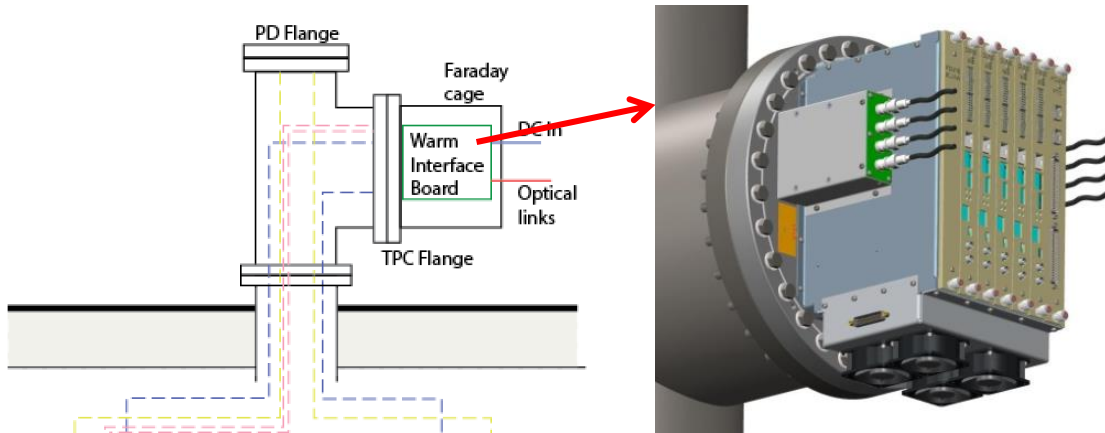
Timing, control and data flow



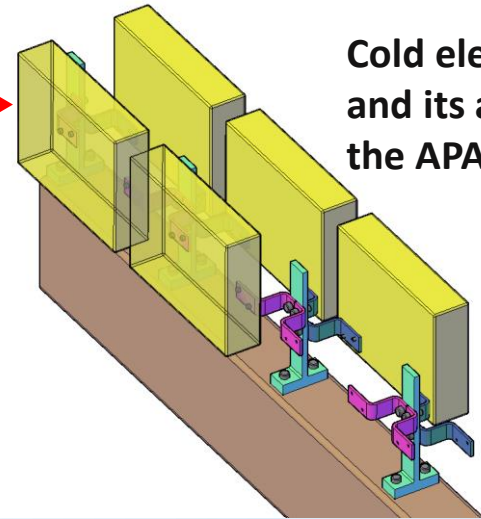
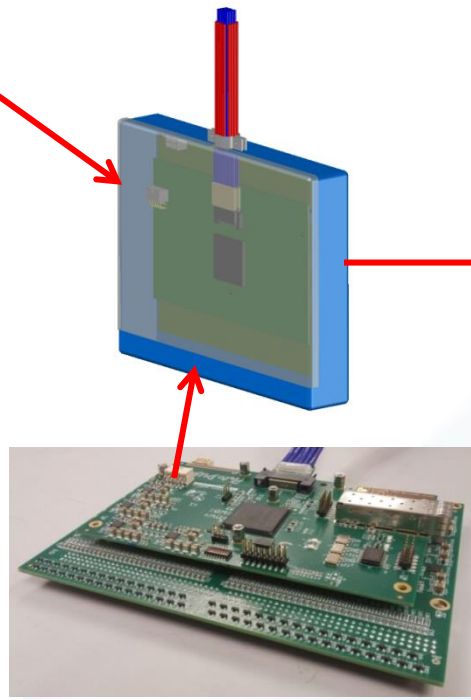
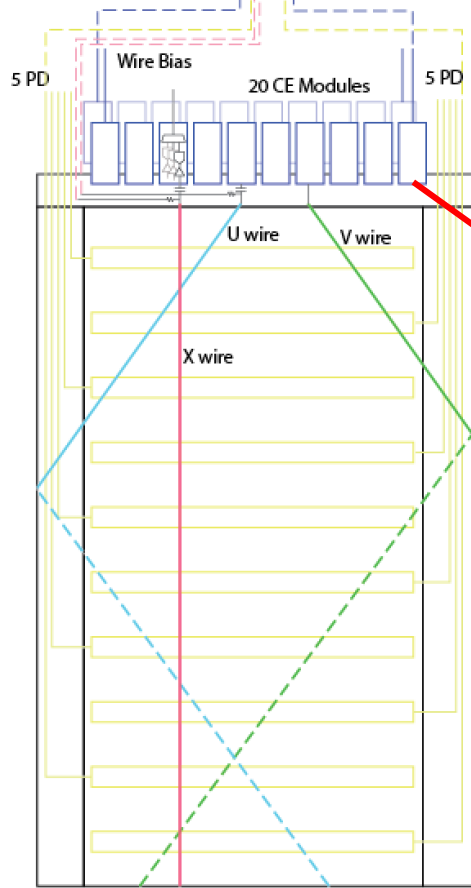
Power distribution

Integral System Design Concept

A necessary (but not sufficient!) condition to achieve a good performance, **the integral design concept** of APA + CE + Feed-through, plus Warm Interface Electronics with **local diagnostics** and strict isolation and **grounding rules** will have to be followed

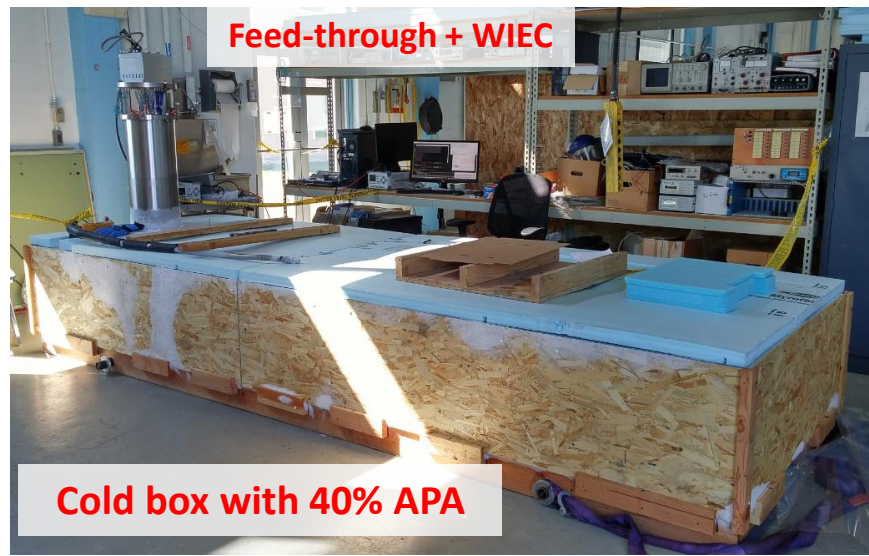


ProtoDUNE-SP



Cold electronics module and its attachment to the APA frame

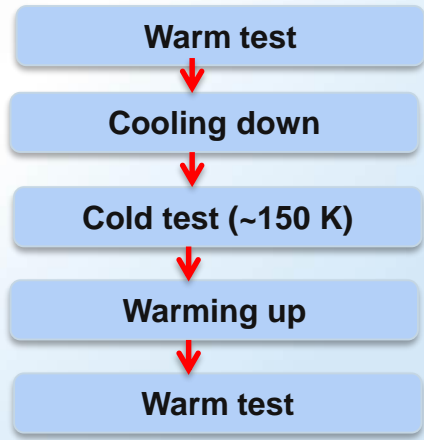
Integration Test Stands at BNL and CERN



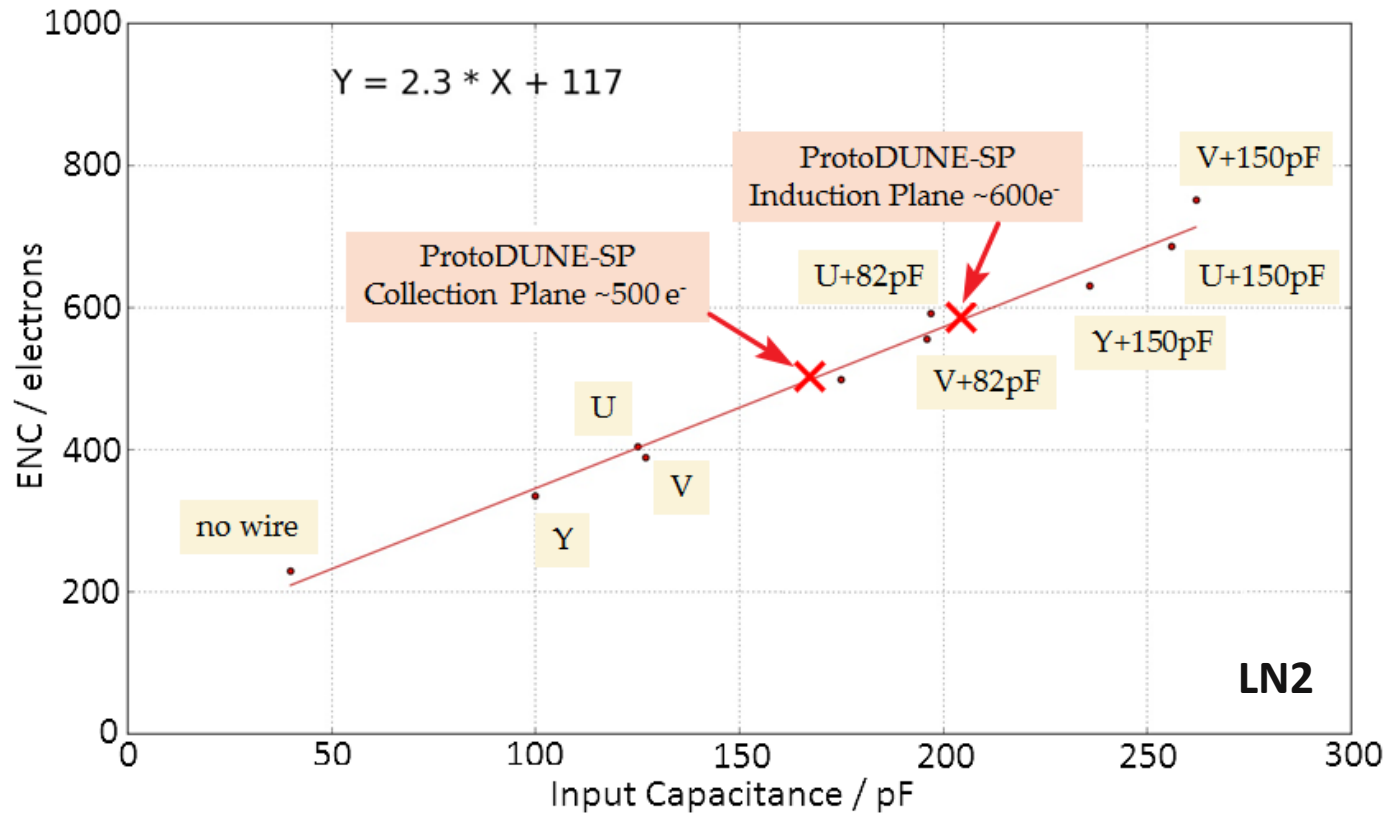
40% APA: 2.8m x 1.0m, 1024 wires



DUNE APA: 6m x 2.3m, 2560 wires



ENC Projection Based on 40% APA



- **40% APA**

- U/V wire: 4.0 m
- Y wire: 2.8m

Note: 82pF and 150pF mica capacitors are added on some wires

- **ProtoDUNE APA**

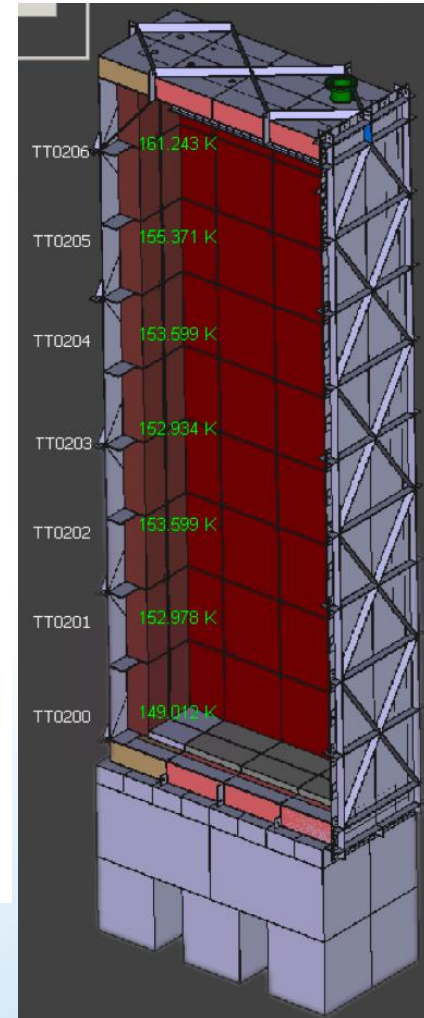
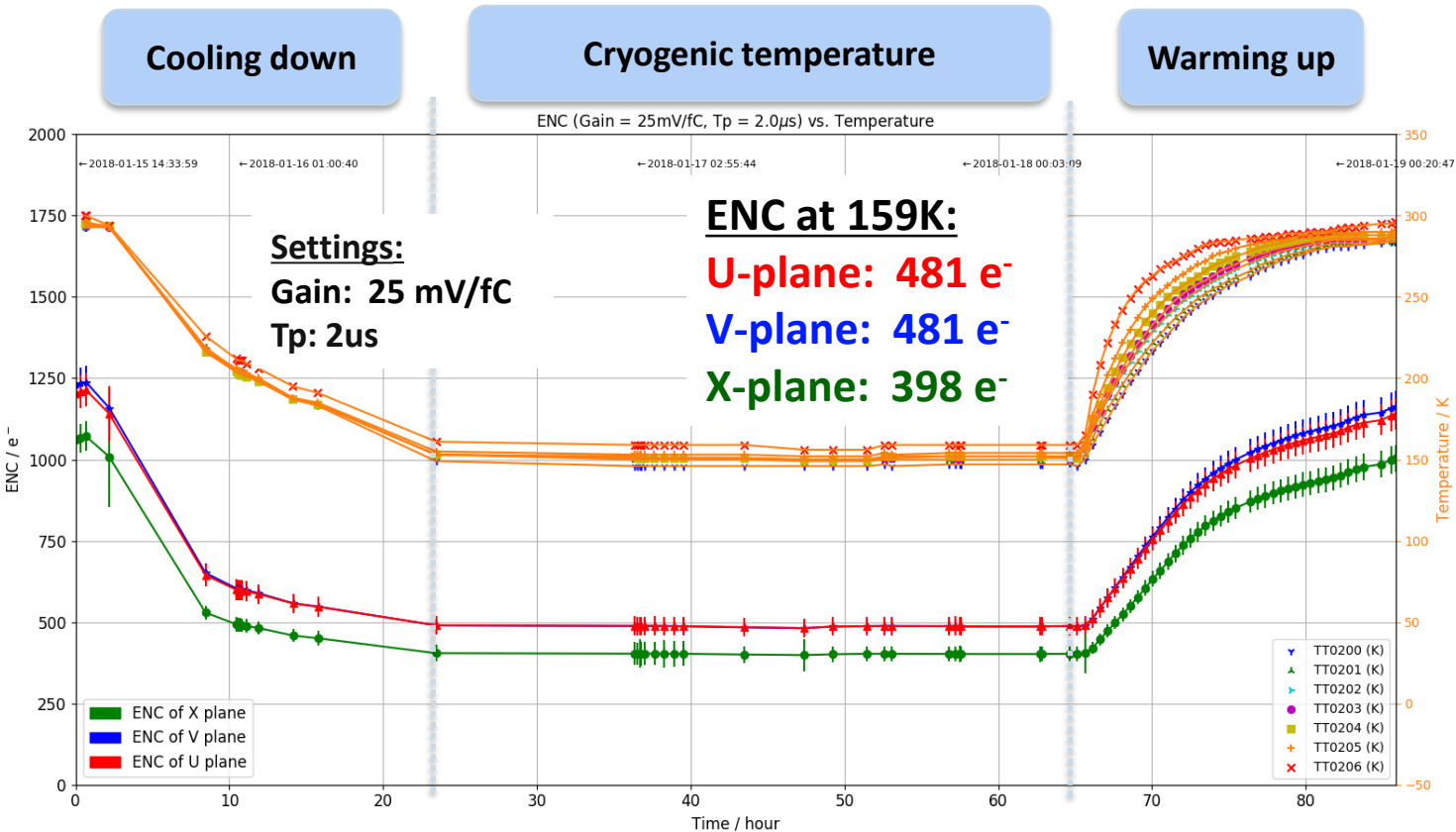
- U/V wire: 7.39m
- Y wire: 6.0m

- **DUNE Far Detector**

- Same APA as ProtoDUNE-SP
- Threshold: 1,000 e⁻
- Goal: as low as possible

CERN Cold Box Integration Test

APA2 (2018-01) Cold nitrogen gas with lowest temperature reached $\sim 159\text{K}$



1. Uniform gain (77 e^-/bin) is applied for calculating noise of all channels
2. HV Bias voltages were off
3. Data are read out chip by chip over local diagnostic GbE port.

ProtoDUNE-SP CE Status in Detector Operation

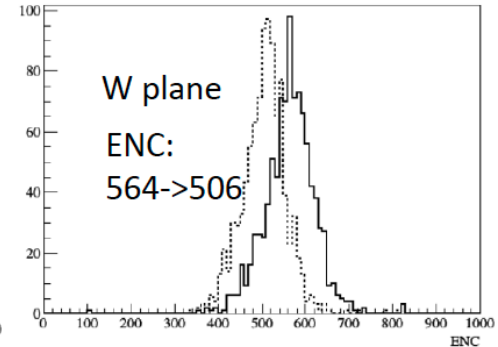
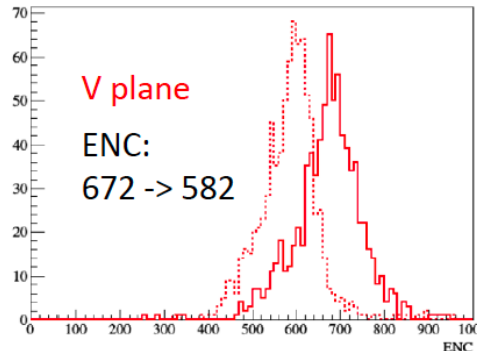
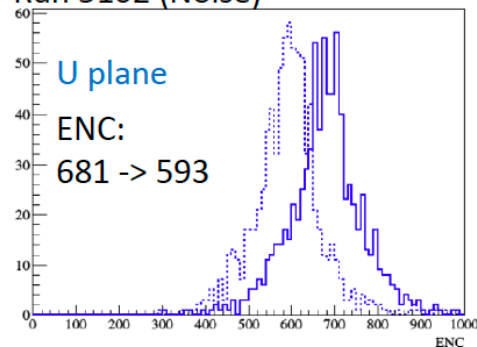
- No FE channels got damaged by bias during CERN cold box integration test
 - No cathode but nominal wire bias voltages under strong LAr air flow
- With 180kV cathode and nominal bias voltages
 - 99.74% (15320 of 15360) of TPC channels are active
 - Only 4 inactive cold electronics channels
 - 92.83% TPC channels are good with excellent noise performance
 - Raw data: Collection ENC ~560 e⁻, Induction ENC ~670 e⁻
- Total 6 inactive cold electronics channels at the end of Run I in 2020

09/13/2018

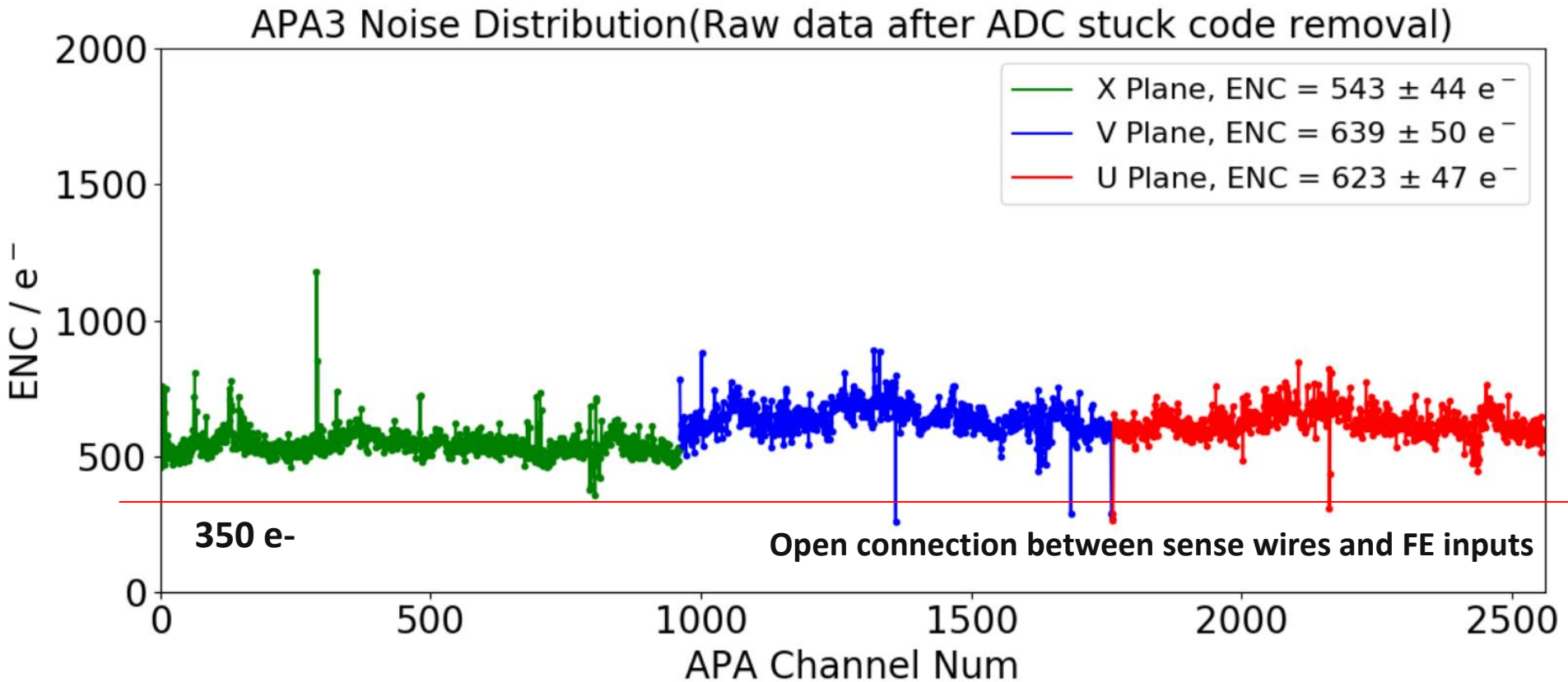
09/23/2018

Item	test#1	test#5	test #18	test #35	Recently
Drift	off	120kV%	160kV	180kV	180kV
Bias	off	on	on	on	on
FE Inactive	0	2	4	4	6
Channels (good & <800e-)	14397	14297	14179	14259	/

Run 5102 (Noise)

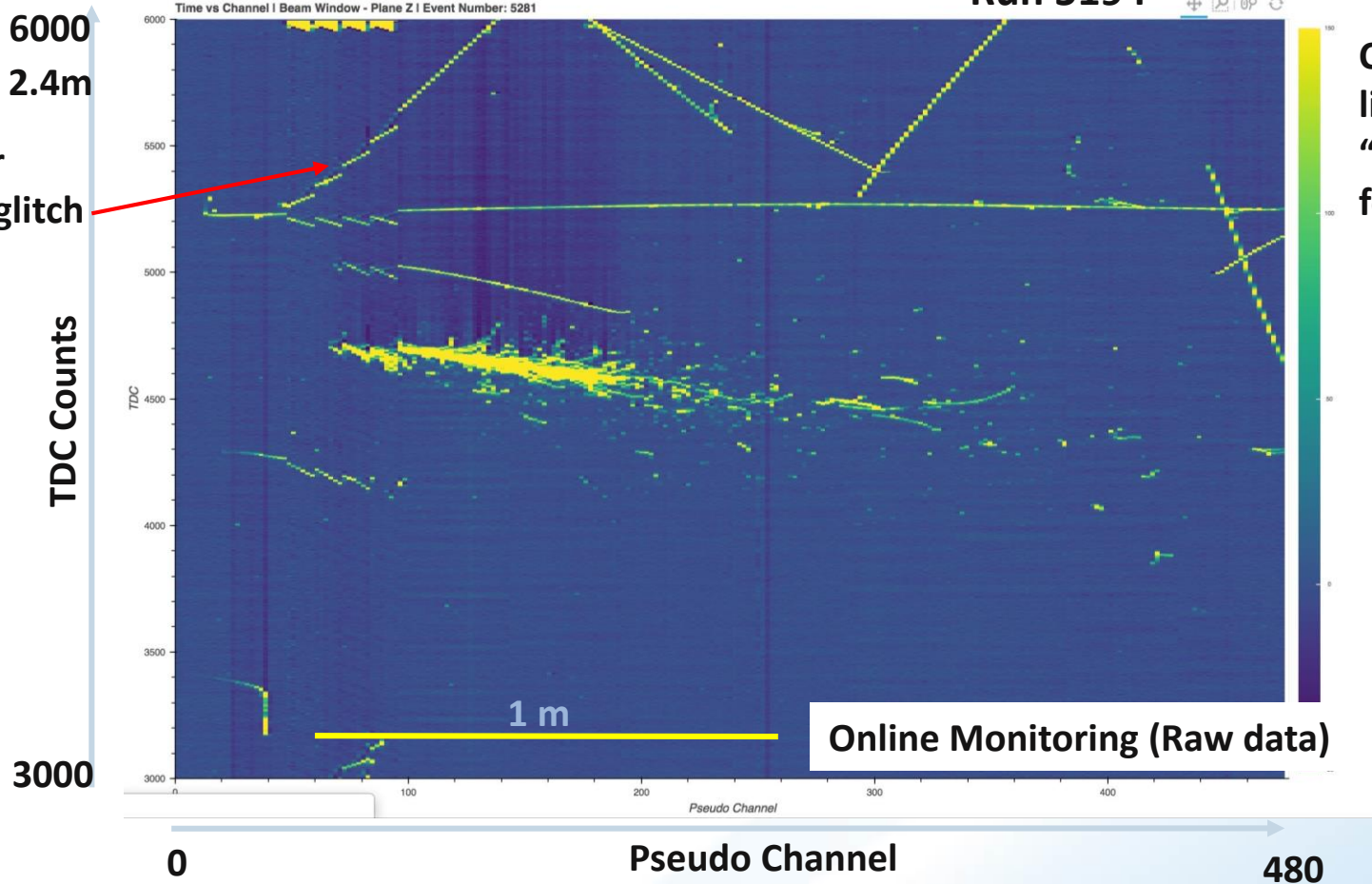


APA3 Noise Distribution in ProtoDUNE-SP Commissioning



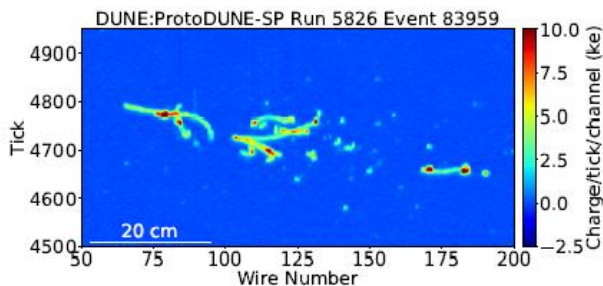
Shower Event under 7GeV Beam

Run 5194

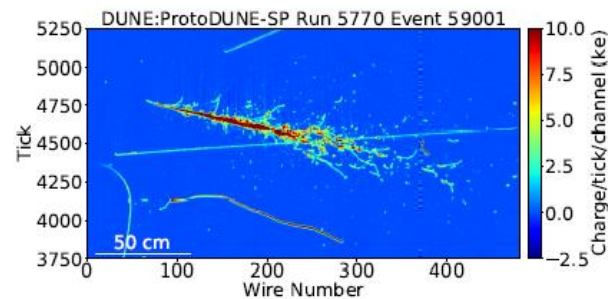


First results on ProtoDUNE-SP LArTPC

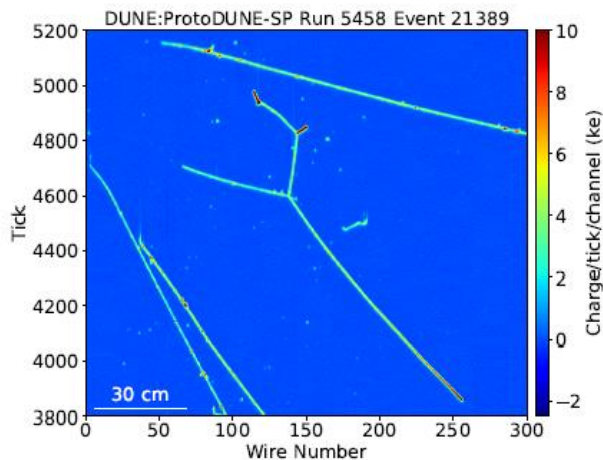
- ArXiv:2007.06722, being published in JINST



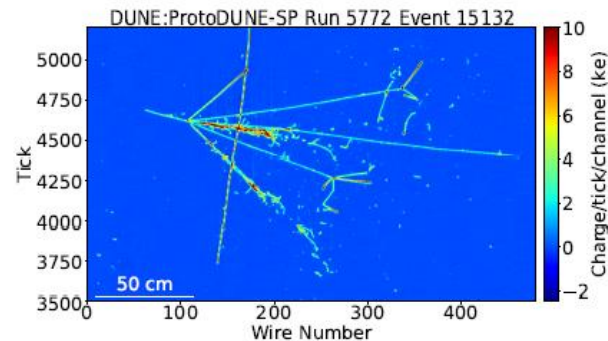
(a) A 0.5 GeV/c electron candidate.



(b) A 6 GeV/c electron candidate.



(c) A 1 GeV/c pion candidate.



(d) A 6 GeV/c pion candidate.

Successful ProtoDUNE-SP experience assures DUNE SP LArTPC

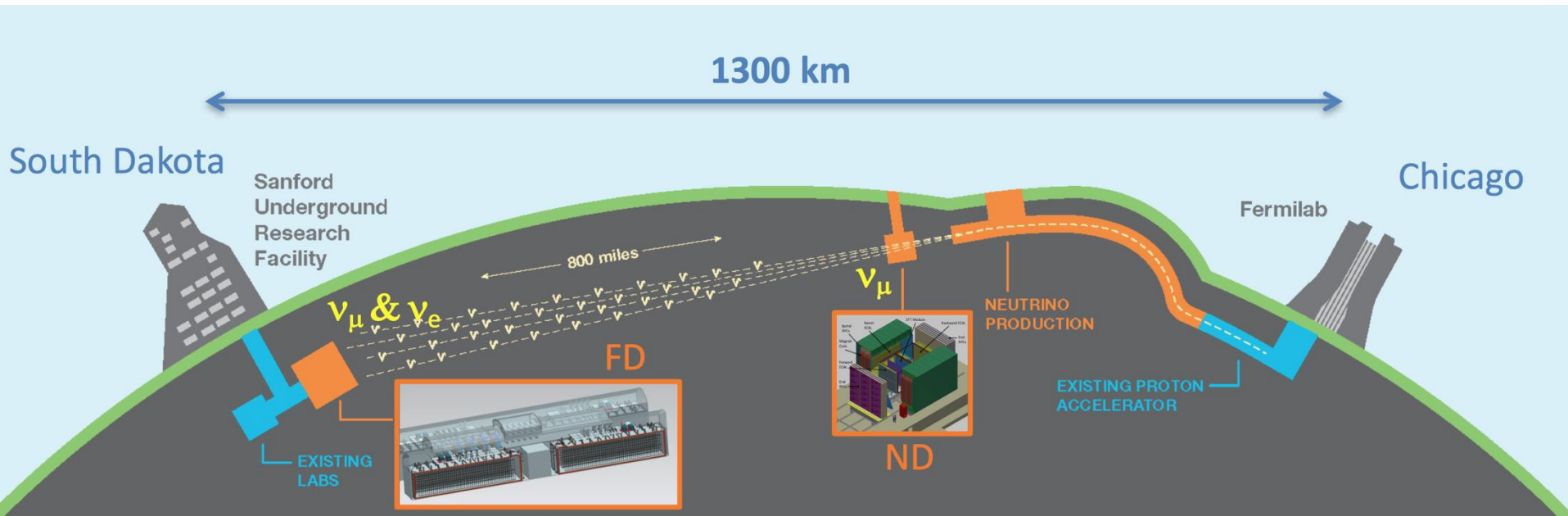
Outline

- Liquid Argon TPC in Neutrino Experiments
- Cryogenic Readout Electronics (CE)
 - Advantages
 - A Brief History
 - R&D on CMOS Cryogenic Electronics
- **Cryogenic Readout Electronics Applied in LArTPCs**
 - ProtoDUNE-SP
 - DUNE Far Detector

} Long Baseline Neutrino Experiments
- Summary

Only focus on single phase LAr TPC detector with wire electrode in neutrino experiments

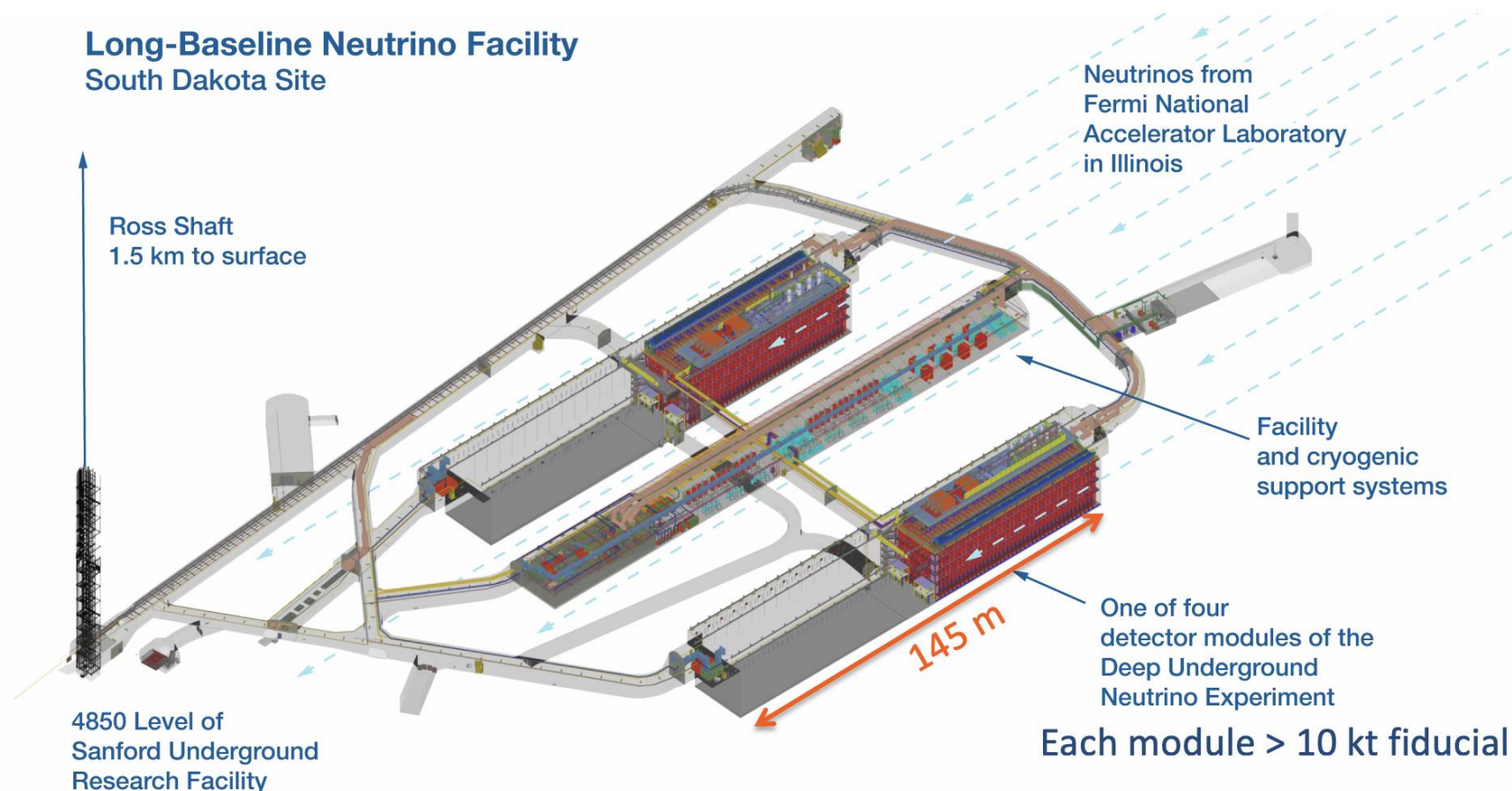
Long Baseline Neutrino Program: LBNF/DUNE



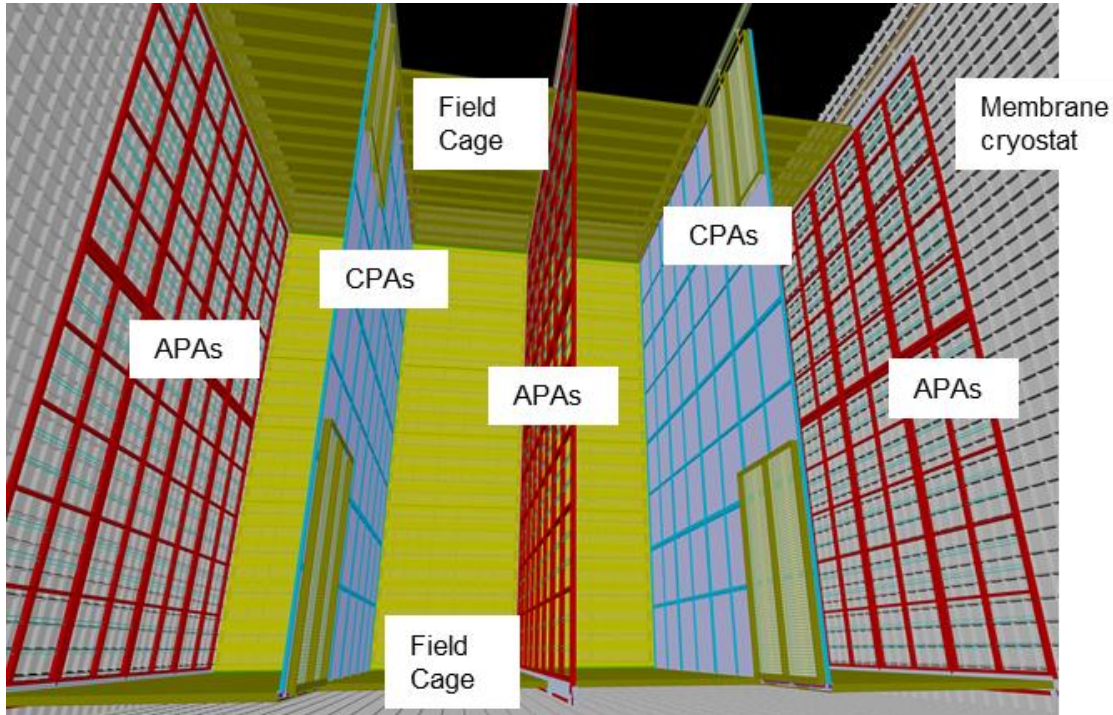
- Neutrino beam from FNAL to Homestake
 - 1,300 km long baseline
 - 1.2 MW (\rightarrow 2.4 MW)
- Two parallel caverns each have two 10 kt detector pits with a laydown space in between
- The CF utilities and cryogenics are in a separate parallel cavern, to alleviate conflicts with cryostat & detector installation

DUNE Far Detector

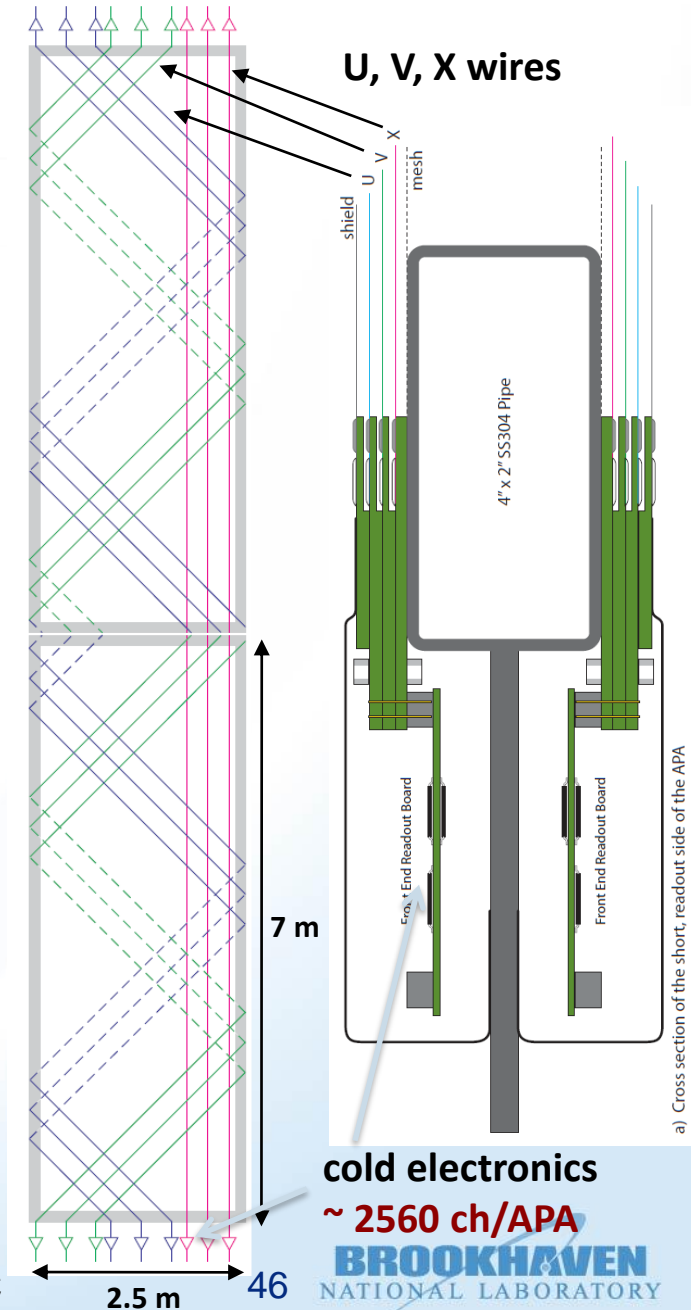
- Four separate 17 kt (> 10 kt fiducial) LAr TPCs
- 4 identically sized cryostats: 2 single phase (SP) + 1 dual phase (DP) + 1 “opportunity” (this 2+1+1 plan is described in TDR)



DUNE Far Detector

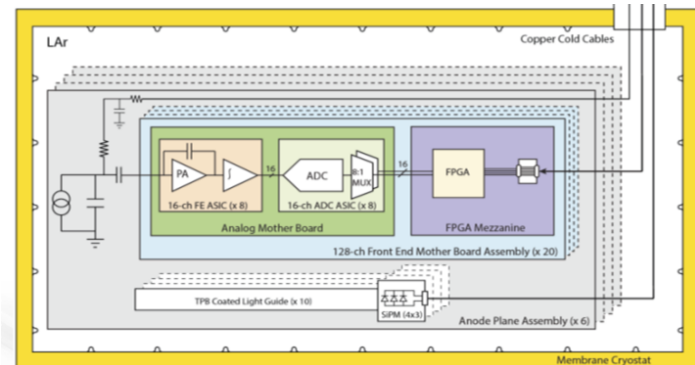


- APA, CPA & front-end cold electronics system for single phase DUNE far detector
- DUNE 10 kt Far Detector
 - ***384,000 channels***
 - 24,000 FE ASICs/24,000 ADC ASICs
 - 6,000 COLDATA ASICs
 - 3,000 Front End Mother Board assemblies

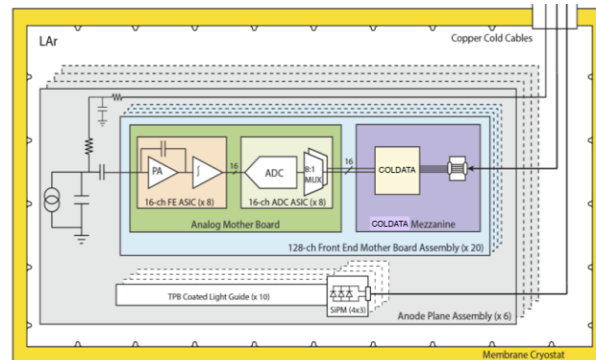


Cold Electronics FEMBs

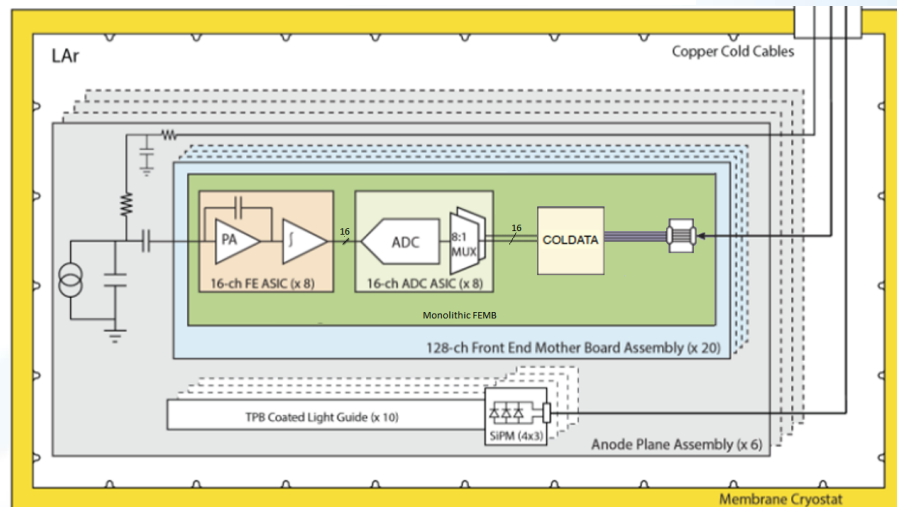
FPGA Mezzanine based FEMB



Mezzanine Three ASIC FEMB



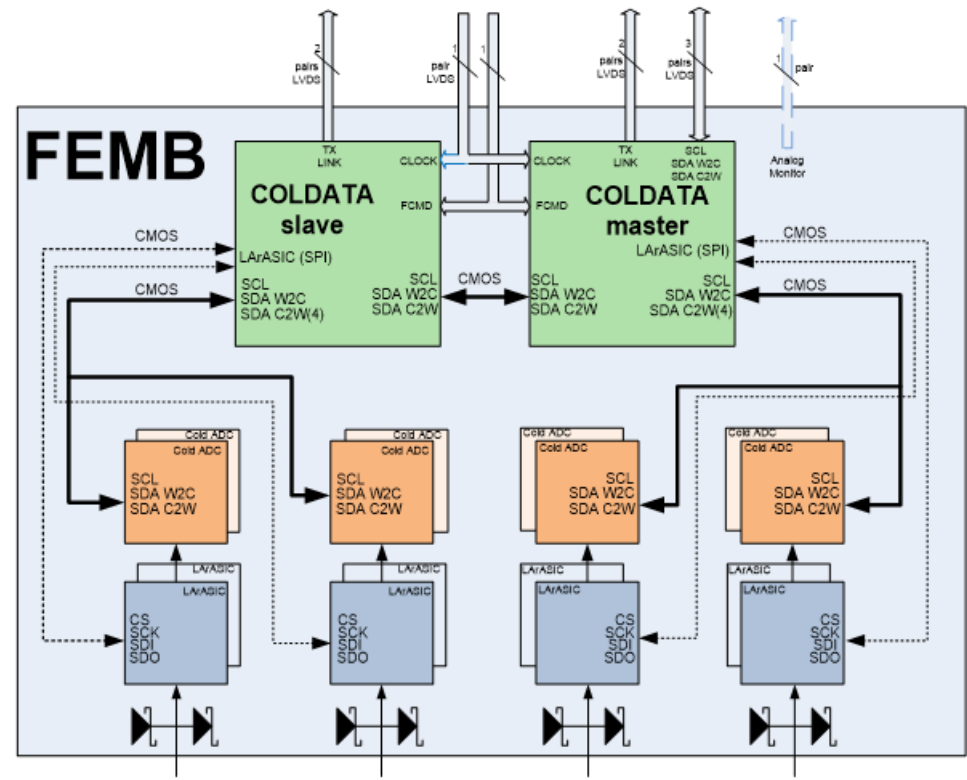
Monolithic Three ASIC FEMB



- FPGA Mezzanine based FEMB
 - LArASIC + ColdADC + FPGA
- Mezzanine Three ASIC FEMB
 - LArASIC + ColdADC + COLDDATA
- Monolithic Three ASIC FEMB
 - LArASIC + ColdADC + COLDDATA

Monolithic Three ASIC FEMB

- Data cable IO (9 Pairs)
 - 1.28Gb/s TX data link (4 pairs)
 - 2 for each COLDATA
 - I2C link (3 pairs)
 - SDA_W2C standard LVDS
 - SDA_C2W standard LVDS
 - SCL standard LVDS
 - 62.5MHz clock
 - FAST COMMAND
- COLDATA shared signals from WIB
 - 62.5MHz clock
 - Fast command
- COLDATA I2C relay
 - COLDATA has a master slave topology, the master COLDATA interfaces to the WIB using standard LVDS and relays the I2C link to the slave COLDATA and the 8x ColdADC ASICs
- 8x independent SPI links for LArASICs, 4x links per COLDATA



FROM APA

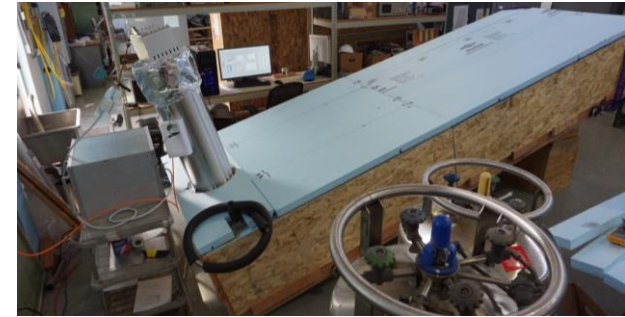
A very Promising Progress towards DUNE CE



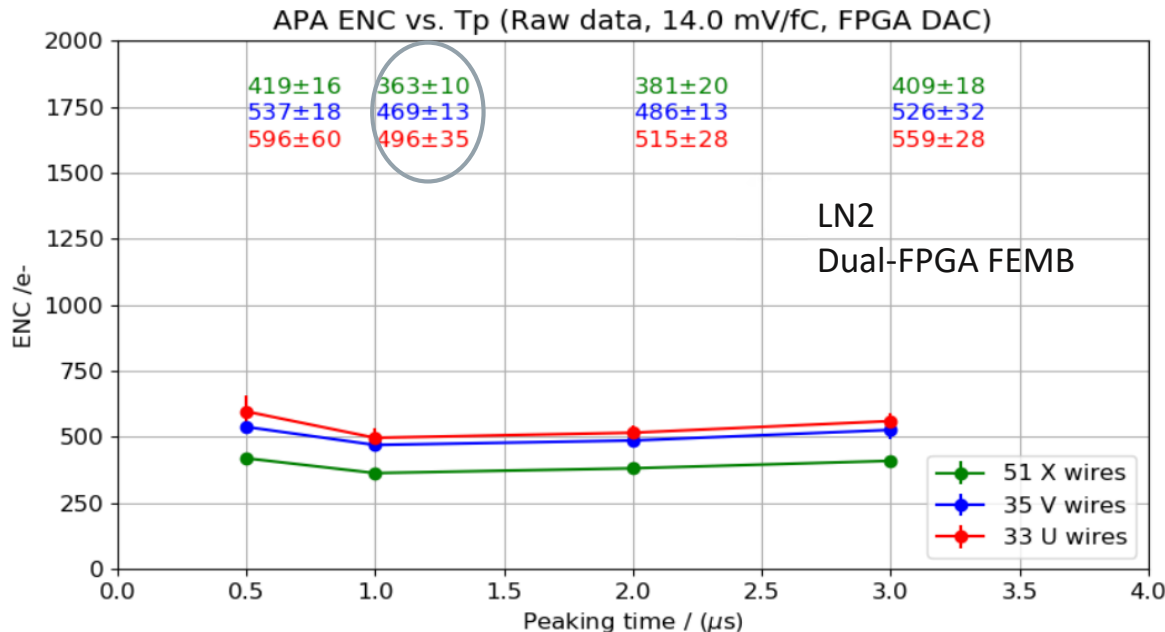
SBND FEMB (FE + COTS ADC + FPGA)



Dual-FPGA FEMB (FE + ColdADC + FPGA)



40% APA integration test stand



- DUNE intermediate FEMB (Dual-FPGA FEMB) gets reasonable noise performance

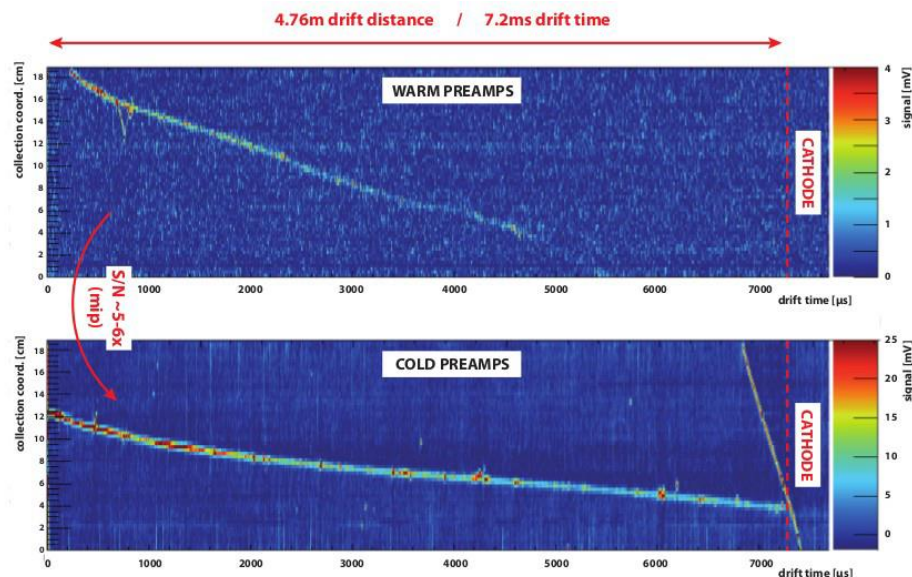
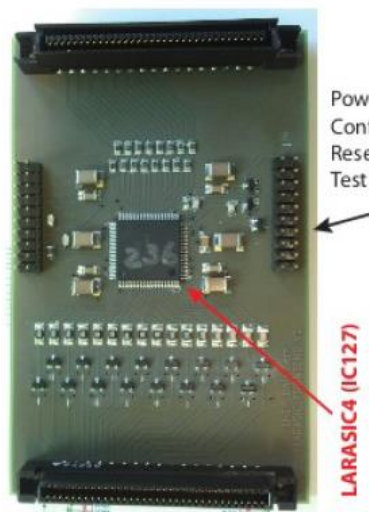
- Gain confidence in final FE + ColdADC + COLDATA FEMB solution

Summary

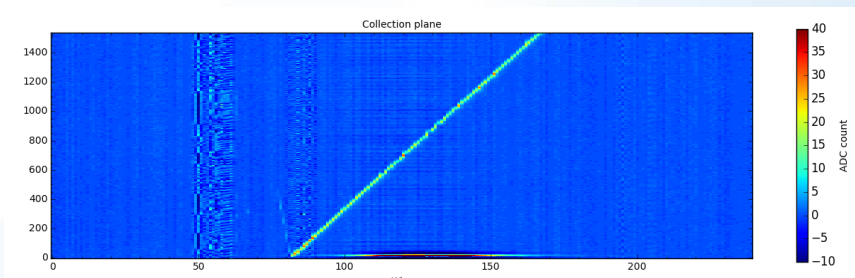
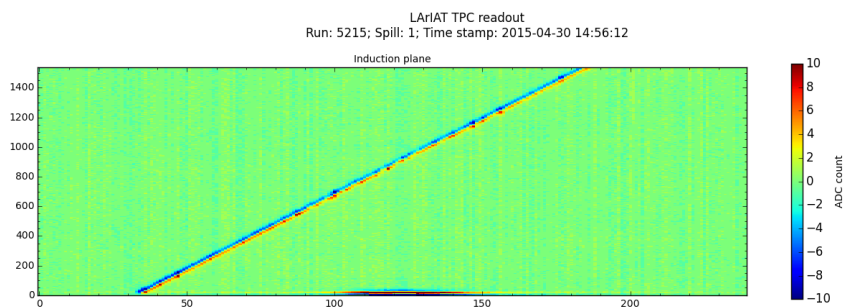
- Readout electronics developed for low temperatures (77K-300K) is an **enabling** technology for noble liquid detectors for neutrino experiment
- **An integral design concept** of APA + CE + Feed-through, and Warm Interface Electronics with local diagnostics and strict isolation and grounding rules is crucial for success of LArTPC experiment
- Excellent performance of ProtoDUNE-SP
 - HV, liquid argon purity, and **signal-to-noise**
 - A successful validation towards DUNE-SP LArTPC
- DUNE FD TPC Readout Electronics development proceeds smoothly
 - ProtoDUNE-SP RUN II in 2022 will be instrumented with final 3-ASIC FEMB

BACKUP

Significant S/N Improvement with Cold FE ASIC



5-6x Improvement on S/N with Cold FE in ARGONTUBE (BERN)
 Courtesy of Igor Kreslo @ University of Bern

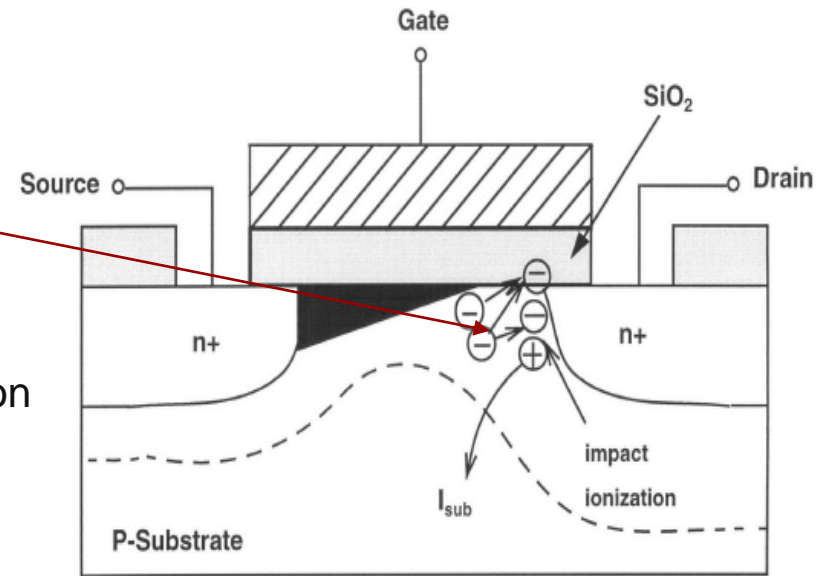


Cold FE ASIC in LArIAT

S/N reaches ~50/1 (from Carl Bromberg @ MSU)

Basics on Hot Carrier Effects

- Some hot electronics exceed the energy required to create an electron-hole pair, resulting in **impact ionization**
 - charge trap in oxide, interface generation → shift in V_{th} and g_m
 - “Degradation”: a decrease in I_{ds} and g_m and increase in V_{th} is due to interface state creation
- **Substrate current** is a monitor of **impact ionization** And of **interface states creation**
 - increases with drain voltage
 - is higher in short channel devices
 - has a maximum at $V_{gs} \approx V_{ds}/2$
 - **increases as the temperature decreases**
- Reliability at cryogenict temperature can be guaranteed by
 - decreasing V_{ds}
 - i.e. decreasing the supply voltage
 - decreasing V_{gs}
 - i.e. decreasing the drain current density
 - increasing L
 - i.e. non-minimum channel length devices



$$\tau \propto I_{sub}^{-3}$$

"LAr TPC Electronics CMOS Lifetime at 300K and 77K and Reliability under Thermal Cycling," IEEE Trans. on NSci, 60, No: 6, Part: 2, p4737(2013)

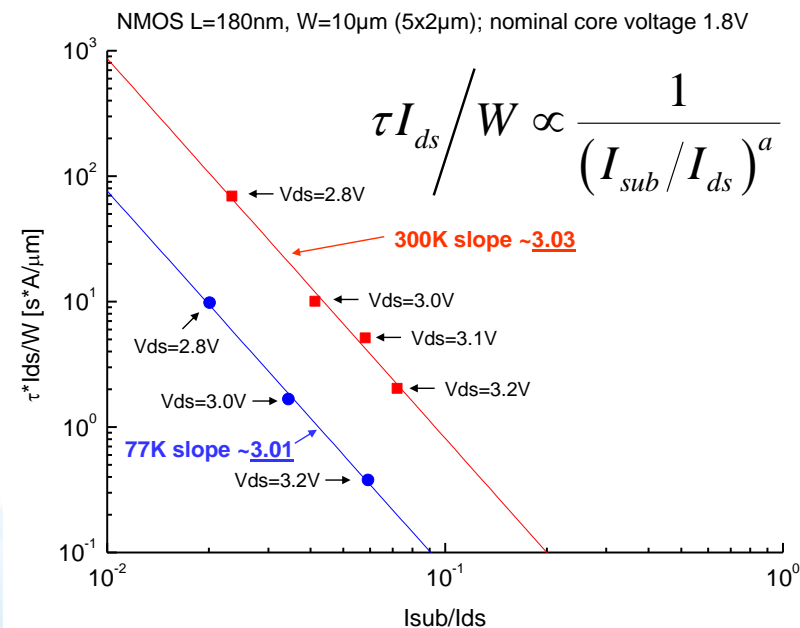
Accelerated Lifetime Test (ALT)

■ CMOS in DC operation

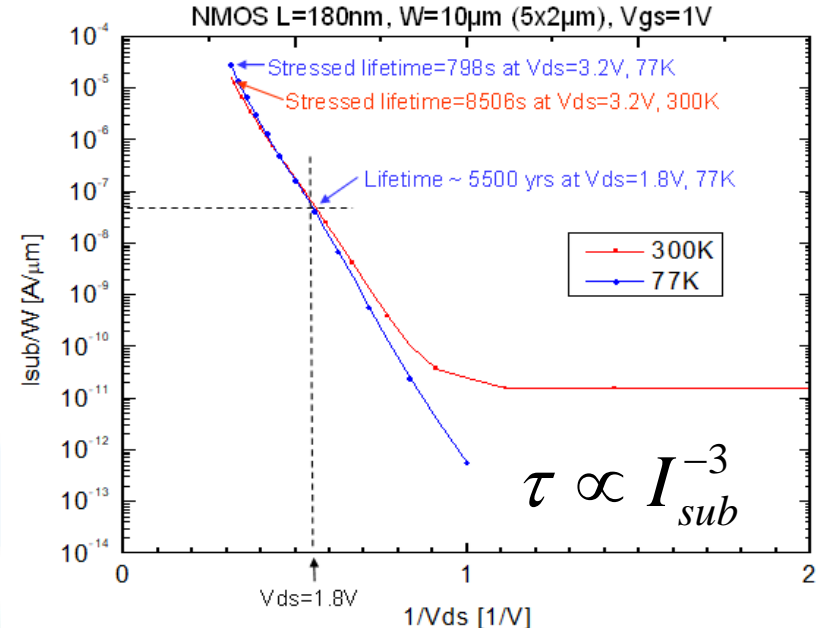
- ALT at any temperature (well-established by foundries) transistor is placed under a severe electric field stress (large V_{DS}), to reduce the lifetime due to hot-electron degradation to a practically observable range.

■ CMOS in AC operation

- Lifetime of digital circuits (ac operation) is extended by the inverse duty factor $4/(f_{\text{clock}} * t_{\text{rise}})$ compared to dc operation. This factor is large (>100) for deep submicron technology and clock frequency needed for TPC

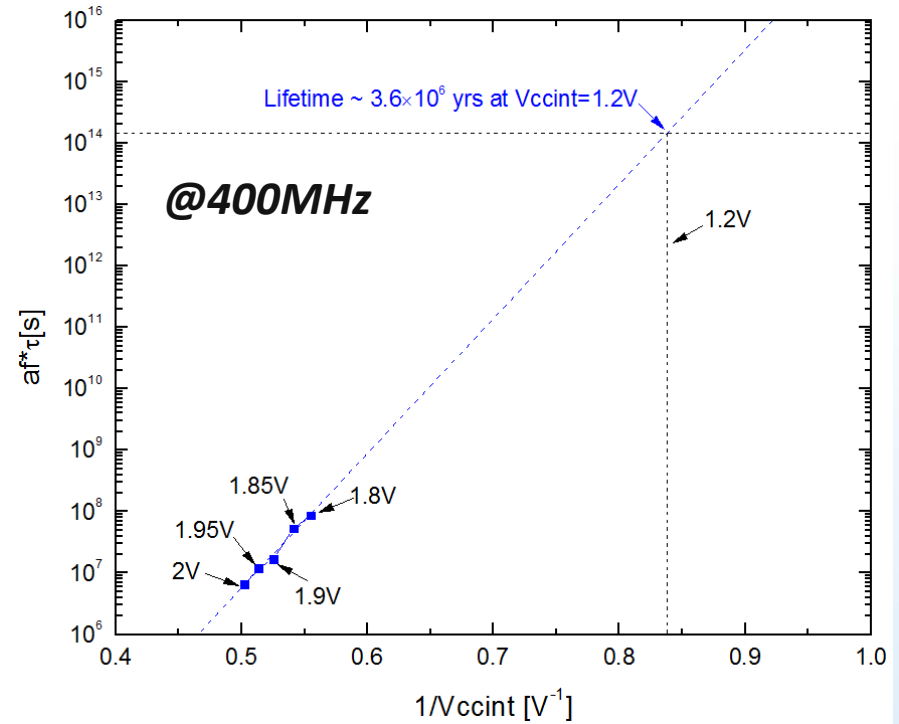
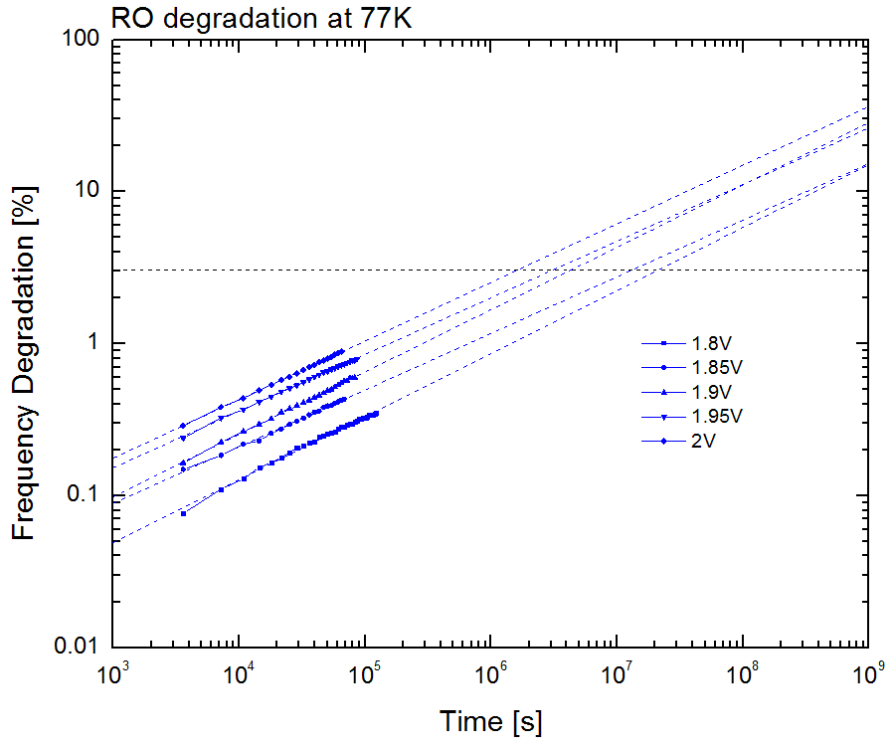


Measurement Type I: "Stress Plot"



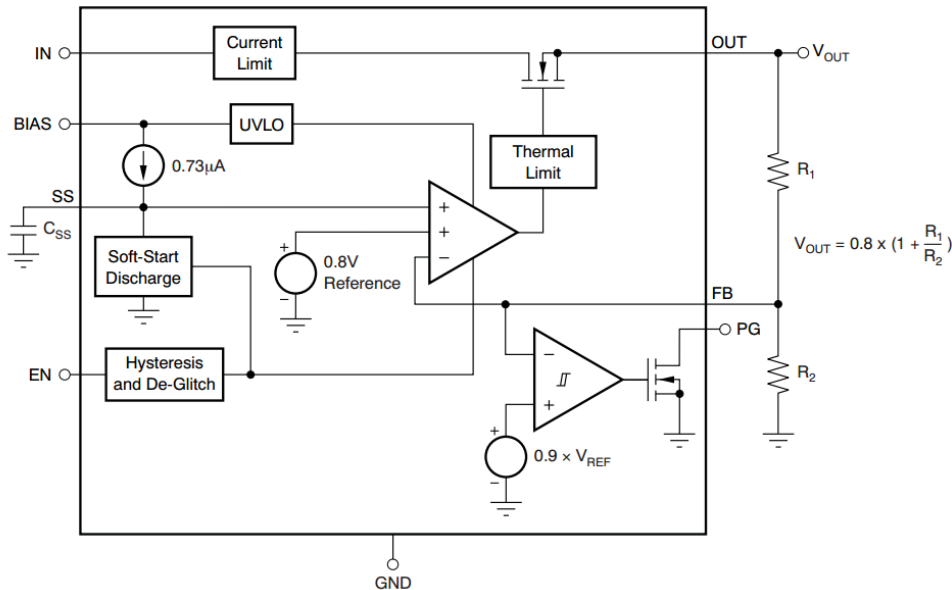
Measurement Type II: Substrate current I_{sub} vs $1/V_{ds}$

Lifetime Projection of FPGA

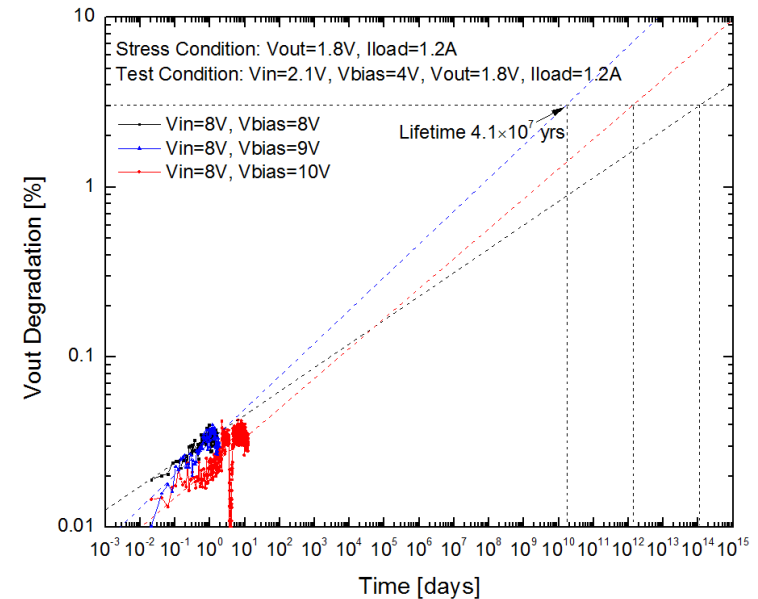


- Traditionally, lifetime is projected by empirical equation $\log_{10}\tau \propto 1/V_{ds}$. The target operation frequency is 400MHz while the RO is stress under 1.7GHz. To include the effect of higher stress frequency, frequency acceleration factor α_f is introduced which is defined as $\alpha_f = \frac{f_{\text{stress}}}{f_{\text{target}}}$. The equation for lifetime projection is modified as: $\log_{10}\alpha_f\tau \propto 1/V_{ds}$
- Following the above equation, lifetime of FPGA at 77K is projected to be 3.6×10^6 years for 3% degradation criteria, giving a wide margin over the physical target (>20 years).

Regulator Stress Test



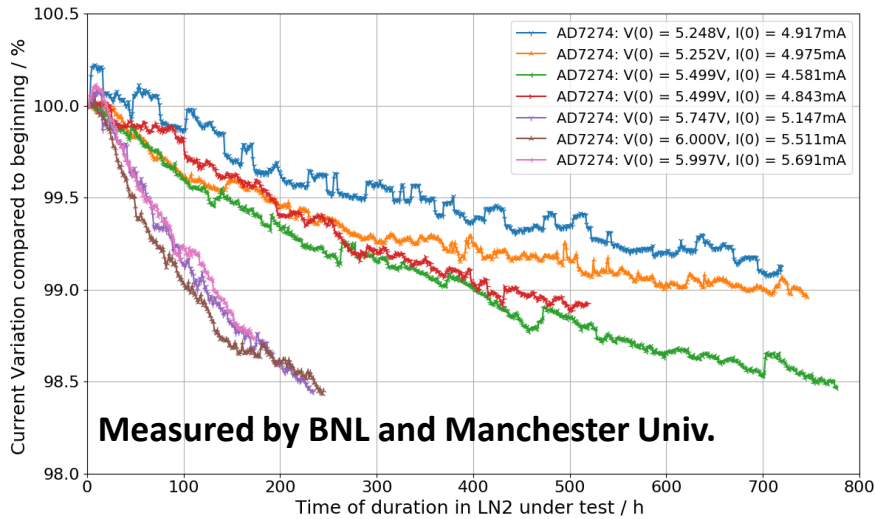
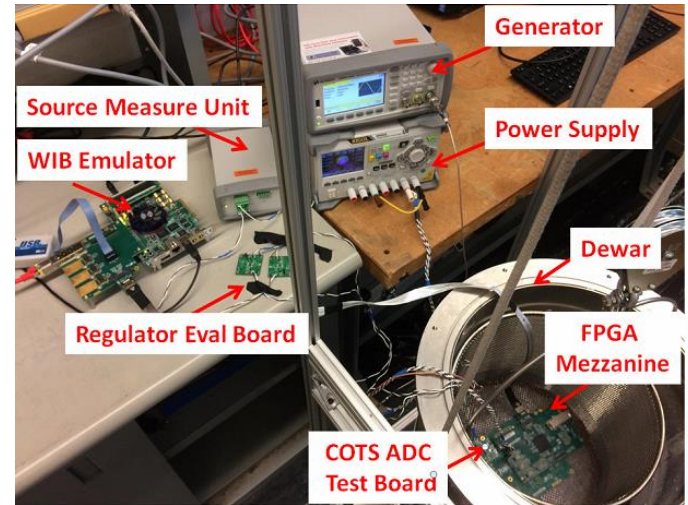
Block diagram of TPS74201 from the datasheet. Pin IN is the input voltage of the regulator while BIAS is the bias voltage for the internal logics. The absolute maximum voltage for both voltages is 6V.



Regulators are stressed under different voltages. For criteria of 3% degradation, the regulator under stress ($V_{in}=V_{bias}=8V$) already exhibits a lifetime of more than 10^7 years. Therefore, the operation of the regulator under normal operation ($V_{in}=2.1V$, $V_{bias}=4V$) at 77K is not of concern.

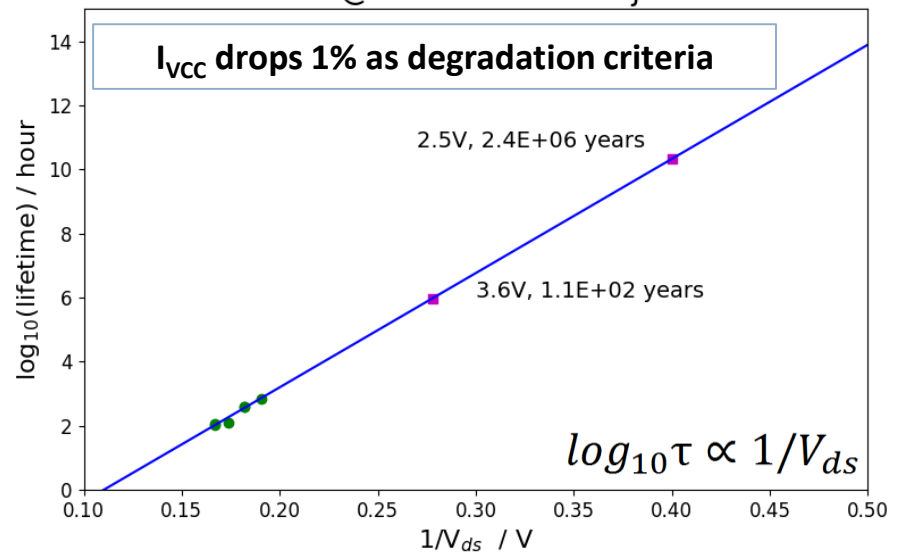
SBND COTS ADC Cold Lifetime Study

- The COTS ADC work **benefits the future** program, which serves as a backup for DUNE far detector
- **AD7274** has gone through extensive lifetime study
 - 100% cold yield
 - 0.25 LSB scale DNL measurement
 - < 5 mW at 2MS/s



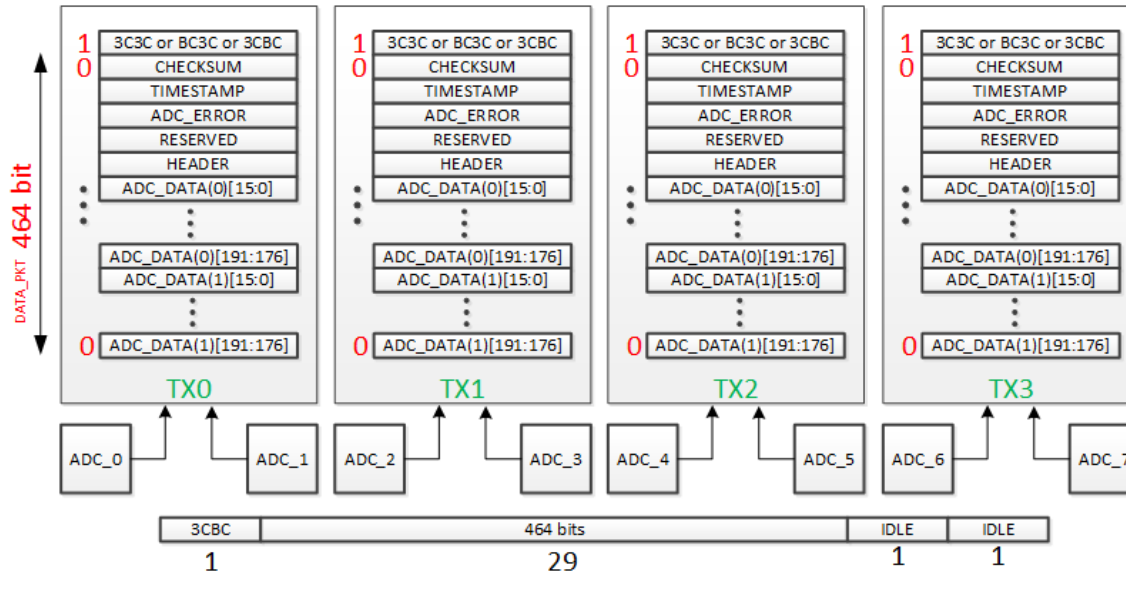
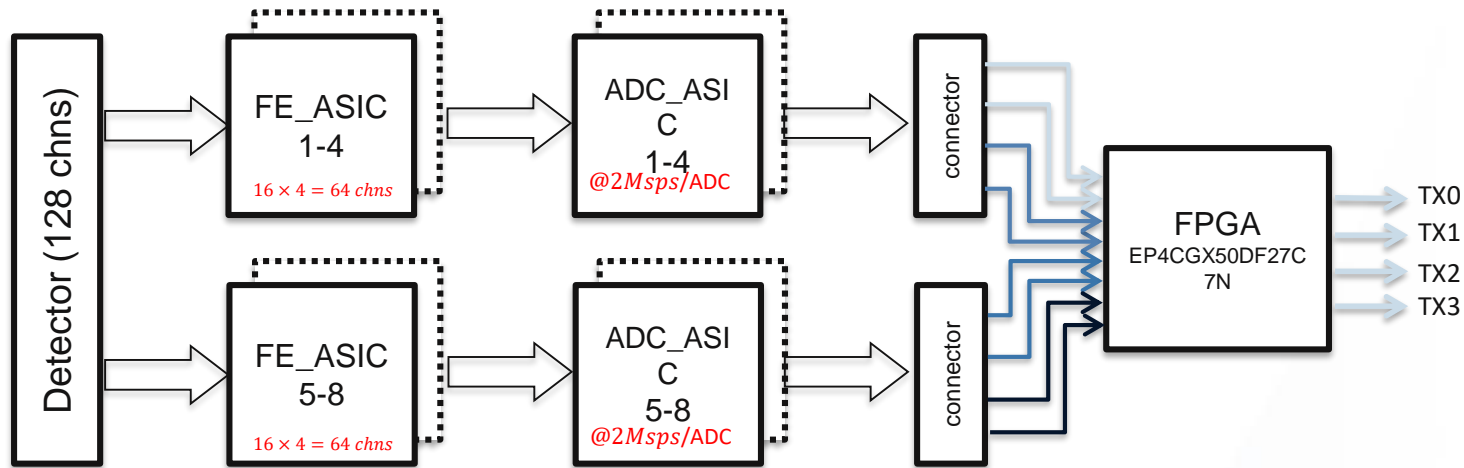
- The HCE is negligible for COTS ADC used in SBND, and we'll be staying out of HCE during the detector operation

AD7274@LN2 Lifetime Projection



SBND collaboration has made decision to use COTS ADC

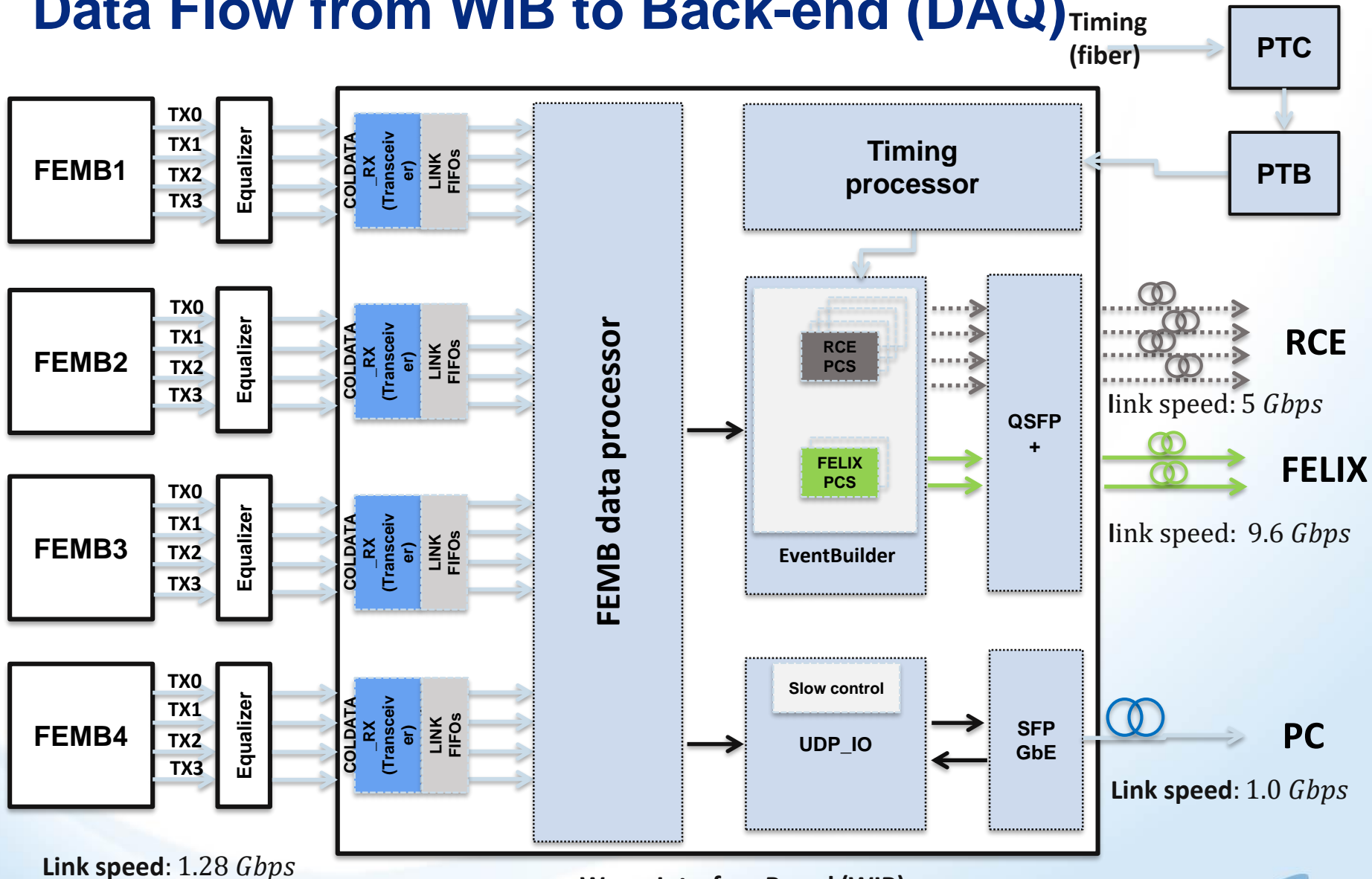
Data Flow from FEMB to WIB



For each Tx lane

- **Data rate of payload**
 $29 \times 16\text{bit} \times 2\text{MHz} \times 1.25(8B/10B) = 1.16\text{Gbps}$
- **Data rate of physical link**
 $32 \times 16\text{bit} \times 2\text{MHz} \times 1.25(8B/10B) = 1.28\text{Gbps}$

Data Flow from WIB to Back-end (DAQ)



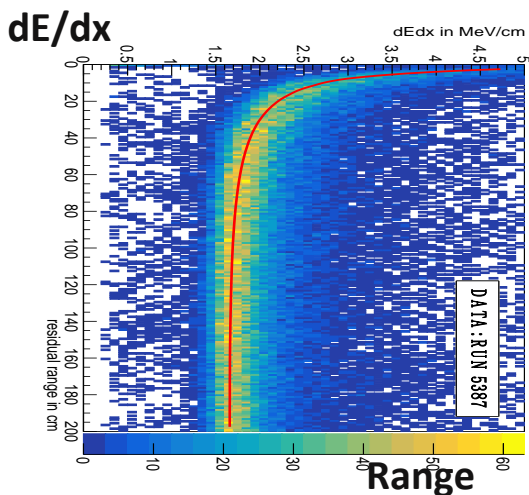
Link speed: 1.28 Gbps

Warm Interface Board (WIB)

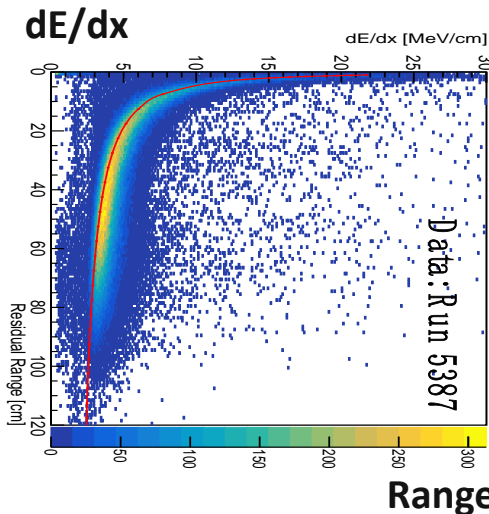
S.Gao – CE for LArTPC

Excellent Detector Response

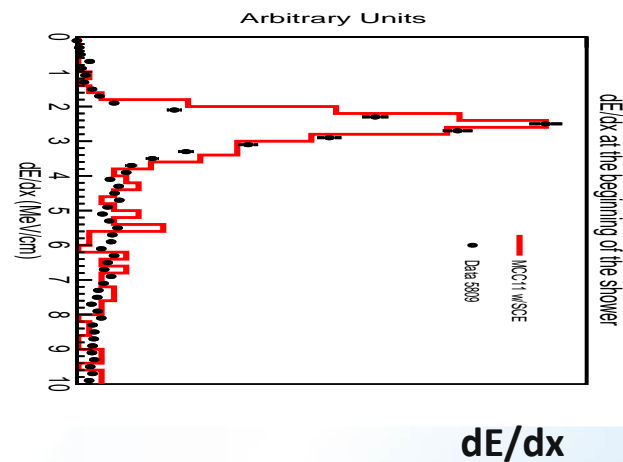
Good agreement between measured specific energy loss (dE/dx) and expectations from simulations.



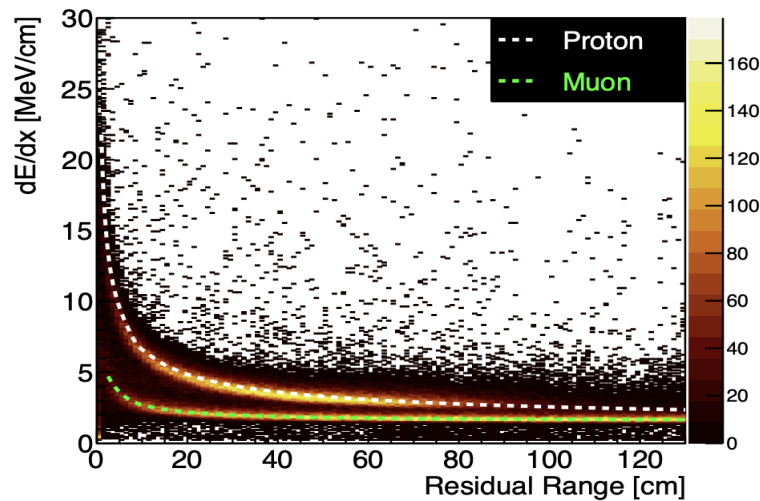
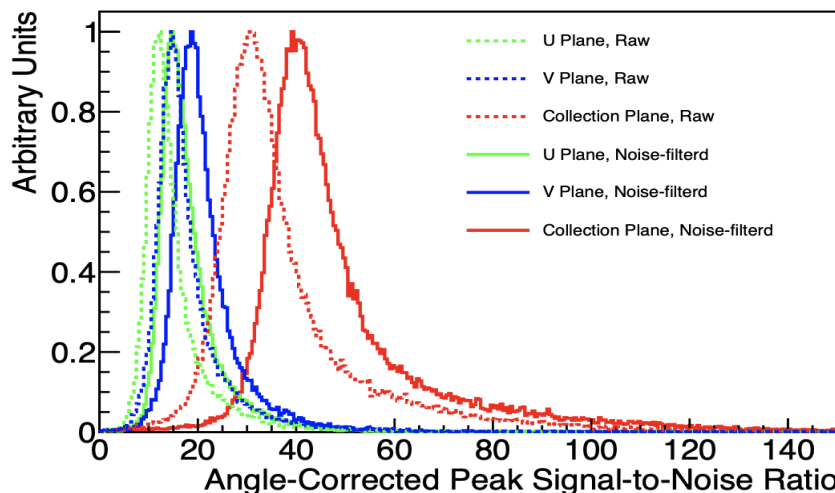
Cosmic ray muons



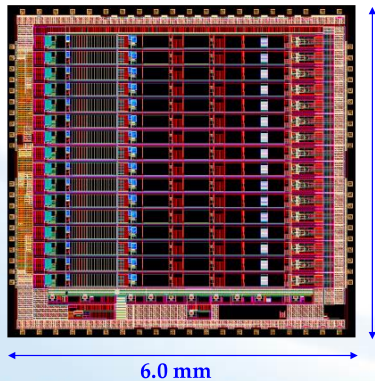
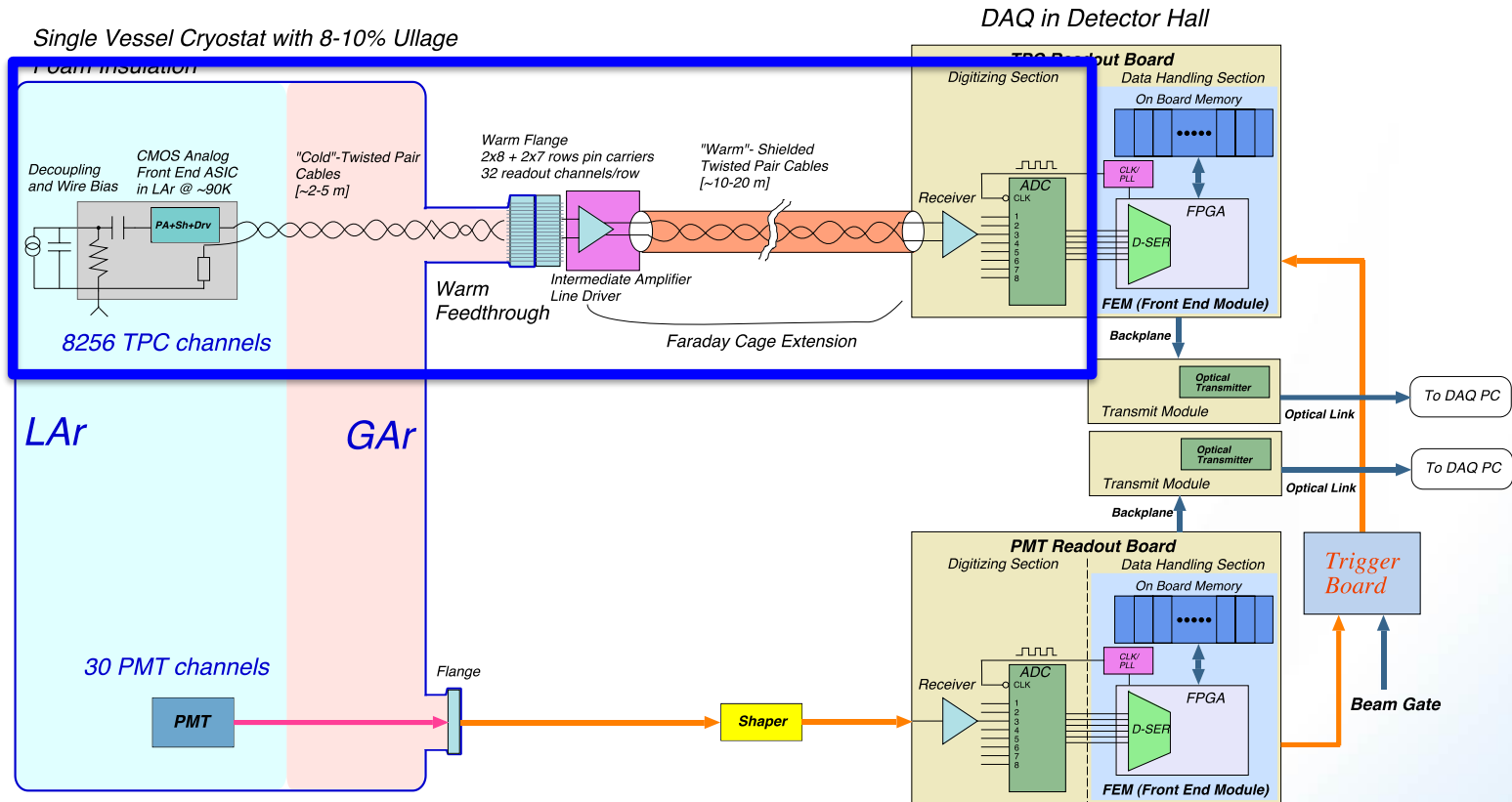
1 GeV beam stopping protons



1 GeV beam positrons

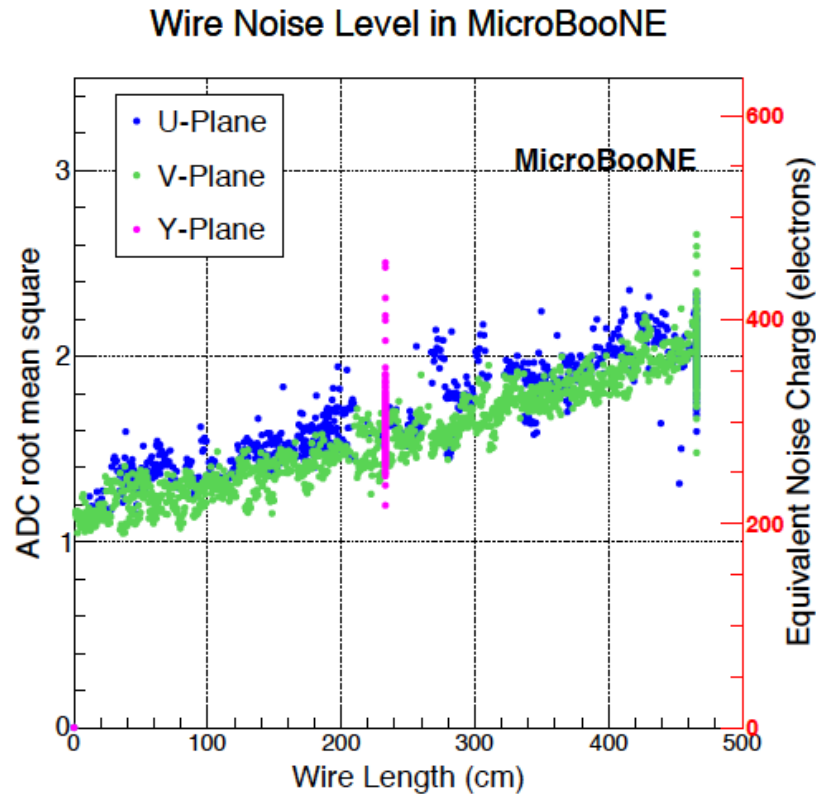


MicroBooNE Readout Electronics System



- MicroBooNE is the **first** experiment instrumented with cold CMOS ASICs
- Analog front end ASIC designed in 180 nm is running in LAr (~89 K) to achieve optimal signal to noise ratio
- The MicroBooNE front end readout electronics system was designed as an **integral system**, with TPC, signal feed-through and warm interface electronics

MicroBooNE TPC Noise vs. Wire Length

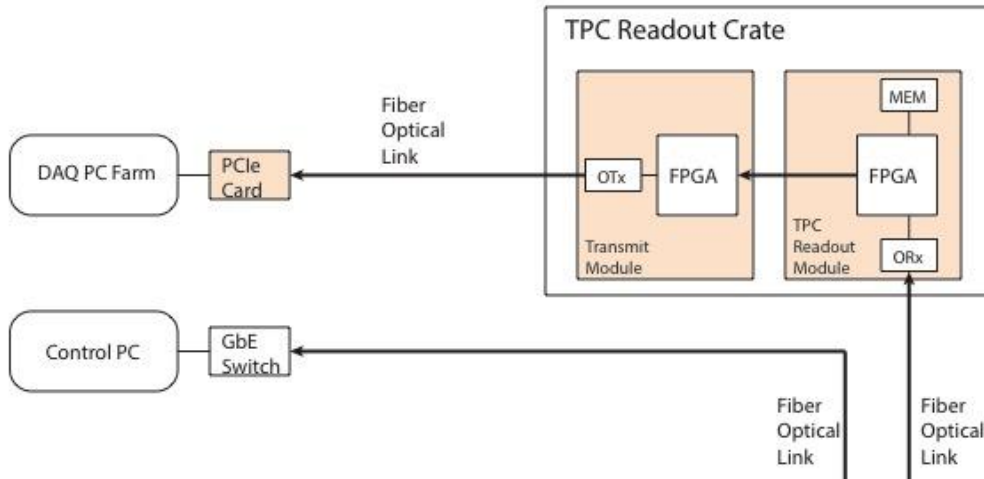


- ENC after noise filtering is **< 400 electrons** for 85% of channels, in agreement with bench tests of FE ASIC
 - SNR is improved by more than factor of 3 compared to previous large scale LArTPC experiment (e.g ICARUS)
- Excellent work by MicroBooNE physics and cold electronics team at BNL was published
 - R. Acciarri *et al.* [MicroBooNE Collaboration], "Noise Characterization and Filtering in the MicroBooNE Liquid Argon TPC," JINST **12**, no. 08, P08003 (2017)

SBND and ProtoDUNE-SP Electronics System

- SBND and ProtoDUNE-SP share many common development of front end readout electronics
 - SBND: 11,264 channels vs. ProtoDUNE-SP: 15,360 channels
 - Shared development of Cold FE ASICs
 - The functionality of the FEMB (Front End Mother Board) is the same
 - Small differences in layout are required due to the different wire spacing, choice of ADC and readouts in the two detectors
 - FPGA mezzanine has minor difference on connectors due to the choice of cold cable
 - The feed-throughs are similar from an electrical connection point of view, but different in cold cable interface
 - The Warm Interface Electronics is similar with small differences in the way the timing protocols are handled.
- Both systems follows the *integral design* concept
 - APA + cold electronics + warm interface

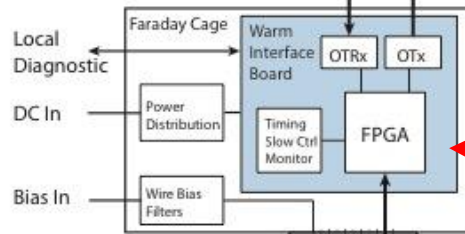
SBND TPC Electronics



Back End Electronics

Front End Electronics

Complete data readout at the feed-through for test and commissioning



Warm Interface Electronics: crate with 28 boards

Signal Feed-through (4 sets)

Cold Cable (4 bundles)

Cold Electronics:

- 704 FE ASICs/11,264 COTS ADC/88 Cold FPGAs
- 88 Front End Mother Board assemblies

