SMALL SENSOR DIODES WITH LFOUNDRY 150NM

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Status of LFoundry

The SMIC Chinese foundry quietly sold LFoundry to startup Wuxi Xichanweixin

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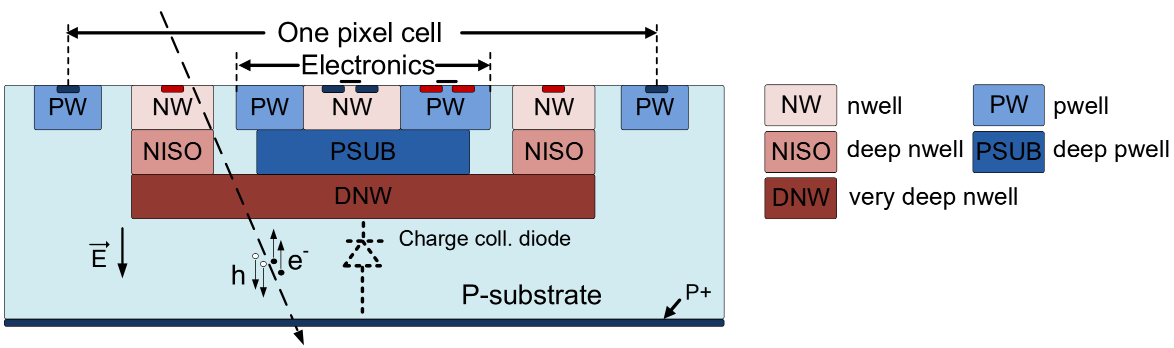
WHY USING LFOUNDRY 150NM FOR HEP EXPERIMENTS?

LFoundry 150 nm CMOS technology

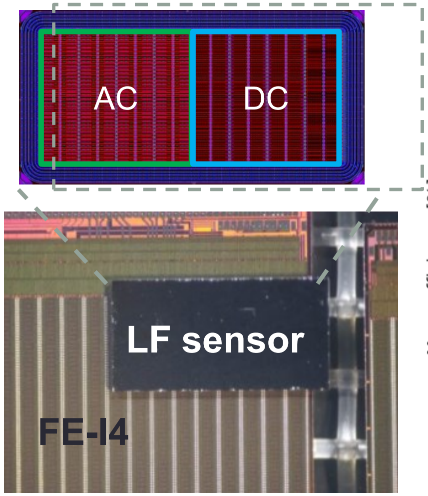
High-rad. environment=> fast charge collection => depleted sensitive layer => $d \sim \sqrt{\rho \cdot V}$

- Up to 7 metal layers
- Multiple nested wells
  - => DNW as a large collection electrode
  - => No restriction to PMOS inside pixel
- High res. (> 2 kΩ·cm) P-substrate
- High reverse bias ~ 350 V
- Backside thinning & processing possible

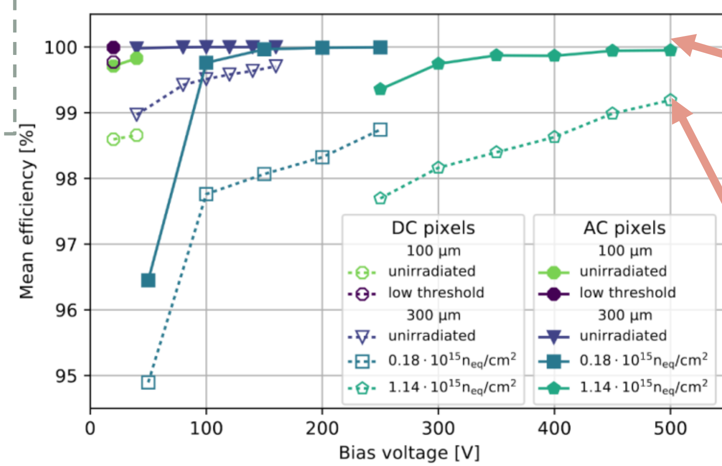


- Uniform drift field 🙂
- High Cd ☹

LFoundry passive CMOS : bare sensor performance proven

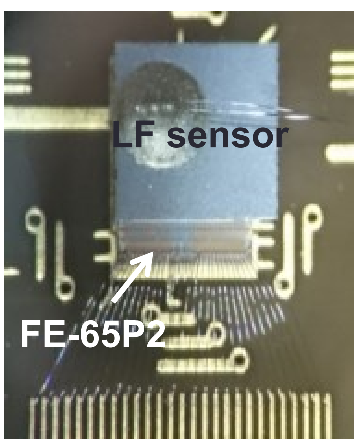


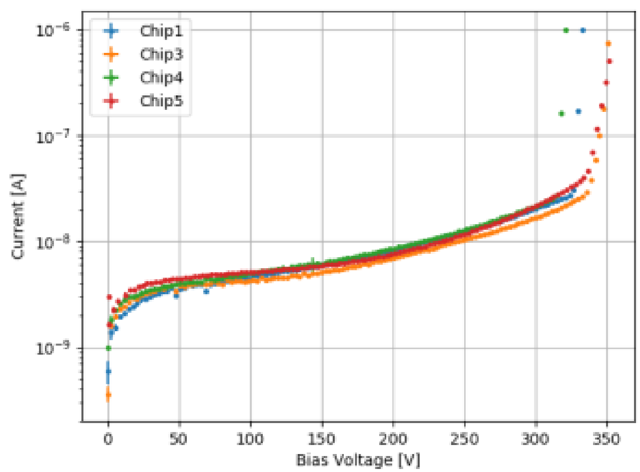
D.-L. Pohl, et al., doi.org/10.1088/1748-0221/12/06/P06020



AC pixels, $1.10^{15} n_{eq}/cm_2$
=> *Efficiency* ~ 100%

DC pixels, $1.10^{15} n_{eq}/cm_2$
=> *Efficiency* > 99%
=> *Similar to ATLAS IBL planar sensor*

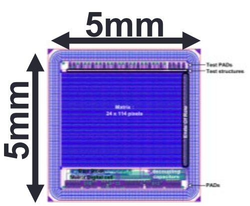




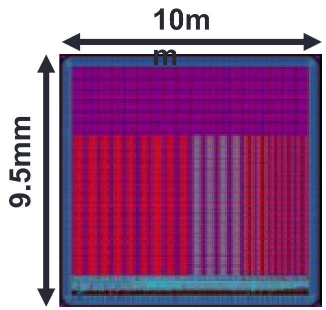
Breakdown @ ~ 350 V

LFoundry prototyping line (ATLAS)

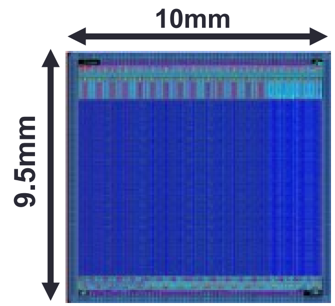
CCPD_LF

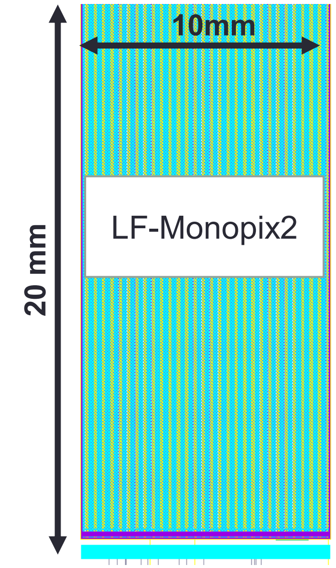


LF-CPIX (Demonstrator)



LF-Monopix1 (Monolithic)





CCPD_LF
- *Subm. in **Sep. 2014***
- *33 x 125 μm^2 pixels*
- *Fast R/O coupled to FE-I4*
- *Standalone R/O for test*
- *Bonn/CPPM/KIT*

LF-CPIX (DEMO)
- *Subm. in **Mar. 2016***
- *50 x 250 μm^2 pixels*
- *Fast R/O coupled to FE-I4*
- *Standalone R/O for test*
- *Bonn/CPPM/IRFU*

LF-Monopix1
- *Subm. in **Aug. 2016***
- *50 x 250 μm^2 pixels*
- *Fast column drain R/O*
- *Bonn/CPPM/IRFU*

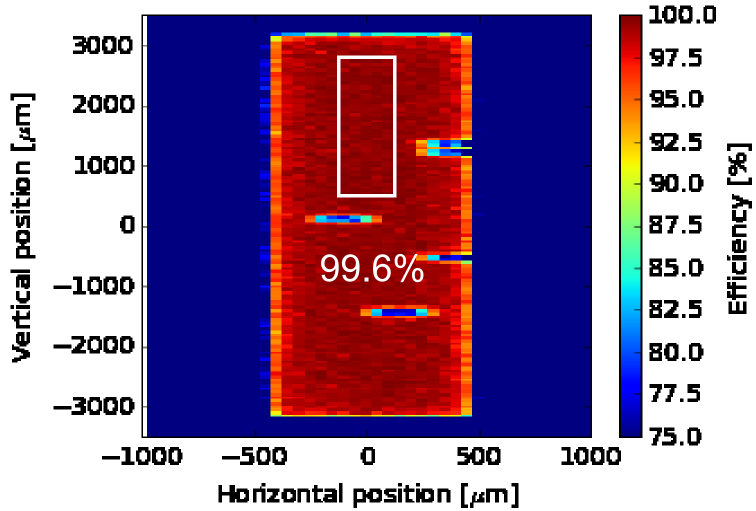
LF-Monopix2
- *Subm. in **May. 2020***
- *50 x 150 μm^2 pixels*
- *Full height matrix*
- *Fast column drain R/O*
- *Bonn/CERN/CPPM/IRFU*

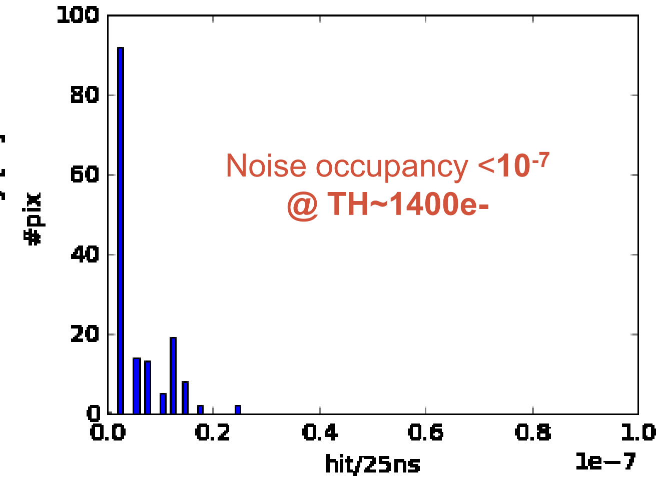
Include also test structures and passive sensor design

LF-MONOPIX1 : ELSA test beam; Efficiency

- Non-irradiated

TH tuned by noise
Columns: 16-20
HV: -200V
Temp: dry ice

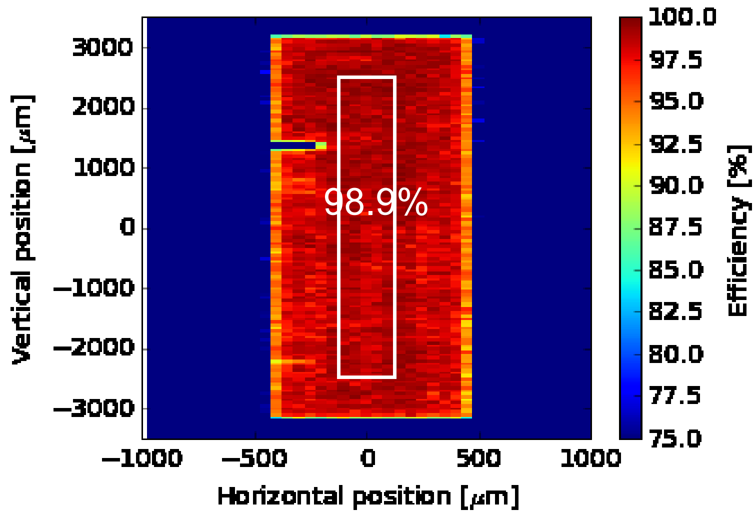


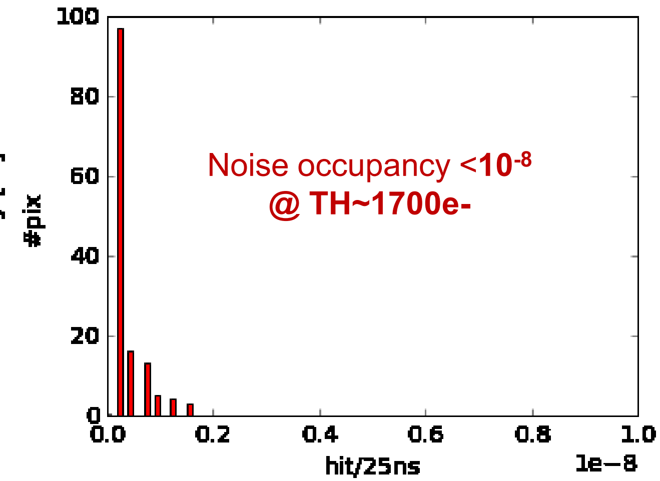


- 1 x $10^{15} n_{eq}/cm^2$

TH tuned by noise
Columns: 16-20
HV: -130V
Temp: dry ice

Reactor neutron at Ljubjana

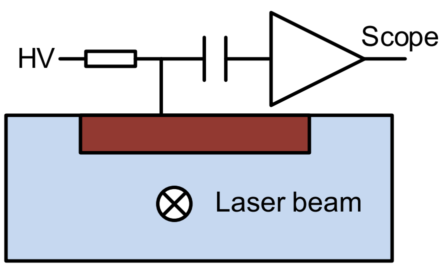


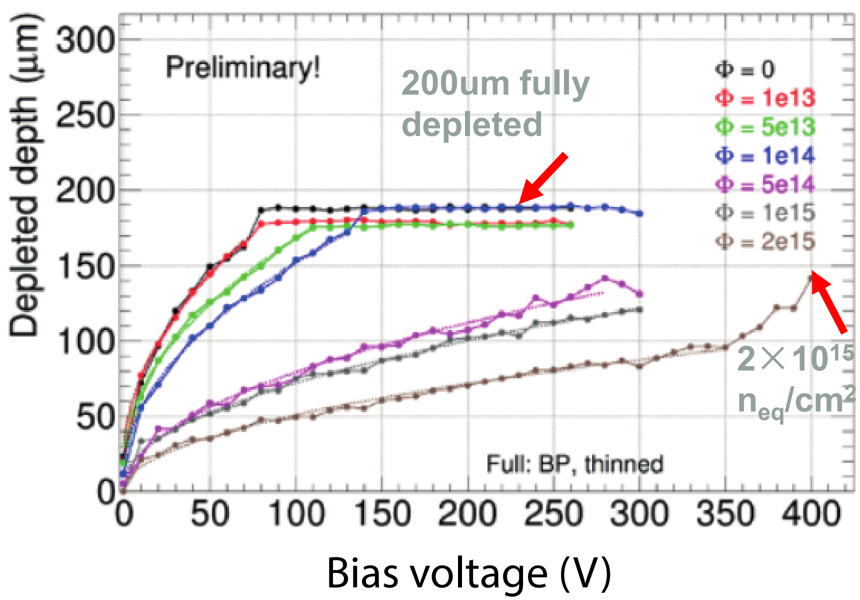


Depletion depth

- Investigated by Edge TcT on LFoundry test structures (2k ohms wafer resistivity)
  - *Depletion depth ~ 140 μm after 2×10^{15} n_{eq}/cm^2*

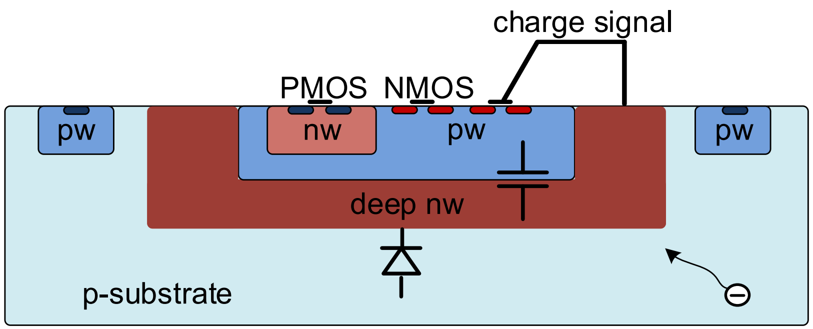
I.Mandić. et al.. doi.org/10.1016/j.nima.2018.06.062

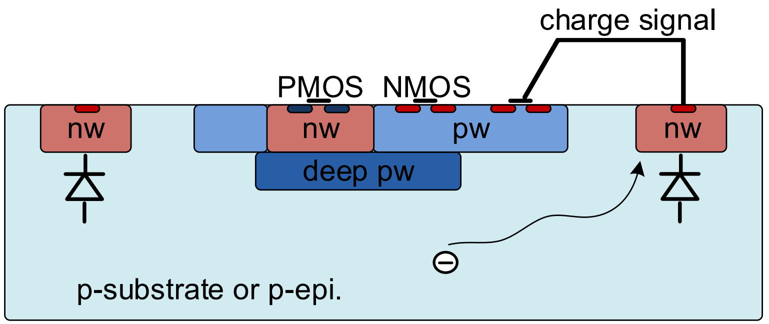




LFOUNDRY 150NM CAN BE USED FOR SMALL SENSOR DIODES?

Sensor design approaches





- ***Large*** charge collection electrode
  - => HR + HV for depletion
  - => no/little low field region
  - => on average short(er) drift path

  } **radhard**
- **Large** sensor **capacitance** (pw & dnw !)
  - => noise & speed (power) penalty
  - => possible x-talk (digital to sensor)

- ***Small*** charge collection electrode
  - => very **small** sensor **capacitance**
  - => lower power budget for analog FE
  - => Less prone to x-talk
- On average **long(er)** travelling path and potentially **low field region**

I. Peric, DOI: 10.1016/j.nima.2007.07.115
T. Kishishita, et al., DOI: 10.1088/1748-0221/10/03/C03047
P. Rymaszewski, et al., DOI: 10.1088/1748-0221/11/02/C02045
T. Hirono, et al., DOI: 10.1109/NSSMIC.2016.8069902

R. Turchetta, et al., DOI: 10.1016/S0168-9002(00)00893-7
W. Dulinski, et al., DOI: 10.1109/TNS.2004.832947
A. Dorokhov , et al., DOI: 10.1016/j.nima.2010.12.112
M. Havránek, et al., DOI: 10.1088/1748-0221/10/02/P02013

First try of small sensor diode CCPD_LF Ver B (2015)

It was made to reach HV=+200V with huge and big Guard-Rings distance.
But Process limitation only allows +30V

1.1.1 PIXEL TYPE B

As the positive High Voltage is applied on the DNwell, all the active components don't need to be isolated from the Psubstrate.

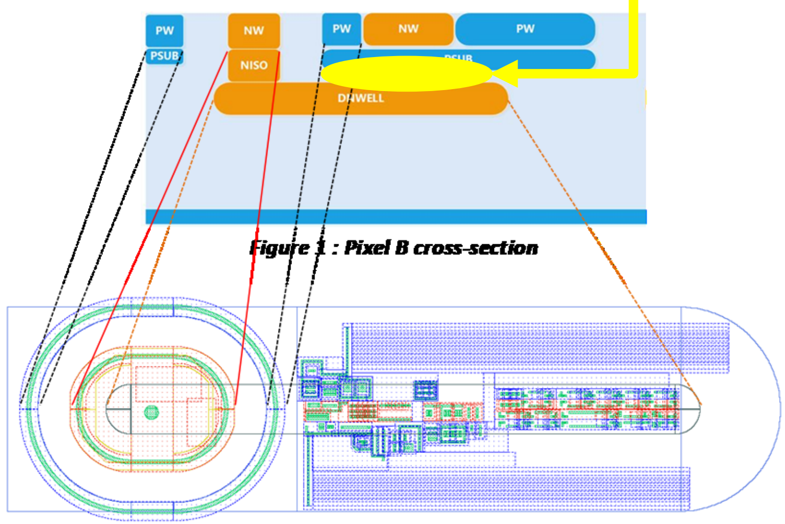
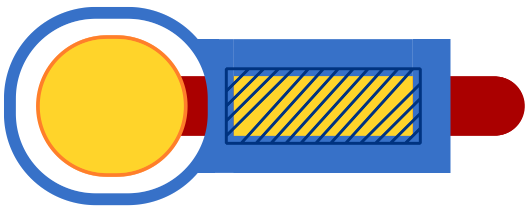


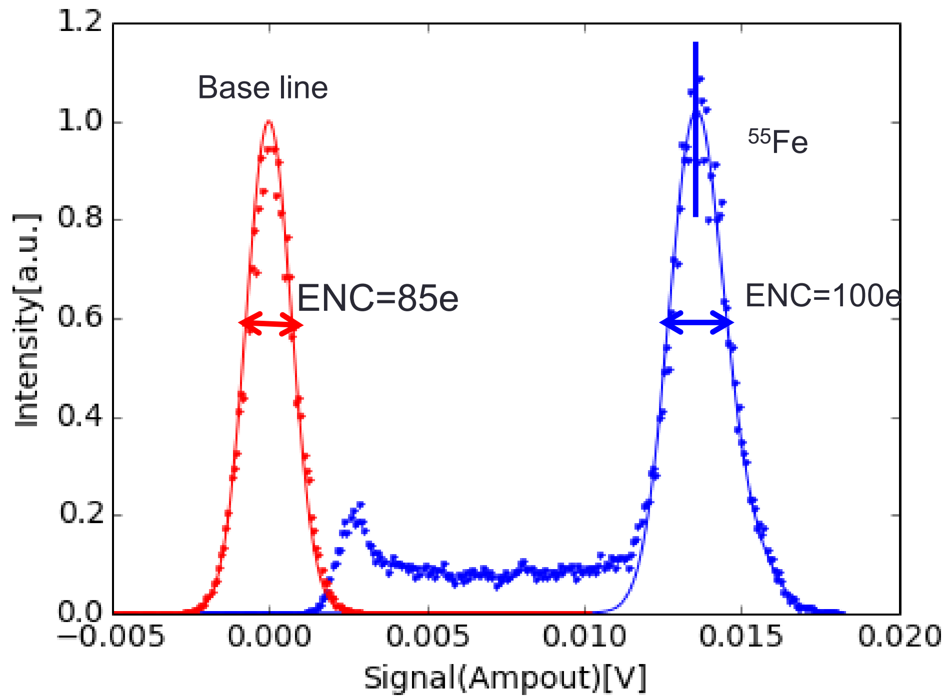
Figure 1 : Pixel B cross-section

Figure 2 : Pixel B layout

CCPD_LF Ver B : Fe55 detection



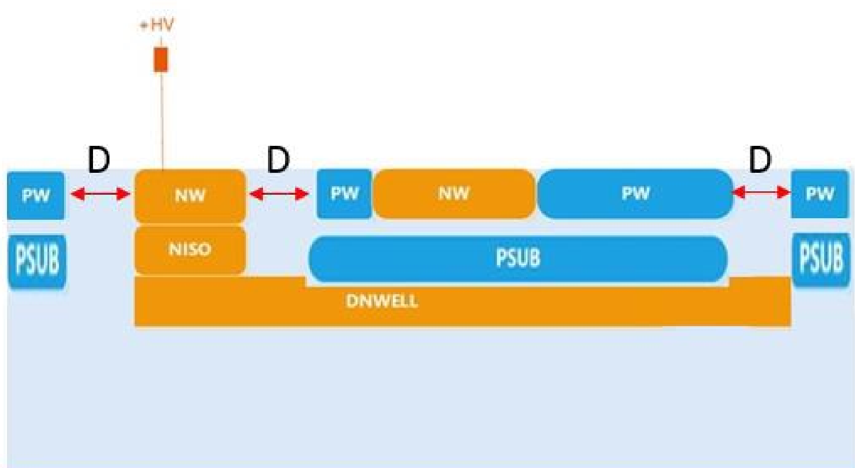
Bias : 20V ; Source: ^{55}Fe

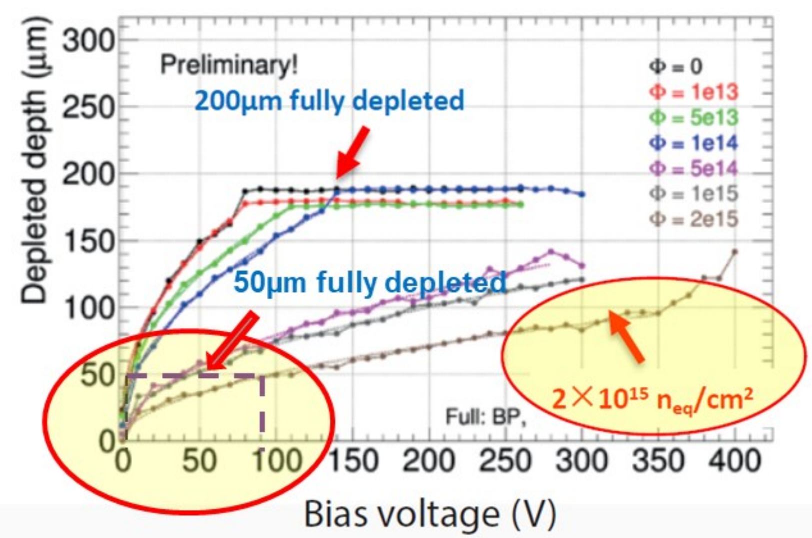


LFOUNDRY 150NM
NEW SMALL SENSOR DIODES

New Rad-Hard Small pixel approach

- Let think to reach a pixel size of 50µm x 50µm x 50µm
  - 50µ x 50µ square and 50µ depth
  - From ~10V (no Irrad) to 90V (2x10^{15} neq/cm²)
  - With Backside Metallization
  - Less restrictive guardings
  - Uniform drift field

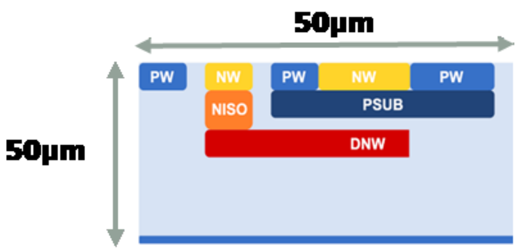




I.Mandić, et al., DOI: 10.1016/j.nima.2018.06.062

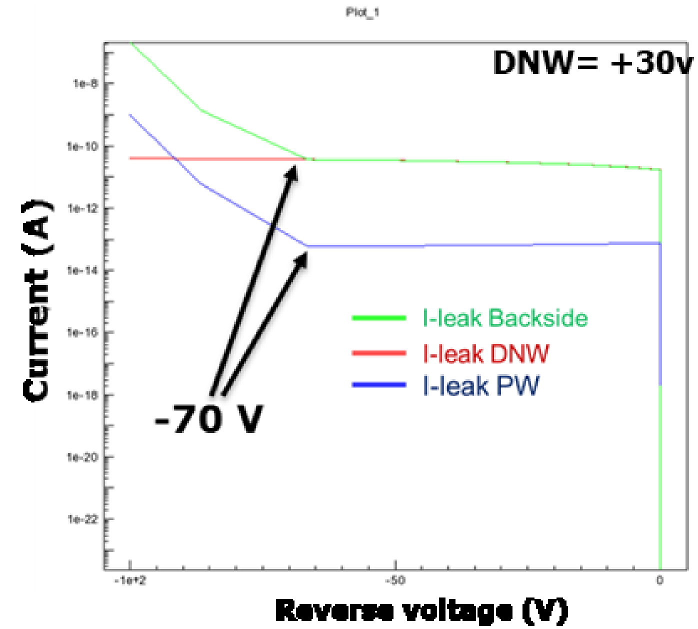
D= distance (very important parameter)

How to reach HV=100V?



Smaller size of the pixel (50µm× 50µm x 50µm)

The total Voltage potential (top to bottom) at **100 V** is achieved and the substrate is fully depleted (50µm)

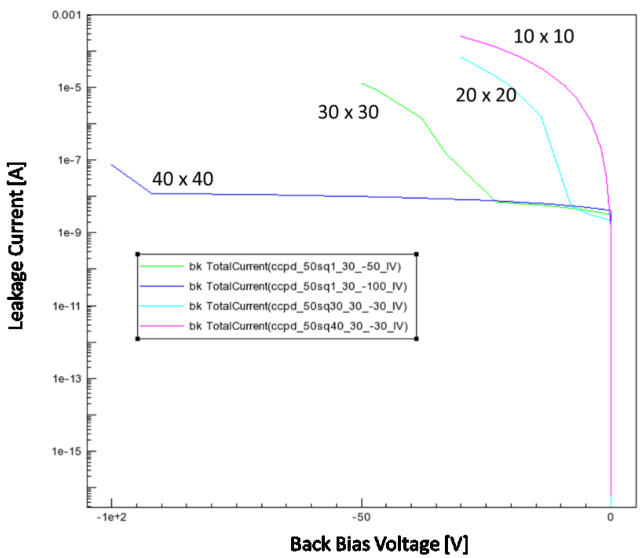


By applying Voltage on TOP and Bottom

And the thickness should be 50µm if we want to keep the pixel efficiency

All TCAD simulations come from TCAD profile from foundry and all results were validated by Lfoundry.

TCAD simulations

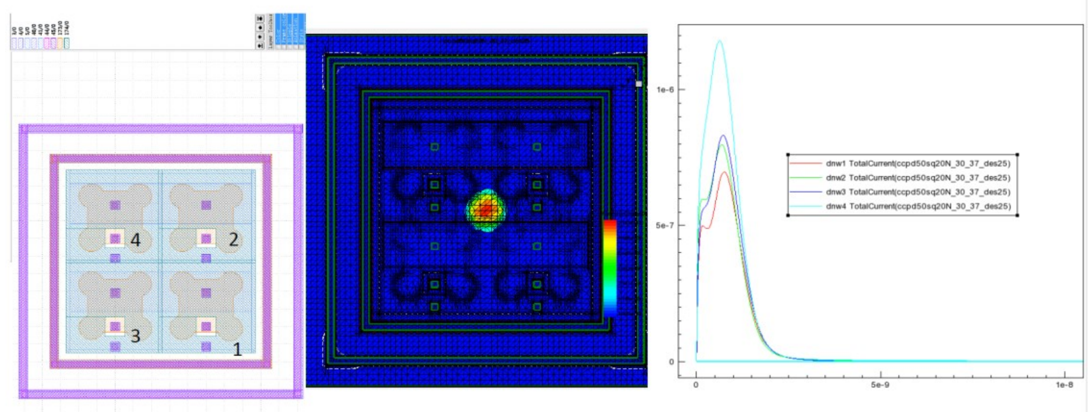


10nA/px leakage current for different diode (DNW) sizes, for a top bias of 30 V

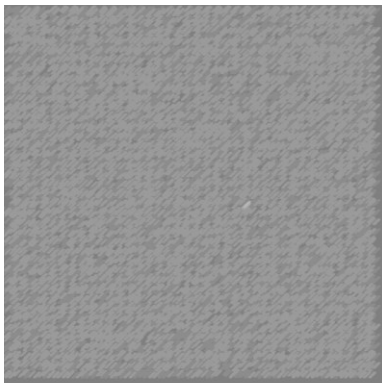
The study also shows that the pixel corners represent a weak point, since the distance between DNW is at its maximum. This means a higher probability for a punch-through between the PSUB layer and the substrate. To resolve this problem, two diode structures were proposed:

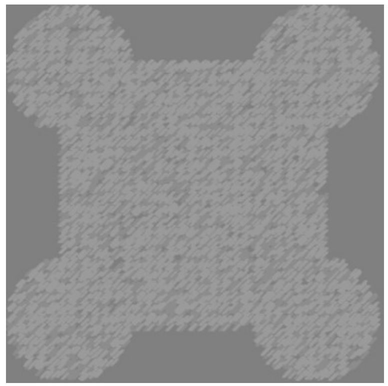
- Square (as a reference)
- Mickey ear square (to minimize the distance)
- Hexagonal (where the maximum distance between DNW is constant)
- Hollow Hexa (to minimize the Capacitance)

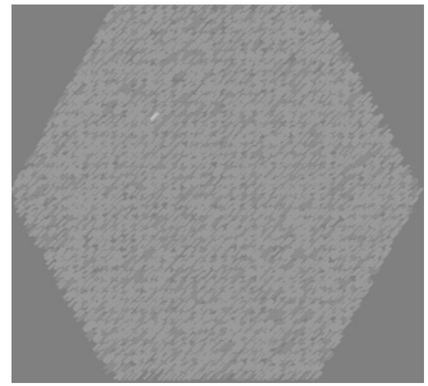
MIP simulation



Small sensor diodes flavors


Square


Mickey

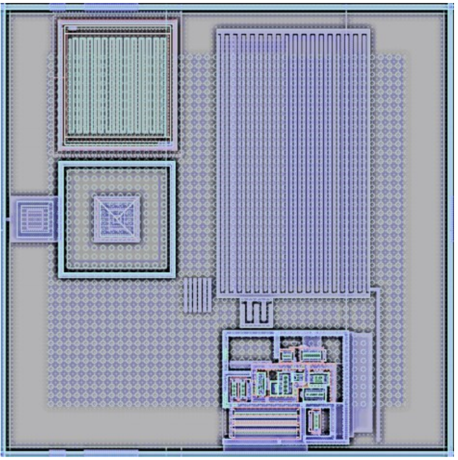

Hexa


Hollow Hexa

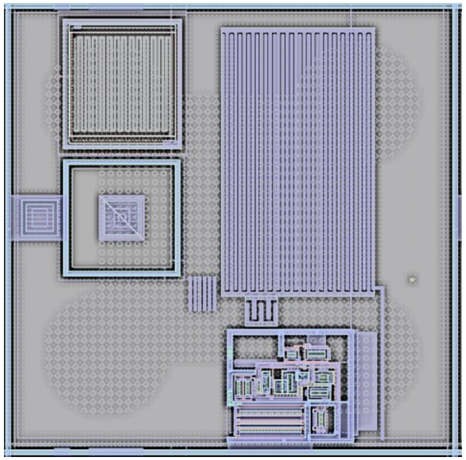
DNW structure	Capacitance [fF]	Breakdown voltage [V] (Back Bias)
Square 40 x 40	126	-100
Mickey 30 x 30	107	-70
Hexagone 30	77	-66
Hollow Hexa 30	55	-66

From TCAD simulation

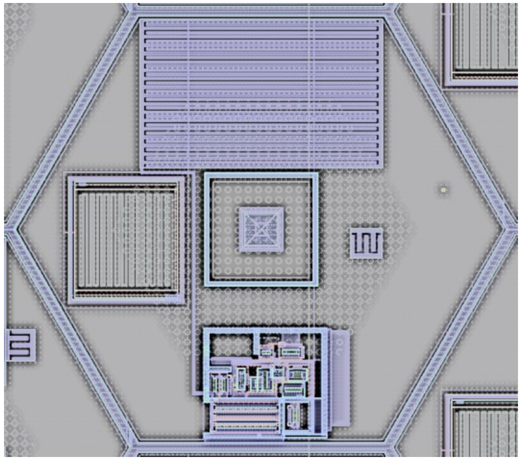
Small pixels flavors



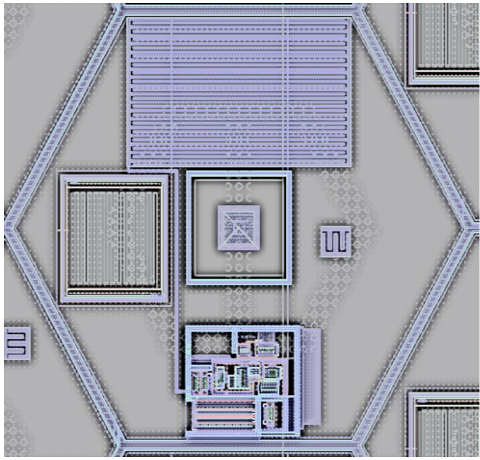
Square



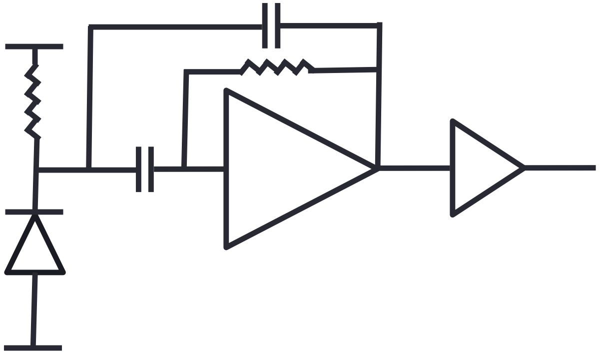
Mickey



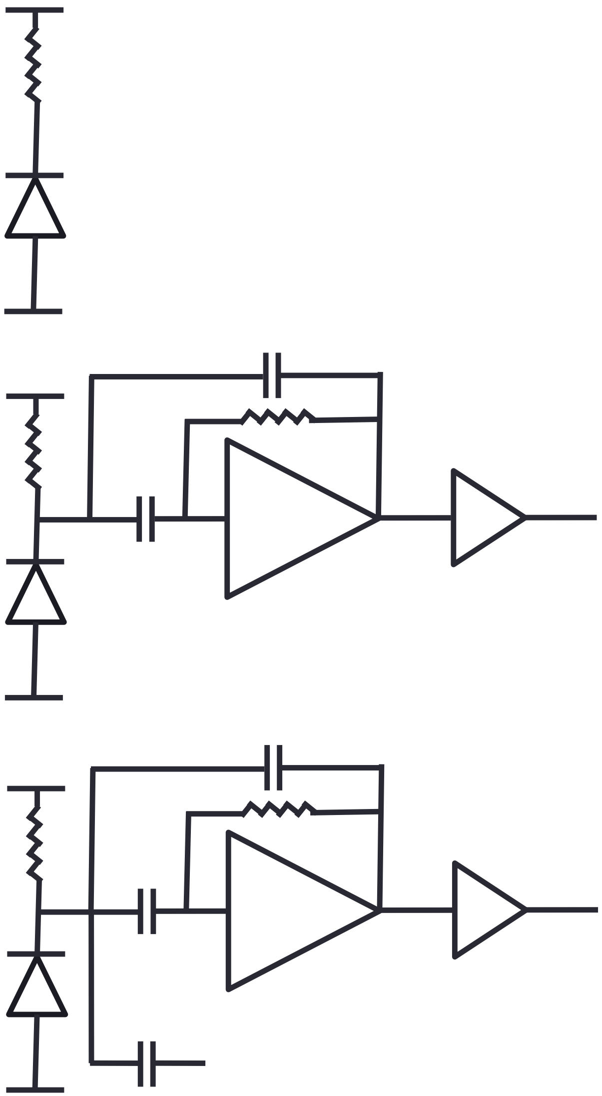
Hexa

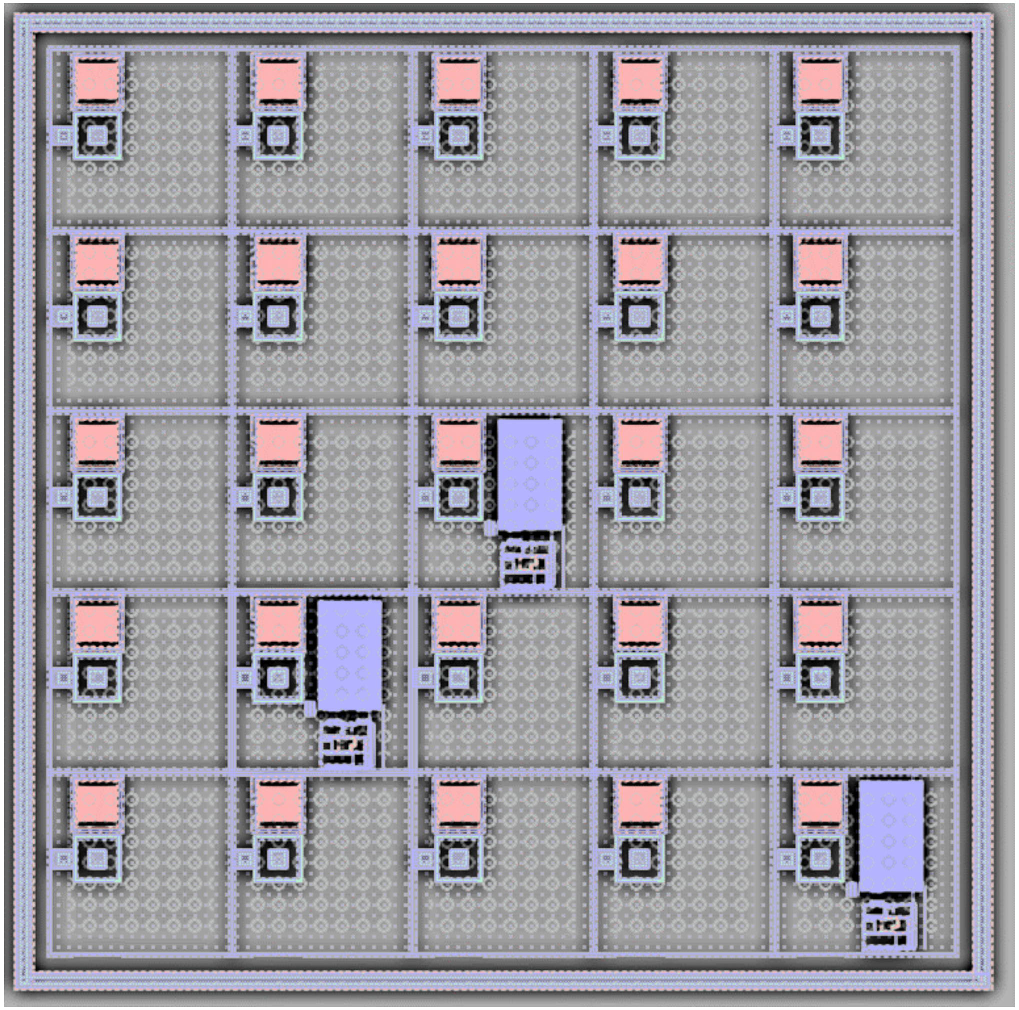


Hollow Hexa

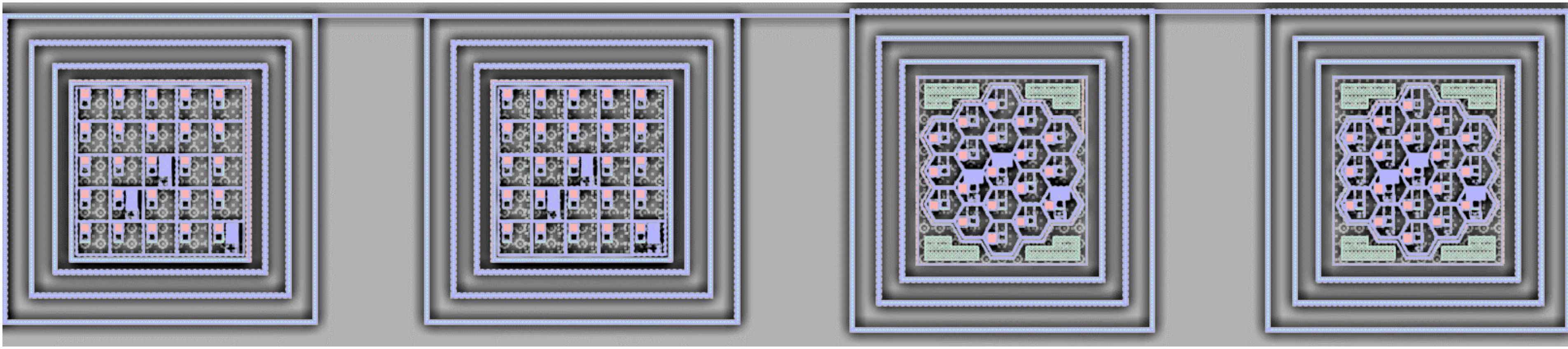


Small pixels matrix (25 "square" pixels)





Small pixels test chip



25 « Square » pixels | 25 « Mickey » pixels | 19 « Hexa » pixels | 19 « Hollow Hexa » pixels

- This test chip is a part of the LF-MONOPIX2.
- The tape-out was in may 2020.
- Expecting delivering chip : end of 2020
- Test features (with and without radiations)
  - E-TCT
  - Analog readout of the pixels
  - …

Summary

- Small sensor DMAPS (fully depleted with uniform drift field) can be designed by using LF 150nm without any process modification
- A 50µm x 50µm pixel size test chip was designed on 2020
- The test chip with several pixel flavours will be evaluate at the end of 2020. The wafer resistivity will be 2kohms.
- Leakage current, BV voltage, MIP simulation were simulated by using doping profile.
- All simulations were reviewed by the LFOUNDRY

- Can we plan to design a bigger matrix for the RD50-MPW3? Which pixel architecture, pixel readout? Specifications?