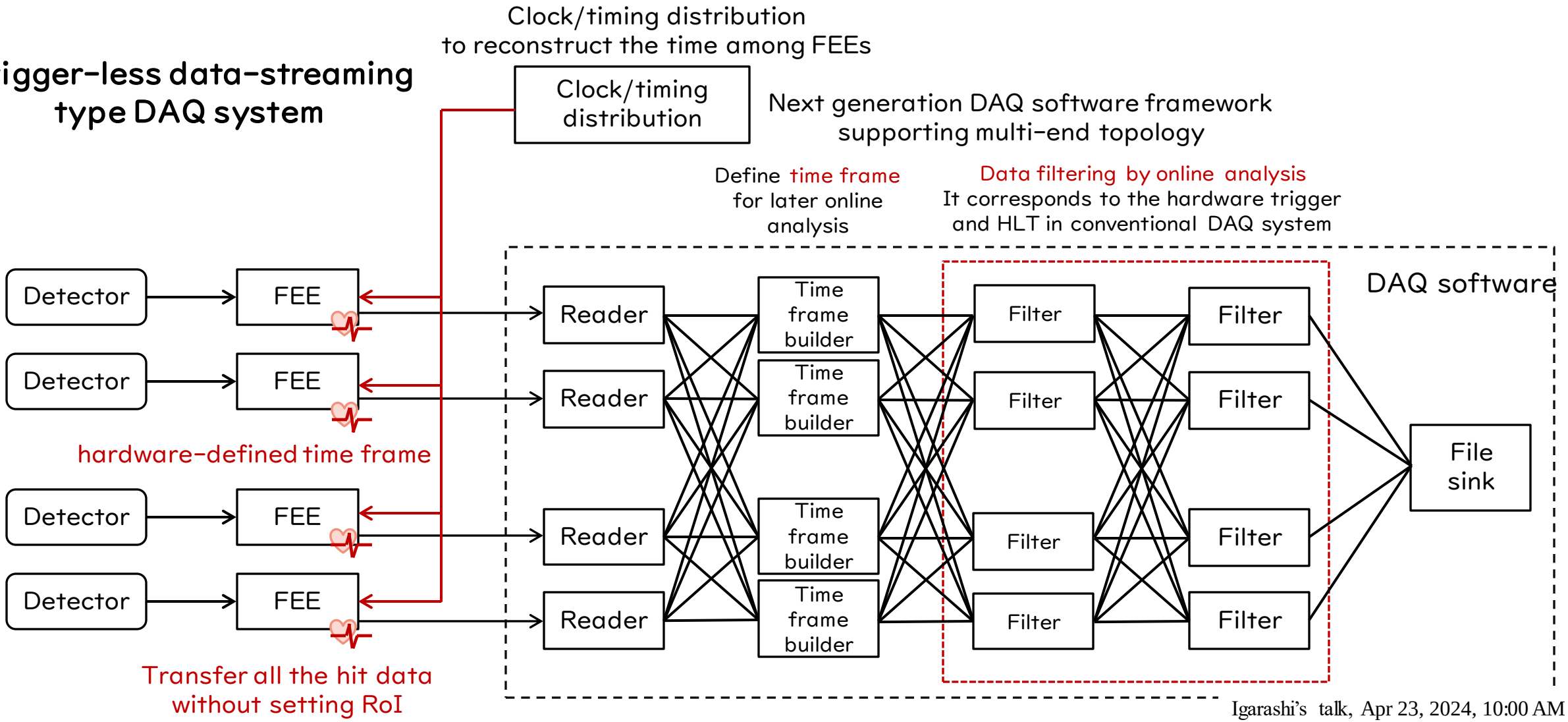
# General-purpose data streaming TDCs for nuclear and hadron experiments in Japan

R. Honda, C.S. Lin, M. Shoji, M. Ikeno[A]

KEK IPNS, RCNP[A]

# Toward trigger-less data-streaming DAQ system

**Trigger-less data-streaming type DAQ system**




Igarashi's talk, Apr 23, 2024, 10:00 AM

We aim to develop a general purpose trigger-less DAQ system.
As the first step, the general-purpose data streaming type TDCs are developed for nuclear and hadron experiments in Japan.

# Development policy

**Scalability**
- Should be scalable from single FEE node (stand-alone) to a few thousands FEE nodes.
  - Mbps – Tbps

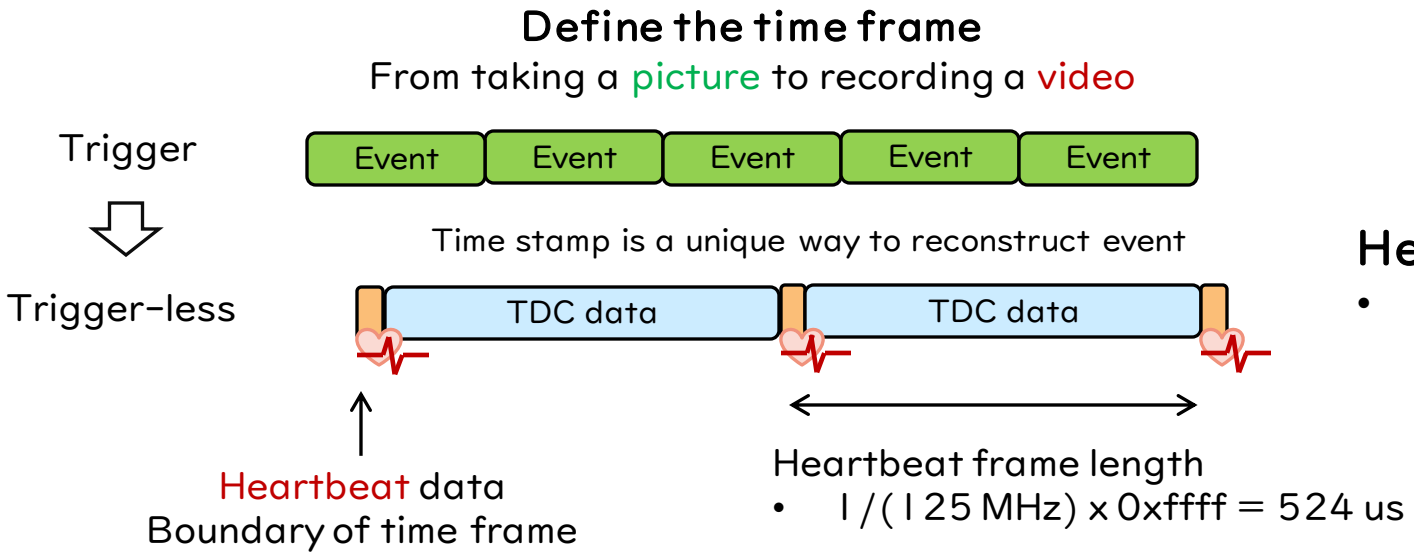
**Simple to use and maintain**
- Usable for a small experiment not having the DAQ team inside.

**Standardization**
- We would like to promote standardization of developed items under the SPADI-alliance
  - Please check Ota's talk, Apr 23, 2024, 10:20 AM
- A DAQ system for many experiments

FEE should not rely on the timing signal from the accelerator
- RF (Cyclotron)
- Bunch timing (Synchrotron)
- Kicker timing
- Flattop timing (Slow extraction of synchrotron)

} If necessary, record them by TDC and requires in the software

# Data collection relying only on timestamps




R. Honda et al., PTEP, ptab128, https://doi.org/10.1093/ptep/ptab128

## Heartbeat method

- technique to reconstruct the time without a long-length time stamp.
  - Insert a special data word periodically generated by 16-bit heartbeat counter

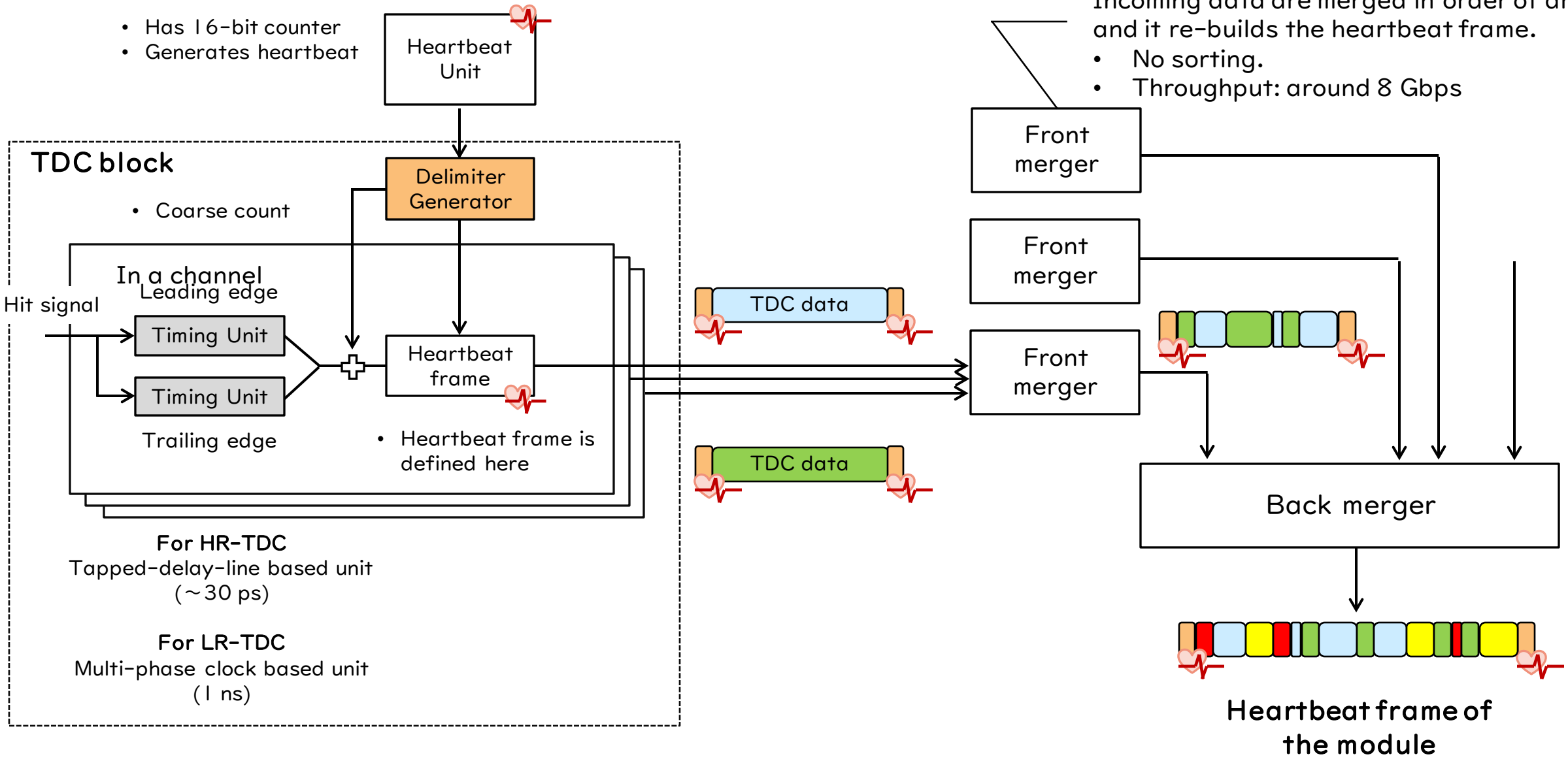
## Basic design of our Str-TDC

- TDC data: Heartbeat counter (16-bit) + fine-count (N-bit)
- Heartbeat data: Has 24-bit frame number

## How long can we measure the time?

- Time stamp length: (24+16+N) bits corresponding to 2.4 hours

# Simplified block diagram of Str-TDC



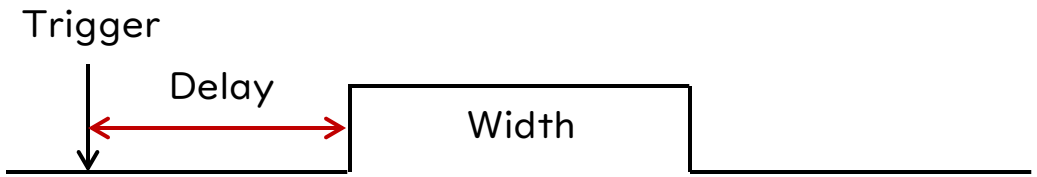
# Details of TDC block

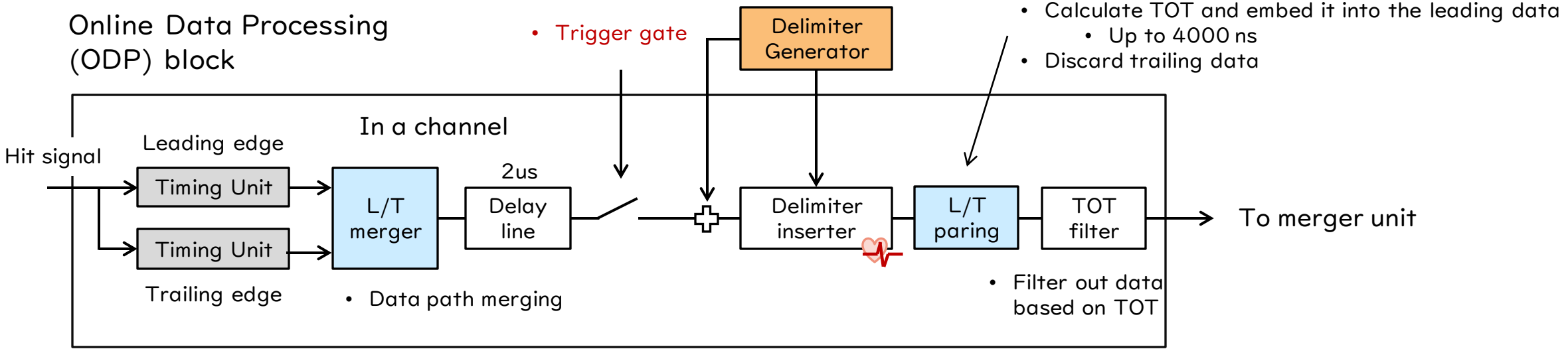
**Leading and trailing data paring**

- It reduces data size and allows us to use TOT based filter

**Trigger emulation mode**

- It makes the event gate after receiving the trigger, we expect to use it,
  - if the PC performance is not enough for the full-streaming mode
  - if the experiment has some special FEEs requiring the hardware trigger

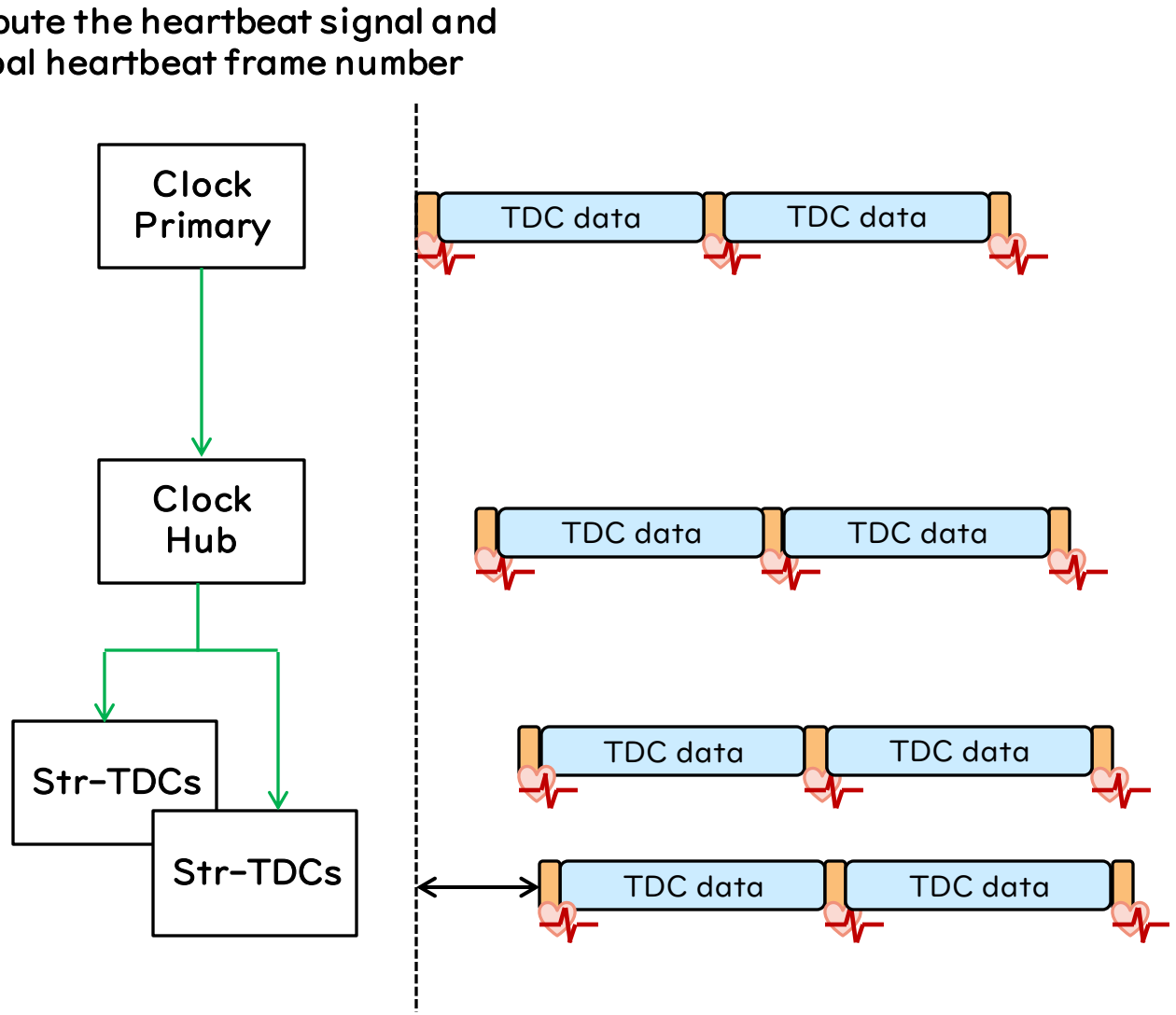


# Clock synchronization

**MIKUMARI-Link [1]**
- Frequency synchronization
  - 125 MHz in our system
  - Based on Clock-Duty-Cycle-Modulation [2]
  - Implemented using IOSERDESE2
- Link layer protocol
  - Define the point-to-point communication rule

**LACCP (Local Area Common Clock Protocol)**
- Clock synchronization
- Provide the time offset to the heartbeat unit in each module by measuring the round trip time with 78 ps precision.
- No software support is necessary. It automatically adjust the clock by just connecting a fiber cable.





[1]. R. Honda, IEEE TNS, Vol. 70 (6), 1102 (2023).
[2]. D. Calvet, IEEE TNS, Vol. 67 (8), 1912 (2020).

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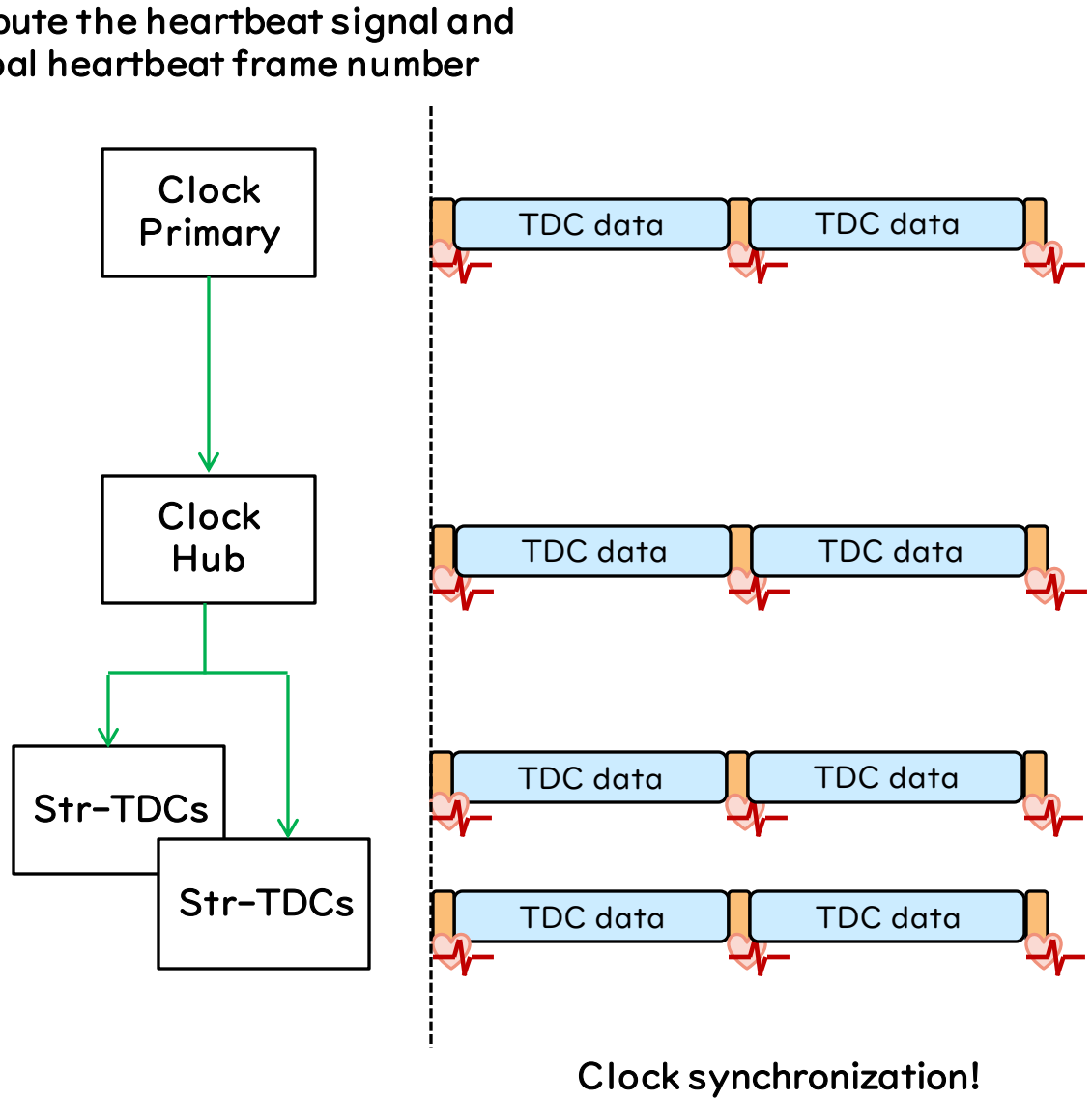
- Provide the time offset to the heartbeat unit in each module by measuring the round trip time with 78 ps precision.
- No software support is necessary. It automatically adjust the clock by just connecting a fiber cable.

- LACCP is independent from the DAQ function
  - The local clock domain is defined by the primary, and the DAQ (Str-TDC) just refers it.
  - If the DAQ is stopped, it continues to run.
  - No special meaning for 0 o'clock

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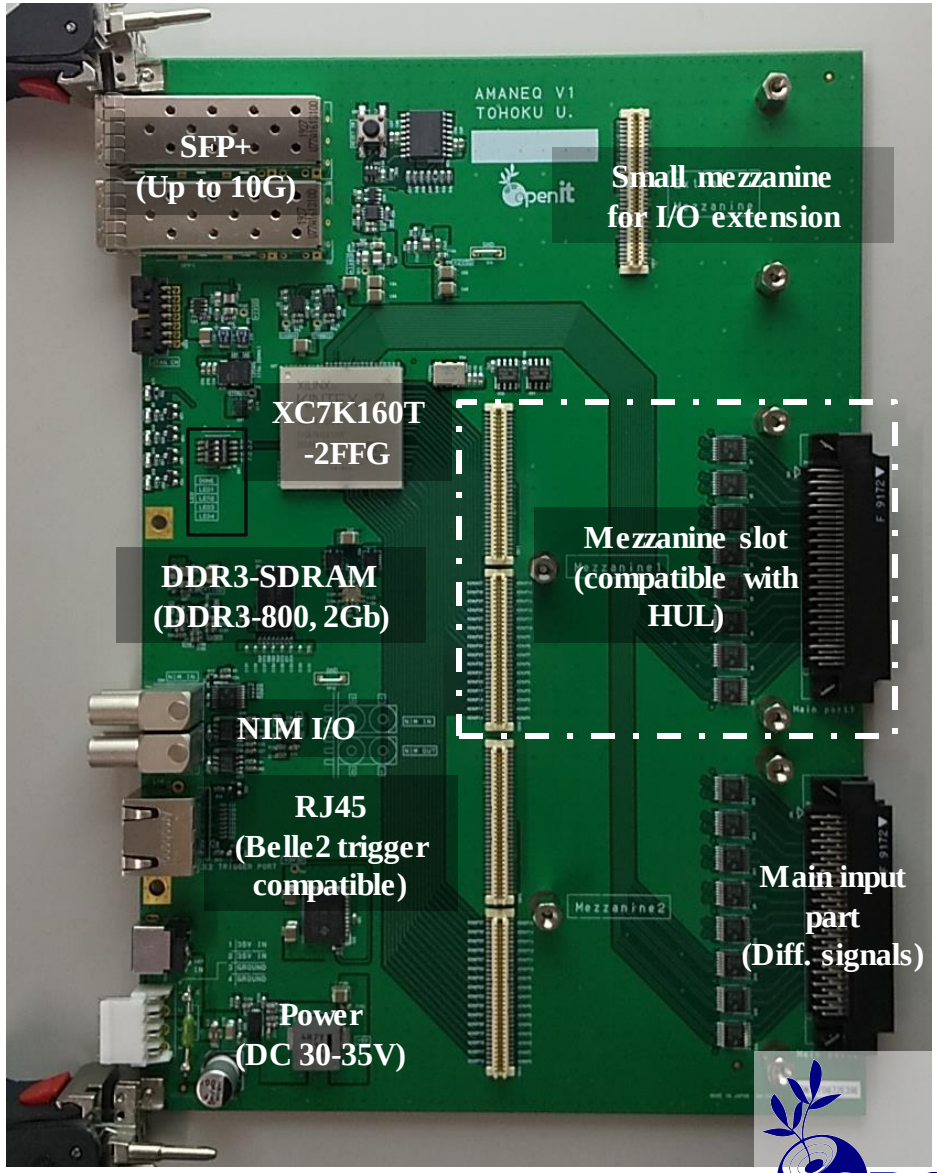
# Implementation to electronics

# Hardware



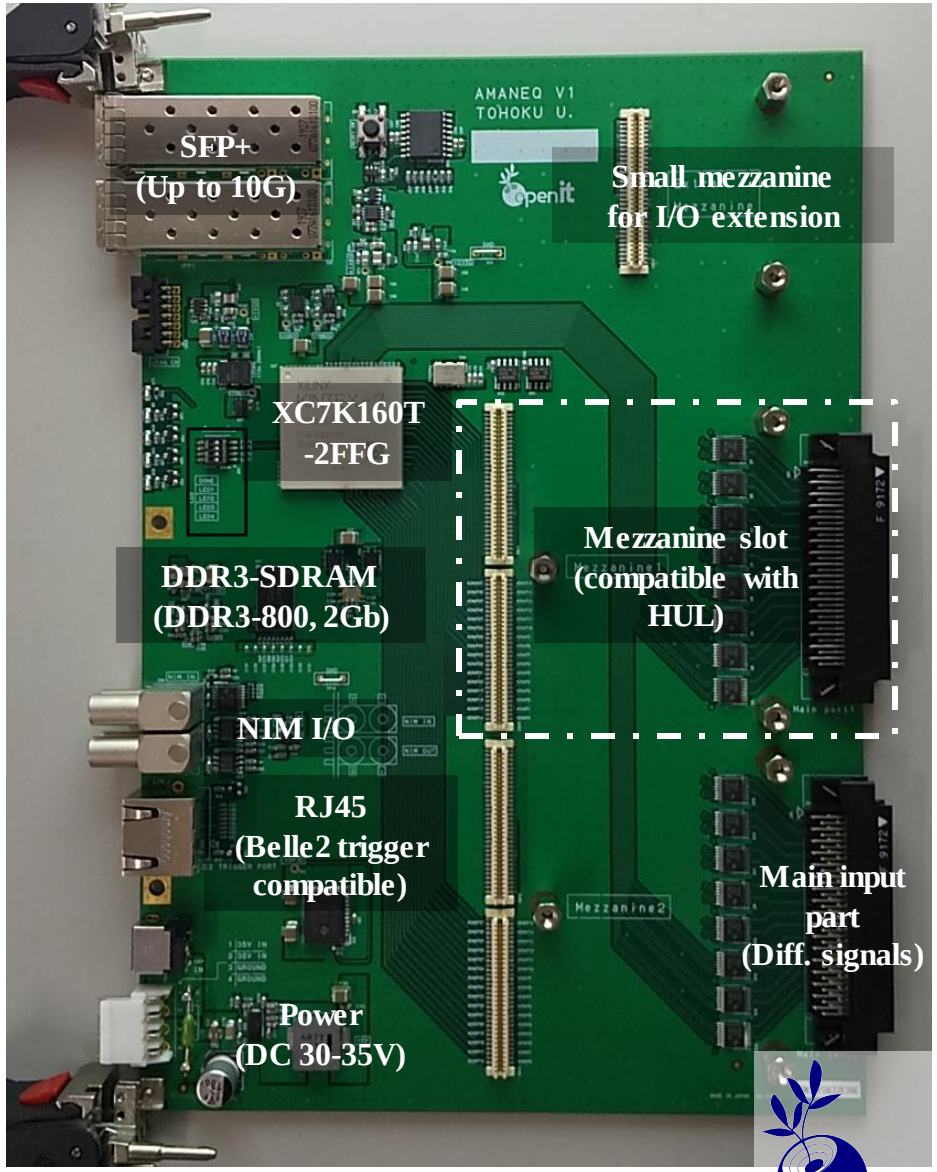

**A main electronics for network oriented trigger-less data acquisition system (AMANEQ)**

- Kintex7 with speed grade -2
  - Transceiver bandwidth up to 10Gbps
  - Can implement SiTCP-XG [3] (10Gbps TCP/IP)
- Has two mezzanine slots
- Has a jitter cleaner (CDCE62002)
- DDR3-SDRAM as a de-randomizer
  - DDR3-1333 with 16-bit bus width.
  - 2 Gb
- Powered by the external power supply with DC 30-35V

General purpose logic module
It plays several roles,
Clock Primary, Clock Hub, **Str-HR-TDC**, and Str-LR-TDC.

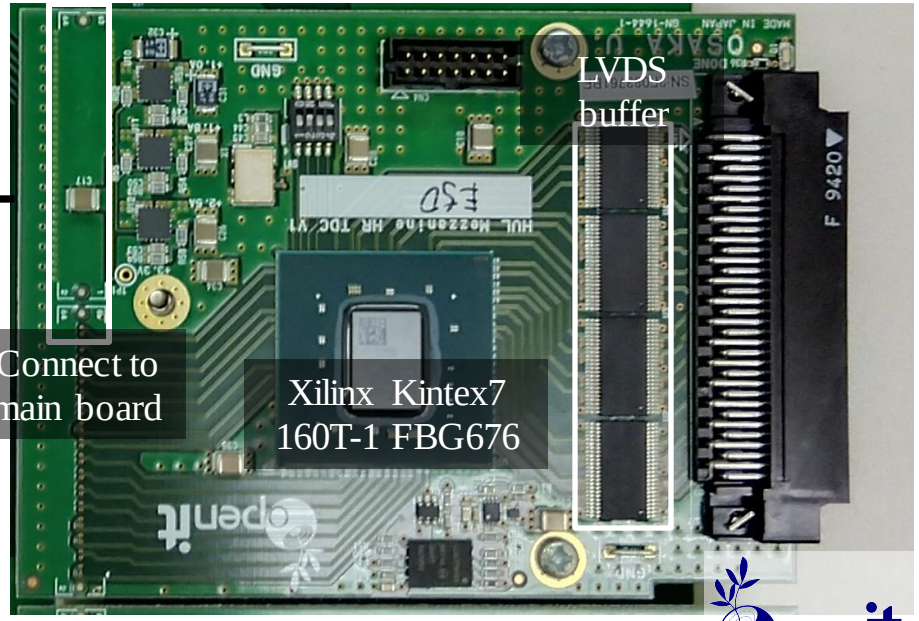
About SiTCP-XG, see
[3]. https://github.com/BeeBeansTechnologies/SiTCPXG_Netlist_for_Kintex7

# Hardware for streaming high-resolution TDC




Attach

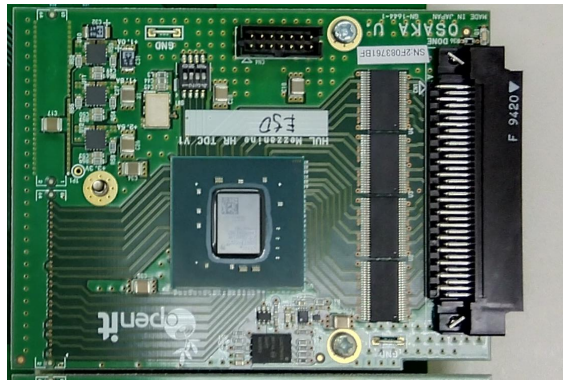
HUL/AMANEQ mezzanine HR-TDC

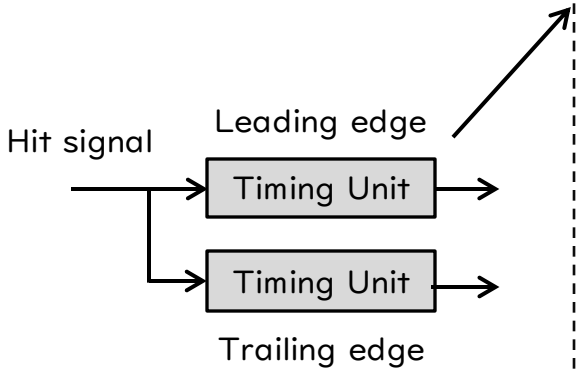


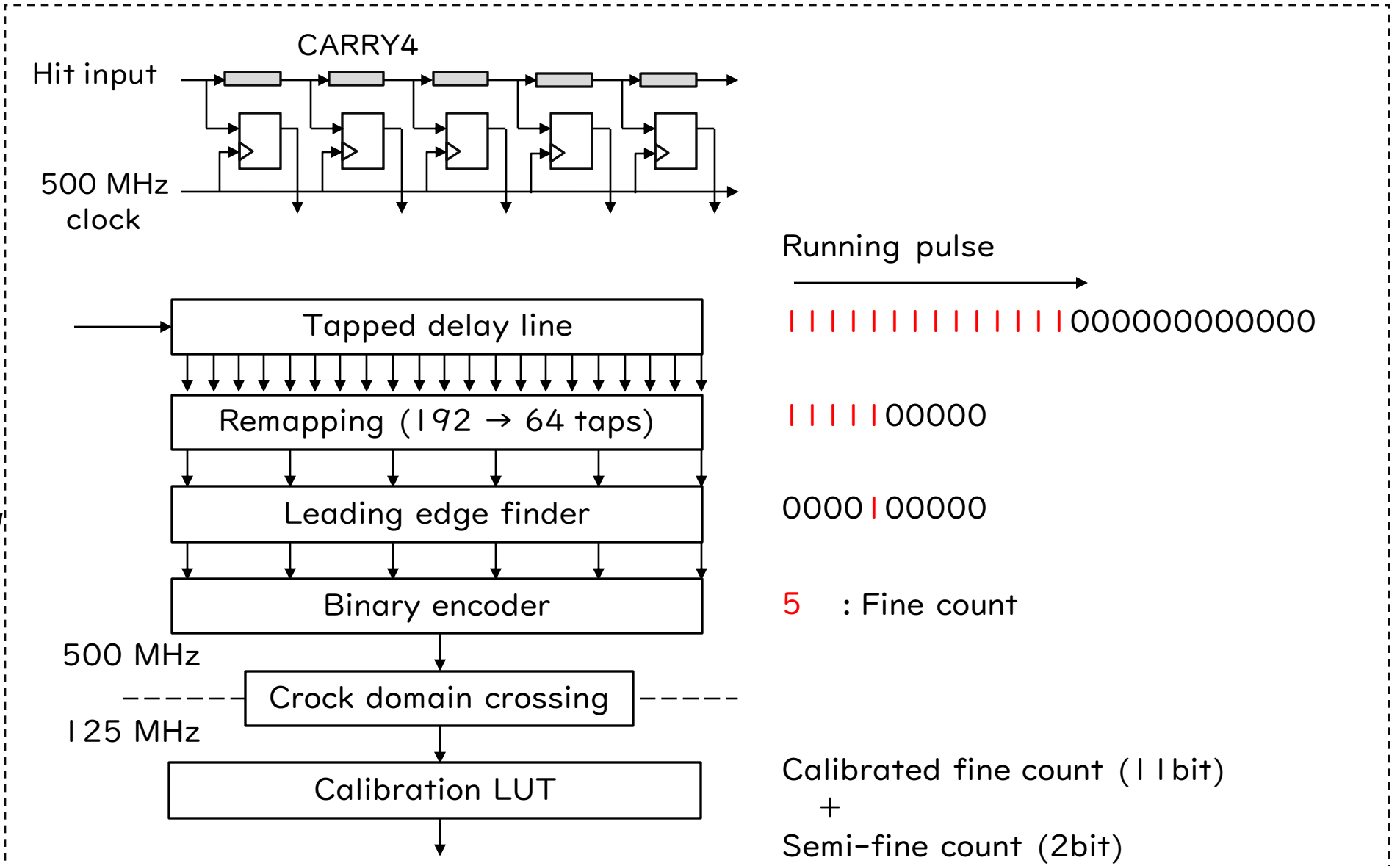

32 ch tapped-delay-line (TDL) based HR-TDC

- Input IO std.: LVDS
- TDL consists of a CARRY4 primitive chain.
  - Target resolution: 20-30 ps in σ
- Both leading/trailing edges

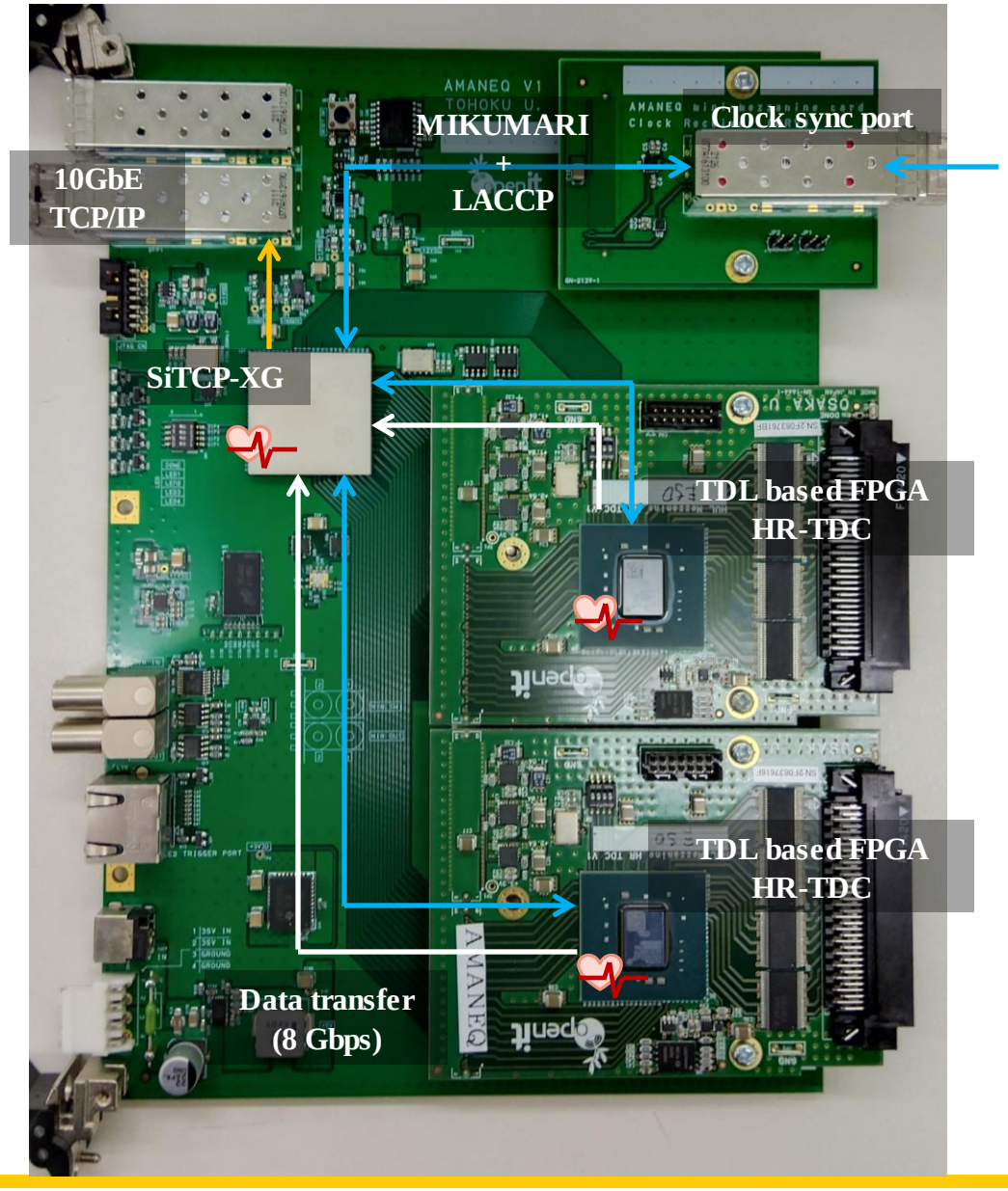
# Hardware for streaming high-resolution TDC





# Streaming HR-TDC on AMANEQ




## AMANEQ Str-HRTDC

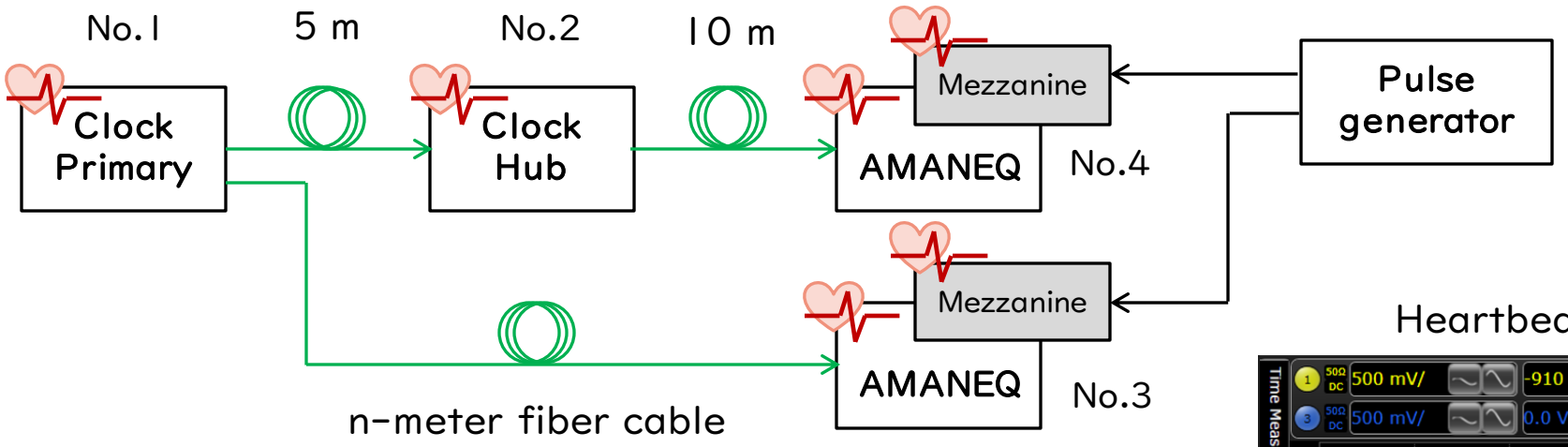
- Str-TDC blocks are divided to two FPGAs
  - TDC block and front merger are into FPGA on the mezzanine cards
  - Back merger is into FPGA on AMANQ.
- Heartbeat unit is running in each FPGA
  - Synchronized by the upstream FPGA

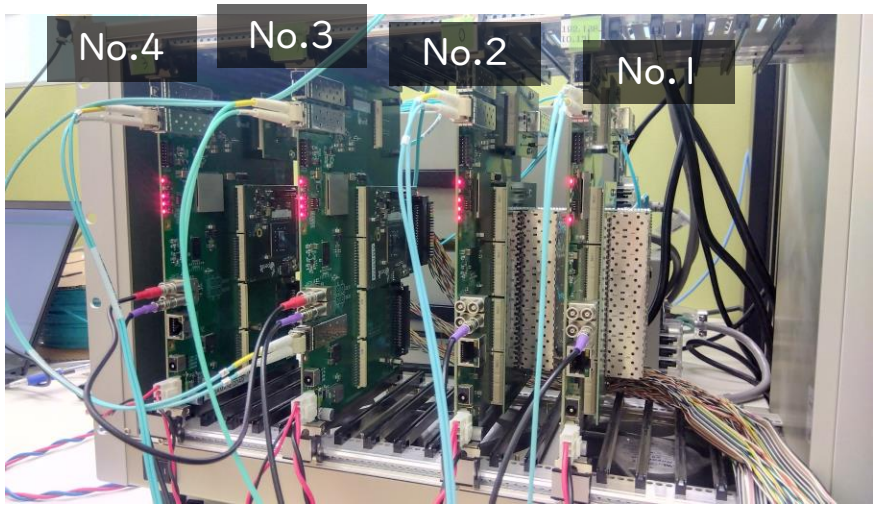
## Specification

- Input : 64 ch (32+32)
- Timing resolution: Discussed in later page
- Data link: 10GbE
  - TCP/IP provided by SiTCP-XG
- Internal data bandwidth: 8Gbps
  - Max capable input rate is 2 MHz/ch in average

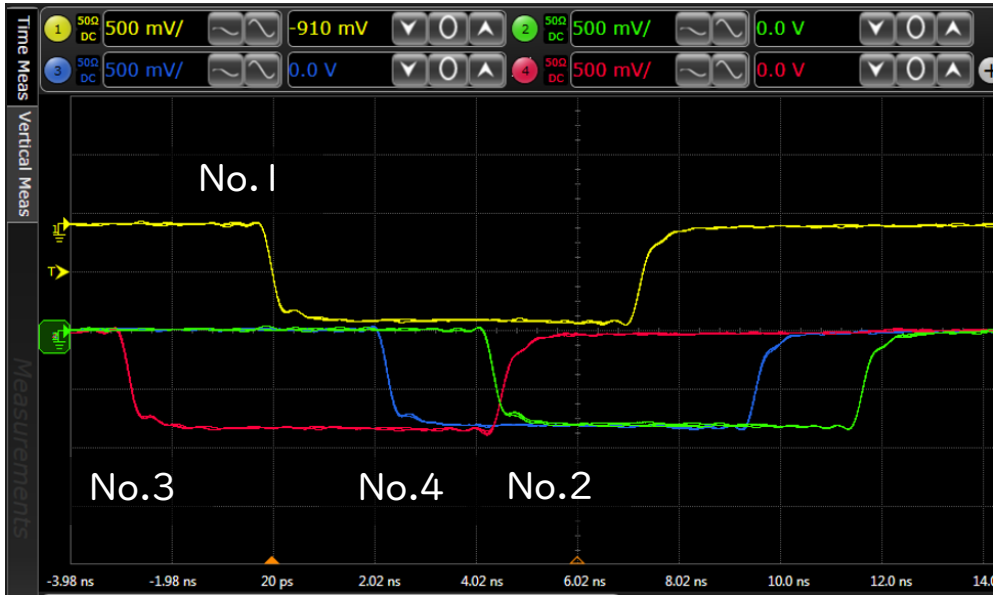
# Performance evaluation

# Clock synchronization test



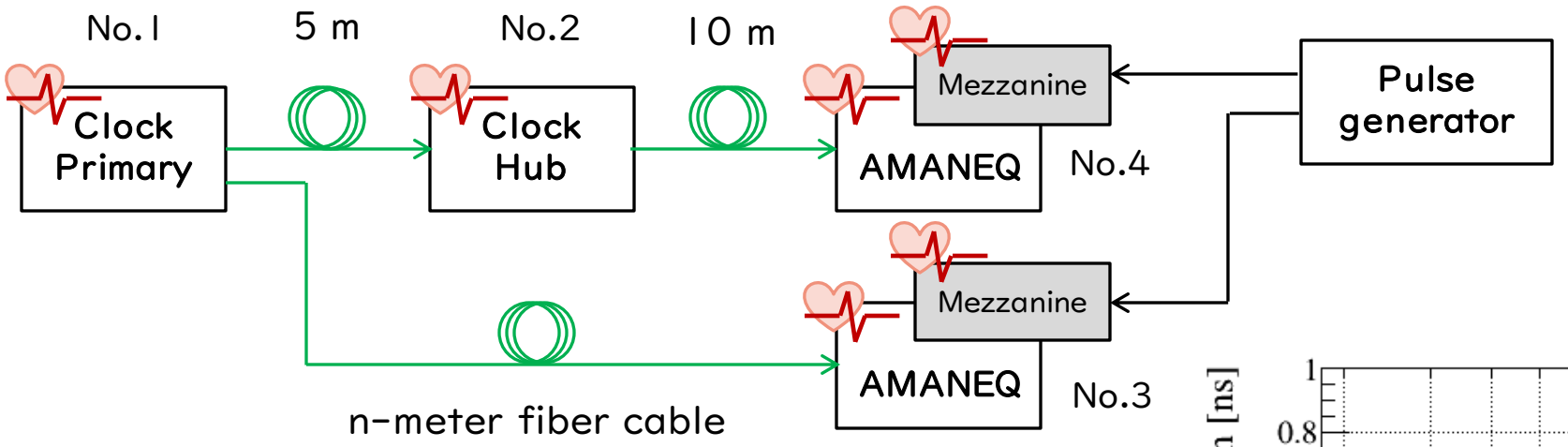




Heartbeat signals from AMANEQs

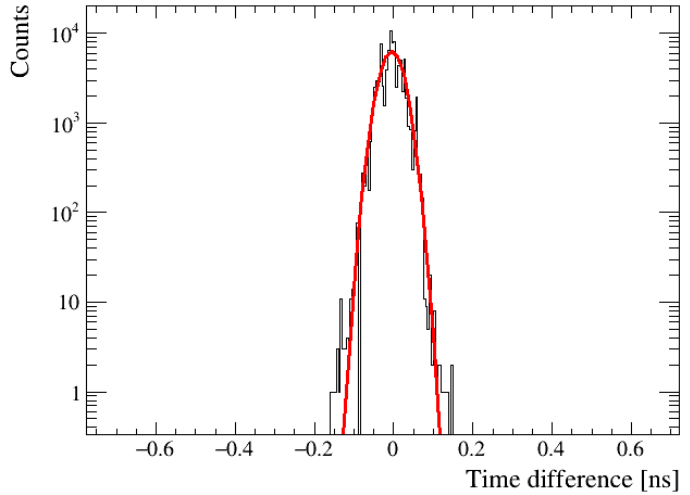


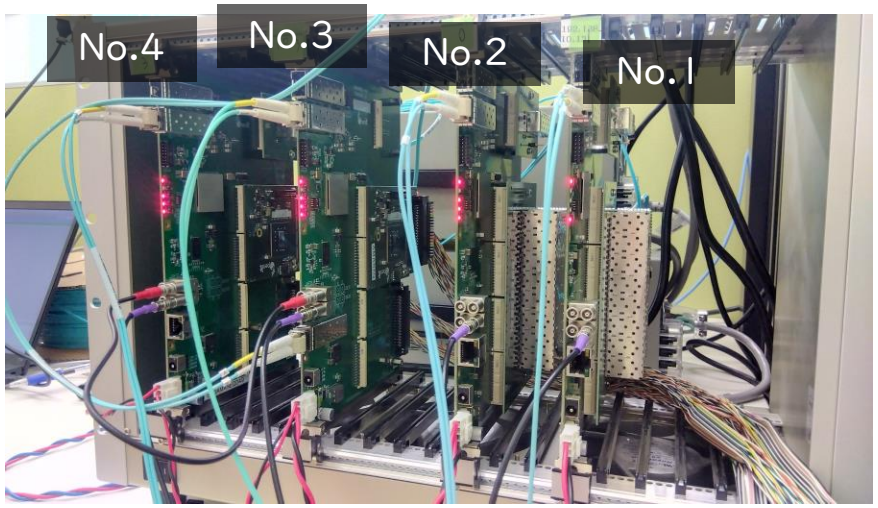

```
#D:   -- My offset --
Heartbeat count offset: 47(376 ns)
Local fine offset:      -2200(-2148.44 ps)
LACCP fine offset:      2176(2125 ps)
```

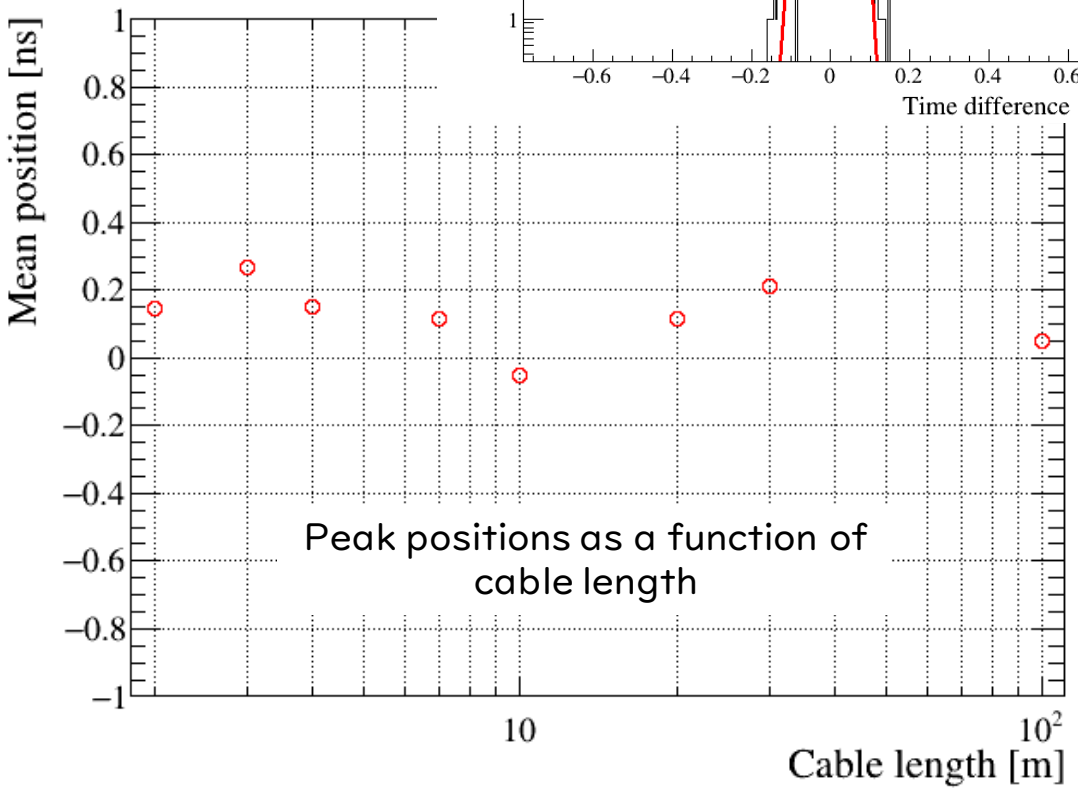
# Clock synchronization test




Time difference between two TDCs

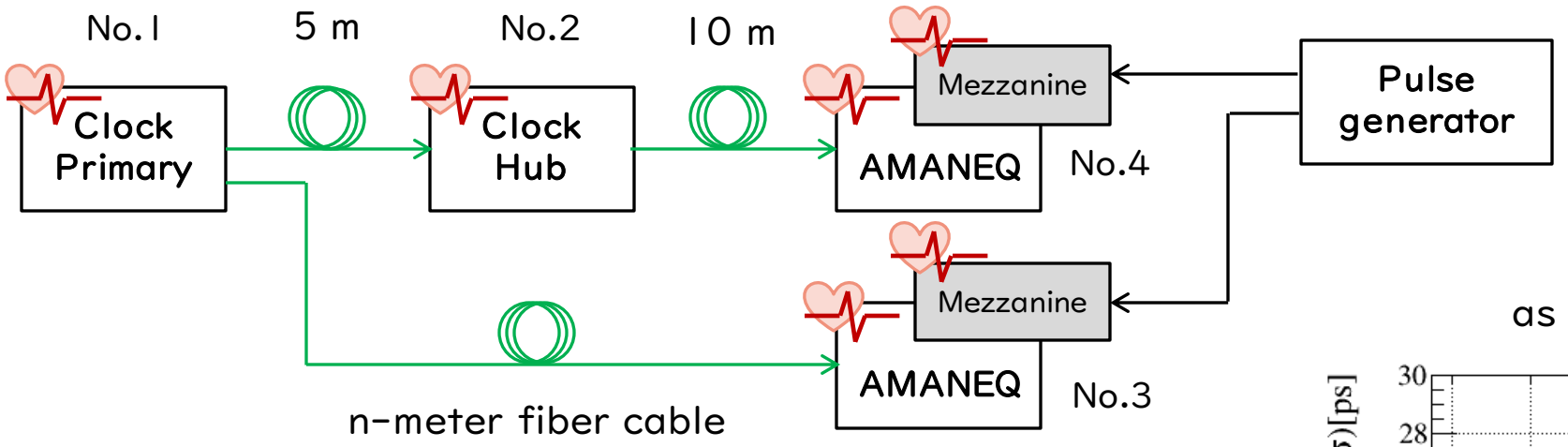


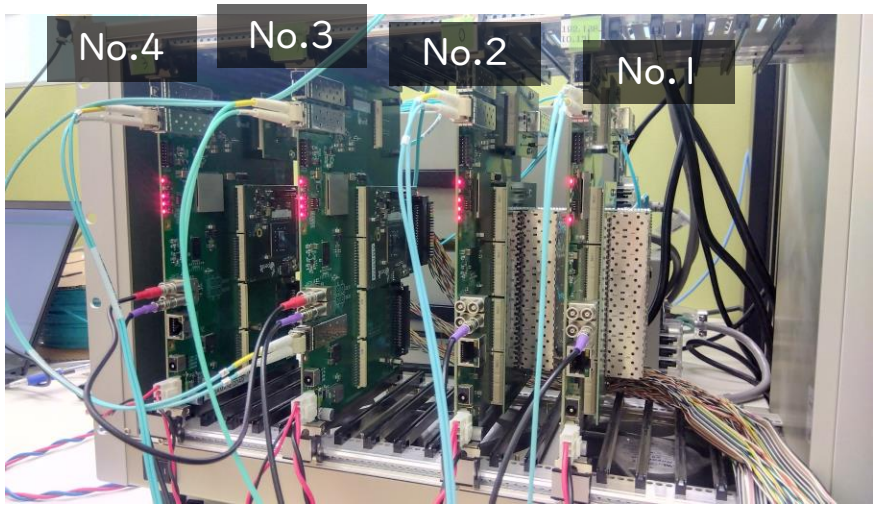



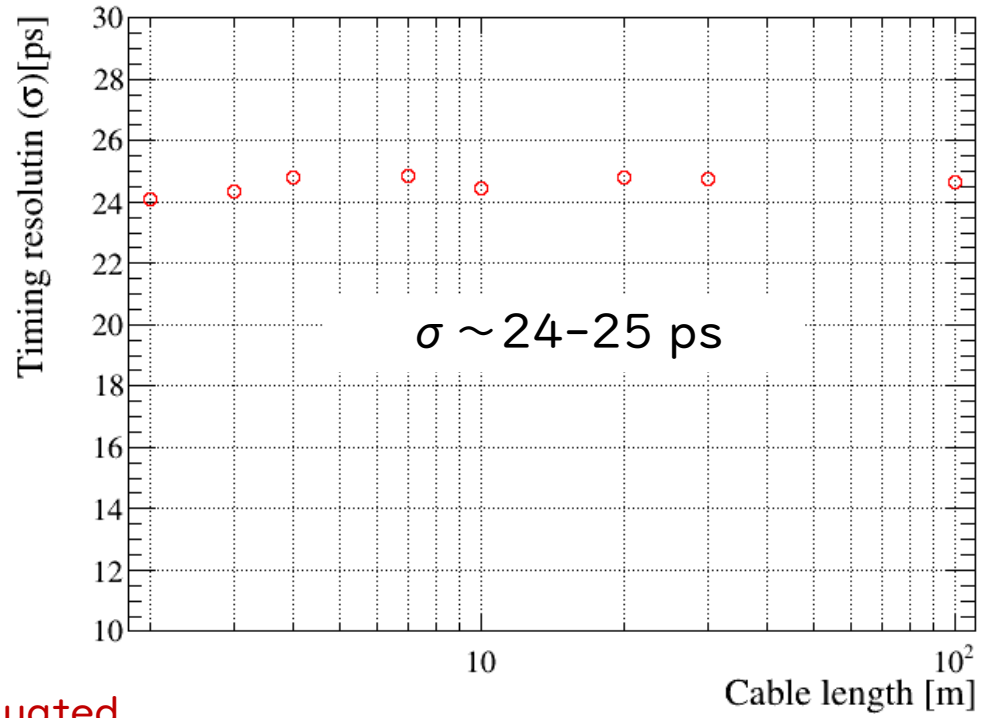

TDCs with clock synchronization protocol with around 200 ps accuracy is developed!

# Timing resolution




Timing resolutions
as a function of cable length



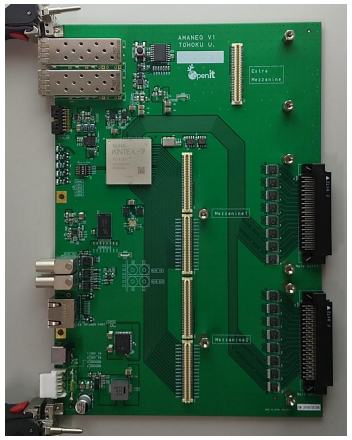

The timing resolution was simultaneously evaluated,
and there is no cable length dependence of the timing resolution.

# Future prospects

By combining the MIKUMARI, LACCP, and Heartbeat method, we have developed

- Clock-Primary
- Clock-Hub
- Streaming HR-TDC
- Streaming LR-TDC

} **Realized on AMANEQ**



Implemented into CIRASAME module

CIRASAME

128 ch SiPM readout module with CITIROC*

*Developed by OMEGA/Weeroc in France

**We plan to implement them in various front-end electronics, which will be developed under the SPADI-alliance.**

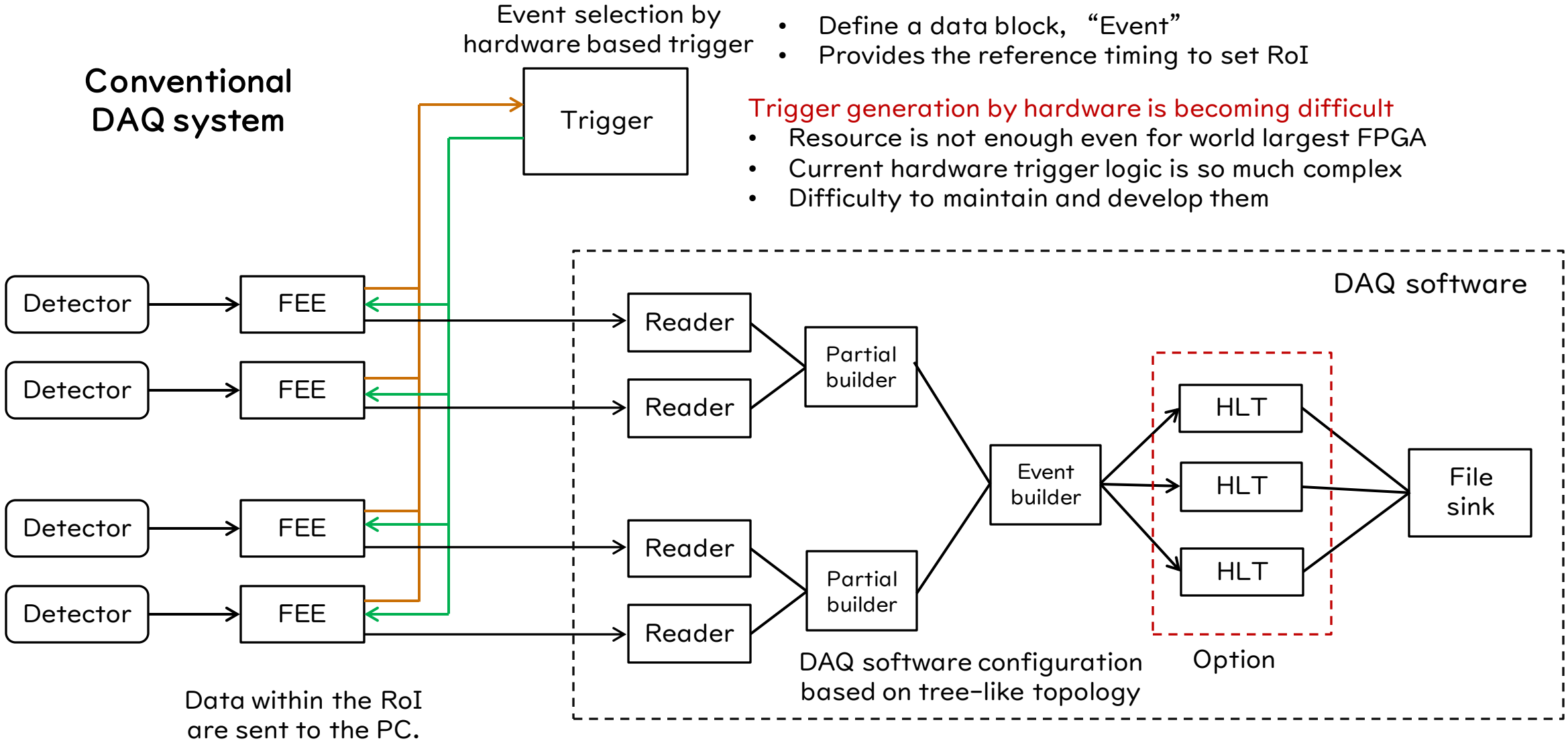
SPADI Alliance

# Summary

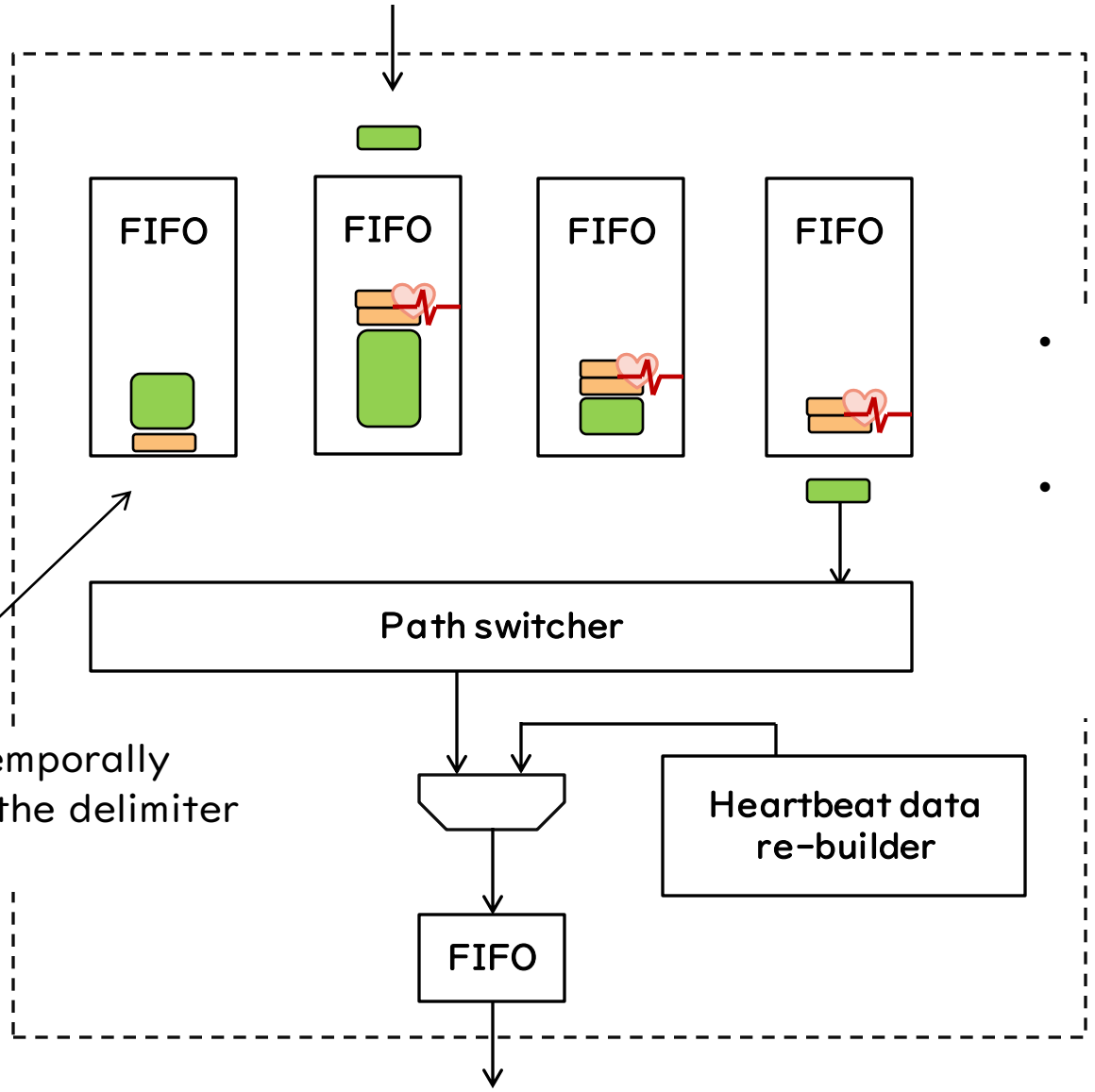
- We developed the general purpose data-streaming type TDC (Str-TDC) for the development of the trigger-less DAQ system for the nuclear and hadron experiments in Japan.
- Key technologies of this work
  - Heartbeat method provides a time frame and realizes the continuous timing measurement without a long-length local counter.
    - 16-bit heartbeat counter + 24-bit frame number => 2.4 hours length
  - MIKUMARI link technology achieves the clock frequency synchronization and the timing pulse distribution with the fixed latency.
    - It is based on Clock-Duty-Cycle-Modulation
  - Local Area Common Clock Protocol (LACCP) is a upper layer protocol of the MIKUMARI link.
    - Clock synchronization by the round trip time measurement with 78 ps precision.

- Clock-Primary, Cock-Hub, Str-HR-TDC, and Str-LR-TDC have been developed and implemented into AMANEQ.
- We tested the Str-HR-TDC to evaluate the synchronization accuracy of the TDC modules and the timing resolution.
  - Each HR-TDC mezzanine card is synchronized with around 200-ps accuracy. No cable length dependence.
  - Obtained timing resolution does not have a cable length dependency, and it is around 24-25 ps in sigma.

# Toward trigger-less data-streaming DAQ system



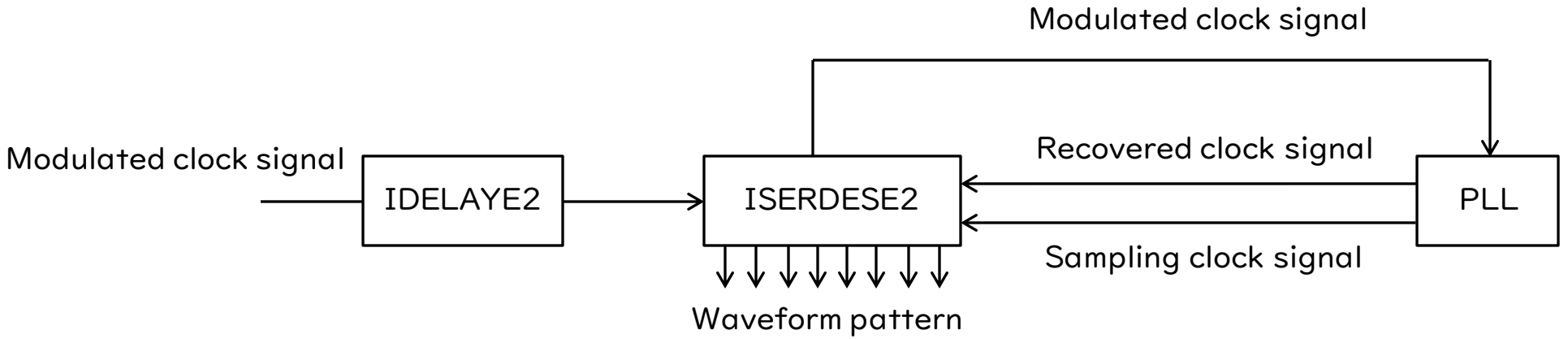
# Merger unit




Data readout is temporally stopped because the delimiter is found.

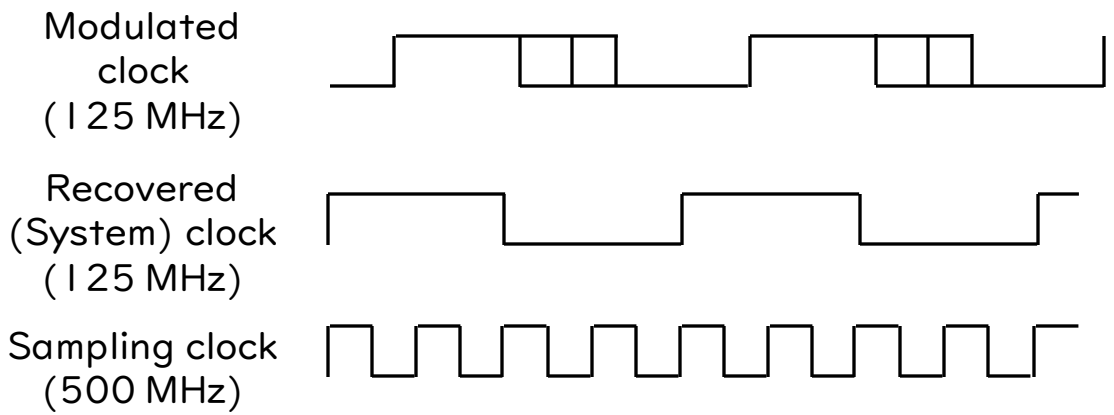
- Path switcher selects the FIFO to be read by checking flags from FIFOs
  - Younger channel is read first
- Stop reading temporally when the heartbeat delimiter data is found.
  - If delimiter data are found in all the channels, it re-builds and inserts the delimiter data.

# LACCP method

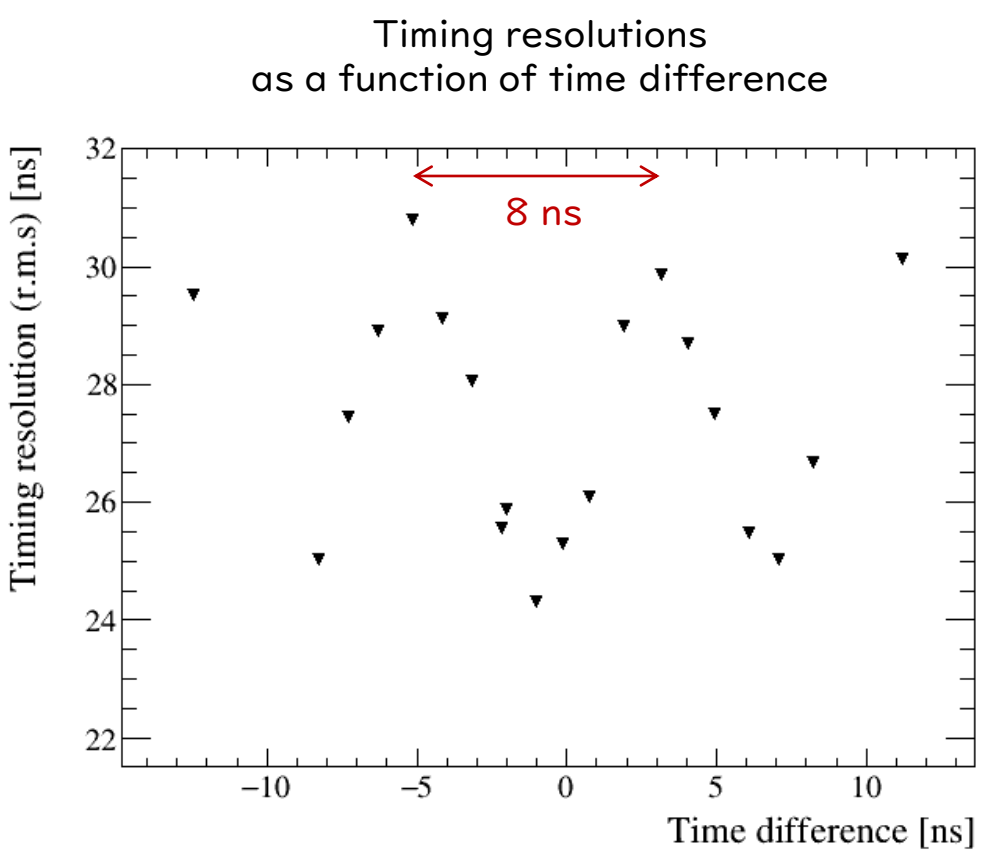


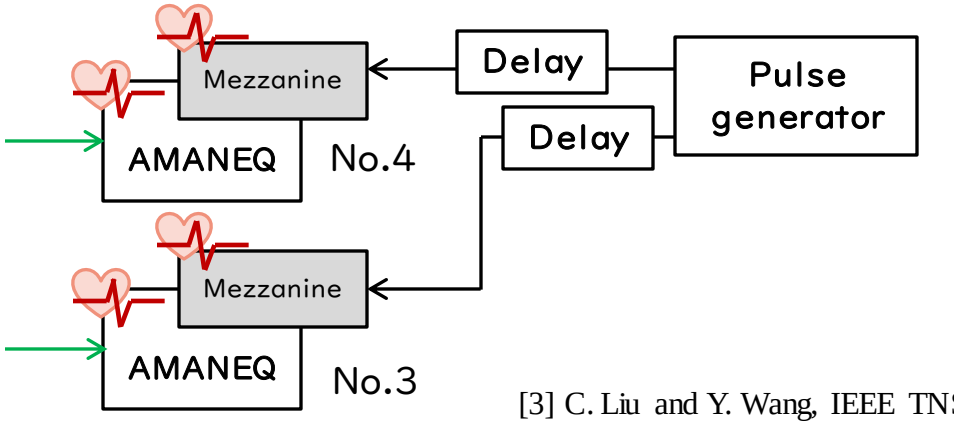

Origin of LACCP fine offset ↔

Possible to calculate from IDELAY tap value and the ISERDES bitslip number



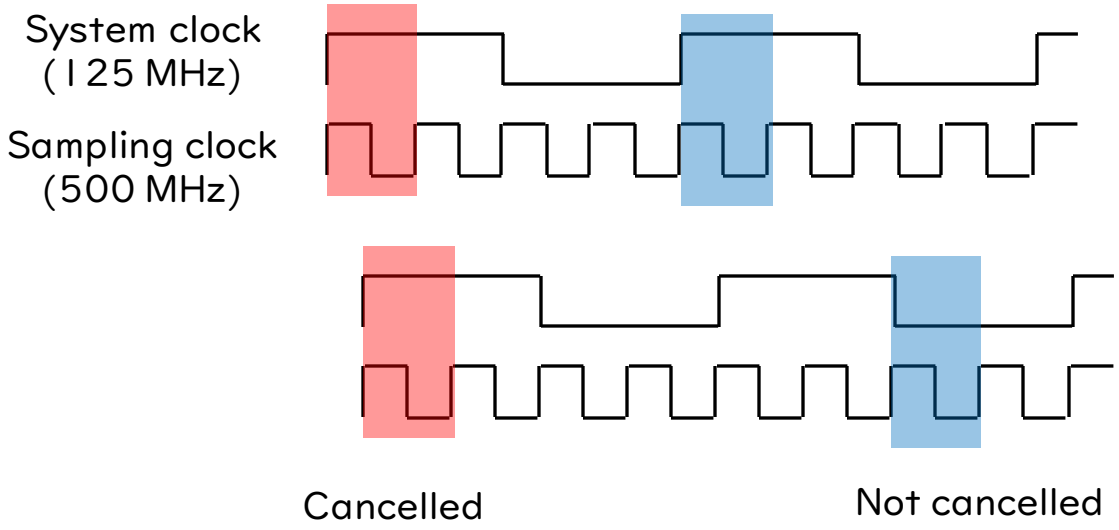
# Timing resolution




[3] C. Liu and Y. Wang, IEEE TNS, vol. 62, no. 3, 773 (2015)

This effect is probably originated from the ground noise comes from the system clock signal as discussed in [4], since our system clock frequency is 125 MHz (8ns).



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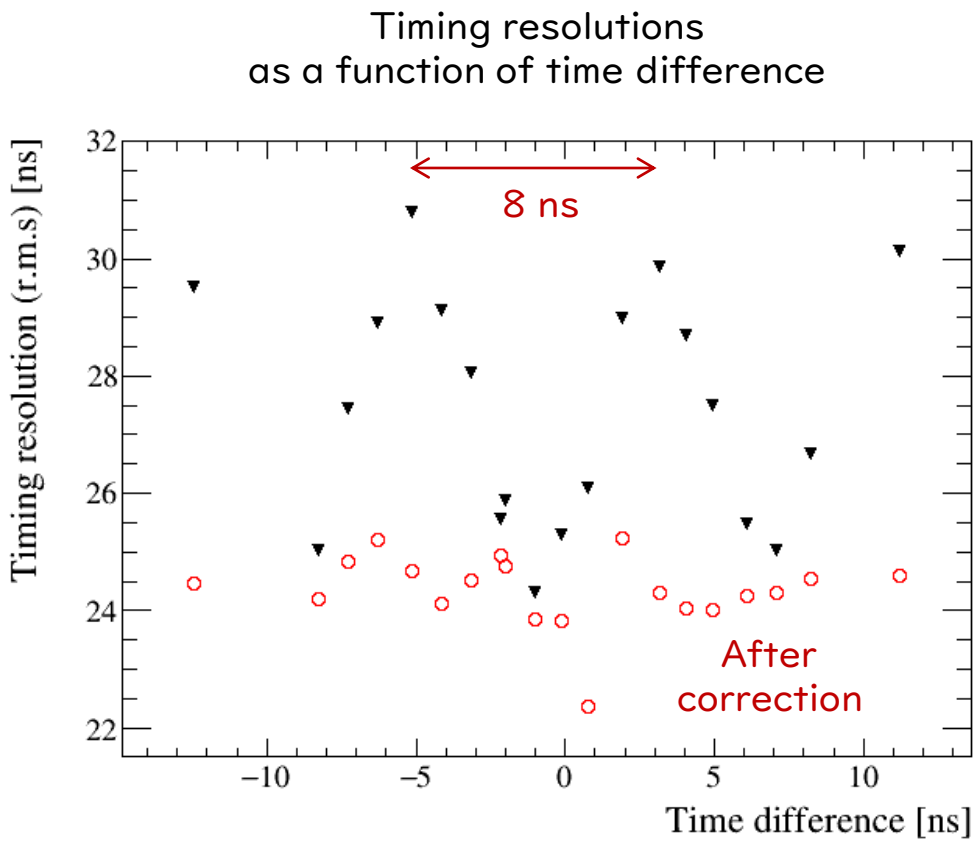


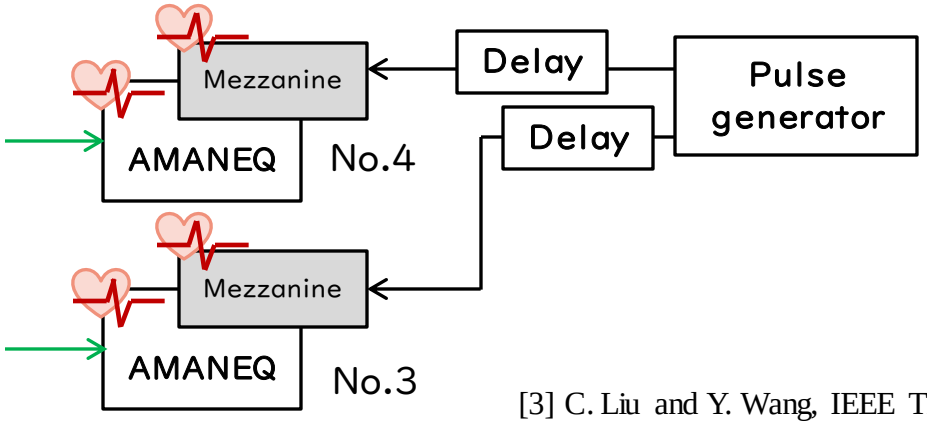


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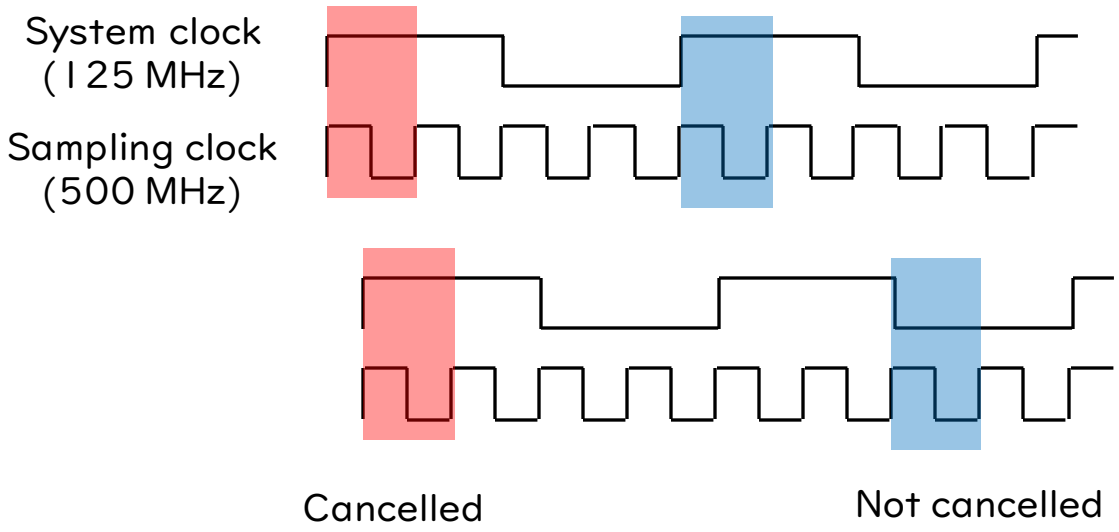
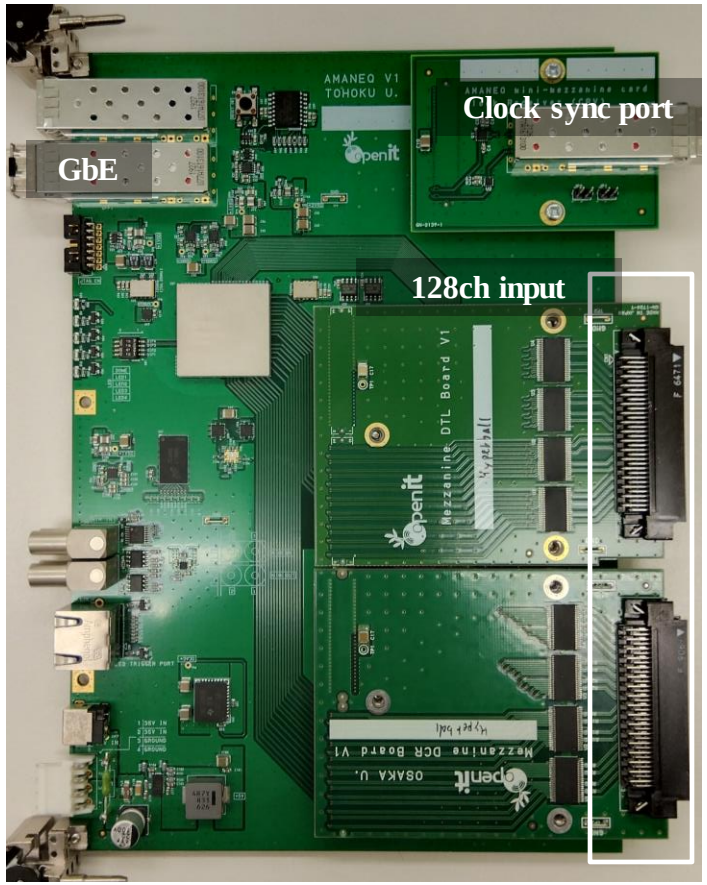
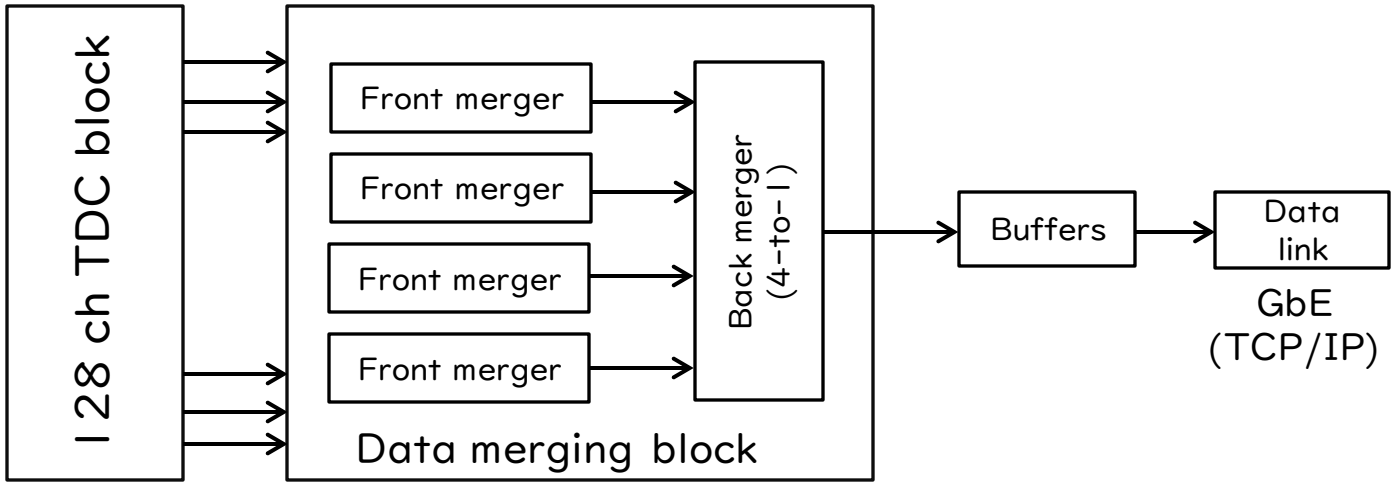


# Streaming LR-TDC on AMANEQ



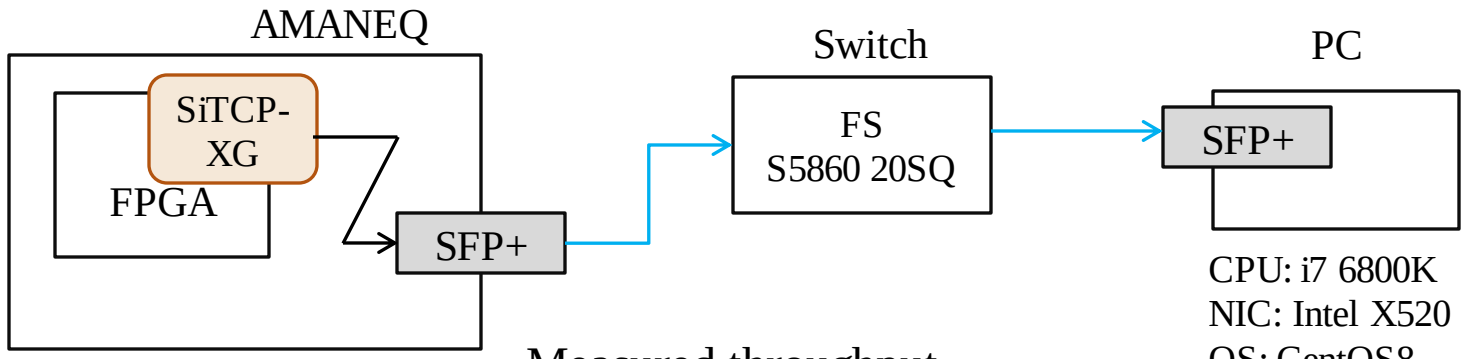

**Str-LR (low-resolution)-TDC**
1ns precision TDC

- All the blocks are implemented into the FPGA on AMANEQ.
- Data link: GbE (TCP/IP)



# Data transfer speed via SiTCP-XG

Test setup

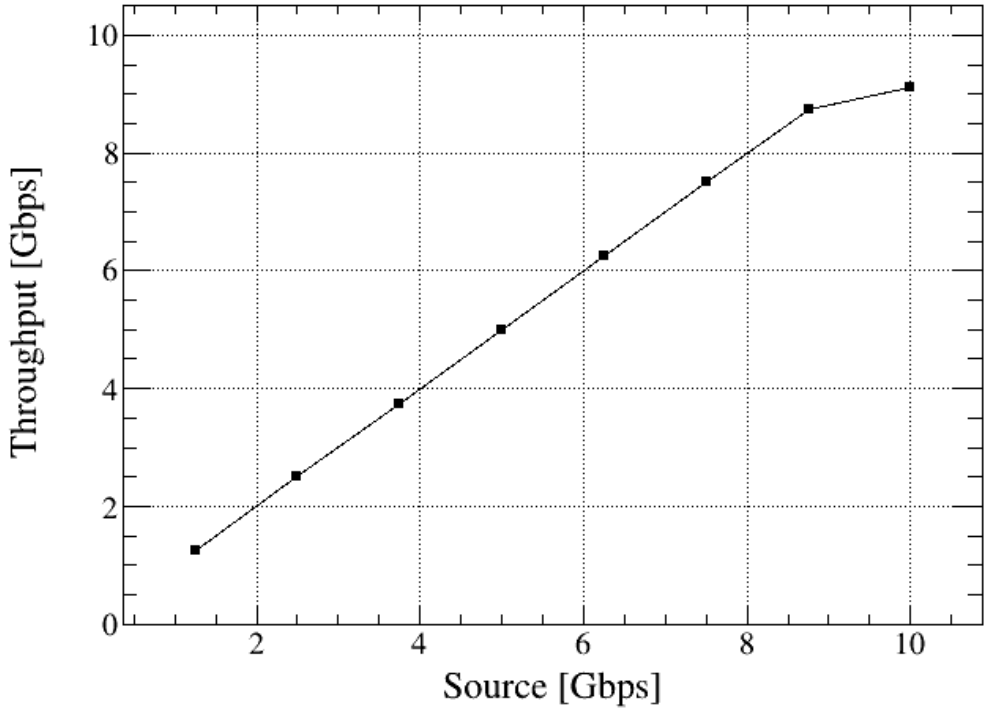



Read data using C++ software.

CPU: i7 6800K
NIC: Intel X520
OS: CentOS8

Tested by H. Sendai (KEK E-sys)

Measured throughput




Obtained throughput: 9.12 Gbps
~96% of TCP payload limit (MTU 1500)

About SiTCP-XG, see
https://github.com/BeeBeansTechnologies/SiTCPXG_Netlist_for_Kintex7