An FPGA-Based Emulator and Test System for the 3D-SOI chip CPV-4

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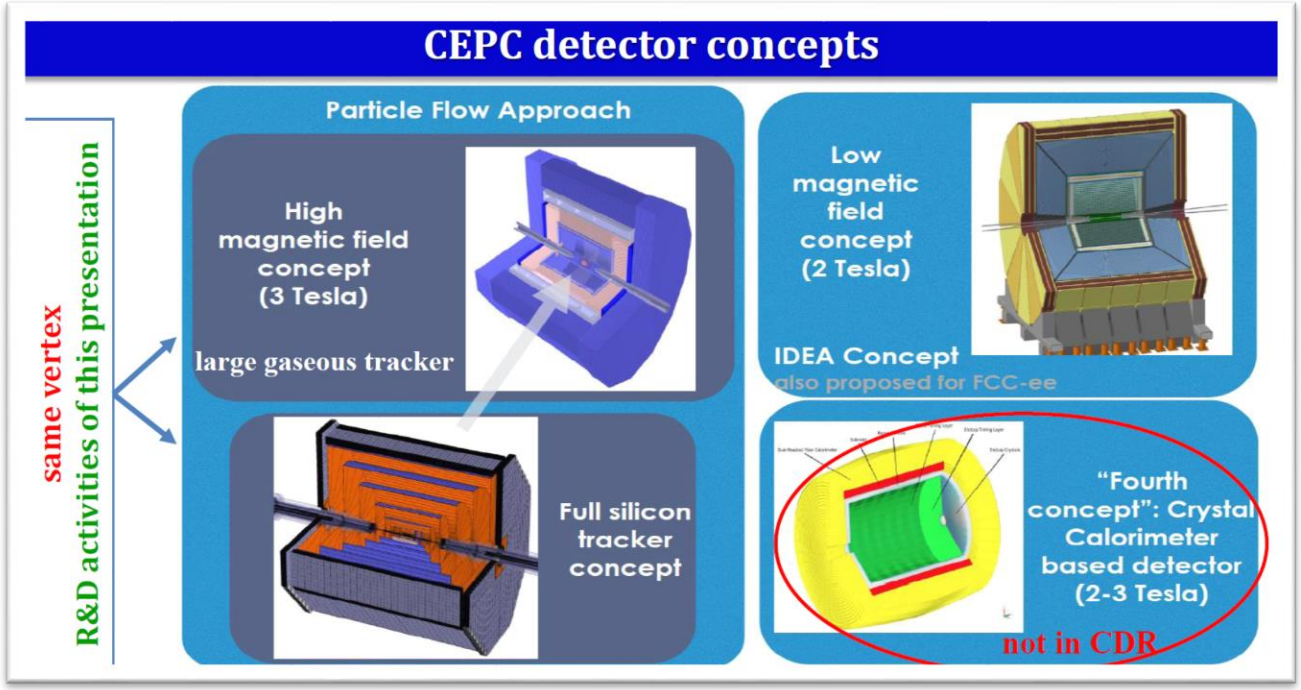
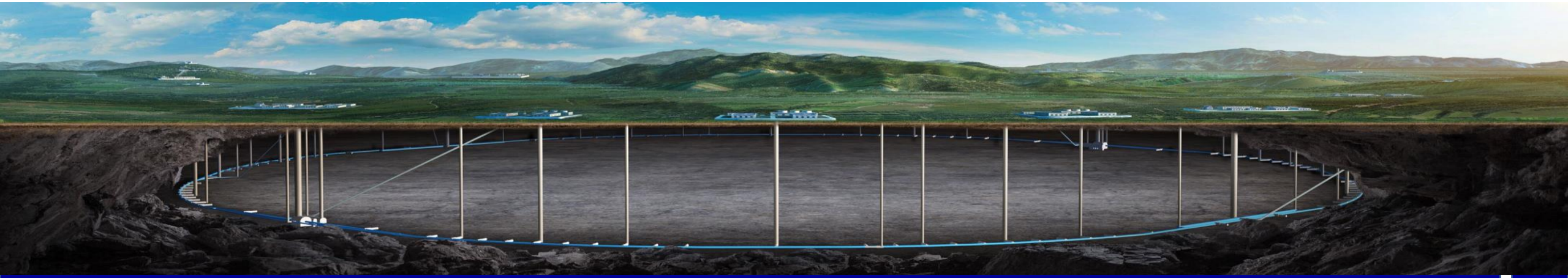
Outline

1 Introduction——CEPC proposal for particle physics

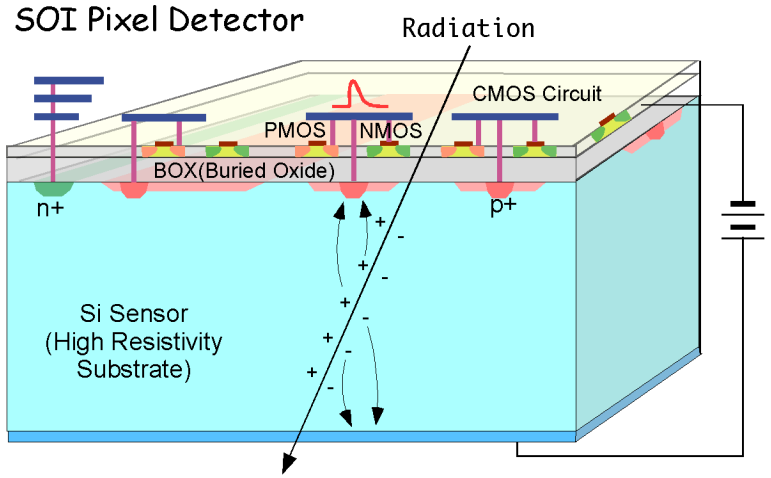
- Circular Electron-Positron Collider (90, 160, 250 GeV)
  - Higgs factory (10^6 Higgs)
    - Precision study of Higgs (m_H, J^{PC}, couplings), Similar & complementary to ILC
    - Looking for hints of new physics
  - Z & W factory (10^{10} Z^0)
    - Precision test of SM
    - Rare decays
  - Flavor factory: b, c and QCD studies
- Vertex Detector
  - High spatial resolution
  - Low power consumption
  - Low material





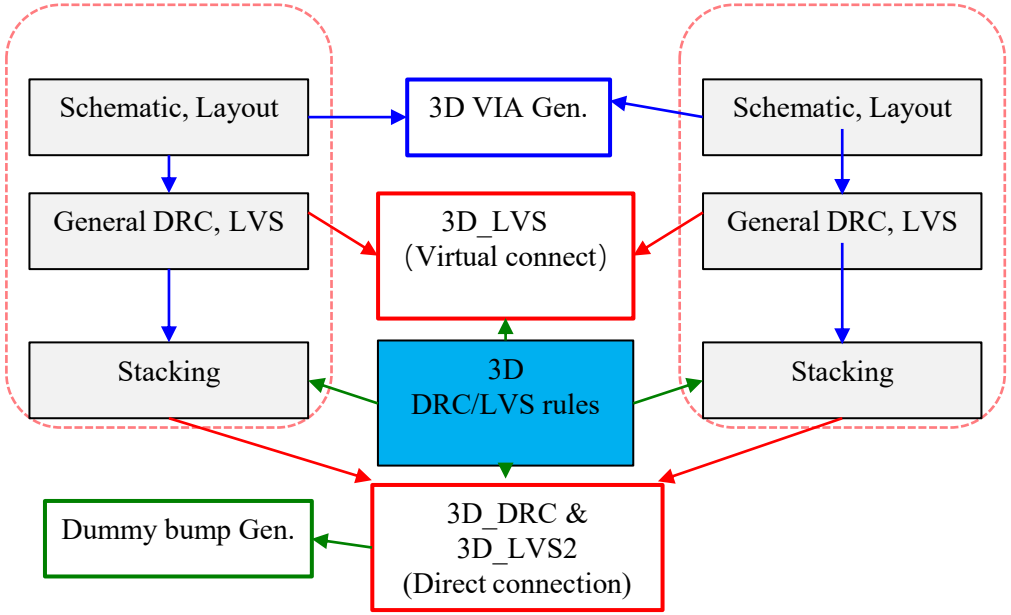
1 Introduction——Development of SOI Pixel Sensor

- Sandwich structure
  - Top: Independent signal processing circuit with pixels as the unit (Device Layer), inherits the advantages of SOI integrated circuits
  - Middle: **SiO_2 insulation layer** (metal via array for one-to-one electrical connection)
  - Bottom: Sensor diode array with pixels as the unit
- **200 nm** FD-SOI CMOS process （Device Layer）
  - Low leakage low power applications
  - 1 Poly 5 Metal layers
  - MIM Capacitor (1.5 fF/um^2), DMOS
  - Core voltage = 1.8 V, IO voltage = 1.8/3.3 V
  - **PDK (Process Design Kit) customized for charged particle and X-ray detection**
- **Flip-chip: Increase integration by using flip-chip technology (3D-SOI)**



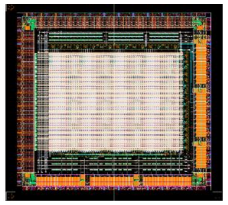
1 Introduction——3D architecture of CPV(compact pixel for vertex)-4

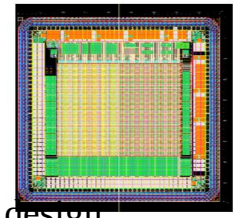
- 3D Vertical Integration
  - **Reduce pixel size** to achieve **high spatial resolution**
  - Increase integration for a **superior readout scheme** (time stamp + low power consumption)
  - Provide superior **detection performance**
- CPV-4 is the first trial of 3D design
  - **Upper Chip**：**Pixel logic** and **matrix readout logic**
  - **Lower Chip**：PDD sensing diode + amplifier/comparator
  - Using gold micro bumps to achieve pixel-level array connections
- Very complex design flow
  - 3D-compatible DRC(Design Rule Check) and LVS rules



3D-SOI design flow

Upper chip design



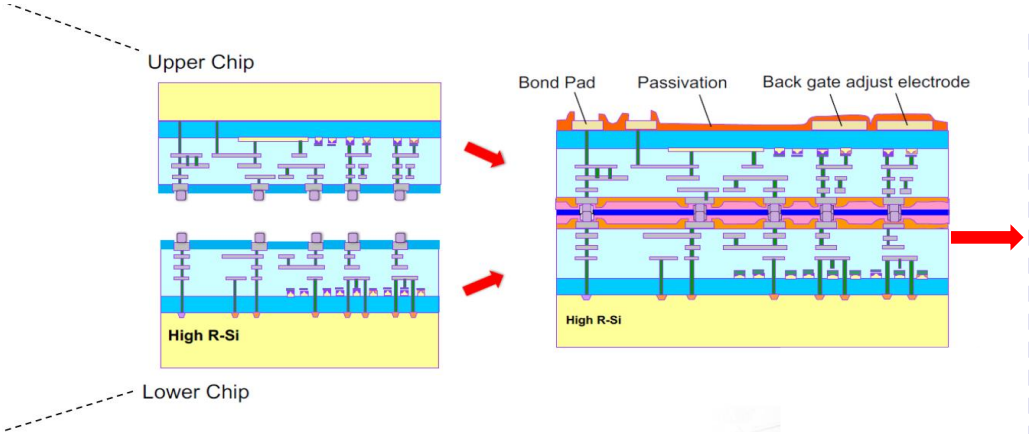


Lower chip design

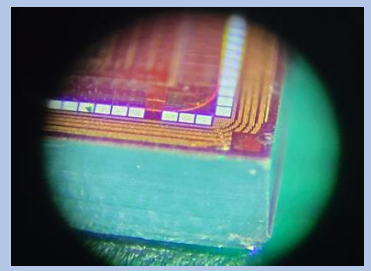
Delivery of separate chips

3D processing

Delivery of 3D chips



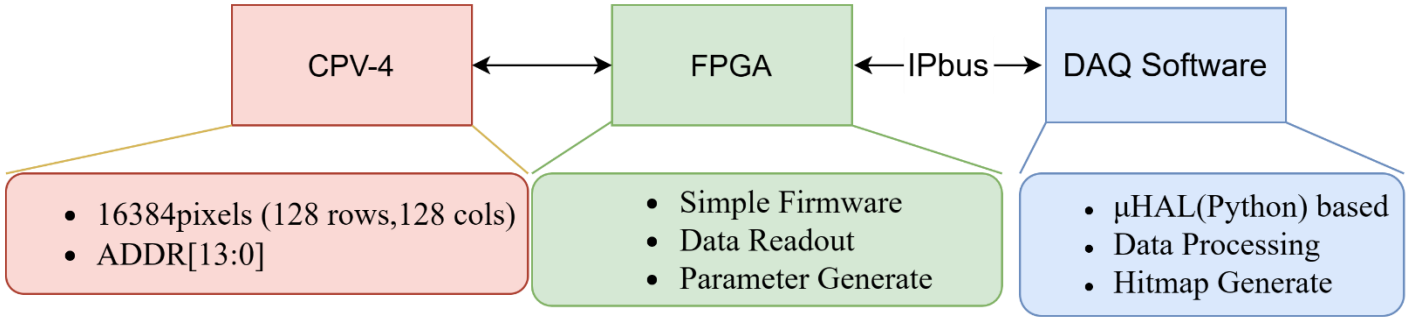
■ CPV-4：



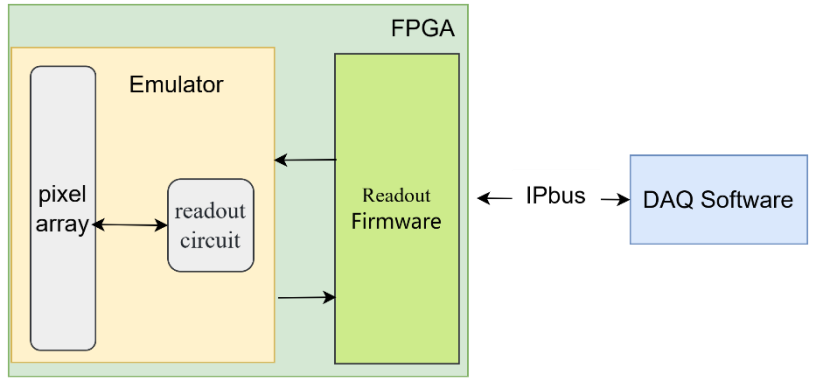
- Pixel size: 21.04 μm * 17.24 μm
- Spatial Resolution< 3 μm
- Power Consumption<50 mW/cm^2
- Time Resolution< 1 μs

1 Introduction——The validation of design and process

- **Challenges**
  - **First trial of 3D design**, high technical difficulty
  - **First time using 3D integration process**, low yield
- **Requirements for the testing and verification system**
  - Basic function requirements: Chip configuration, data readout
  - Tests can be carried out on **upper chips**, **lower chips** and **3D chips** separately
  - Convenient debugging
  - Short development cycle
- **CPV-4 upper tier chip Emulator**
  - Debugging and verifying the functionality of the test system
  - Verifying the logical correctness of the CPV-4 upper chip



CPV-4 Test Verification System Architecture

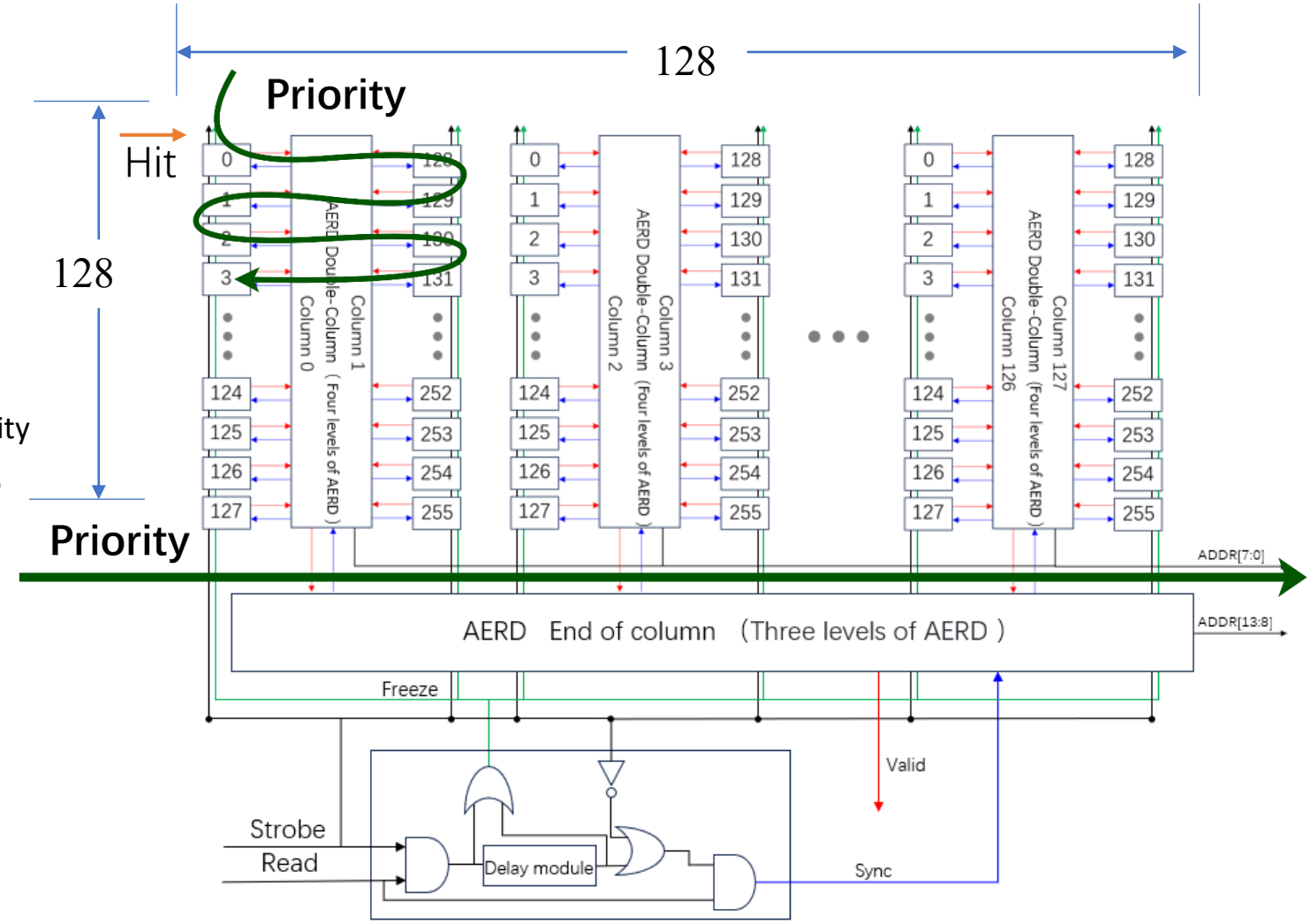


CPV-4 replaced by Emulator

2 Design and Implementation of Emulator

- Architecture of the CPV-4 upper chip

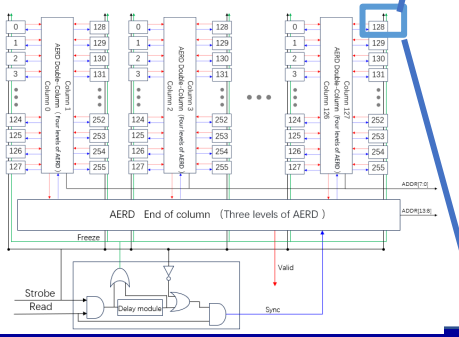
  - **Pixel array circuit:**
    - 128(row)×128(col)
    - Receive and store hit signals
  - **Readout circuit:**
    - Arranged in double columns
    - Read out the hit pixel addresses in order of priority （**AERD（Asynchronized Encoder Reset Decoder）**）



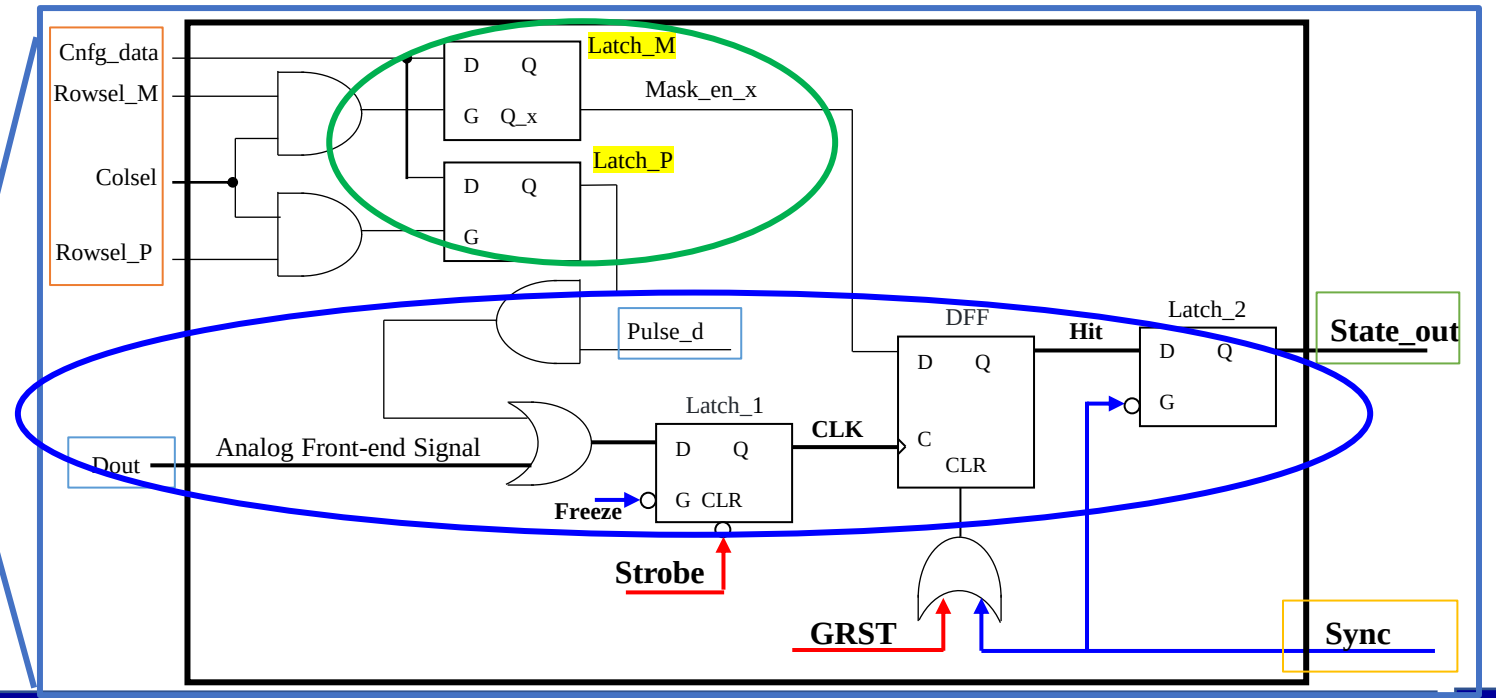
Upper chip circuit

Design and Implementation of Emulator——Pixel Internal Logic

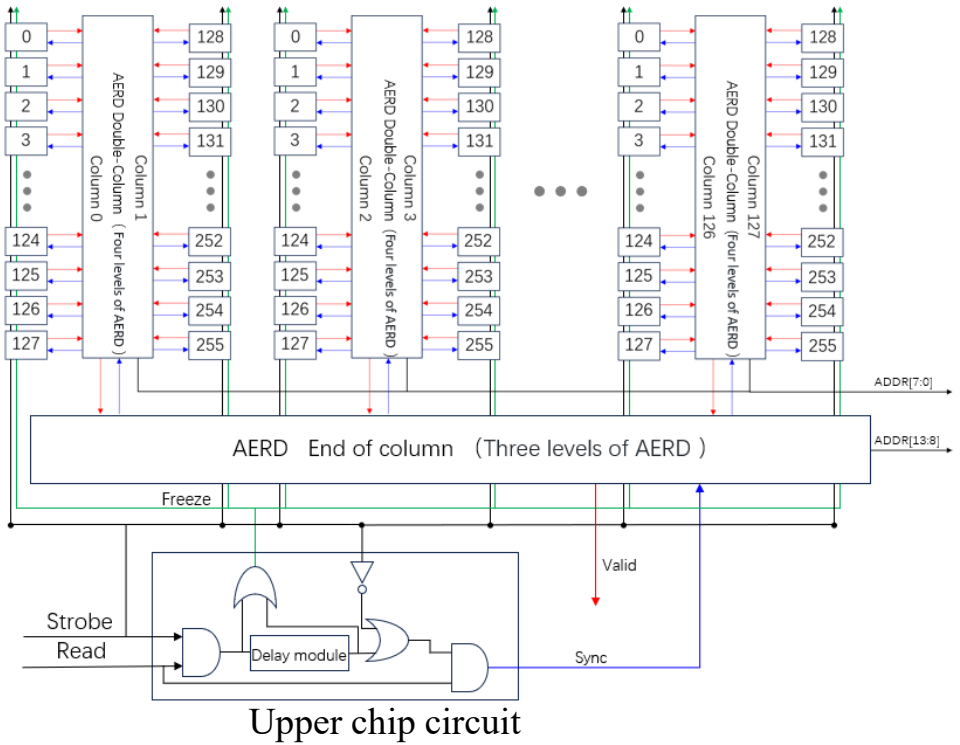
- **Hit response：**
  - **Working mode:** Continuous mode, Trigger mode
  - **Input:** Dout, Pulse_d
  - **Pixel state output:** State_out
  - **Sync:** Reset the pixel state
  - Respond and store hit information
- **Register control**
  - Latch_M
  - Latch_P



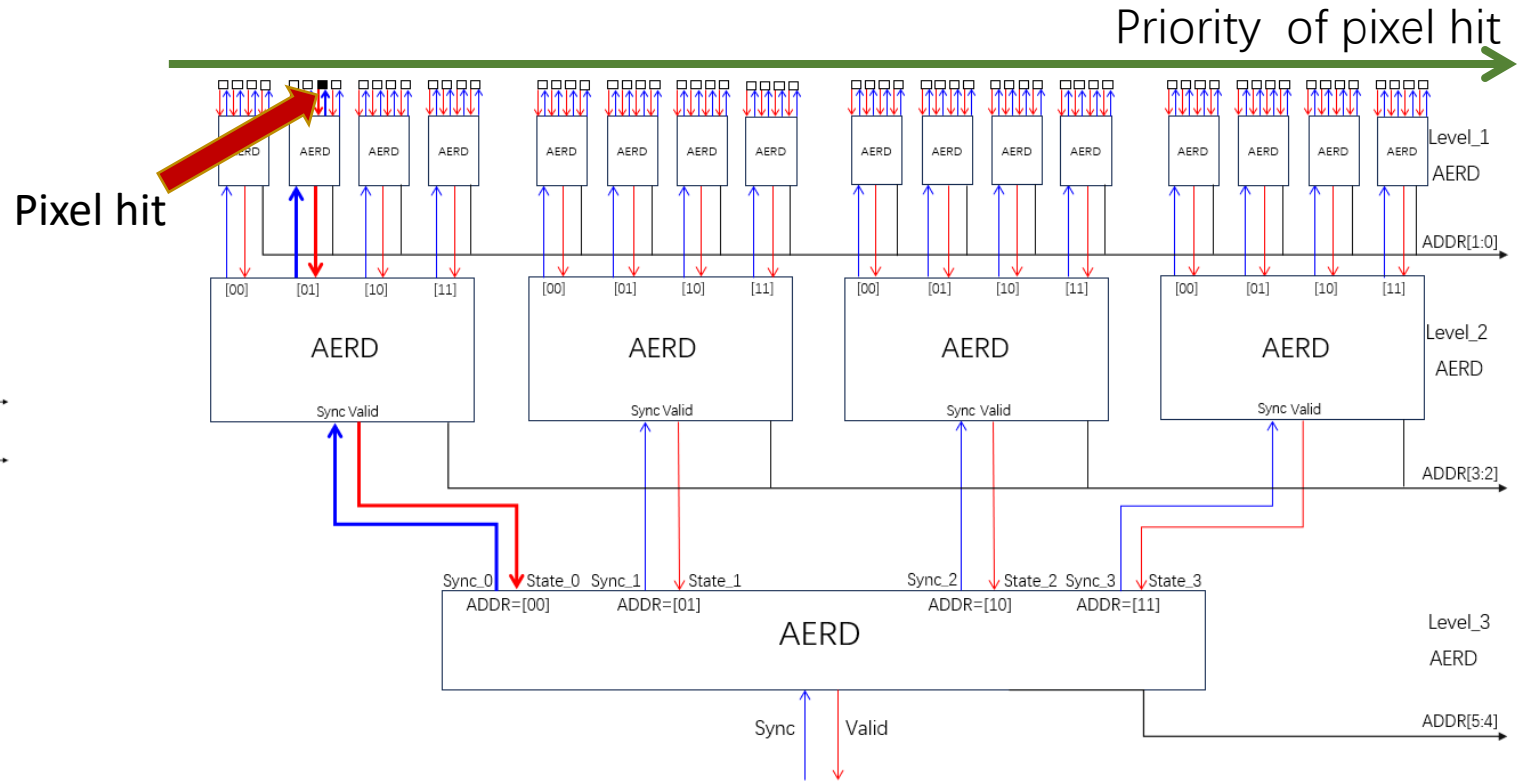
Pixel Internal Circuit



2 Design and Implementation of Emulator——Readout circuit



Upper chip circuit

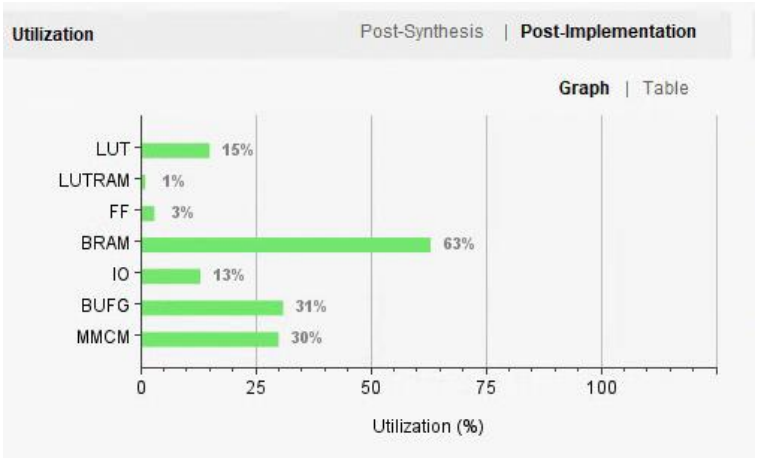


Tree-like cascade method of AERD circuits

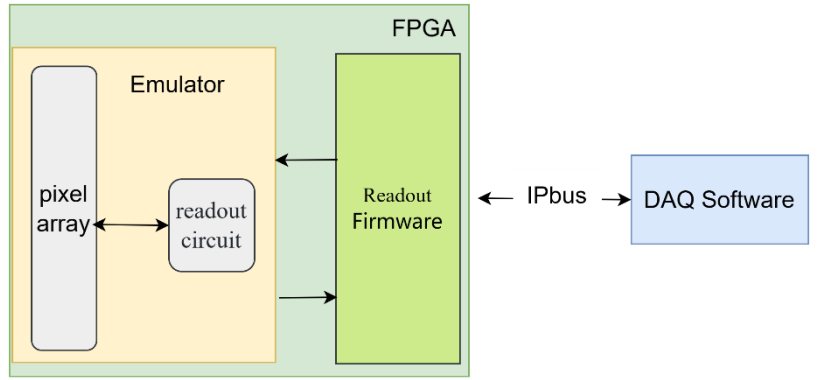
- **AERD（Asynchronized Encoder Reset Decoder）**
  - Four inputs, read out the encoded address, receive sync reset signal
- **Readout Circuit in CPV-4 upper-tier chip:**
  - Readout method: Multi-level AERD readout, according to priority, sequentially read out the hit pixels and reset the state of the readout pixels
  - Readout structure: **4-level AERD** inside the array, **3-level AERD** outside the array
  - Readout result: Encoded address signal **Addr[13:0], valid hit signal**

2 Design and Implementation of Emulator——Implementation on FPGA

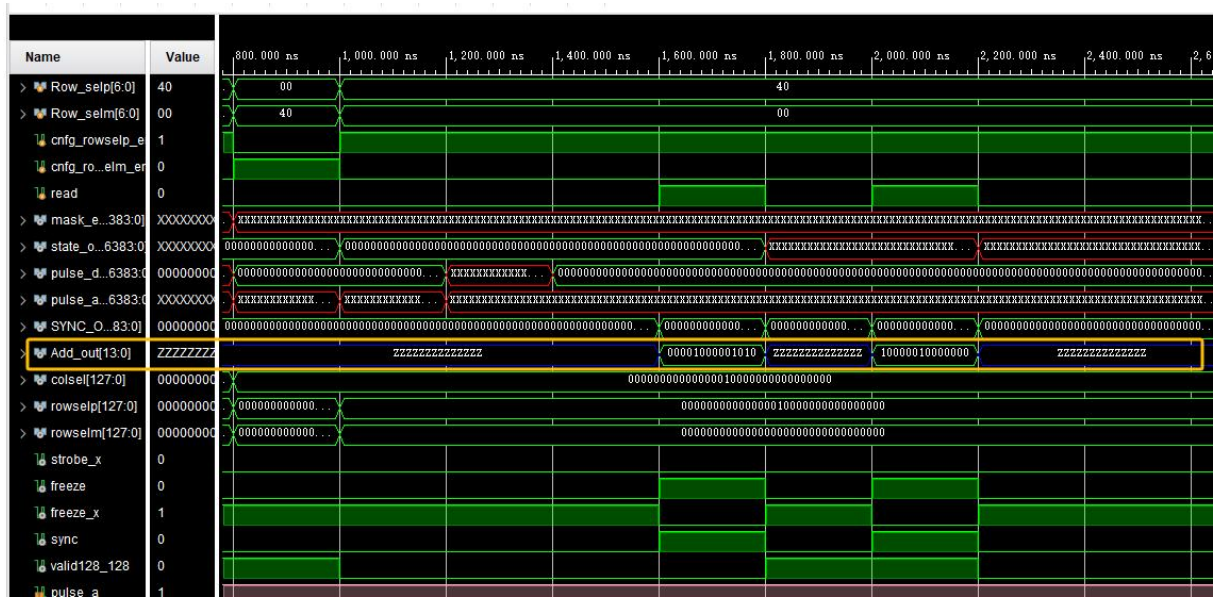
- **Complete the implementation of the emulator on the FPGA board**
- **The readout module will also be implemented on the same FPGA board**
- **Pixel array size:** 128(rows)×32(cols)
- **Implementation method:** Verilog
- **FPGA model:** XC7K325T
- **Readout data:** Addr[13:0], valid hit bit



Resource utilization of the emulator and readout firmware



CPV-4 replaced by Emulator



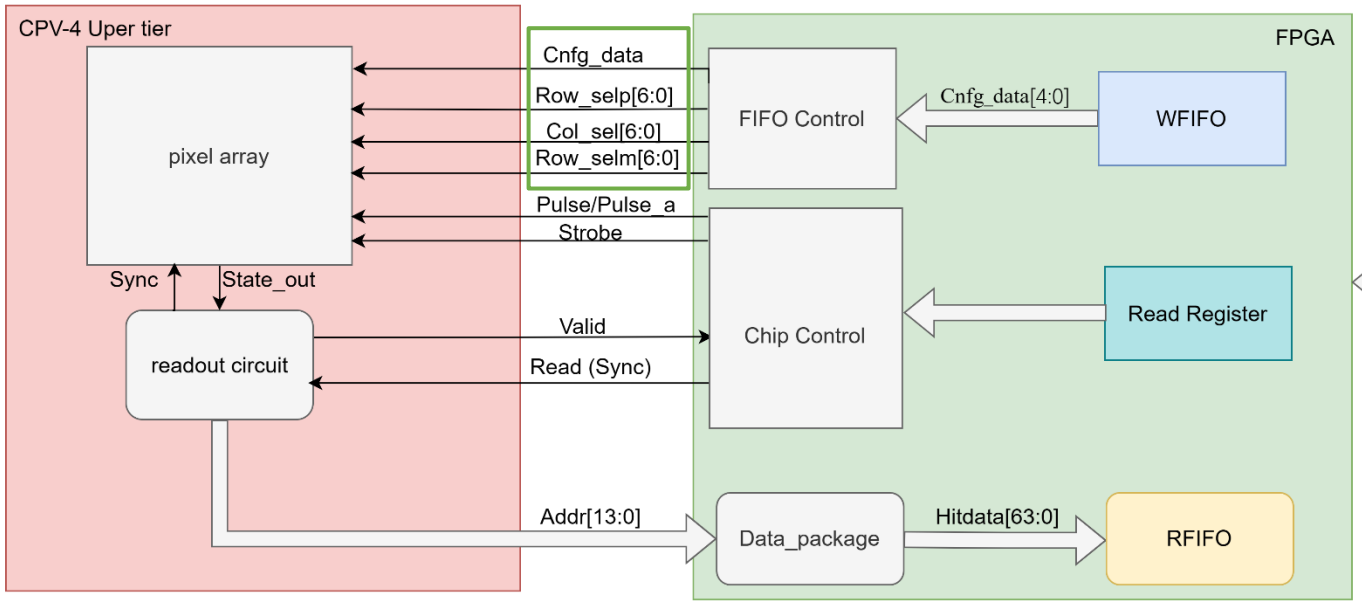
Behavioral Simulation Result of CPV-4 Upper Tier Emulator

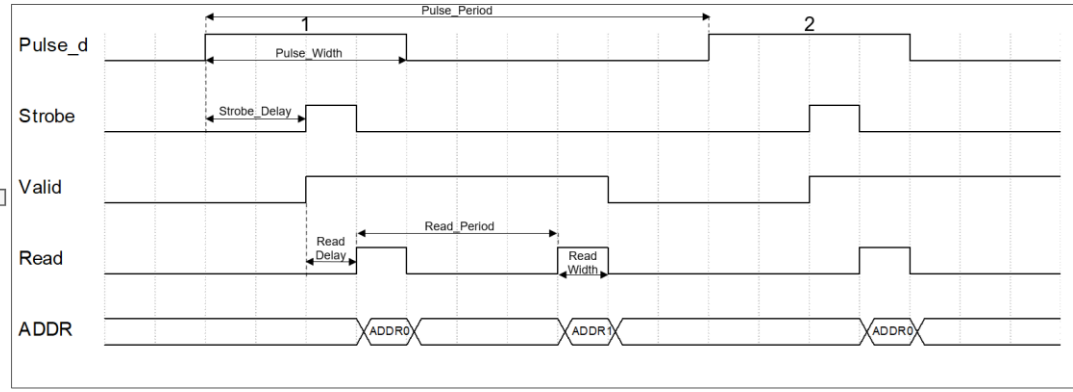
Ideal implementation of upper-tier chip circuit

3 Test system design——CPV-4 Interface Logic

- Upper-tier Chip provides the complete logic interface between the 3D chip and the readout firmware.
  - Operation mode selection (Strobe)
  - Pixel state configuration (Col_sel, Row_selp,Rpw_selm, Cnfg_data)
  - Data readout (Read(Sync))
  - Pulse testing (Pulse/Pulse_a)
- The emulator can be fully compatible with the chip interface logic.

Can respond to various parameters provided by the readout firmware
Every pixel can be selected for state configuration
Simulate different experimental environments to obtain different results

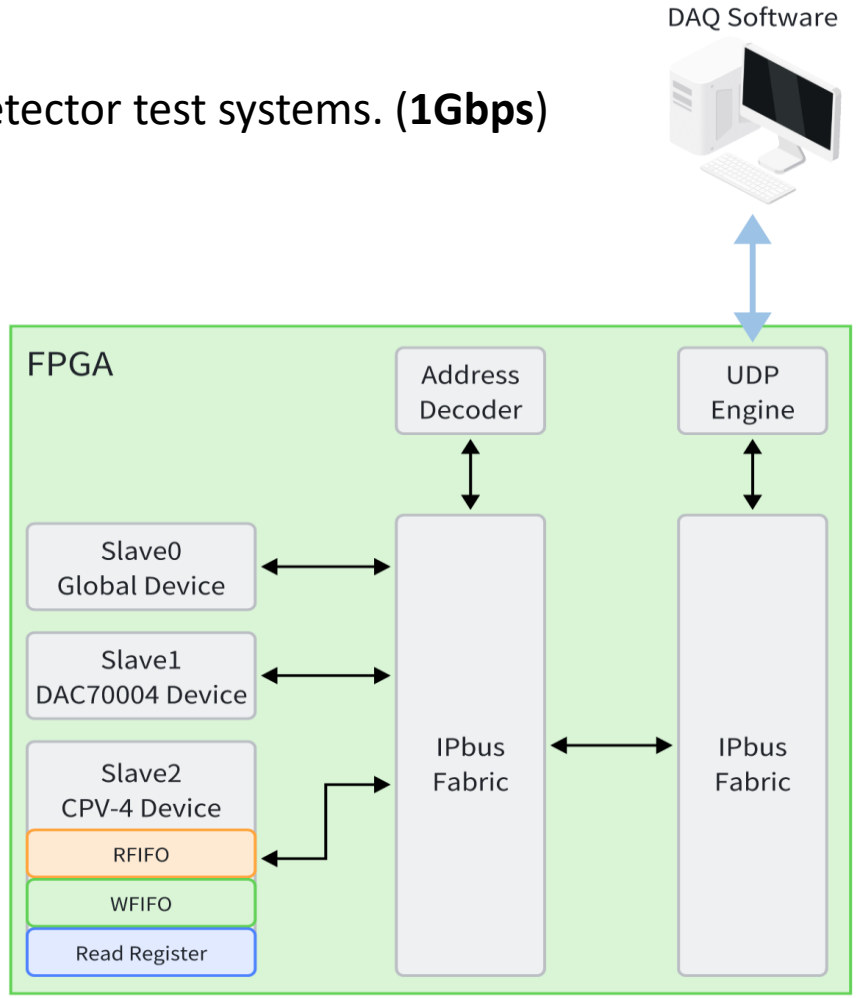




Adjustable parameters

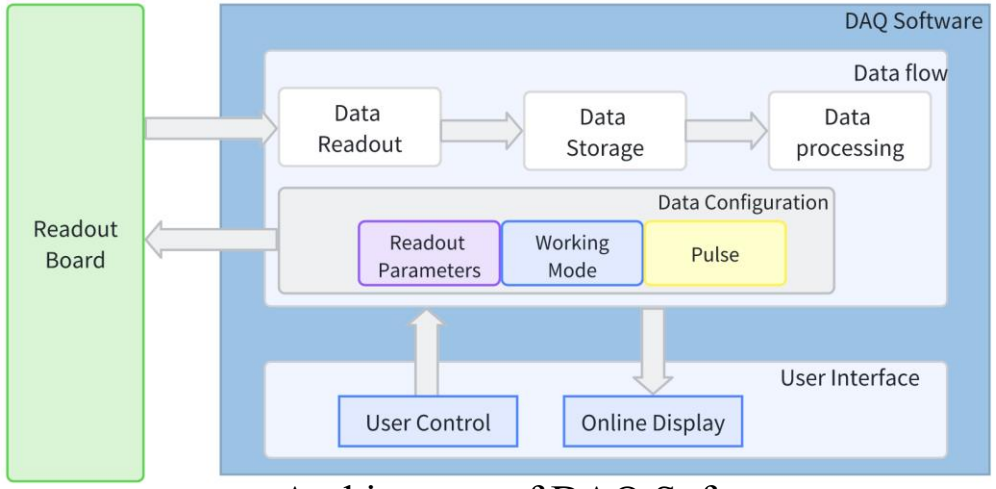
3 Test system design——IPBUS Implementation

- Using the IPbus protocol as the data transfer protocol
  - A simple, reliable, IP-based protocol for controlling hardware devices.
  - The data transfer capability is sufficient to meet the needs of small-scale detector test systems. (**1Gbps**)
- Three slave devices are developed according to controlling needs:
  - Slave 0: Used for system reset logic
  - Slave 1: Control the DAC70004(on the chip board)
  - Slave 2:
    - Sets the working mode and parameters of the CPV-4
    - Writes the configuration of each pixel (WFIFO)
    - Stores the hit pixel address information(RFIFO)



The IPbus slaves in Firmware

3 Test system design——DAQ Software



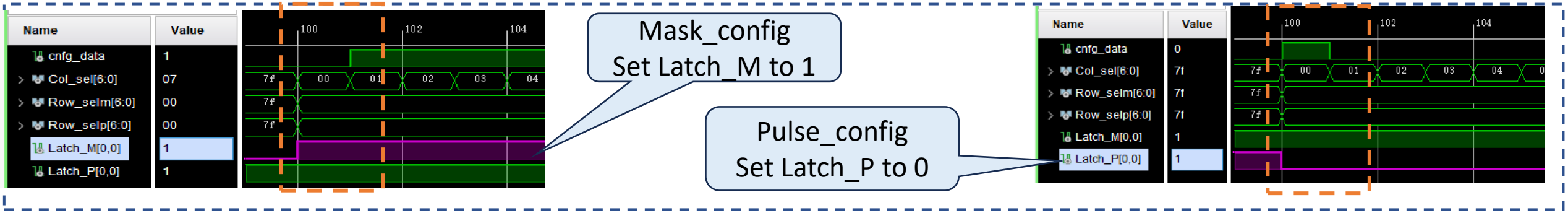
Architecture of DAQ Software

- Developed with Python API
- Data flow system
  - Data readout: Periodic query and read data from RFIFO.
  - Data storage: Save raw data in hexadecimal format to a file.
  - Data processing: Decode the data to get addresses, timestamp.
  - Configuration: Chip operating modes(FPGA), readout parameters(FPGA), pixel states(CPV-4)
- User Interface
  - command execution
  - Information interaction:
    - configuration information
    - hitmap display
    - operation status display

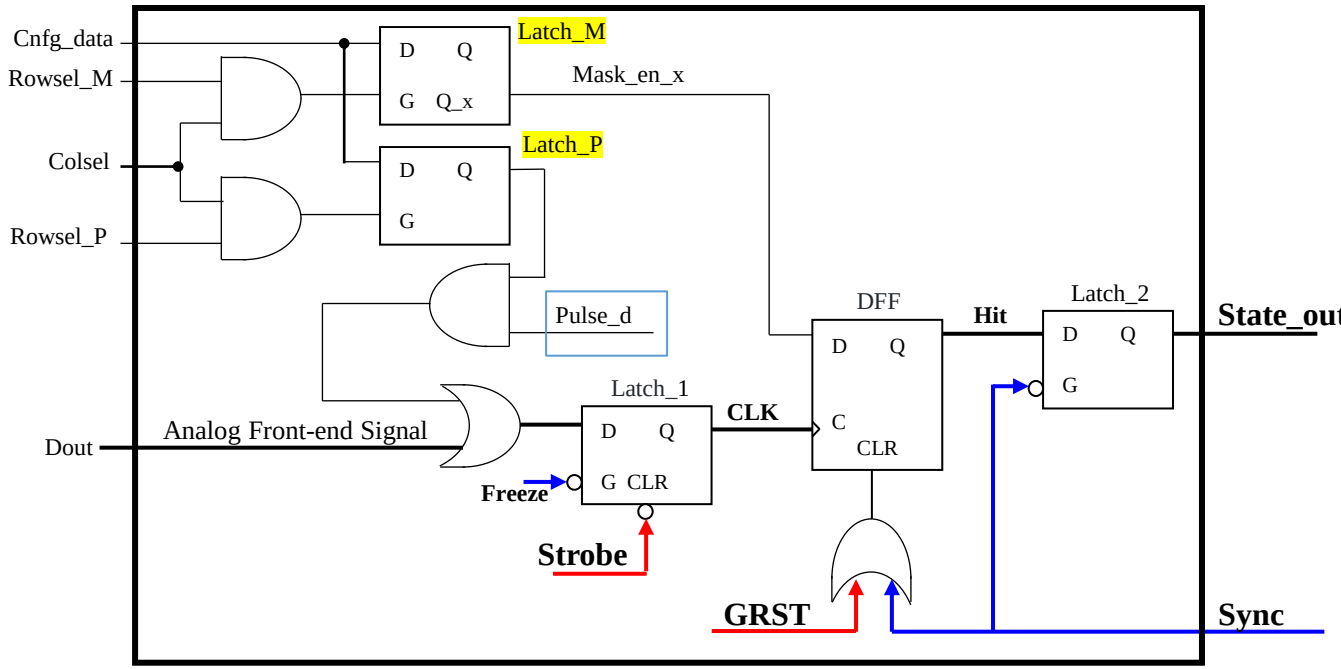
Implement all the functions required during the chip testing process

4 Joint debugging with Emulator

- Pixel configuration(Pixel[0,0])



Pixel configuration successfully

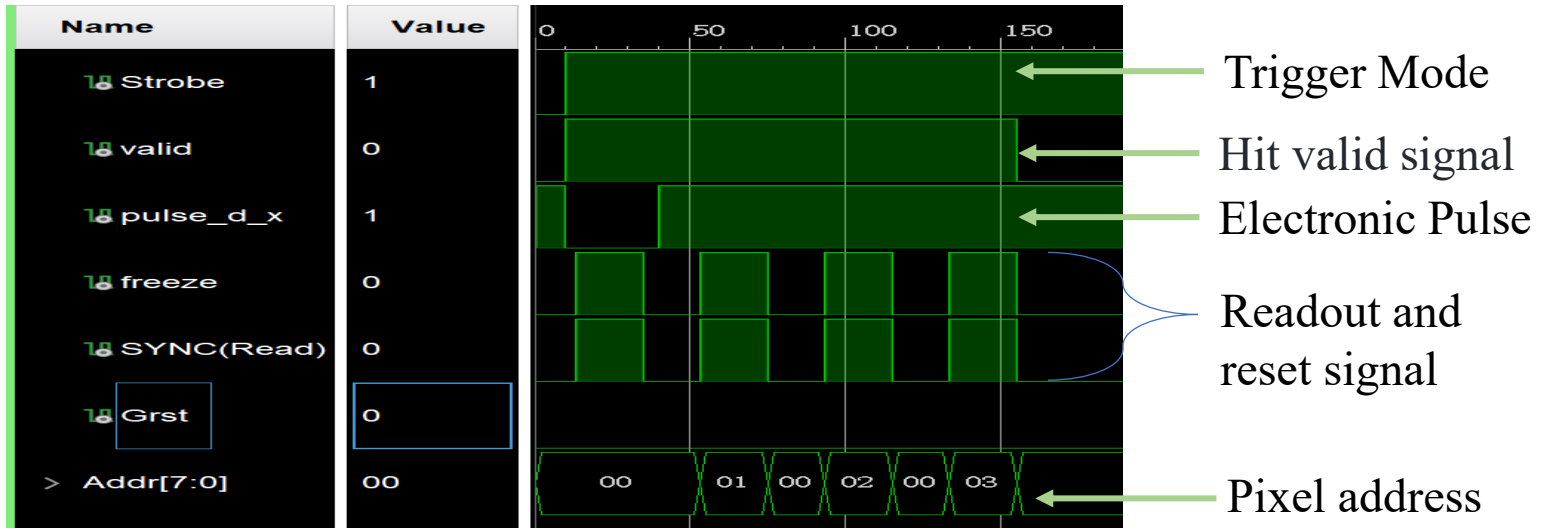


4 Joint debugging with Emulator : Electronic Pulse Tests

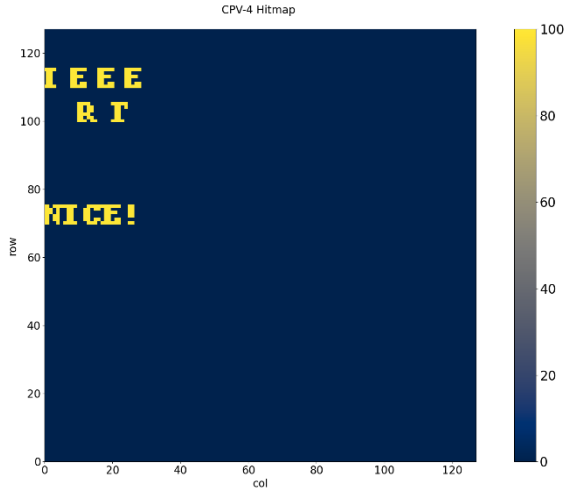
- Parameter Setting:

Parameters	Emulator
Operation_mode	Continuous
Pulse_Num	1
Pulse_Width	3 μs
Read_Period	4 μs
Read_Delay	0.2 μs
Read_Width	2.2 μs

- Integrated Logic Analyzer Results:



- Readout Result:

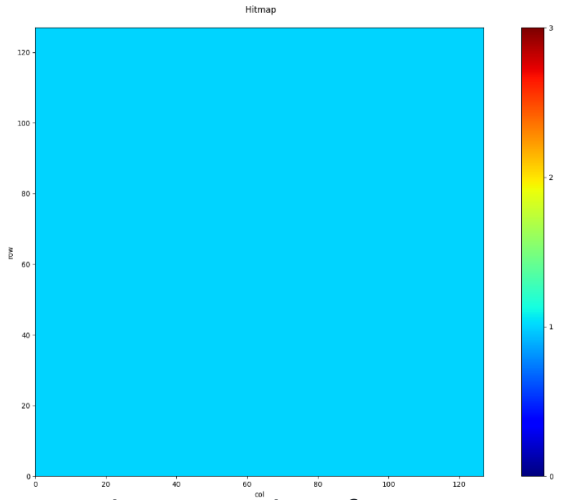


Readout results of specific pixel for 100 pulses

- **Readout Successfully**
- **Emulator works properly**
- **Parameter configuration function works successfully**

4 Tests on CPV-4

- Tests on the upper chip
- Tests on 3D chip
  - Pixel configuration
  - Electronic pulse tests
  - Driving force is **insufficient**
  - **CPV-4 functions properly**



Full Array Readout Results of CPV-4 upper Chip

Parameter	Emulator	Upper chip	3D chip
Operation_mode	Trigger	Trigger	Trigger
Pulse_Num	1	1	1
Pulse_Width	3 μs	3 μs	3 μs
Strobe_Delay	2.5 μs	2.5 μs	2.5 μs
Strobe_Width	0.6 μs	0.6 μs	0.6 μs
Read_Period	0.4 μs	4 μs	8 μs
Read_Delay	0.5 μs	0.5 μs	0.5 μs
Read_Width	**0.2** μs	**2.2** μs	**6.3** μs

Comparison of timing parameters between emulator, upper chip, and 3D chip

5 Summary

- **Developed the CPV-4 upper chip emulator on the FPGA board**
  - Implemented all functions of the CPV-4 Upper Tier pixel array and readout logic
- **Testing and verification system**
  - Implemented parameter configuration and readout functions
- Through joint debugging with the CPV-4 upper chip emulator and the testing system, it is proven that:
  - **Emulator works properly**
  - **The logic of the CPV-4 upper chip is correct**
  - **The testing and verification system is fully functional and runs correctly**
- **The fully functional test and verification system** has been used for **the testing and verification of the CPV-4 chip**

Thank you!