Development of Radiation-tolerant Slow-Control Board based on Atom Switch-based FPGA

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Kazuki Ueno (Osaka University/QUP)

Nanae Taniguchi (KEK/QUP),

Toshitsugu Sakamoto, Makoto Miyamura (NanoBridge Semiconductor, Inc.)

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Outline

- Introduction
- Atom switch FPGA
- Irradiation tests
- Slow-Control board
- Summary

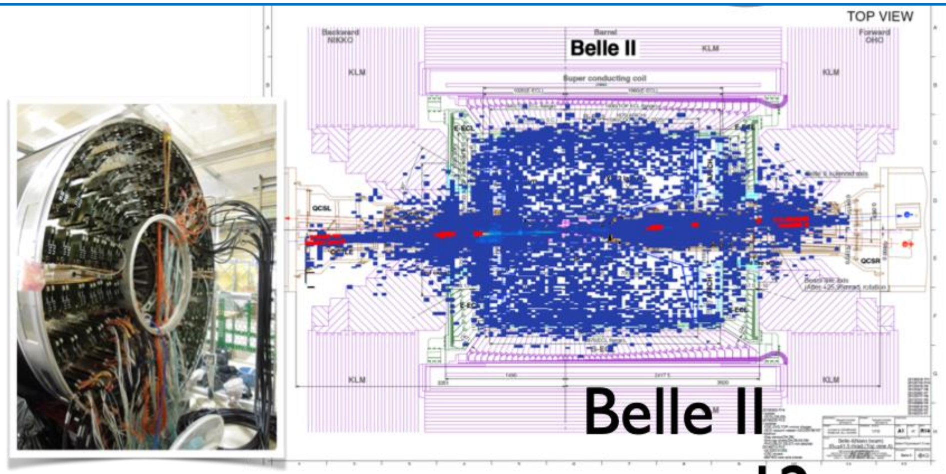
Accelerator experiment and radiation

Trend

higher energy
higher luminosity
higher intensity

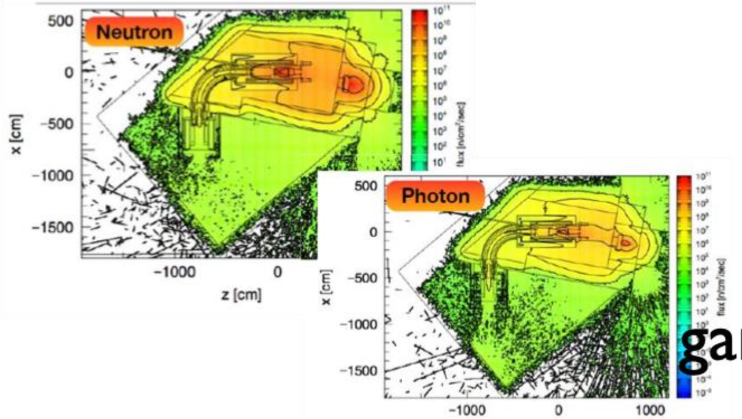
Radiation tolerance for electronics(incl. sensor) will be **more important**.

examples of radiation level



neutron $>10^{12}$/cm2
gamma ~1kGy (10 years)

x 5-10



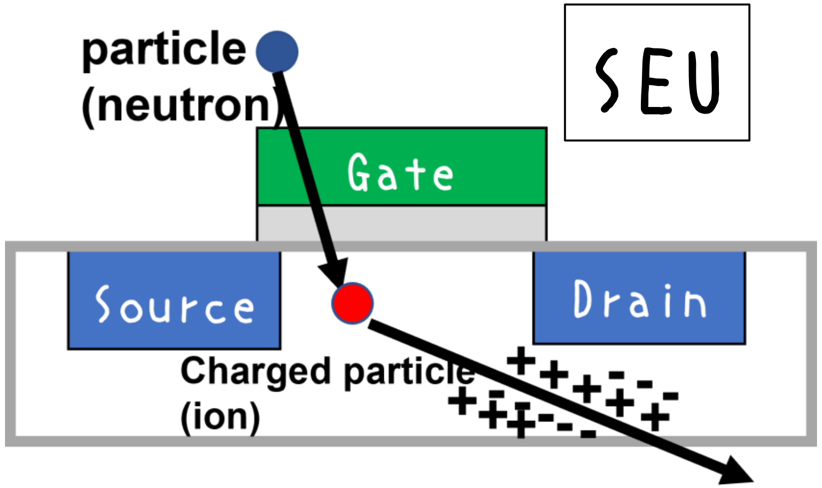
COMET

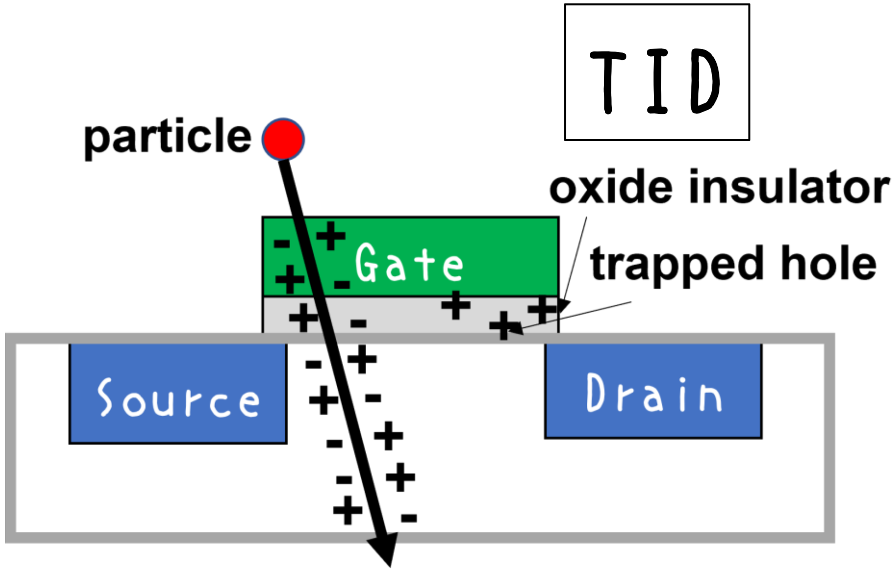
neutron $\sim 10^{12}$/cm2
gamma ~1kGy (200days)

x >5-10

Radiation effects

- Single Event Upset(SEU) (soft error)
  - Bit flip by neutron (nuclear reaction, recoil) and high energy heavy particles.
- Type Inversion
  - Hard damage in semiconductor by neutron.
- Total Ionizing Dose Effect (TID)
  - Permanent damage by fixed charge from large amounts of radiation (gamma-ray).
- Displacement Damage Dose (DDD)
  - Permanent damage by displacement of crystal lattice atom from radiation (electron, proton, large amounts of neutrons).





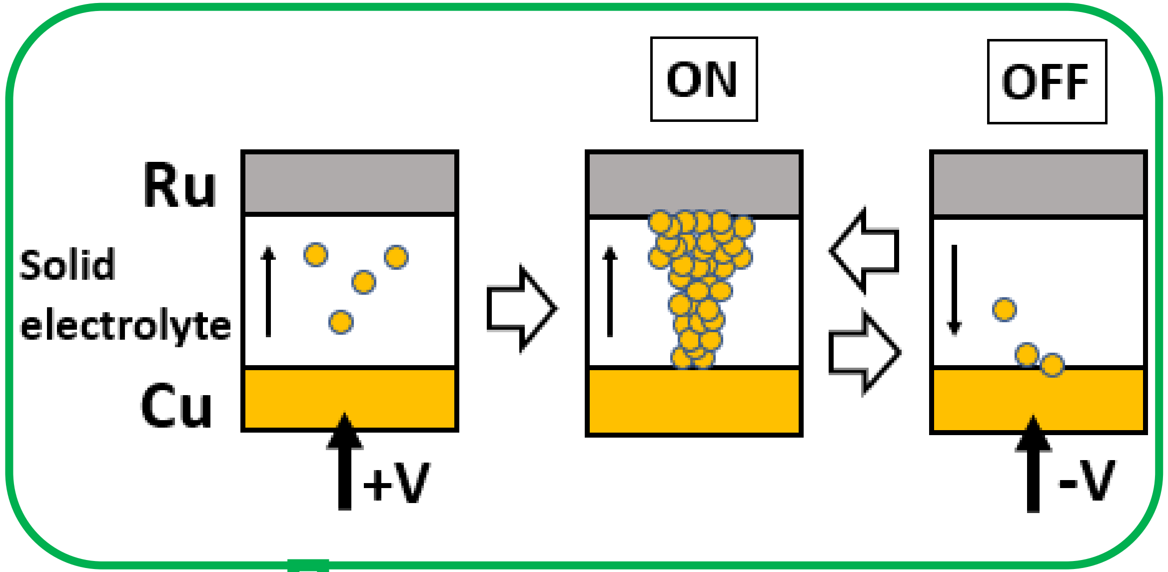
For future experiments

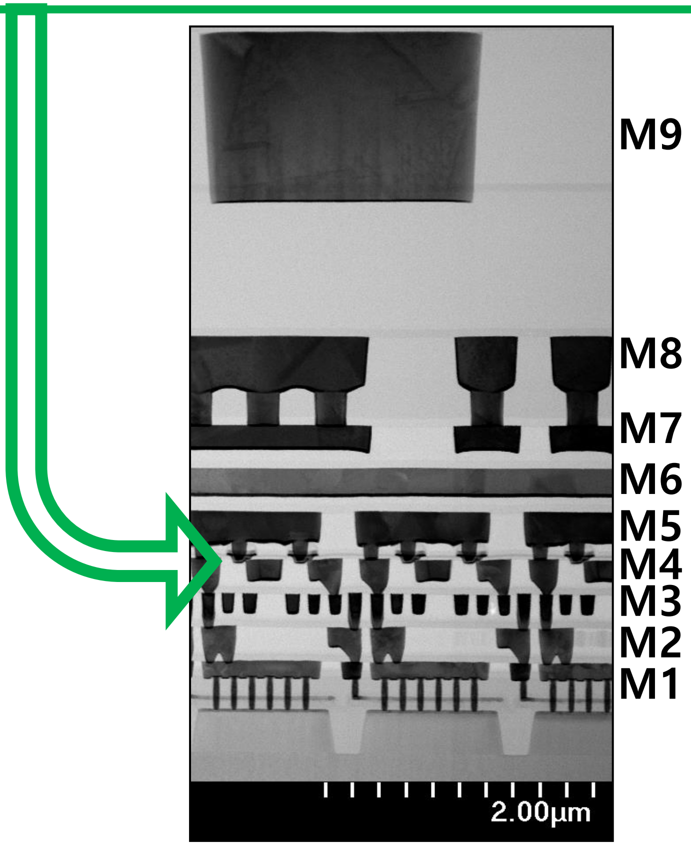
- Current situation
  (example) Soft error on FPGA
  - Error correction/mitigation code
  - Re-configuration
- Future
  - Countermeasure is indispensable.
  ⇨ Use of Atom switch
  (Atom switch-based (AS) FPGA)

Atom switch FPGA

Atom switch(AS)

Conductive bridge is formed in polymer solid electrolyte between inert Ru and active Cu electrodes.



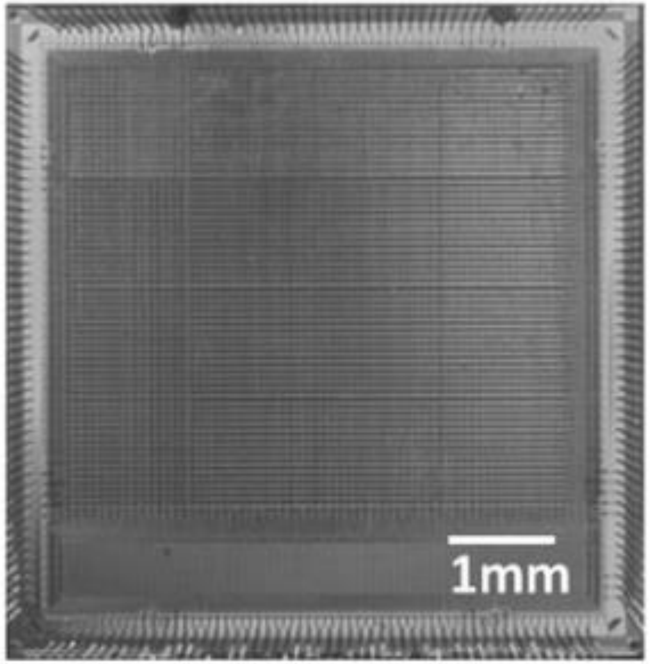


Specification

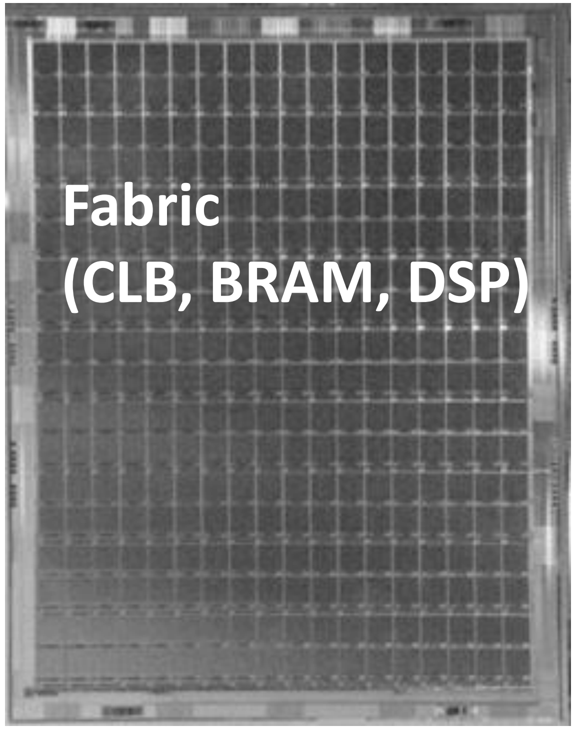
- resistances for ON/OFF : ~2k/200MΩ
- # of rewriting times : > 10^3
- retention time : > 10 years
- Switch capacitance : < 0.2fF
- SEU free in principle

AS-FPGA

Examples of AS-FPGAs



Item	Spec.
LUT	33,792
Flip Flop	33,792
BRAM	768
SRAM size	1,536 kbit
rated vol.	1.1V
IO vol.	1.8V
AS bit	50 Mbit
process	40nm



Process	**28nm CMOS**
LUTs	**4input LUT 171k slices**
Block RAM	**4bx1024word Dual Port 980 slices**
PLL	**5**
CLK trees	**8 (hard wired)**
DSP	**648 slices**
GPIO	**240 (Programmable)**
LVDS	**16**
Core voltage	**1.05 V**
IO voltage	**1.8 V**

AS-FPGA

- Features
  - Rad-hard (error rate < 1/100)
  - Low power consumption (< 1/10)
- Current status
  - irradiation test with heavy ion and pulsed laser
  - verification test on satellite

In principle OK for our purpose

We need to **confirm feasibility**.

- tolerance to very high radiation level
- usability
- etc...

Irradiation tests

Neutron irradiation tests

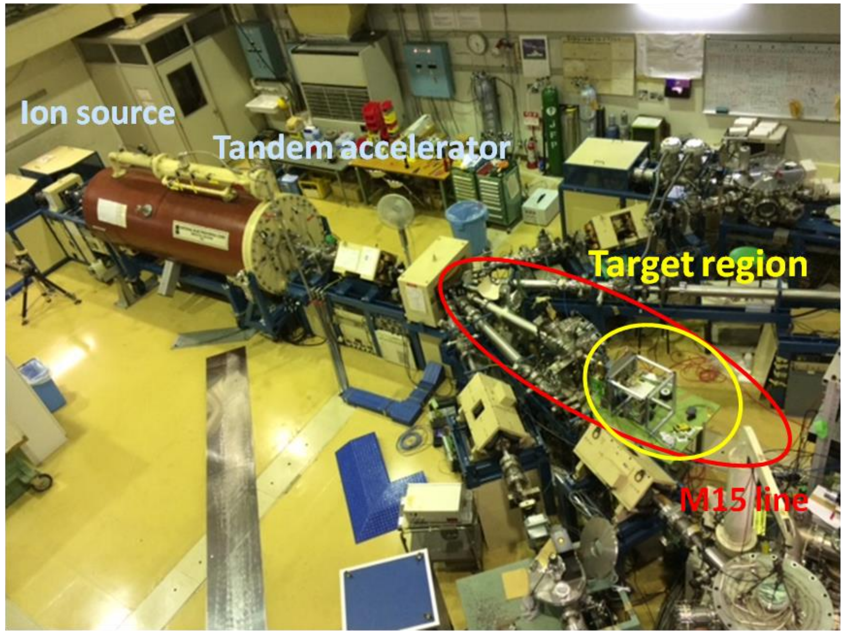
Tandem accelerator @ Kobe Univ.

- Beam : 3 MeV deuteron
- Target : Be (ϕ20 mm)
- Neutron energy : 2 MeV (<7 MeV)
- Flux : 4.9×10^{6} Hz/cm^2 @ 10cm from target (beam current = 1 μA)

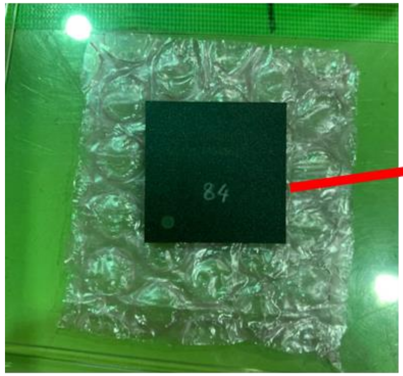
Reactor @ KUR

- Method : Pneumatic Tube
- Rated thermal power : 5 MW
- Neutron energy : broad
- Flux : > 10^{13} Hz/cm^2

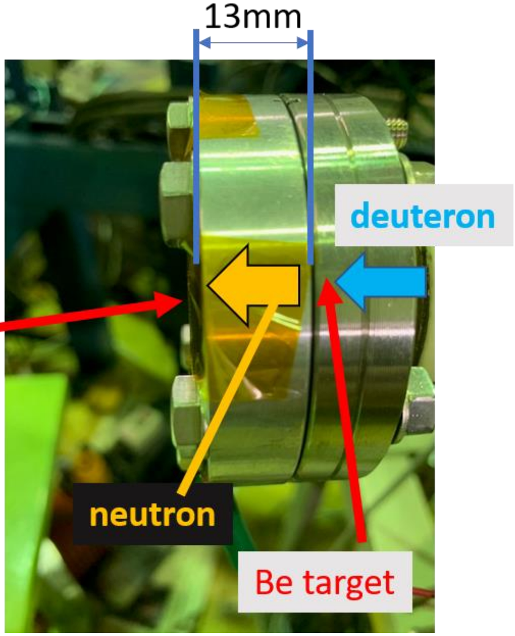
SEU and DDD measurements



Tandem facility



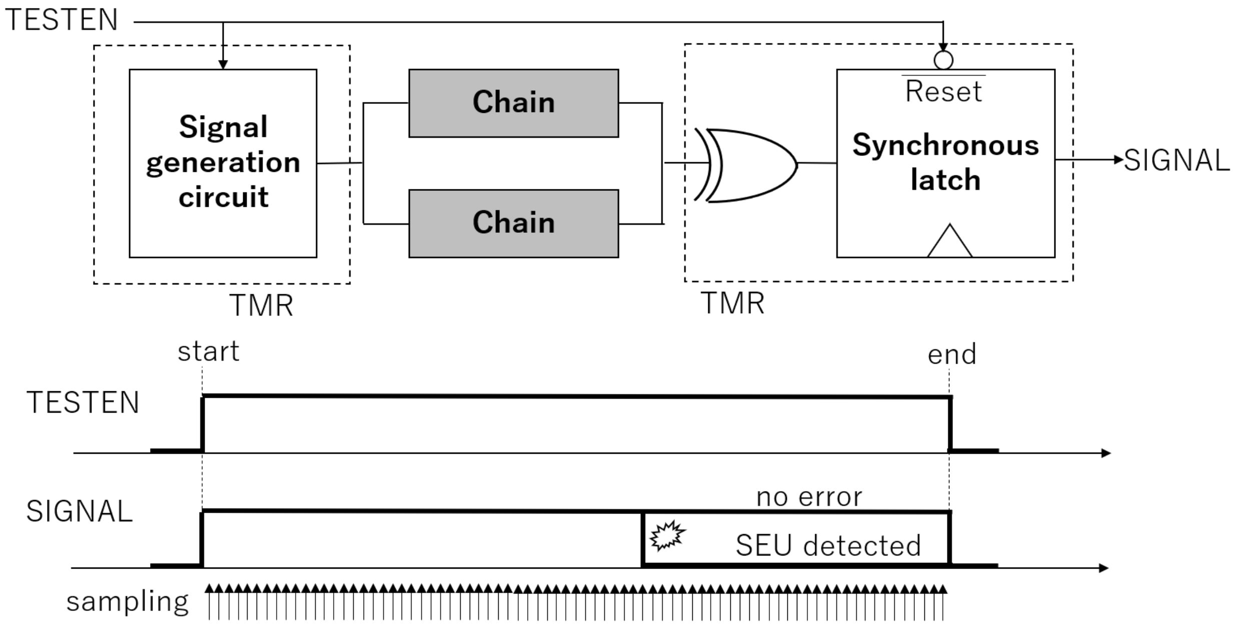
Packaged AS-FPGA



Neutron irradiation tests

SEU counts were measured with 4 types of chains.

NO SEUs were observed in AS FPGA!



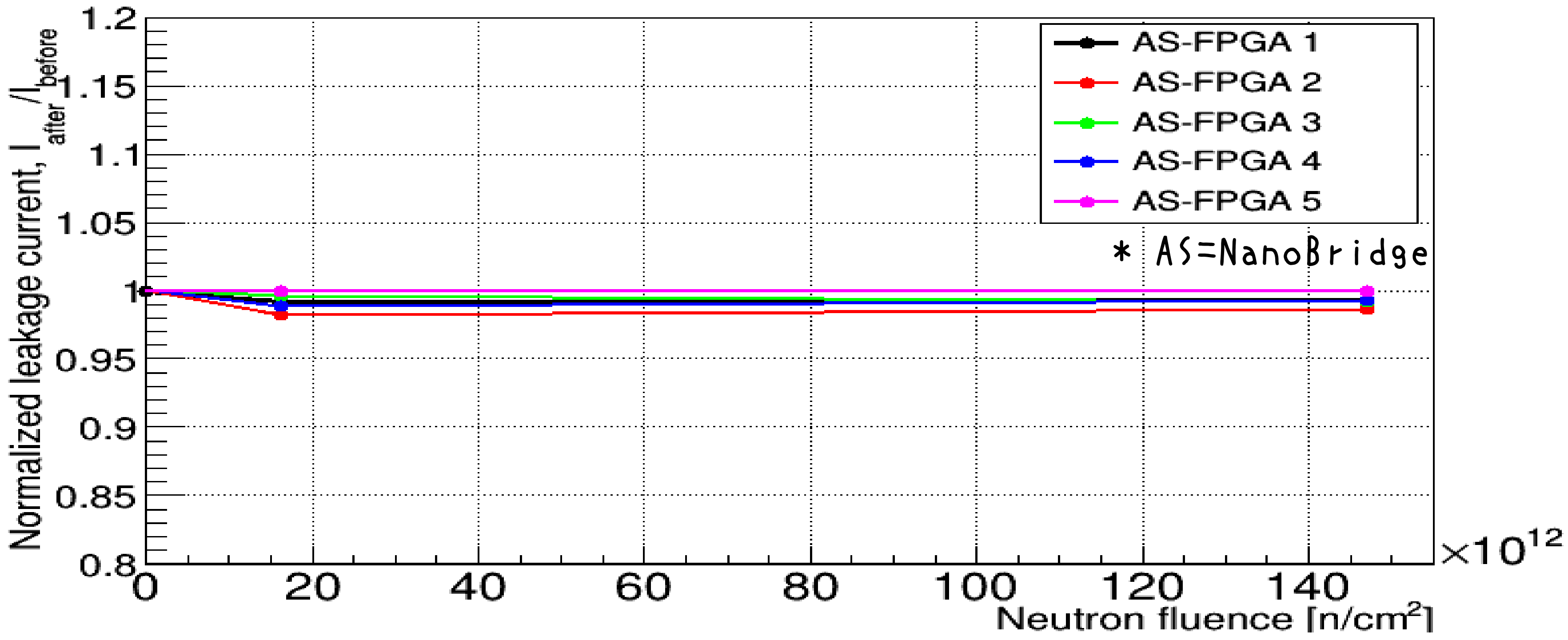
Schematic view of evaluation circuit for SEU

Results of SEU counts

DUT type	Scale	Neutron fluence(n/cm^2)	SEU counts
SRAM	2 kbit	1.6×10^{11}	5
AS1	96 CLBs	3.6×10^{11}	0
AS2	368 CLBs	1.7×10^{11}	0
DFF+AS	468 CLBs	1.5×10^{11}	0

Neutron irradiation tests

Leakage current was measured before/after irradiation.



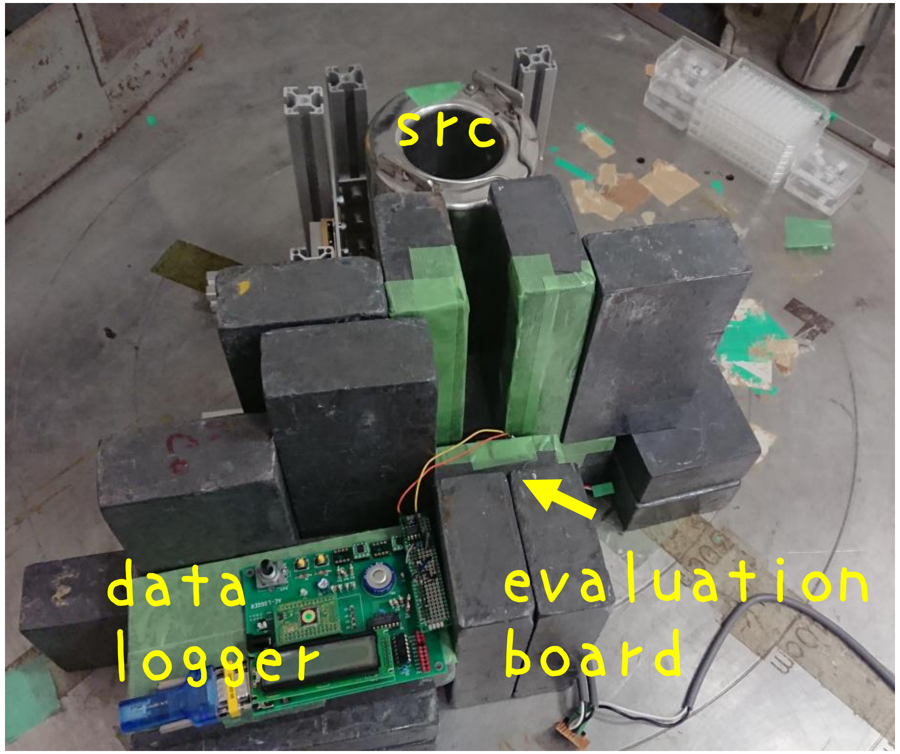
NO DDDs were observed!

Irradiation tests

gamma-ray irradiation tests

RI Center @ Tokyo Institute of Technology & QST

- Src : Co-60
- Dose rate : 500 Gy/h
- Total dose : 10 kGy

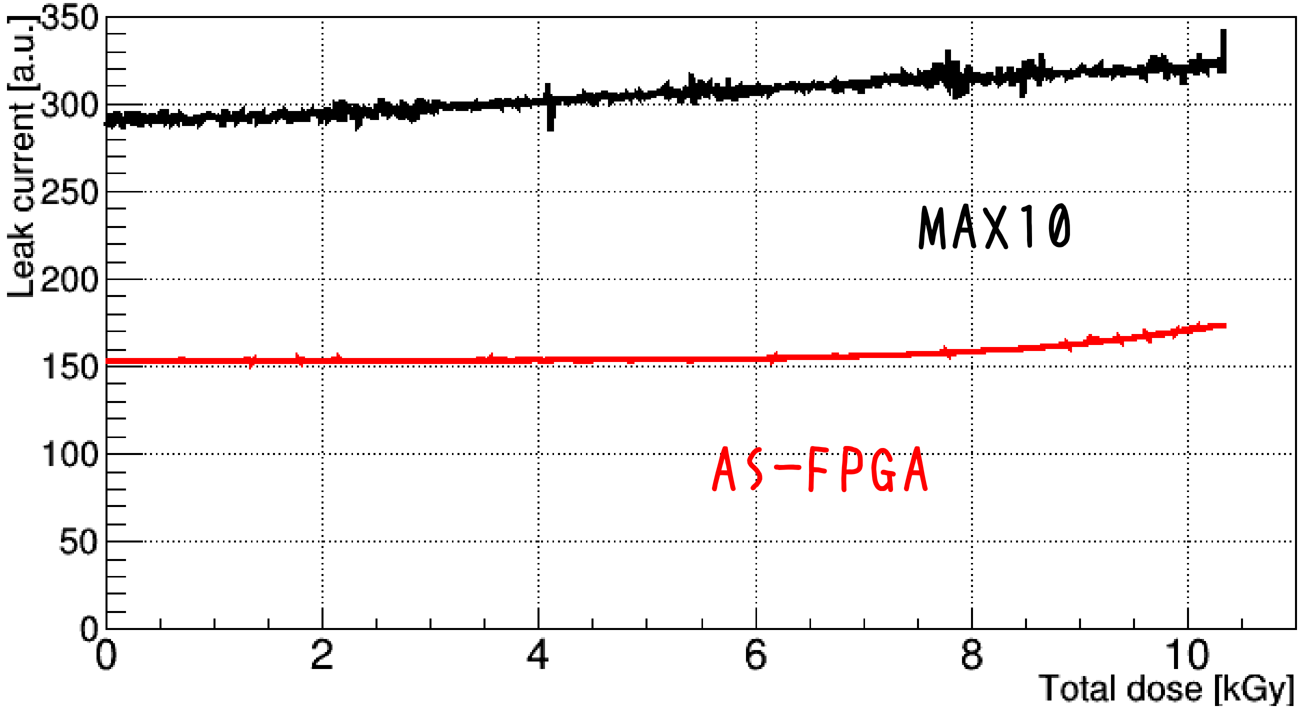


Experimental setup

TID measurements

gamma-ray irradiation tests

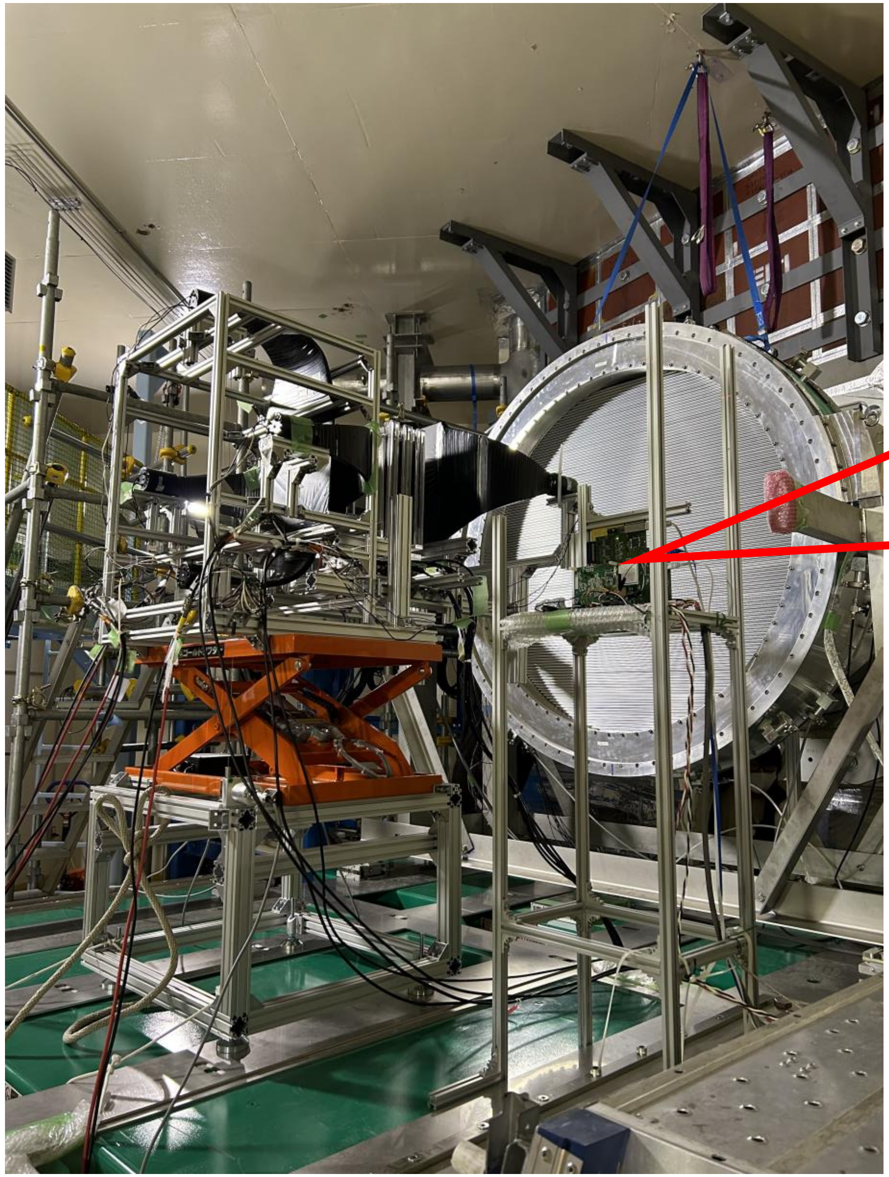
Leakage current were measured during irradiation.

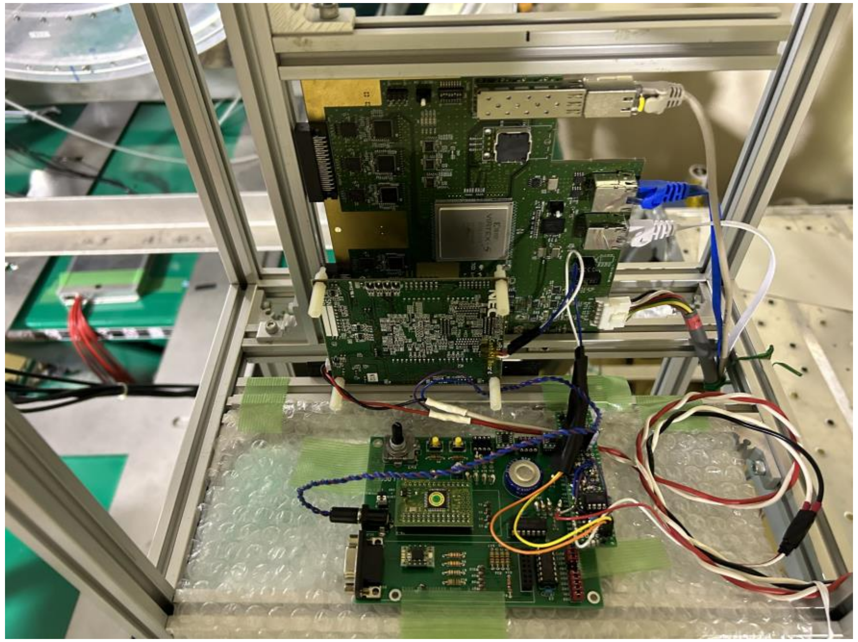


NO change was seen up to 6 kGy.

After 6 kGy, leakage current increased slightly due to degradation in CMOS.

Demonstration at experimental environment





AS-FPGA operation was tested in COMET first beam environment.

Successfully operated!

Feasibility

- It was found that AS-FPGA had potential to use for future experiment.
  - No SEUs up to at least 10^{11} n/cm^2.
  - No DDDs up to at least 10^{14} n/cm^2.
  - No TIDs up to at least 10 kGy.

examples of SEU rate for some FPGAs
(Y. Nakazawa et al., NIMA 936 (2019) 351)

Table 1

Summary of soft error rates and ratios of re-downloading time and total measurement time. The BRAM MBE rates of Artix-7[1] and Kintex-7 were not estimated due to low statistics. The CRAM URE rates in the COMET experiment were estimated by using the neutron fluence of 1×10^{12} neutron/cm^2.

	CRAM		BRAM		CRAM URE rate in COMET [h^{-1}]	Dead time
	SEU [[n/cm^2]$^{-1}$]	URE [[n/cm^2]$^{-1}$]	SEU [n/cm^2]$^{-1}$ kB^{-1}	MBE [[n/cm^2]$^{-1}$ kB^{-1}]		
Virtex-5	$(4.6 \pm 1.4) \times 10^{-8}$	$(1.4 \pm 0.4) \times 10^{-10}$	$(7.0 \pm 2.2) \times 10^{-11}$	$(9.7 \pm 3.1) \times 10^{-13}$	1/27	0.024%
Artix-7[1]	$(3.4 \pm 1.0) \times 10^{-8}$	$(1.2 \pm 0.4) \times 10^{-11}$	$(7.6 \pm 2.3) \times 10^{-12}$		1/30	0.034%
Artix-7[2]	$(2.9 \pm 0.9) \times 10^{-8}$	$(5.4 \pm 1.7) \times 10^{-11}$	$(7.0 \pm 2.3) \times 10^{-12}$	$(1.4 \pm 0.6) \times 10^{-12}$	1/67	0.031%
Kintex-7	$(2.6 \pm 0.8) \times 10^{-8}$	$(5.7 \pm 1.8) \times 10^{-11}$	$(8.7 \pm 2.7) \times 10^{-12}$		1/64	0.011%

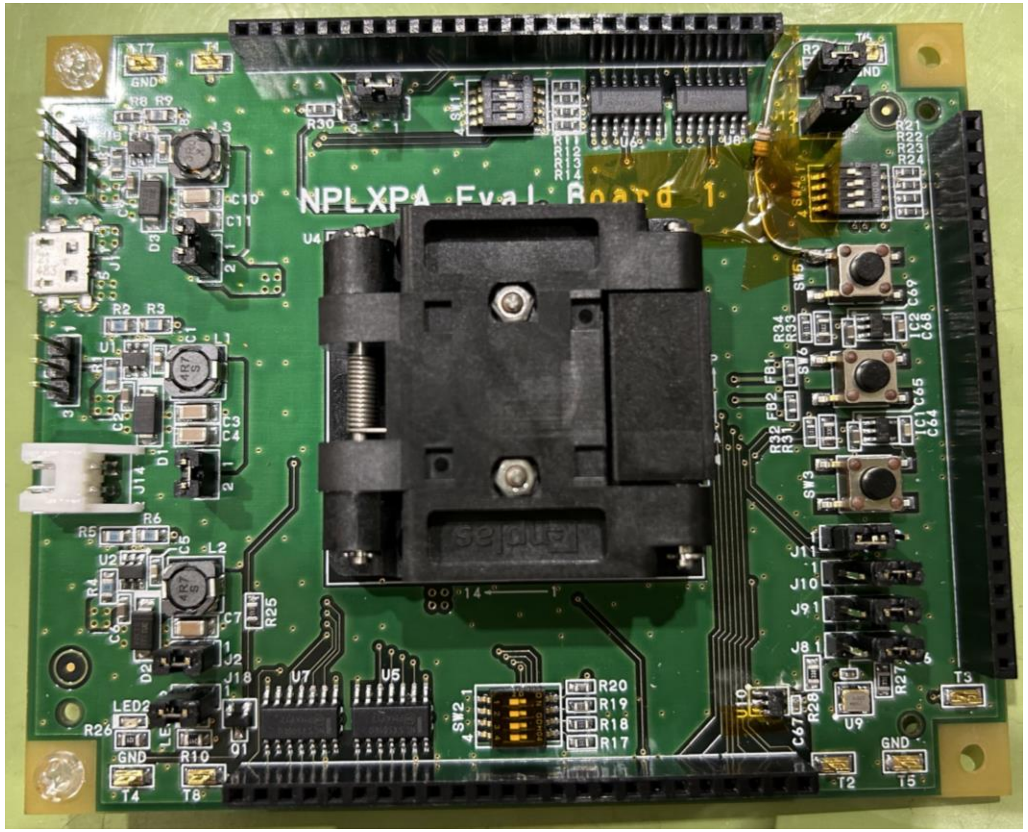
- More irradiation tests with higher level are needed.
- Usability check is important.

  -> Development of Slow-Control board.

Slow-Control (evaluation) board

Purpose

- Develop Slow-Control device
- Evaluate functions as FPGA under high radiation environment.
- Provide feedback for development of program tool.



Slow-Control board

- General I/O
- LED
- Switch

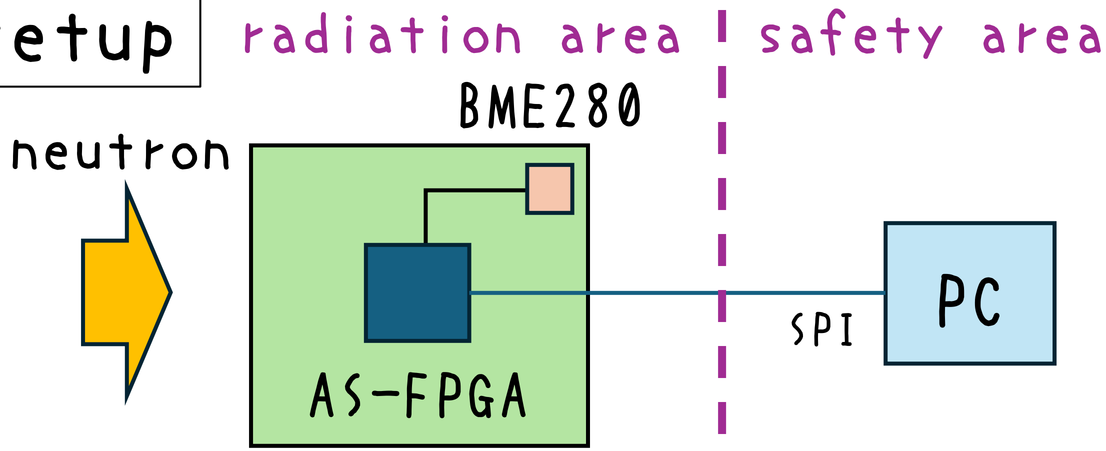
general environmental sensor can be easily connected.

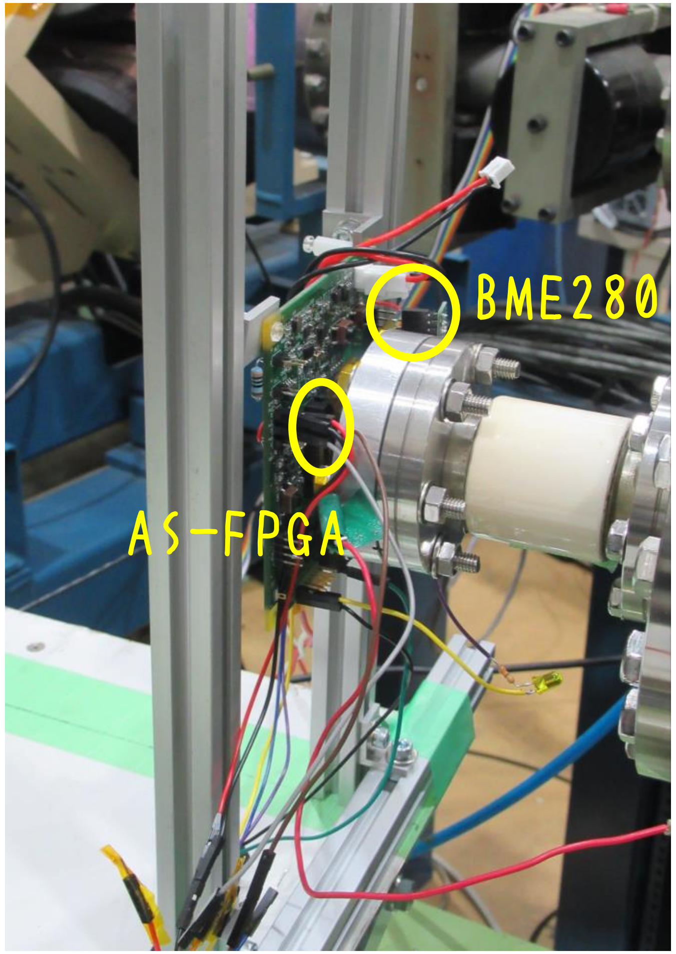
Neutron irradiation test

Environment monitor test @ Kobe Univ.

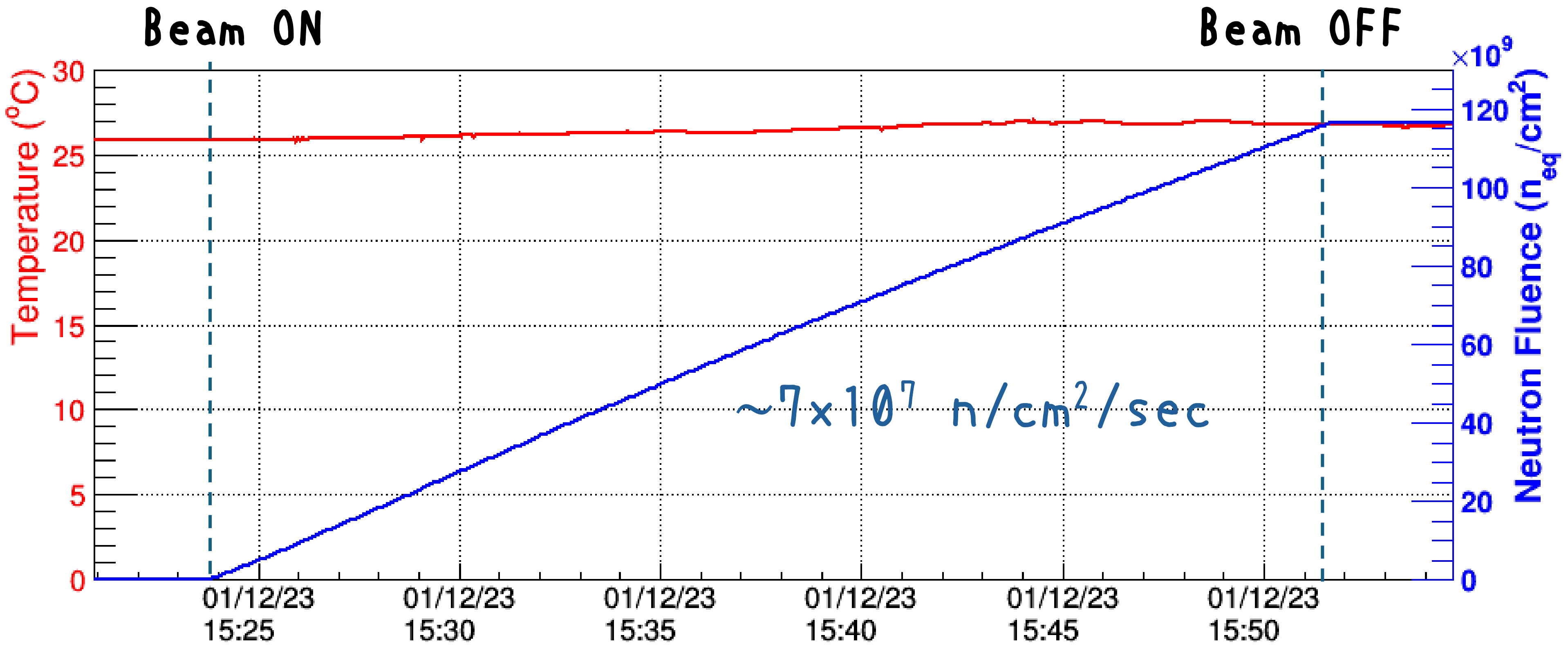
- Bosch BME280 (temperature sensor) was connected.
  - rad-hard up to > 10^{12} n/cm^2.
- Simple logic was implemented.
- Operation test at high radiation environment was performed.

setup





Result



We have **successfully** operated the "Slow-Control board" and taken data under the high radiation environment!

Summary

- Countermeasure against radiation is important for future accelerator experiment.
- AS-FPGA is the one of the candidates.
- Feasibility check was done using neutrons and gamma-rays.
- Slow-Control board using AS-FPGA was developed.
- Operation test under the high radiation environment was successfully done.

future work

- More irradiation tests with higher radiation level are needed.
- Program tool will be developed.
- Fast signal handling will be considered.