





# System Design and Prototyping of the CMS Level-1 Calorimeter Trigger at the High-Luminosity LHC

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24th IEEE Real Time Conference - ICISE, Quy Nhon, Vietnam

Date: 25 April 2024

# Talk in 23<sup>rd</sup> Real Time Conference:



https://ieeexplore.ieee.org/document/10049675

Stems 8

System Design and Prototyping for the CMS Level-1 Trigger .... at the High-Luminosity LHC

**Oral Presentation** 

**()** 20m

Speaker

KUMAR, Piyush (University of Hyderabad, India)

DAQ System & Trigger - I

# **High Luminosity LHC and Phase-2 Upgrade**

### □ High Luminosity LHC

- Higher the luminosity: the more data the experiments can gather.
- □ Helps in the searches of new physics.
- **Phase-1**: Current CMS architecture and data taking.
- Phase-2: architecture during HL-LHC, proposed to be start during year 2029 and onwards.

### L1 trigger upgrade:

- More granular information
  - **25 times increment for calorimeter trigger.**
- □ Advanced and more complex algorithms.
- Usage of:
  - Large FPGAs.
  - High-speed optical links (25 Gbps).
- Latency: 12.5 μs
- □ Replacement of electronics infrastructure
  - □ from µTCA to ATCA [7] standard
    - Rack
    - Crate
    - Board

# Summary of CMS HL-LHC Upgrades

![](_page_2_Figure_20.jpeg)

[Ref: 1]

# **Trigger system**

- □ At design parameters the LHC produces:
  - □ ~billions of events per second in CMS detectors.
  - Corresponds to petabyte of data per second.
- **D** Problem:
  - □ It is impossible to store and process this large amount of data.
  - Most of the events are not interesting.
- □ Solution:
  - a drastic rate reduction must be achieved.
    - TRIGGER SYSTEM.
- Two level of triggering strategy
  - Level-1 (Hardware): 40 MHz to 750 kHz
  - High level trigger (Software): 750 kHz to 7.5 kHz.
- D Phase-2 Level-1 Trigger
  - □ Processing CMS three sub-detector system.
    - Calorimeter
    - Tracker (First time inclusion in the system)
    - Muon system
- □ Final decision by global trigger (GT).

![](_page_3_Figure_19.jpeg)

# **CMS L1 trigger - a hardware perspective**

![](_page_4_Figure_1.jpeg)

CMS detector and Front-end electronics

![](_page_4_Picture_3.jpeg)

Backend and trigger system at CMS USC: electronic rack hosting multiple crate

![](_page_4_Figure_5.jpeg)

**Trigger algorithm on FPGA** 

![](_page_4_Picture_7.jpeg)

Crate hosting 12 APx FPGA boards

![](_page_4_Picture_9.jpeg)

APx FPGA board

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# **APx Philosophy**

- Aim is to provide generic trigger processing board to fulfill the requirement of Phase-2 in terms of
   Computational power
  - Computational power.
  - □ High bandwidth.
- Designed at University of Wisconsin.
- Features single FPGA as the main processing element.
- APd1 First demonstrator board.
  Based on XCVU9P FPGA (3 SLR)
   SLR: Silicon logic region
  - [Ref: 8]
  - Support 100 of 25 Gbps optical links for algorithm.
- SLR division and links capacity of the APd1 board have larger design implication.

![](_page_5_Picture_10.jpeg)

APd1 board [Ref: 2]

![](_page_5_Figure_12.jpeg)

## **Phase-2 Level-1 Calorimeter Trigger Architecture**

□ Two level architecture.

- Regional calorimeter trigger (RCT).
- Global calorimeter trigger (GCT).
- Proposed to implement using 46 APx boards.
- □ The levels are further subdivided into three layers.
  - Layer-1
    - RCT: 36 APx boards.
  - Layer-2
    - GCT barrel: 3 APx boards.
    - GCT endcap: 6 APx boards.

Layer-3

- GCT sum: 1 APx boards
- Latency requirement:
  - Output to correlator trigger: 3 µs
  - Output to global trigger: 4 µs
- Device Utilization: < 50%
- Main feature: Identical division of the calorimeter detector.
  - Can be prototyped using only 4 boards.

![](_page_6_Figure_19.jpeg)

# **Calorimeter Trigger Objects**

- The L1 trigger algorithms are developed to identify physics objects, i.e., electrons, photons, hadrons (jets) and missing transverse energy (MET).
- Electromagnetic and hadrons particles interact differently in the calorimeter.
  - Different clustering scheme
    - Different cluster sizes

![](_page_7_Figure_5.jpeg)

# Major Design and Prototyping Constraints

![](_page_8_Picture_1.jpeg)

- Algorithm
- Data transmissions.

## Utilization

Device utilization is preferred to be low < 50%.</p>

□ 10 years of operations.

- Input/Output constraints
- 100 links available in APd1
- Decides the algorithm processing region.
- The transceivers (MGTs) are distributed throughout the FPGA.
  - Algorithm require early partitioning and floorplanning.

![](_page_8_Figure_12.jpeg)

![](_page_8_Picture_13.jpeg)

## Two important cases in Prototyping

## Case-1:

Algorithm can cover the detector in identical region with one region require > 100 links

## Case-2:

- Algorithm can process a detector region using < 100 links.</p>
- However, the algorithm coverage is not identical.
- Need to develop multiple algorithm.
- □ Making prototype difficult.
- Need to find a balance between detector coverage, required links, and identical division.
  - □ Make prototyping easier.

# **RCT region coverage**

![](_page_9_Picture_1.jpeg)

![](_page_9_Figure_2.jpeg)

## **Regional Calorimeter Trigger (RCT) Prototyping**

- RCT v2.0 functionality is subdivided into three individual IPs
   IP1
- Implementation in 2 SLRs.
  SLR2
  - SLR1
- The HCAL towers information at IP3.
- Bitstream is successfully tested
  - Using LHC events (standalone mode)
  - □ 3 unique physics events.

![](_page_10_Figure_10.jpeg)

![](_page_10_Figure_11.jpeg)

![](_page_10_Figure_12.jpeg)

LUT	16%
FF	13%
F <sub>MAX</sub>	361 MHz

## **GCT Barrel**

Process 16 RCT boards.

□ Functionality division (SLR2 and SLR0):

IP1

IP2

 A time-slice module developed in VHDL for sending the data to correlator trigger.

□ SLR1:

□ CaloObject algorithm

Jets

- Taus
- Partial MET

□ Input: 64 links

Latency: 692 ns.

• Output:

- □ 48 links to correlator trigger
- G links to GCT sum board
- Bitfile is generated and tested with LHC events of test vector.

![](_page_11_Figure_16.jpeg)

## **GCT Endcap**

- HGCAL backend sends detector information in 18 time-slices (TM18).
  - Algorithm at calorimeter trigger runs without any time-multiplexing (TM1).
  - Demultiplexing (TM18 => TM1) is required before GCT endcap algorithm.
- DEMUX algorithm is developed in VHDL
  - serving two time slices per SLR.
  - **Reduces the utilization by half.**
- Prototyping one SLR can easily scale to one board
  - One board can easily scale to 6 boards.
  - □ Make prototyping faster.
- Floor planned in two separate regions to reduce the net delays
  - DEMUX: 2 clock regions
  - □ Jet algorithm: 6 clock regions
- Bitfile is tested for multiple LHC events.

![](_page_12_Figure_14.jpeg)

![](_page_12_Picture_15.jpeg)

Algorithm post Prototyping	Utilization and F <sub>MAX</sub>
LUT	6%
FF	7%
F <sub>MAX</sub>	360 MHz

Latency: 661 ns

# **Prototyping Calorimeter Trigger System**

<mark>Board to</mark> Board	Latency in µS (budget)
RCT => GCT barrel	1.8 (3)
RCT => GCT barrel, endcap => GCT SUM	2.4 (4)

![](_page_13_Picture_2.jpeg)

- Prototyping of the complete CALO system using 4 APd1 board.
- □ The boards are aligned with MC input pattern filled at
  - ECAL Crystals and HCAL towers: input buffers of RCT board
  - HGCAL tower and clusters: input buffers of GCT endcap board.
- Output is captured at GCT SUM and matches with
  MC == HLS == RTL == Bitfile

![](_page_13_Figure_8.jpeg)

# Summary

- An architecture of Phase-2 calorimeter trigger is proposed which uses 46 APx FPGA boards.
- The architecture comprises two level and further sub-divided in three layers.
- Algorithms are developed for all board flavors which satisfies the main constraint of latency and utilization.
- Algorithms are tested and validated on APd1 board.
  MC == HLS == RTL == Bitfile
- □ Following are the multi-board tests are performed and validated successfully.
  - $\Box$  2 board test: RCT v2.0 => GCT barrel
  - □ 3 board test: GCT barrel, GCT endcap => GCT sum
  - □ 4 board test: RCT, GCT barrel, GCT endcap, GCT sum.
- With availability of algorithms prototyped at each layer and input test vectors, entire Phase-2 calorimeter trigger is prototyped using 4 APd1 boards and 16 optical links.

## References

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- [2] The Phase-2 Upgrade of the CMS Level-1 Trigger. (2020). [Techreport]. CERN. https://cds.cern.ch/record/2714892.
- [3] Dris, Stefanos & Foudas, C & Troska, J.. (2010). Performance of the CMS Tracker Optical Links and Future Upgrade Using Bandwidth Efficient Digital Modulation.
- □ [4] Julia Handl. Jet Energy Calibration of the CMS Detector with  $Z(\rightarrow e+e) + Jet$  Events at  $\sqrt{s} = 13$  TeV, 2016.
- □ [5] https://home.cern/resources/image/experiments/cms-images-gallery
- □ [6] https://en.wikipedia.org/wiki/Large\_Hadron\_Collider
- [7] https://www.picmg.org/openstandards/advancedtca/
- [8] https://docs.xilinx.com/v/u/en-US/wp380\_Stacked\_Silicon\_Interconnect\_Technology

# THANK YOU...

# BACKUP....

# **GCT sum Prototyping**

- □ Final layer of the calorimeter trigger
- Combine all the information of the calorimeter trigger.
- □ Re-assemble the data according to the global trigger requirements and send it in six time slices (TM6).
- 32 input links
  - □ 8 x Three GCT barrel board.
  - □ 8 from GCT endcap board.
- Calculate the final MET
  - Using CORDIC algorithm.
    - 🖵 cosφ
    - **Ω** sinφ
- □ 6 output links.

![](_page_18_Picture_12.jpeg)

Algo component	Latency (clock cycles)
CORDIC	29

	Utilization and F <sub>MAX</sub>
LUT	5%
FF	4%
DSP	4%
F <sub>MAX</sub>	365 MHz

71,V0X	AIYIA	X2Y14	¥5714	Х <b>47]4</b> (Л	L <u>R</u> 2
170X	X IY13	X2Y19	21/2X	X4713	21x5X
χ0Υ12	21.A.1.X	X2Y12	21./2X	21.A.P.X	21.45.X
170X	11/17	X2Y1)	11,2X	X4711	11.45.X
0170X	01.41X	X2Y10	01.42 X	X4Y10	01.45 X
67 <b>0</b> Х	641X	Х2Ү9	642 X	Х4Ү9 00	KSY Sx
8Y0X°	841X	Х2Ү8	842 X	X4Y8	X5Y8
хоү	XIYI	X2Y7	XZYJ	X4Y7	X5Y7
χογε	541X	X2Y6	942 X	Х4Үб	X5Y6
ZOY	5.1X	X2Y5	5.42 X	X4Y5	XSYS
X0Y4	¥174	Х2Ү4	¥374	Х4Y4 00	XSX 199
хоүз	SXIX	X2Y3	2,42	X4Y3	X5Y3
X0Y2	2717				X5Y2
τλοχ	tary				Max.
хоус	DATE				Diana's

GCT Sum including CORDIC

# **RCT and GCT barrel region coverage**

![](_page_19_Figure_1.jpeg)

## **Design flow**

![](_page_20_Figure_1.jpeg)

# CMS Phase-2 L1 Calorimeter trigger

Processing four calorimeter subsystem

Electromagnetic calorimeter (ECAL).

□ Hadronic calorimeter (HCAL).

□ Forward hadronic (HF).

 High-granularity calorimeter (HGCAL).

Implemented in two level

 Regional calorimeter trigger (RCT)

Global calorimeter trigger (GCT).

Further sub-divided in three layers.

![](_page_21_Figure_10.jpeg)

# **Regional Calorimeter Trigger (RCT)**

- Algorithm summary:
  - IP1:
    - Prepare clusters and towers
  - □ IP2:
    - **Cluster merging**
    - Sorting of clusters
  - IP3
    - □ Final stitching
    - □ Final sorting
    - ECAL and HCAL merging.

![](_page_22_Figure_11.jpeg)

IP1 performs the stitching of the RCT region

 Latency of the algorithm in all the direction
 3 clock cycles

Create full tower
 information.
 Cluster + tower

Full tower latency: 2 clock cycles.

![](_page_23_Figure_5.jpeg)

# **IP2: PF Clustering**

□ Input: Full tower of 10 RCT region.

### □ Procedure:

□ Creating overlapping region □ 17x4 -> 21x8

- Finding peak tower in 21x8 region.
- Calculating 3x3 PF cluster energy.
- Removing the peak tower for next iteration
- Repeating the steps eight times.
- Output: 48 PF cluster in 6 RCT boards.
- Latency of making eight PF cluster:
  80 clock cycle.

			_	 _	_	_	_		_			_			
Latency (clock cycles)	η													3x3 PF clust	e
3															
3															
2															
80															
114	0-33														
Utilization and F <sub>MAX</sub>		-													
30%															
18%														↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓	<mark>│</mark>
360 MHz														8	
		Į													
		-				0	-19	)			Ċ	Þ	•		

21

Algo component

Stitching in eta

Stitching in phi

48 PF clusters

Total latency

LUT

FF

 $\mathsf{F}_{\mathsf{MAX}}$ 

Full towers

# Jet and tau algorithm

□ Input: Full tower of 16 RCT region (34 x 32).

Subdivided in two half (positive and negative eta).

 Uses supertower methodology to reduce the geometry in threefold.

Supertower: group of 3x3 tower.

 $\Box$  34x32 tower region =>:

 $\square$  +  $\eta$ : 12 x 8 supertowers: 6 jets

- η: 12 x 8 supertowers: 6 jets

One jet region: 9x9 in tower3x3 in supertower.

	<mark>Algo</mark> component	Latency (clock cycles)	Jet cluster	•
;	Making two 8x12 supertower	2		
)-	Finding peak supertower in the bin of 12	3		8 n
	Making 3x3 jet around the peak	3		
	Total latency	99		
		Utilization and F <sub>MAX</sub>		Ļ
	LUT	7%	12Φ \	
	FF	5%	\ Peak supertower	
	F <sub>MAX</sub>	367 MHz	Latency one Jet:12 clock cycles	26

# **GCT Endcap**

- Prepare jet and taus cluster.
- □ Internal input links: 108
- Geometry: 20 x 72 endcap towers
- Create supertower for jet calculation
  - **2**0x72 => 6x24
- $\hfill\square$  Jet calculation step
  - Finding peak in the region of 6x24
  - Calculating jet cluster of size 3x3 around the peak
  - Removing the peak for next iteration
- Total 6 jets
- Output: 4 links

Algo component	Latency (clock cycles)
Making 6x24 supertower	9
Making jet and removing the peak	20
Total latency of Jet and taus algorithm	146

DEMUX + Jet	Utilization and F <sub>MAX</sub>
LUT	6%
FF	8%
F <sub>MAX, DEMUX</sub> F <sub>MAX, Jet</sub>	384 MHz 361 MHz

![](_page_26_Figure_14.jpeg)

- The SSI technology integrate multiple Super Logic Region (SLR) components placed on a passive Silicon Interposer (fig 3).
- Each SLR contains the active circuitry common to most Xilinx FPGA (Field programmable gate array) devices. This circuitry includes large numbers of:
  - 6-input LUTs (Look-up tables)
  - Registers
  - I/O components
  - Gigabit Transceivers (GT)
  - Block memory
  - DSP blocks
  - Other blocks
- The device we are using for our synthesis and implementation is based on Xilinx SSI technology and support three SLRs.
  - Xilinx Virtex UltraScale+ xcvu9p flgc2104-
    - 1-e FPGA

#### Xilinx Stacked Silicon Interconnect (SSI) Technology

![](_page_27_Figure_13.jpeg)

Fig 3: Xilinx FPGA Enabled by SSI Technology\*

\*: UG872 Large FPGA Methodology Guide

# Key design challenges...

- Throughput is increasing almost 9 times (0.28 to 2.41 Tbps) per board compared to the Phase-1 system.
  - Tackled by employing high-end FPGA devices such as XCVU9P: can handle 3.93 Tbps of bandwidth.
- However, the device capability in terms of logic performance, serial bandwidth, and on-chip memory are not scaling in the same fashion.

![](_page_28_Figure_4.jpeg)

# ATCA

- Board total Area ~140 in<sup>2</sup> (~12.68" x 11.02")
- □ Size advantage over microTCA
  - 50% more area, 100% more front panel
- Power and associated Cooling advantage over microTCA
  - □ 400% more available power.
- Crate: the 12U (U is rack unit equivalent to 1.75 inches) tall chassis delivers power, backplane connectivity, cooling, and the slots to maintain up to 16 boards.
- Rack: A rack (generally 46U high) delivers a rigid framework abiding up to three shelves.

# APd1

- Controls in the APx are provided by the IPMC and the ELM. The IPMC board is responsible for crate power on/off control
- □ IPMC also communicate with the crate IPM controller, known as the Shelf Manager.
- Once booted, the ELM Linux system provides configuration and operational support for the platform. This includes initialization of FPGAs
- (bitfile loading and register/memory initialization) and configuration of support devices such as Firefly optical modules

# **Phase-1 Architecture and its Drawback**

- Current architecture support 6.4 Gbps of link bandwidth which is insufficient to handle the 25 times increase in input granularity.
- □ The current architecture lack the support for the new radiation hardened HGCAL trigger.
- □ The FPGA in CTP7 board viz. Xilinx Virtex-7 is unable to satisfy the demand of the Phase-2 calorimeter trigger
  - □ which requires additional MGTs with high bandwidth
  - more logic capacity in terms of
    - LUTs
    - **FF** and
    - DSPs
- On the algorithm side, the current system works over the tower's granularity
  - requires redesigning to work on more precise input, such as ECAL crystals.
  - The current doesn't support the particle-flow (PF) clustering vital for the PF algorithm at the correlator trigger.

# **Phase-1 Architecture and its Drawback**

- □ Input primitives: ECAL, HCAL, and HF tower
- □ Input bandwidth of 6.4 Gbps.
- Organized in two layer
  - Calo Layer-1 using 18 Calorimeter Trigger
    Processor board (CTP7).
  - Calo Layer-2 using 10 Master Processor (MP7) board.
- Layer-1 adopted the regional architecture approach
  - Each board process one phi segment of the detector.
  - Employs identical algorithm.
- Layer-2 adopted the TM approach and works in TMUX9 scheme.
  - One MP7 board for demultiplexing before sending the final output to GT.

![](_page_32_Figure_11.jpeg)

# **Architecture choices**

## Regional approach

- FPGA boards parallelly process the detector geometry (a segment of the detector) to every bunch-crossing.
- Each board employ similar algorithms.
- May require sharing of data between the FPGAs to process the overlapping region.

![](_page_33_Figure_5.jpeg)

## Time-multiplexing (TM)

- □ FPGA boards run identical/different algorithms on different time slice.
- The TMUXN (where N is a natural number) denotes the round-robin scheduling interval of the trigger processing board.
- Requirement for data duplication can be eradicated.
- □ The data arrive and are processed over a more extended time than the regional approach.

## Design flow – from emulator to hardware

- The trigger algorithms are implemented by using a high-level synthesis tool
  - Rapid prototyping
  - □ Codes are written in C++
  - □ HLS Synthesis: generate the HDL
- Provide of latency and very early estimate of resource utilization
- Can implement (place and route) the design without any pin constraint.

Integration of the algo with the APx firmware shell (FS) that provides

- Serial link instantiation (MGT hard block).
- □ LHC clock connectivity
  - Trigger timing and control distribution (TCDS)
- □ AXI interface to the controlling system
- □ Support to test and ILA debug the design
  - Playback (input) and capture (output) long buffer
  - Able to emulate 113 bunch-crossing of LHC data.

### ALGO

#### Performance Estimates

### Timing (ns)

### Summary

Clock Target Estimated Uncertainty ap\_clk 4.17 2.917 1.25

### Latency (clock cycles)

### Summary

Late	ency	Inte	erval	Type		
min	max	min	max	Туре		
158	158	6	6	function		

Summary					
Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	520	-
FIFO	-	-	-	-	-
Instance	0	0	280881	397283	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	12656	-
Register	0	-	7808	512	-
Total	0	0	288689	410971	0
Available	4320	6840	2364480	1182240	960
Available SLR	1440	2280	788160	394080	320
Utilization (%)	0	0	12	34	0
Utilization SLR (%)	0	0	36	104	0

![](_page_34_Figure_24.jpeg)

# **RCT v2.0 IP1**

- □ Primary cluster function
  - Region: 19x24
  - Creating 3x5, 2x5, and 5x5 cluster
  - This computation is done by calculating the energy of the five strips in the eta direction
  - As the peak position can be arbitrary in the crystal space
  - □ The overall latency is 6 clock cycles.

![](_page_35_Figure_7.jpeg)

# **RCT v2.0 IP2**

- □ A 16-input bitonic sorting unit is used.
- **10 CAE level**.
- Considering the unit is pipelined such that the individual stage takes one clock cycle, it can render the sorted results in 10 clock cycles and can initiate a new sort each cycle

![](_page_36_Figure_4.jpeg)

# IP2

### Two output links

## Each output link carries

- □ 18 towers and
- **3** cluster information
- The latency measured for IP2 is 62 clock cycles.

Standalone implementation results	<mark>Algo component</mark>	Latency (clock cycles)	Algorithm post place and route	Utilization and F <sub>MAX</sub>
$\Box$ LUTs: 3%	Stitching clusters	4	LUT	3%
☐ FFS: 2%			FF	2%
	16 input bitonic sort	9	F <sub>MAX</sub>	368 MHz
	Total latency	62		

# IP3

- Receives the information from the IP2 of both the subregions and HCAL towers.
- Perform the stitching of the clusters at the central eta boundary
- Sort the 12 clusters from both the sub-regions using the *bitonic sort* algorithm.
- The final merging of the ECAL and HCAL tower is
- Packs 4 output links to the GCT.
  With 17 towers and 2 clusters of information per link.

![](_page_38_Figure_6.jpeg)

# **RCT v2.0 IP3**

- The merging of ECAL and HCAL also includes the calculation of H/E.
  HCAL and ECAL energy ratio.
- □ The H/E calculation is stored in 4-bit.
- The LBS bit indicates the possibility that either the ECAL or HCAL energies are zero or

Algorithm

place and

LUT

FF

 $F_{MAX}$ 

- HCAL energy is greater than or equal to the corresponding ECAL tower energy.
- A logarithmic scale is employed
  - cover a wide range of differences between the HCAL and ECAL energy profiles
- Packs 4 output links to the GCT. With 17 towers and 2 clusters of information per link.

post route	Utilization and F <sub>MAX</sub>	Algo component	cycles)		
		Stitching clusters	23		
	5%	Cluster merging with tower	72		
	4%	Bitonic sorting	9		
364 MHz		HCAL and ECAL merging with H/E calculation	8		
		Total latency	125		

Latonov (alook

<mark>Algo component</mark>	Latency (clock cycles) and F <sub>MAX</sub>	Algorithm post place and route	<b>Utilization</b>	
104	450	IP1 LUTs	24%	
IP1 Emax	152 364 MHz	FFs	14%	
IP2 F <sub>MAX</sub>	64 368 MHz	IP2 LUTs FFs	3% 2%	
IP3 F <sub>MAX</sub>	125 364 MHz	IP3 LUTs FFs	5% 4%	

# **Global Calorimeter Trigger (GCT) Barrel**

![](_page_41_Figure_1.jpeg)

# **Global Calorimeter Trigger (GCT) Endcap**

![](_page_42_Figure_1.jpeg)

# Continue...

VHDL based design

### 360 MHz clock with 9 words / BX

		8	c	D	1	,	a	н				1	м
1	link_in_0	link_in_1	link_in_2	link_in_3	link_in_4	link_in_5		link_out_0	link_out_1	link_out_2	link_out_3	link_out_4	link_out_5
2	(	1	) (			) 0			0	0	0	0 0	0
3	EEB48B1652708229	E90C01F0BBA779F	D45D6AC3FFF4C66D	A23C28FBE47C7E98	000060E0B2B83F5F	F6612F6C642482AF		EEB48B%52708239		b	0	0 0	0
4	4D24A32209408A4B	<b>BFIECAAEBAF3IC69</b>	EBBISTIDEIHBBID	E5C44E10019E1527	0026349E8368E0C7	96FA83AF60AA4EBE		4D24A32209408A4B	3	0	0	o o	0
5	07N2AD2E3EFC8244	BE47964B4D3A0E71	200E59971DC19261	10 State 252574F7B	BIOSCBA67EEIDED2	300200733E6EB3C1		0762/001L/RFC8244		þ	0	0 0	0
6	D597CAD5600FCDEA	36FC75F39B24DC2E	2D873C92062870	72F, 773C31E1EICE	ED76F44A1E32A26D	7F5DFBAB07A9AA89		D597EAD500FCDEA		0	0	0 0	0
1	E7846AB1C47E2B48	FB5E7DBDB3AB110C	CABADENI00444	C-09073E2570607D	DADE731885983379	MJA93BAD42FC9ID		E7046457847E2B40		þ.	0	0 0	0
8	B771C2D4B1FAC6F9	B%D53D8EA7B5DBB	0272A754E775A556	6BB16BA6F3E2FE38	986EC97EA66C0C45	F8613CA4B29AB728		B771C294RIFAC6F9		0	0	o o	0
3	B383AA6C44F36DIF	2B4E1536BDCEF1F5	2B6BBB3B10AD8EAC	4E380AF439C3E4B8	6BAB717FD44FCSE3	0FA8F233483882DF		B383LACAF36DIF		0	0	0 0	0
10	7A027F6F3CC4832E	F9E2290FCBF09C%	4FID0CFD2CBE585C	F44A245FA8D5726D	2A18877B4F1DAE16	3A3FB7994FtAE88C		7A023-9F3LC4832E	the second s	0	0	0 0	0
11	552401A166084971	1881B3E01F57C474	B055BD9CCEAA4683	4F1655C0789F3399	BIDB75BAAA47EHE	F24C6D664B726F2D			0 552405A366084971		0	0 0	0
12	BC781CA6B4D50B2A	6C5A0D5EE80EDC10	68/ECCA6/E726F3F	FE65A7B673937F70	DA6DD657B7FD09F0	5CF7872D9250882E		ENCONFORBA779F	BC7IIICA6B4D5DB2A		0	0 0	0
10	6B06BAD25EBNE7F	C83E2F7B652536BC	3EEB982350FN345	BF3B3753634F8F78	E9E62019B2B6BA22	090197490068441A		<b>BFECAAEBAF39C69</b>	6B06BAD258B90E7F		0	0 0	0
14	874277BE749C69AE	E32E31CE9A92FDID4	B5F61CDOC1960_C4	VA62C/54 AE0138893	CD2ED5BEC3D64A9B	0CB1IC399BD966AB		EE47964E4D3A0E71	874271EE74369AE		0	0 0	0
15	338F3A0E537222DF	C9B30A6AA2EAB052	B8FW2FA0F0D96FD	E20E7/F04668E54	9559CIDEAE2F67E2	D508C1DA83D86409		36FC7%F39B2IDC2E	338F3/885371220F		0	0 0	0
26	5803298FA058A716	C3CFF67E5C94AAB3	9CD154D8307C35	7720401007892496	4C474989A1853F66	3B3A6B4C035DB636		FB1E7DE0B3AB11BC	58D32-05-098A716		0	0 0	0
用.	D94A9207833DFCEB	7BF166C8236D1CF7	4E424202818CFDE4	I69CCC21D9C78891	SFEBA4A9FA366DF4	CD34980AF27654A4		ENCODOREA785088	DMARCOZECKEB		0	0 0	0
18	J218AD9DE7CCFB69	ABCF09147E10E609	D4C2B108B80C5F4D	ICF852823C28D865	E375B80EFA90E343	CD1C958464D54A6E		284E1536BDCEF1F5	3284 DECCFB69		0	0 0	0
13	EIB05125194F2144F	ACF24E453FE39FC5	EDFEC5957B87FCE3	3BF0097B3C129067	CFDC89AF7AD09079	8A8044CT3F96EEIF		F362230FC8F09C16	BB05F5584F944F		0	0 0	0
20	HCE255F4544F98E	80JEC80758566A99	765A8D5139AF1E34	SC&CF85C99BBA2F8	3A20AEDAC0C7B675	0C45AB6CE1EF0298			0 E88EE57C474	HCE250F4544F98E		9 0	0
21	37E0E6EEC39D36B6	275OF9F8A426BF9D	B6BEBBA62074E49D	A8738919AF9FFF2	8596B3C209CF22%	9C7DB19D8E5429DA		D41D6AC3FFF4C66D	6C5A0D5EE88EDC13	37E0E6EEC39D36E6		0 0	0
22	AEFFC497610CDDB0	C5923DA0FA688092	MA73RE2DERES	2299210043810610	F077FC52234D3E3E	85AF47E417BD30B8		EBBISTICEIMBBIO	C00E2F78652536BC	AEFFC 1610 COE0		0 0	0
22	D006395C579IAA3O	15130E1C14304M1	972C309C7B56E	AIAE8049999C3D	56A5ADEC76E447FE	719A976982D6EF1C		200E5997/DC9C268	E32E3ICE9A92FOD4	D000905C0790A3D		0 0	0
24	BA4C9E5FF5E4932F	AAFF70F740C65355	ODEBCOERE VERY 00	CONTRACTOR OF ADMINIST	DEIDHDEGAEDAE7E	MC6615DAC2D18DF		2D073C9206207008	C9830A6AA2EAB052	3A4C3E3FFTE4332F		0 0	0
25.	62AEE6337606DC9C	6814660E740342AD	42CAF 95234F38-0F7	FEFNERROCISICA	A0455F1A5D323FC5	012FECE53008E134		CABACETER0444388	C3CFF67E5C94AAB3	62AEEED CBDC9C		0 0	0
25	B4545FA682B1CA82	FEFA86CDFB37FD6A	ESCE2DE21EEE284	ASASODHDDFCE837	B32DB8EA49EEF6FF	354FB89681BAFF10		0272A754E775A556	7EF188C8236D9CF7	B4545FA202B1CA02		0 0	0
27	7A0FF7F021DEBB3E	0E8439E979E42%D	ECA7A8938E425977	STEDIE484ADDDAD	364C0630185A912C	E05D76AA7FASA276		2EREEBJENADREAC	ABCF09147E10E609	7A0FF/PP21DEBB3E		0 0	0
20	D0852F44850AE715	6CED3BA50CMF2C8	E692CB6A50DC3296	0238DB3A445386DA	28E5435008334416	BCF4039054CECD2A		4FID0CFD2CBES85C	ACF24E453FE39FC5	DOES2 HOUSE E715		0 0	0
29	J2650ABD7F3FEER6	BUIECONSURACARA	67D9C830F04F0523	34F 035676168E07A	CF882353E54675A	810FE7E2CE873087			0 EUSSECISCCEAA4603	BUECHD/50566A39	22850ABD/F 9FEB66		0
- 99	D4D8F20E940CA8D5	E25076F5E4EFE7C5	OF EFF F 50402E00996E	FC152895127U29-4P	AGE203AEU5425EGP	854D924FC30F0102		AZJC20PEE47C7E90	SEELUCASE/2019	275CF 9F 8A426EF 6D	D4DIF20E9DCAID5		
31	USF 320C7C78EF 094	63F23C7AIDEF1082	JJACC47EZASADE	8.9.73E770009E878F8	31948F A43A033F 24	68D24807B583D637		ESC44E100T9E1527	JEEE/982350P16345	CSS23DA0FA6BB032	L19F-328C-4C-77E-F-094		0
28	016F6A4FC7006716	7A40D2A3BCEB70A3	RE2234CCF7E28	00340404223999	40920243CEMP 92003	HUP OF COZEF 20CEF		E05063E252574F70	ESPERCEDC19602C4	INTEREST AND	ERFLATCING/R		0
20	35568E47C78C%C37	4PD70A900139DF6C	CASOSBOJEP 27 TRE	ALLOSE MODALATE	3E728D49EACDC331	70E SREAE MEDERAL		BI2PATTICIE BCB	BIP 1029 A0P 009CPD	AURP 70F 740C65355	20060E41.7E23C37	0.006-00	0
- 24	CONFIDENCEJENDEE	BCC2D574854CBE0	203887DEEELE 4	THILF SMOELIAATS	4C-62039LIA4ESIA46A	BC/D301966DB43AP		C709073E2570607D	SCURADISO/CSEJ	SEMSECE/40342/AD	CO/PTIESE AND COR		0
2	SILEEDL3//LIALP3A	ALB JOB 2 JANSOLICI	6B6FDC0D3FF3B0AD	DJCRENZERCJCPLURE	SUEDJJ24P ZUEBOBSZ	P 536B3CZAP 65CBD3		ADDREPART JE27 E38	4E4242020RCPDE4	PEPARICUPBJ/PDIA	SUBESCUP DELP 3M		0
	53D034303C4030P	4000000000000000	30300325807248	000/COEEDU0C20P0	PERIOCADOREDED	BUCK BUSH FOR THE		4EJBOAP 4JBLJE4EBB	D4C2BR0BB0C5F4D	0000000000000000	6300340360397		0
21	10/263107/2464/2408	SUSIOF OF INSCINOS	SSUB3407CF PASADF	TOAC MODERCOM	CLAMACUP 4PUS/DB	NORALIZEF 22105		PREASOP AUDITZED	SUPELSSS/BO/PCES	BLEDJERSOL HF2C6	3025315724640450	and the second s	0
2	DADESCEDIFUENZ	DECKSKACCENTANC	EDOADACCADDETAIR	210000000000000000000000000000000000000	01A0DEEDEEEEEE	THEFCADOTEDATECA		BOOK TEORODONENE	EFIELD TO 2007 10 10 10 10 10 10 10 10 10 10 10 10 10	DEDEDEDEACTOTAL AND	E MANUELE ADEE NOS	DADESCEDIO ADMETE	0
2	ADEADA THE REAL PROPERTY	4510103322555437	C2BAFEF74FF74FE20	AAAEODOADAMOEM	ETA SOTO TRESOLO	EXECUTAAD DODE DES		BOILDANDERGERONT	DESERTED ATOTAL	A THE PROPERTY AND	EDEDOCTA PETRICS	ADDA DAR OFFICIAL STREET	0
	ETACHARADOSADE	ANCADOMONDESO	EXCEPTION	E ADDERSONCEAT	EDSC AACOAADONES	A14/00/000000000000000000000000000000000		PROFESSION PROFESSION	EALITIELADONIGON	972C200C705600C0	TAAPDTA SECTORS	ETACINA DOUDE	0
1	DIOE HOCAASEASC?	SIDEAC 715A SEA SIDE	Shansher DE THE	ADAMERNANI	B2AEB936D9D6E87A	0000298948084387		EDNEALATENDAND	EEDOE27EDARCODIA	00749/25/00000000	AFFITTANDADODECC	CHOF THE MAR APPE	0
10	E50017824303E303	ADDASCAF9293981F	AIDREBBODEDATE	Acorden Statements	E752CD484ER08041	2020E2DEE2D2EE2		DADE218865983129	2220100002992456	ANCAENTIAESEDEE	BCC2CS34854CEED	ESCOUTE AND ACT	0
44	72698E84AD67DCER	COSSIBBITIONE AND	ANE INSPORTORIZED ANE	284/166495963000	FED5492338207A4F	B490307C3E9AD4B1		SISECSTEASSCOCAS	1590002909028891	BECENDE20EBE284	AFR15R2349950D23	726SEESEN PROCER	0.005-00
45	DE70034620846.6.18	TOTACA30ADOF ADDO	S22EBOCRA28CRDC	SPACED9423097954	OSC 9C 104469104DE	50506781EE A00418		EPAR717ED44ECSE3	100000000000000000000000000000000000000	ECA749938E426977	40000000000000000000000000000000000000	DE2D02162 PALATE	0
20	0941014CE20625E1	79957C5D10E9028A	0621720442045605	7114530129590204	E7ACC91E7EAA3675	TICEAOTECENAEDO		2A1002704F1DAF16	10E009701C129067	EESCERASODC128E	STIRNE OF 1450 4067	014101414 2062561	
47	0FE27600C0F3827E	B125504618ADACISE	10717017B891F2C7	2028480020909225	290DAR6615A34DBC	3264R3A4458603573		and the same same to the	0 REBISEAAA47F94F	SCREEKSCHIREA2ER	5709CR00F04F0522	9CRAD09D23ttF616	0FE27600D0F9627F
40	B0326B7BB0913C4	1E10108AEDCF2407	E2C23929960F1024	SED6520B0BCB3426	C654A18C22194823	1720CA26AABDEC30		FEEDFECRA2492AF	DAIDOS57B7FD09F0	AR7389BAF9FFF2	BFEFF50402E0994F	2850555966535436	B0326B7B64037C4
43	OF IF 830ED48EF 844	AD87B62A8E47A%	FCBAFED4175EBESt	91F801FA7B7E878C	F5D4676EA3478D79	BCBOBE ME0039658		SEF ABJAF 60AA4FBF	ESEK2019B2B6BA22	2709F79E43BIDE9D	335C47E2A66D805	453A1A322795F497	DEFENDED A44
10	DIAEF 4DIS6857482	F9005CC754%C822	CREDASE 605741CYC2	DEACAECESH70833	10C6734D0EA45647	8020B0B0DE10294		300200733E6EB3C1	CO2EDSBECODE4ASE	FAMBED4999923D	66E2234CCF7E2F11	AICC41009650E690	DRADE 4DRM 57482
-	FEDERALFEREN	6622F82CR0XCACEB	4810346843674515	COSCINCENED745	F05A033954A4F78C	SE27ES7ECBEBICES		2FSC/FBAB07A9AA89	1955CCCEAB2F67E2	E402EE655F409F2C	CASD//EDOBE2FEIRE	SICK4C7RA9EA38B	FEDERACIONE COMP
52	71088E834E960#75	BF2AC555C3HEB77	SALESIBEN FID	AS E AREADEA	D051ADBD94A90BAE	IDEDICEDIA76025		\$13A30BAD42FC98D	4C474389A1851F66	FEFH25IIDCN6CA	203887DEEEDE4CE2	ADDA5CAE9292683E	71D88E804E980F79
53	F9C4E620D4E03430	IA3DE9E8E80FE45D	FIACCCCHASE	AEN DIENSET	SECEE 1010F8E74323	CD7A9769F4C33A9F		FIEDCA4829AB728	SFEBAAASFA366DF4	ABANDHODFCES07	(BEFDC0D0FF9B04D	DDIVIDEB370C1E455	F9C4E8 00 4E0043D
54	F07DF5F68D68EEH	680EE293A4BE4C75	8153338434CF6159	0357438C1AC756E1	6B2BD06MAB5A8D9	C96AA87EC2E58D3D		0FA8F233483882DF	E375E80EFA90E343	95FEDIE484ADDDAD	383CD9325ED72419	IC7AC43A4B0FAD90	F87DF5 service E11
55	AC1989DF59DA7499	7F32B54E42230465	F6FD696F4C973A37	3CA99443D65FA5ID	BI9EDC4098EEAB41	505ED482A024E3043		SA3FB7994F1AE88C	CFDC89AF7AD39379	029ECE9A445386DA	89DE3407CF1A8ADF	78857C5D10E902BA	AC1989C 59DA7499
58	0195ACF44EE579DE	10348F8E25AED7BC	9733E66A973629C7	3D4A300B62AEDCA6	F6D9E2EC86B72189	54DAE4DDB72FD9E2		0195ACF44EE579D6	F24C8D684B728F2D	3A20AEDAC0C7B675	34F035876168E07A	2ETRID872FSEA02C	BUSSOAGISADACSE

Fig 2: RTL simulation

### Latency: 2 clock cycle

Implemented Timing Report

Utilization	Post-Synthes	is   Post-Im	plementation			
		Gr	aph   Table			
Resource	Utilization	Available	Utilization %			
LUT	6592	1182240	0.56			
FF	21162	2364480	0.89			
Timing		Setup   Ho	ld   Pulse Width			
Worst Negative	Slack (WNS):	0.154 ns				
Total Negative	Slack (TNS):	0 ns				
Number of Faili	ng Endpoints:	0				
Total Number o	f Endpoints:	21549				

### Fig 3: synthesis and implementation results

![](_page_43_Picture_7.jpeg)

# **Continue...**

![](_page_44_Figure_1.jpeg)

![](_page_44_Picture_2.jpeg)

# Continue...

- DEMUX code is developed in VHDL
  - 4 input links
  - 24 output links
  - Clock: 360 MHz
- A 2x1 MUX is used to select the input (BX0 and BX9) for the DEMUX IP using a "sel" signal
  - Sel 0: BX0
  - Sel 1: BX9

![](_page_45_Figure_8.jpeg)

![](_page_45_Picture_9.jpeg)