System Design and Prototyping of the CMS Level-1 Calorimeter Trigger at the High-Luminosity LHC

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System Design and Prototyping for the CMS Level-1 Trigger at the High-Luminosity LHC

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20m

Oral Presentation | Trigger Systems | DAQ System & Trigger - I

Speaker

KUMAR, Piyush (University of Hyderabad, India)

High Luminosity LHC and Phase-2 Upgrade

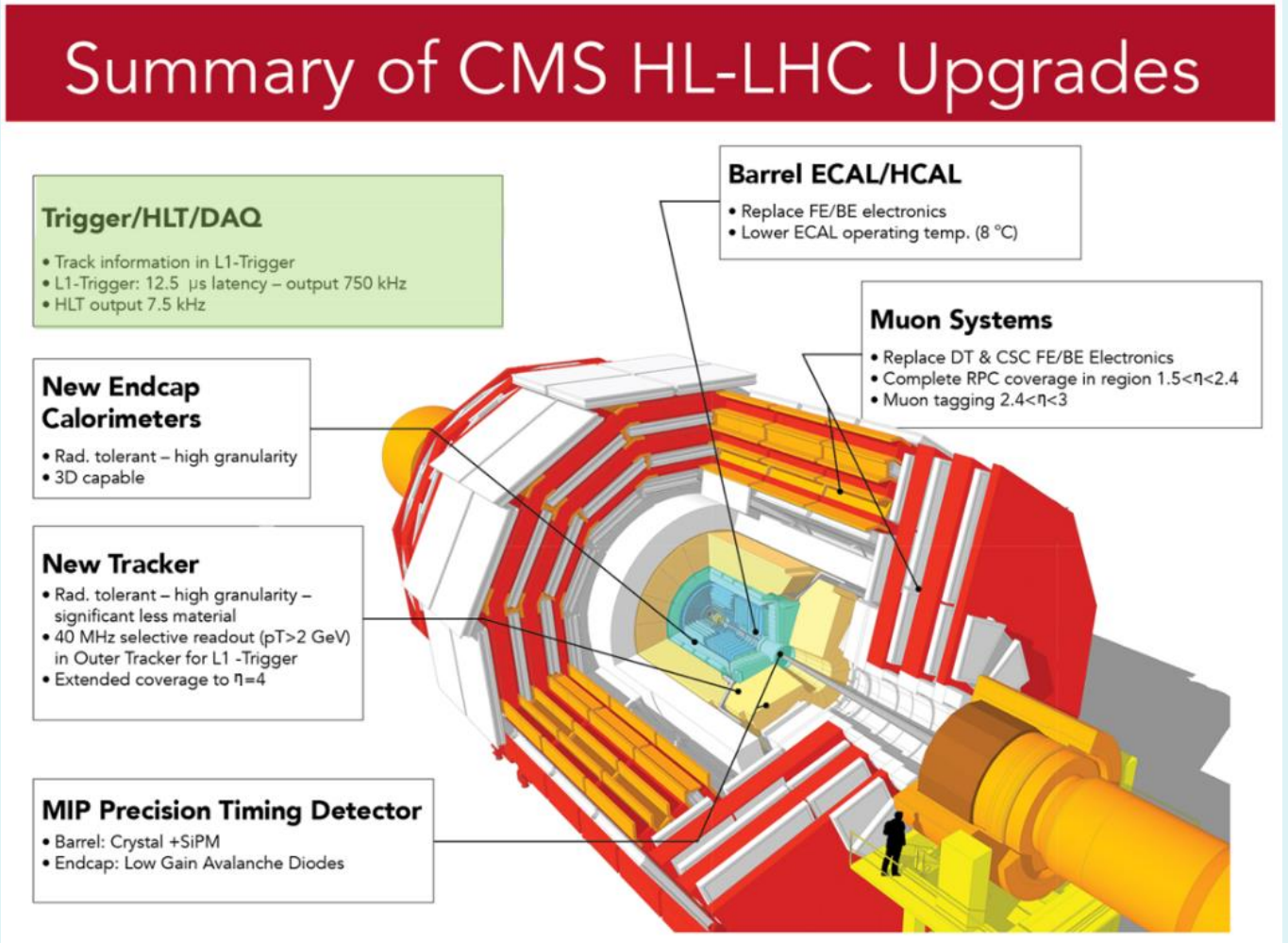
- **High Luminosity LHC**
  - Higher the luminosity: the more data the experiments can gather.
  - Helps in the searches of new physics.

- **Phase-1**: Current CMS architecture and data taking.

- **Phase-2: architecture during HL-LHC, proposed to be start during year 2029 and onwards.**

- L1 trigger upgrade:
  - More granular information
    - 25 times increment for calorimeter trigger.
  - Advanced and more complex algorithms.
  - Usage of:
    - Large FPGAs.
    - High-speed optical links (25 Gbps).
  - Latency: 12.5 μs

- Replacement of electronics infrastructure
  - from μTCA to ATCA [7] standard
    - Rack
    - Crate
    - Board



[Ref: 1]

Trigger system

- At design parameters the LHC produces:
  - ~billions of events per second in CMS detectors.
  - Corresponds to petabyte of data per second.

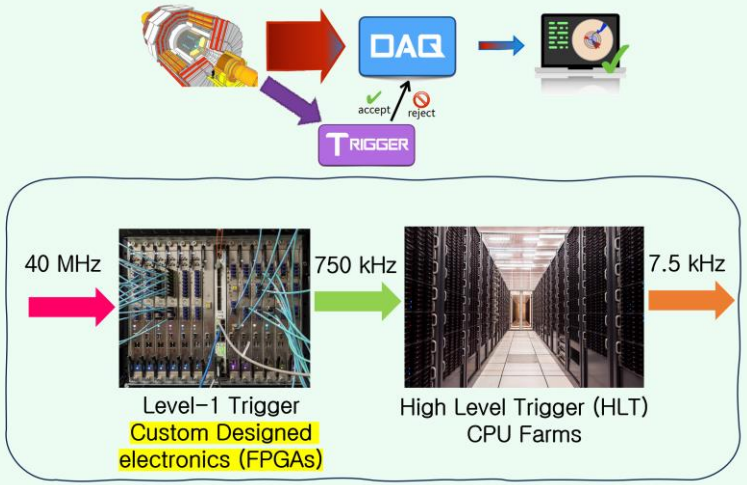
- Problem:
  - It is impossible to store and process this large amount of data.
  - Most of the events are not interesting.

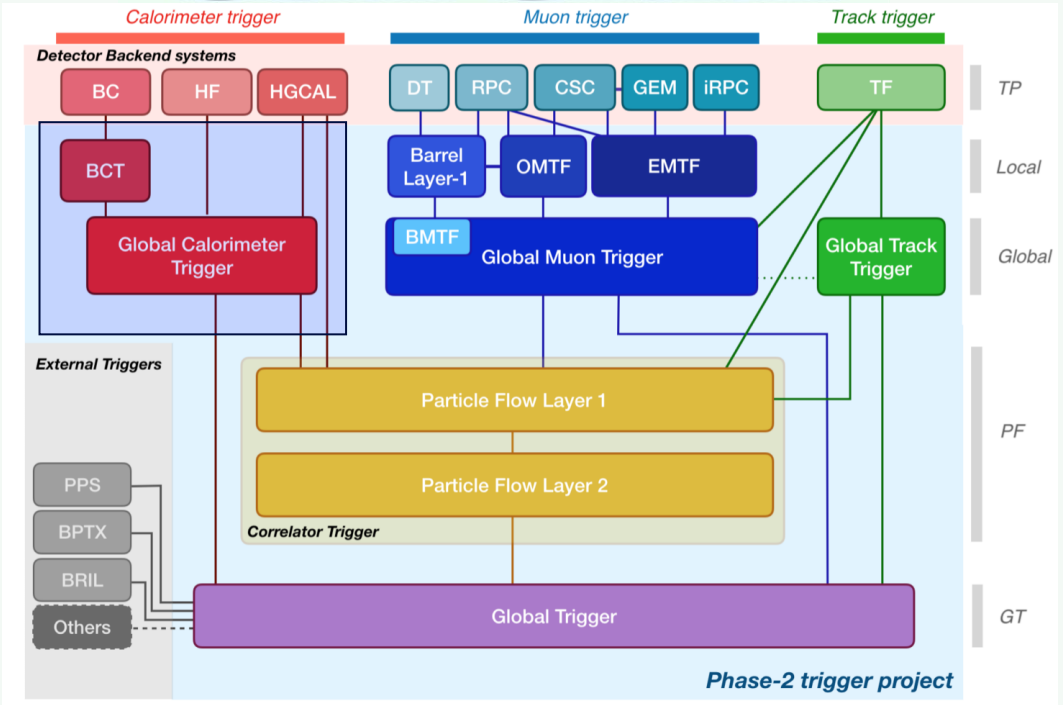
- Solution:
  - a drastic rate reduction must be achieved.
    - TRIGGER SYSTEM.

- Two level of triggering strategy
  - Level-1 (Hardware): 40 MHz to 750 kHz
  - High level trigger (Software): 750 kHz to 7.5 kHz.

- Phase-2 Level-1 Trigger
  - Processing CMS three sub-detector system.
    - Calorimeter
    - Tracker (First time inclusion in the system)
    - Muon system

- Final decision by global trigger (GT).





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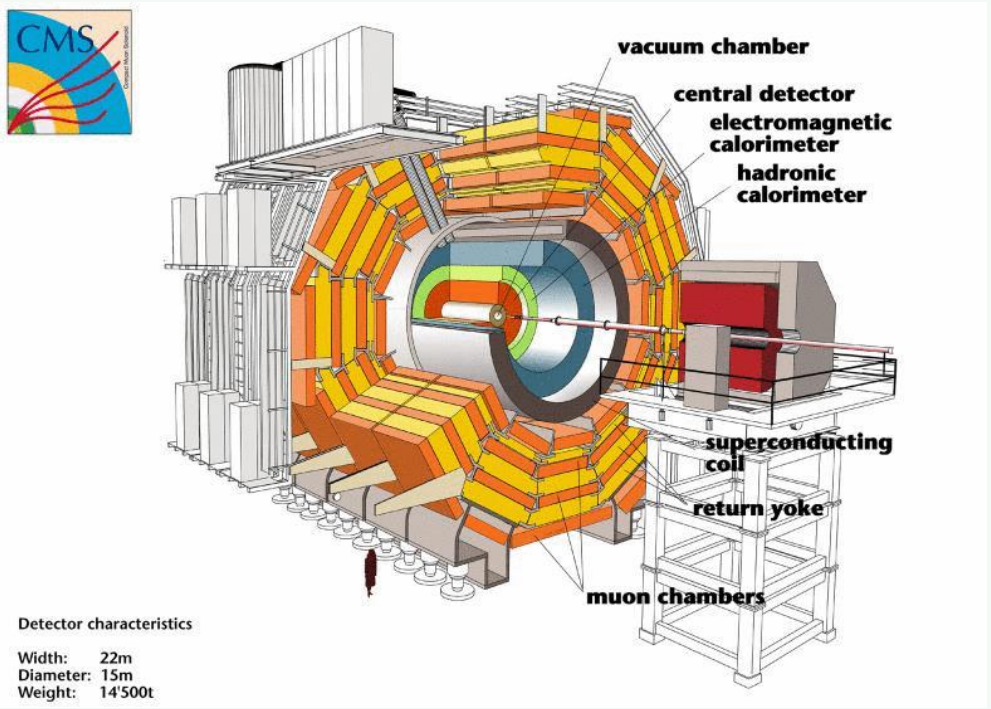
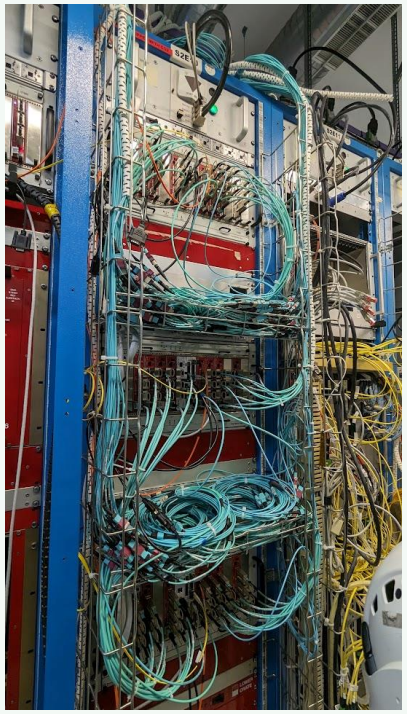
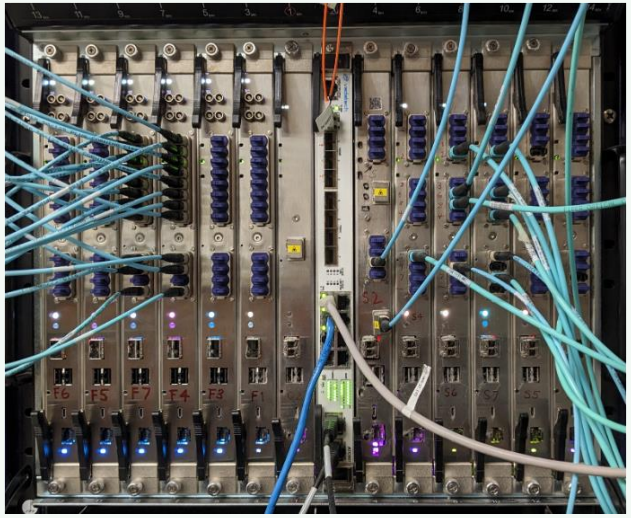
CMS L1 trigger - a hardware perspective



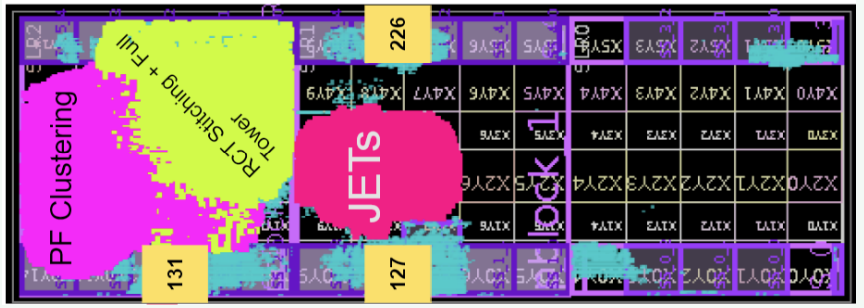
CMS detector and Front-end electronics



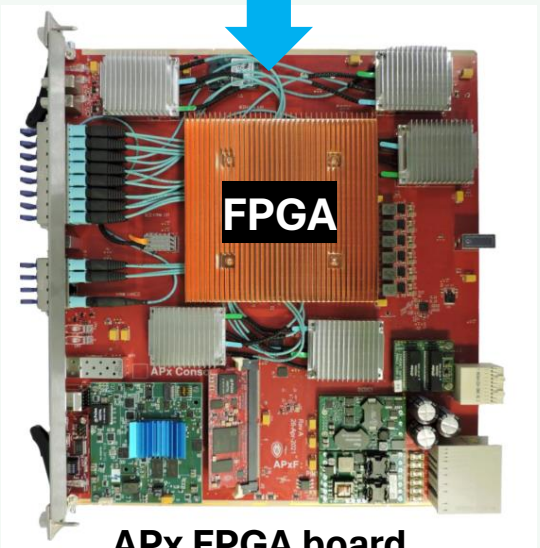
Backend and trigger system at CMS USC: electronic rack hosting multiple crate



Crate hosting 12 APx FPGA boards



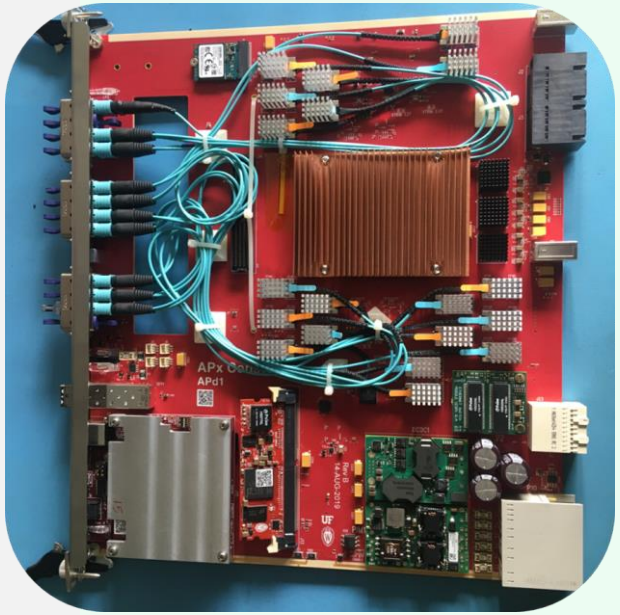
Trigger algorithm on FPGA



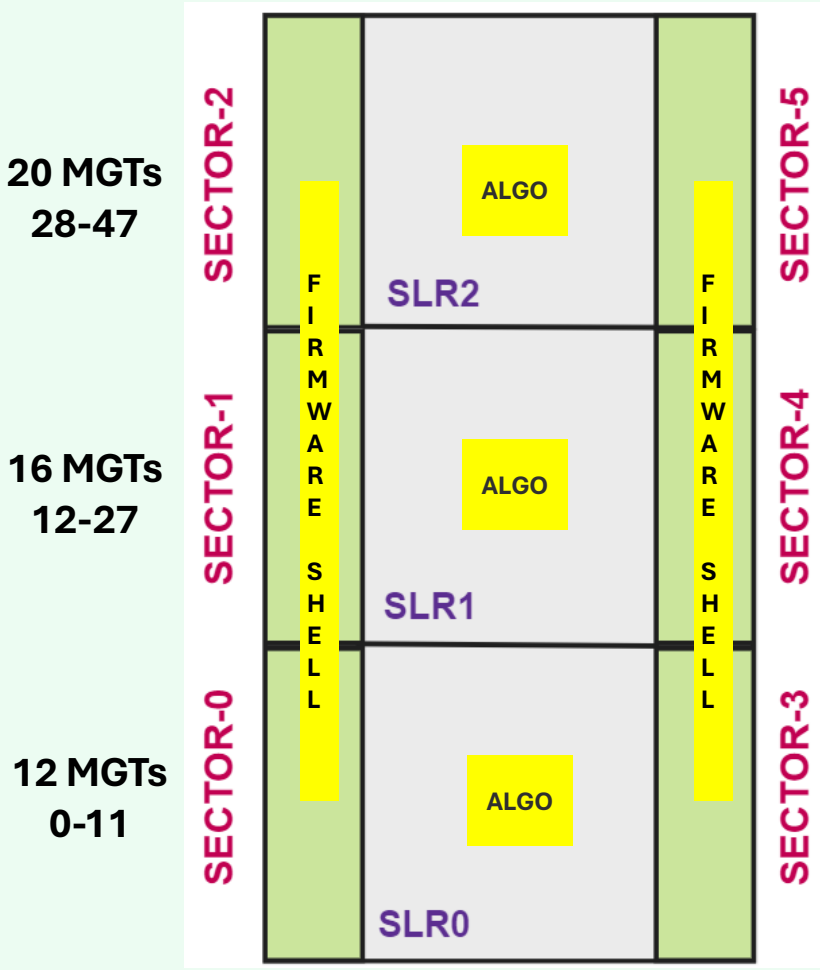
APx FPGA board

APx Philosophy

- Aim is to provide generic trigger processing board to fulfill the requirement of Phase-2 in terms of
  - Computational power.
  - High bandwidth.
- Designed at University of Wisconsin.
- Features single FPGA as the main processing element.
- APd1 – First demonstrator board.
  - Based on XCVU9P FPGA (3 SLR)
    - SLR: Silicon logic region [Ref: 8]
  - Support 100 of 25 Gbps optical links for algorithm.
- SLR division and links capacity of the APd1 board have larger design implication.



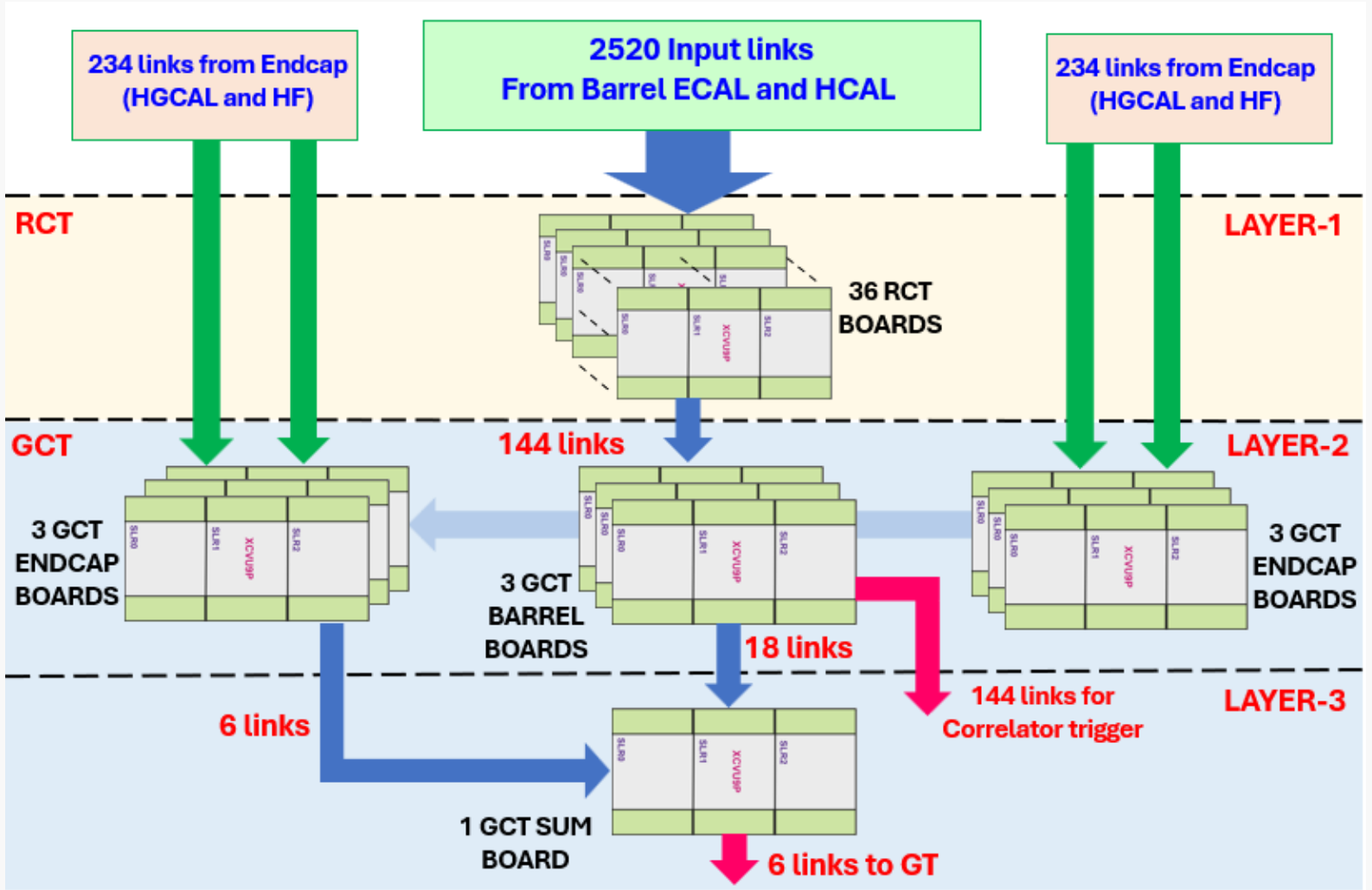
APd1 board [Ref: 2]



XCVU9P FPGA Floorplan

Phase-2 Level-1 Calorimeter Trigger Architecture

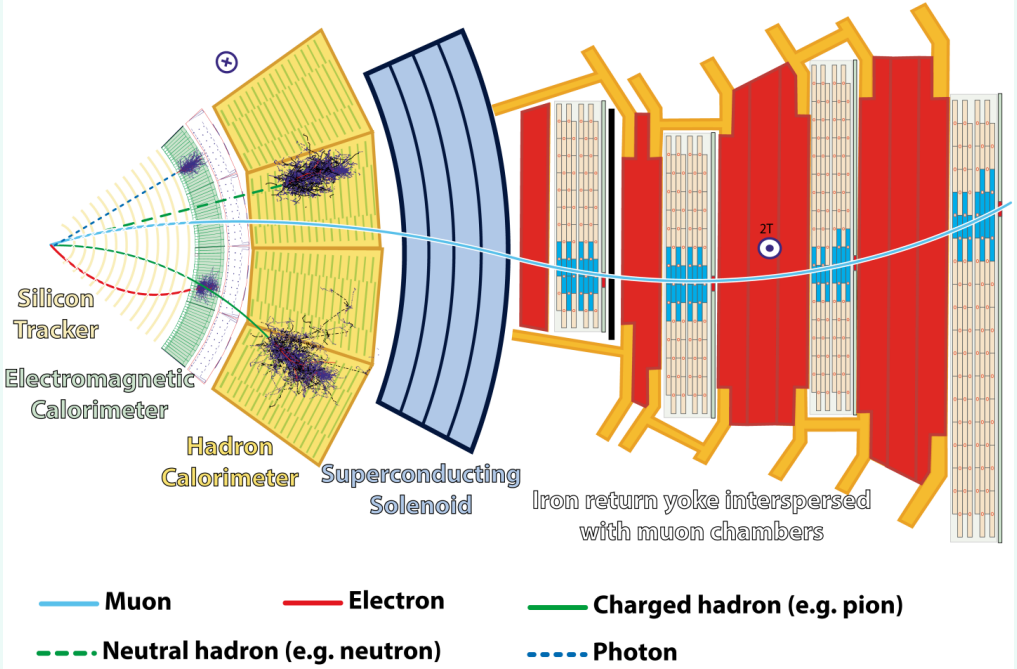
- Two level architecture.
  - Regional calorimeter trigger (RCT).
  - Global calorimeter trigger (GCT).
- Proposed to implement using 46 APx boards.
- The levels are further subdivided into three layers.
  - Layer-1
    - RCT: 36 APx boards.
  - Layer-2
    - GCT barrel: 3 APx boards.
    - GCT endcap: 6 APx boards.
  - Layer-3
    - GCT sum: 1 APx boards
- Latency requirement:
  - Output to correlator trigger: 3 μs
  - Output to global trigger: 4 μs
- Device Utilization: < 50%
- Main feature: Identical division of the calorimeter detector.
  - Can be prototyped using only 4 boards.



Calorimeter Trigger Objects

- The L1 trigger algorithms are developed to identify physics objects, i.e., electrons, photons, hadrons (jets) and missing transverse energy (MET).

- Electromagnetic and hadrons particles interact differently in the calorimeter.
  - Different clustering scheme
    - Different cluster sizes



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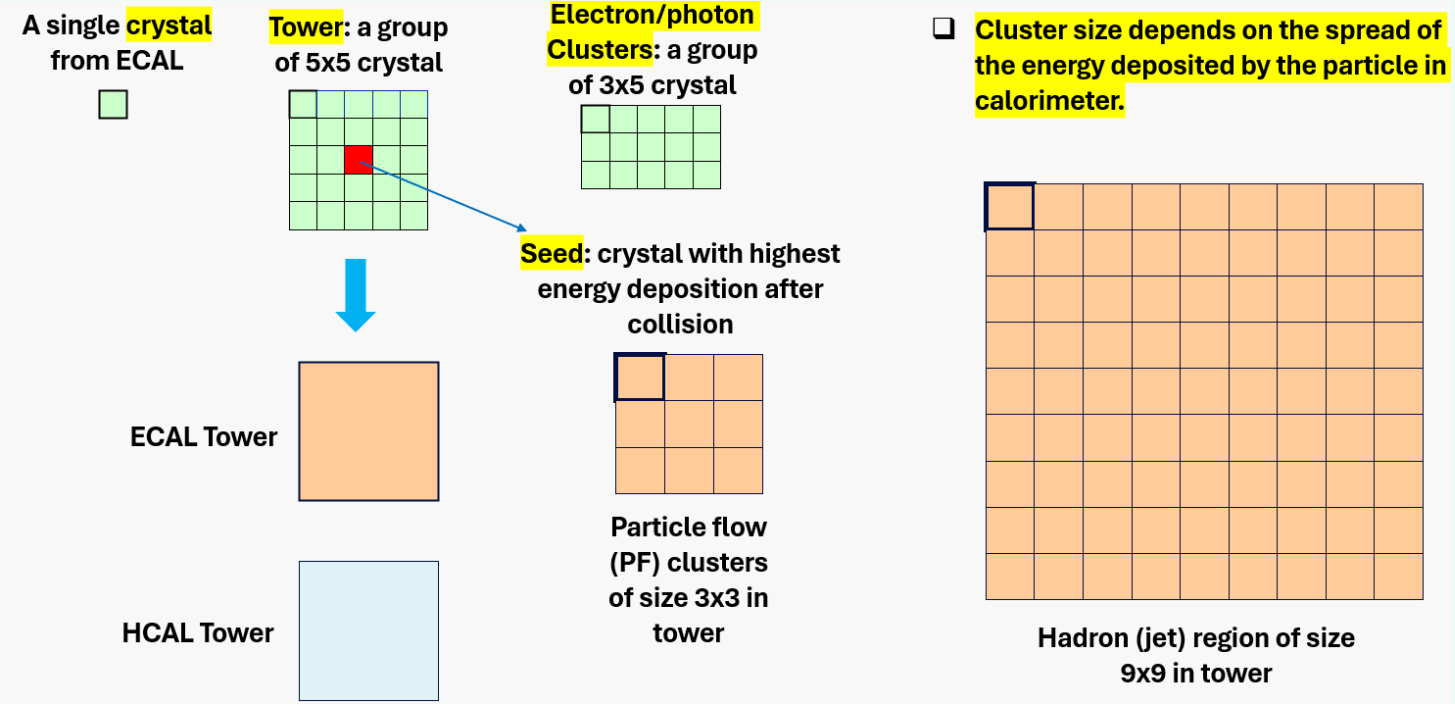


Major Design and Prototyping Constraints

Latency (highest priority)

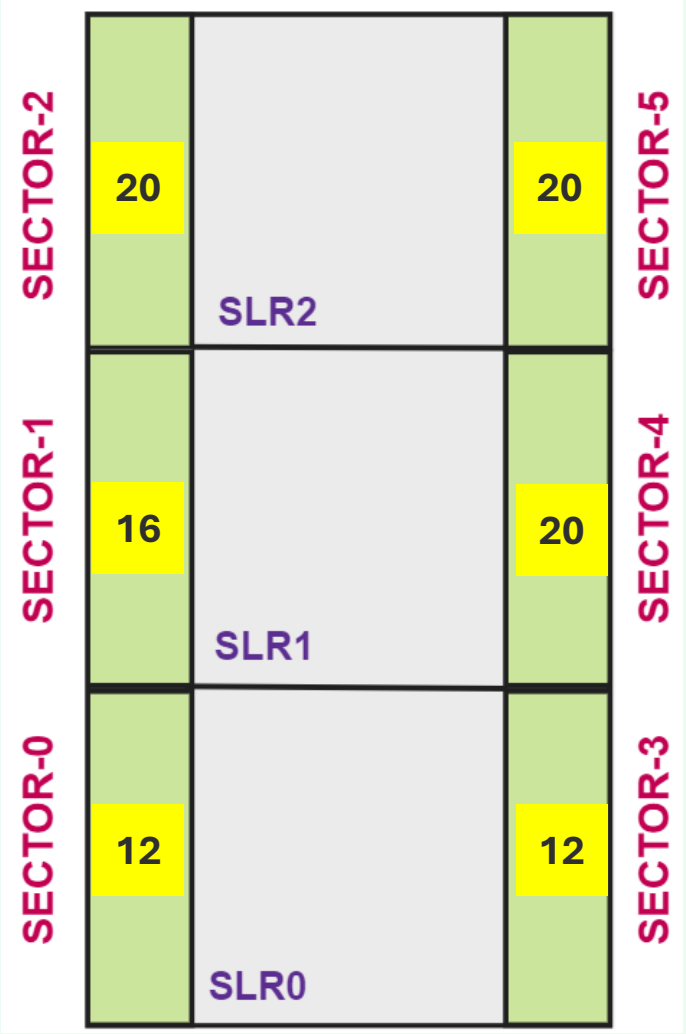
- Algorithm
- Data transmissions.

Utilization

- Device utilization is preferred to be low < 50%.
  - 10 years of operations.

Input/Output constraints

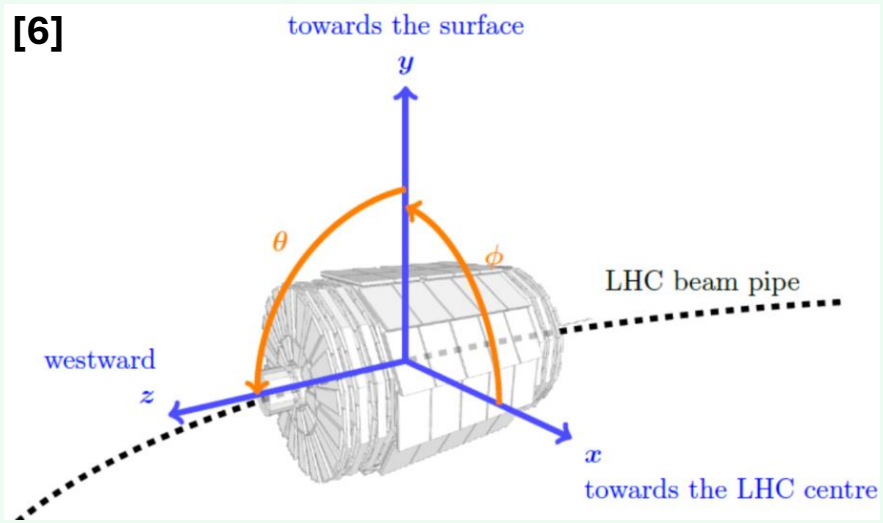
- 100 links available in APd1
- Decides the algorithm processing region.
- The transceivers (MGTs) are distributed throughout the FPGA.
  - Algorithm require early partitioning and floorplanning.



- Two important cases in Prototyping

- Case-1:
  - Algorithm can cover the detector in identical region with one region require > 100 links
- Case-2:
  - Algorithm can process a detector region using < 100 links.
  - However, the algorithm coverage is not identical.
  - Need to develop multiple algorithm.
  - Making prototype difficult.
- Need to find a balance between detector coverage, required links, and identical division.
  - Make prototyping easier.

RCT region coverage



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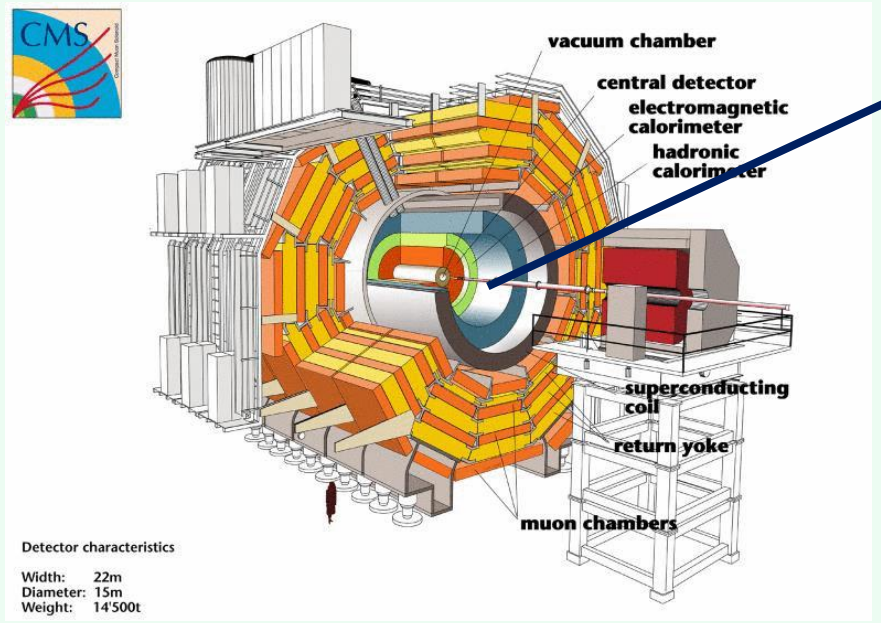
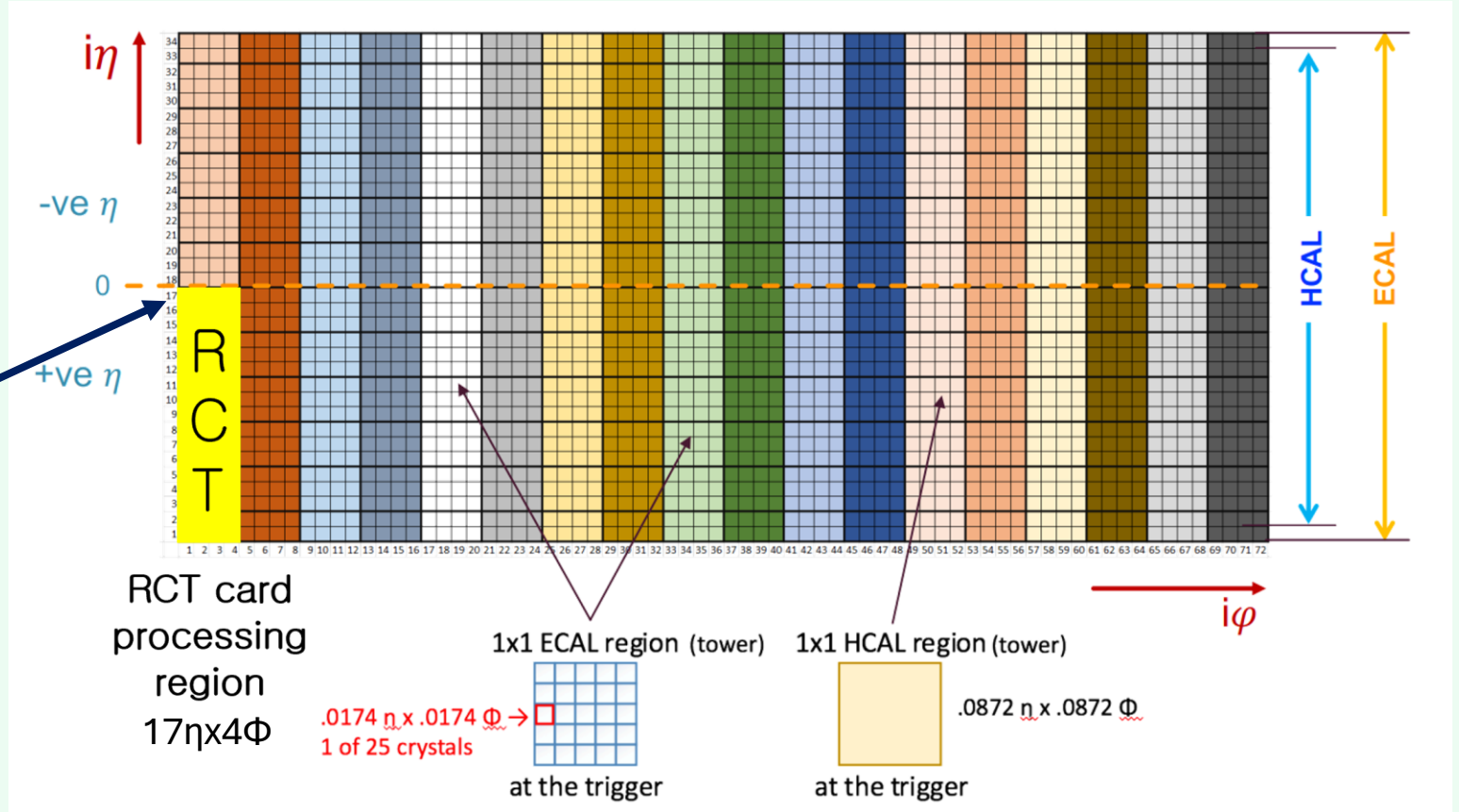
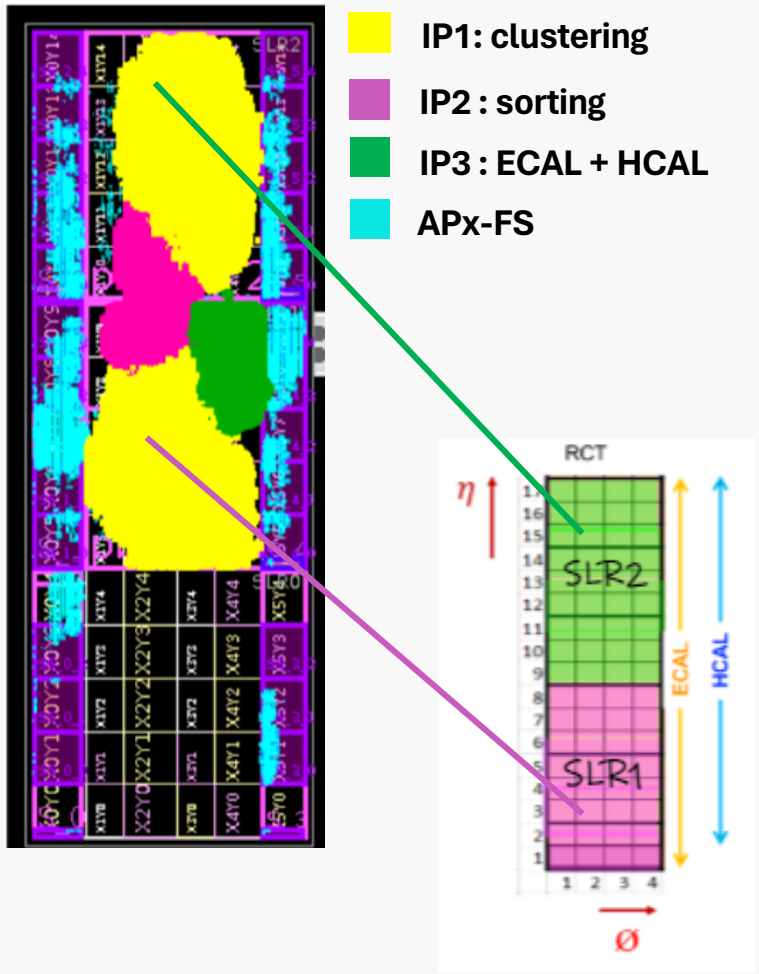
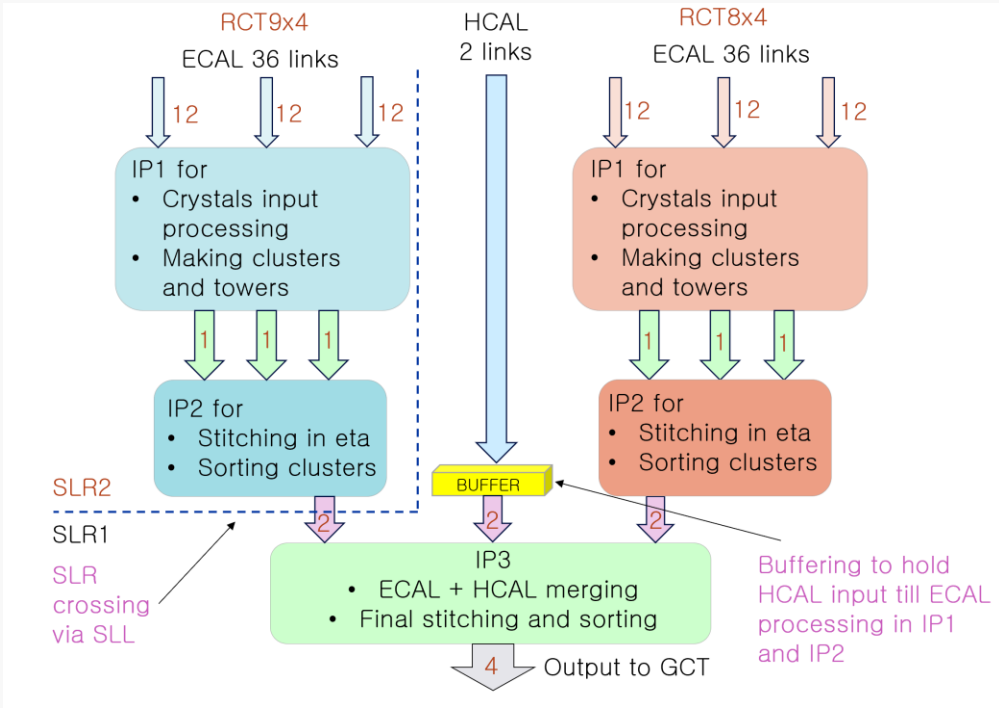




Regional Calorimeter Trigger (RCT) Prototyping

- RCT v2.0 functionality is sub-divided into three individual IPs
  - IP1
  - IP2
  - IP3
- Implementation in 2 SLRs.
  - SLR2
  - SLR1
- The HCAL towers information at IP3.
- Bitstream is successfully tested
  - Using LHC events (standalone mode)
  - 3 unique physics events.
- Latency and F_{MAX}: 1.2 µs, 361 MHz

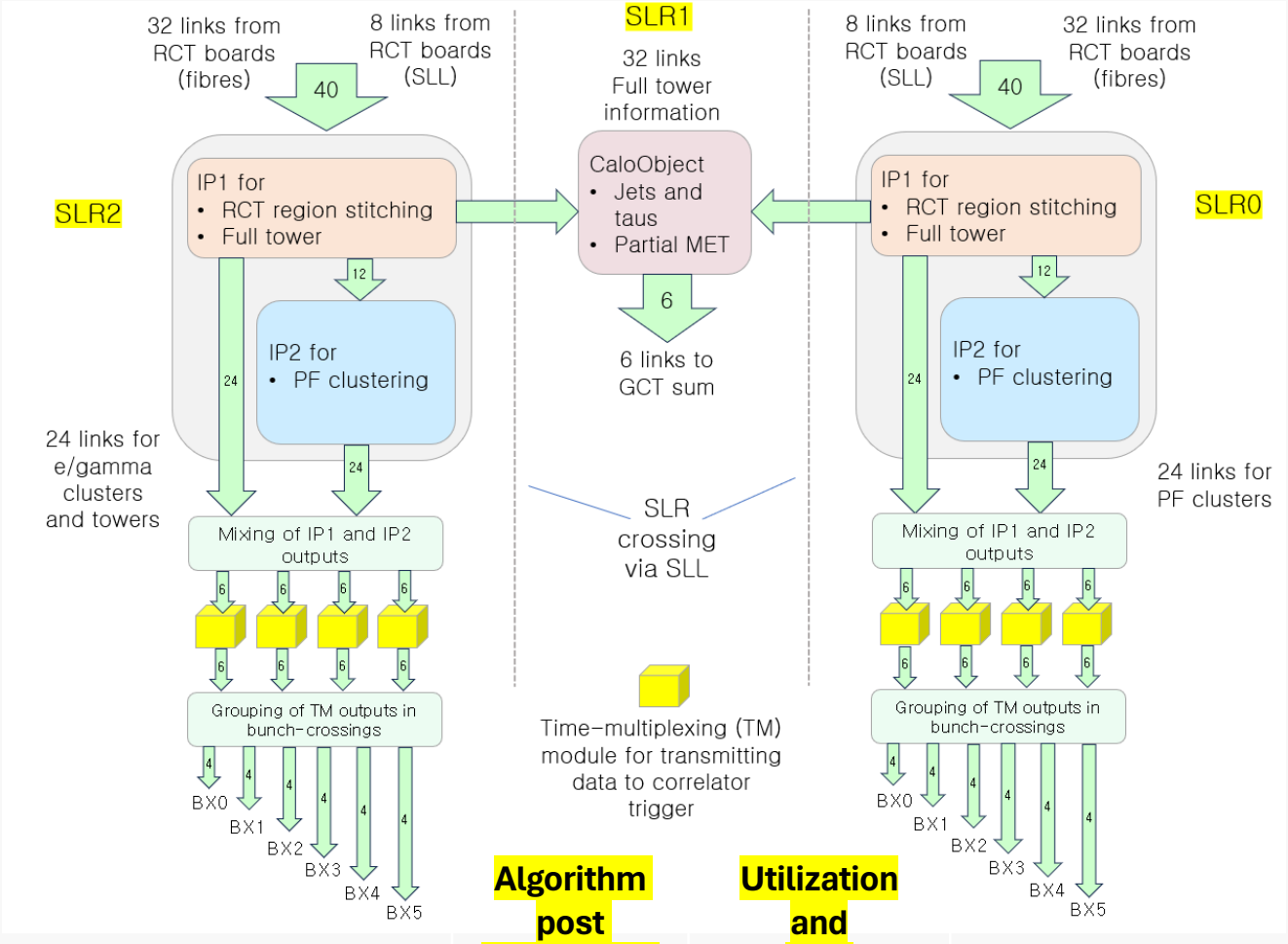


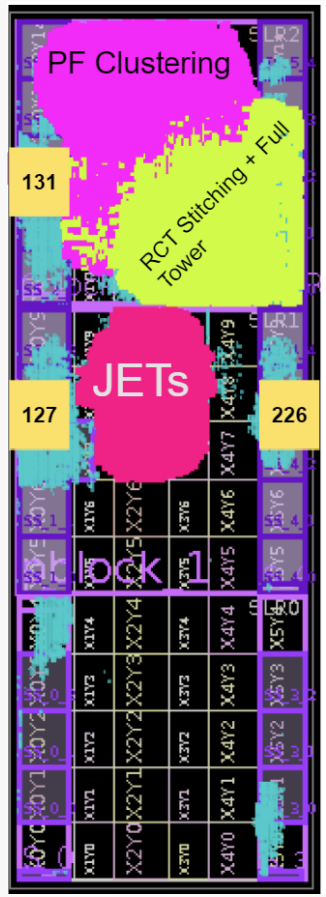


Algorithm post Prototyping	Utilization and F_{MAX}
LUT	16%
FF	13%
F_{MAX}	361 MHz

GCT Barrel

- Process 16 RCT boards.
- Functionality division (SLR2 and SLR0):
  - IP1
  - IP2
  - A time-slice module developed in VHDL for sending the data to correlator trigger.
- SLR1:
  - CaloObject algorithm
    - Jets
    - Taus
    - Partial MET
- Input: 64 links
- Output:
  - 48 links to correlator trigger
  - 6 links to GCT sum board
- Bitfile is generated and tested with LHC events of test vector.
- Latency: 692 ns.





Algorithm post Prototyping	Utilization and F_{MAX}
LUT	22%
FF	18%
F_{MAX}	360 MHz

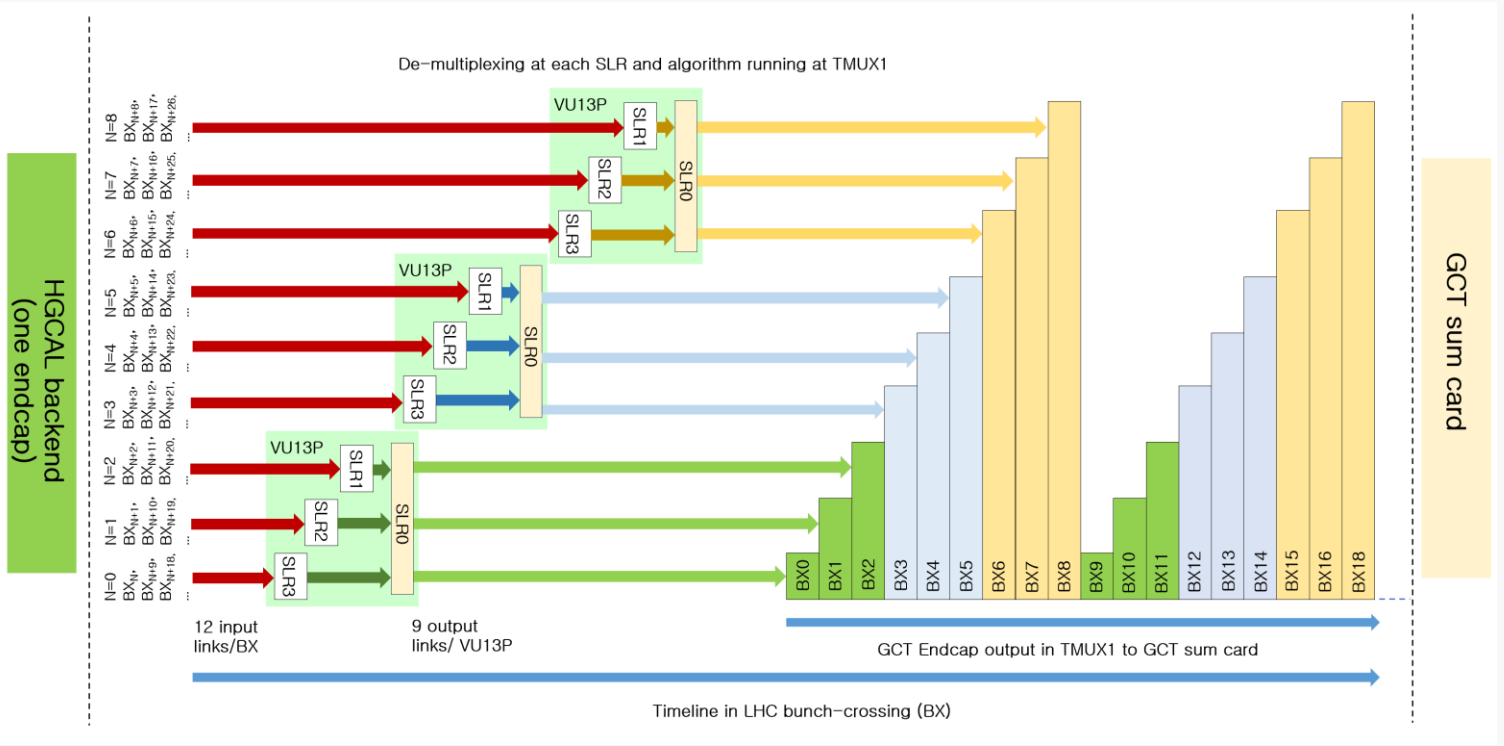
IP1

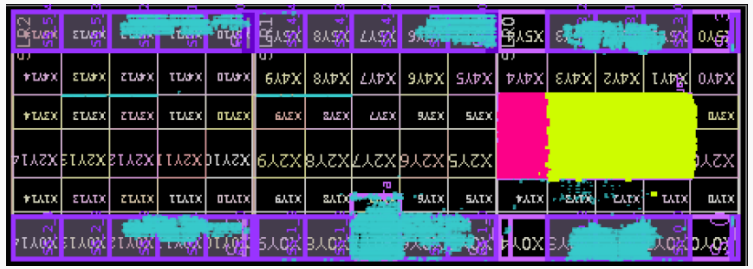
IP2

CaloObject

GCT Endcap

- HGCAL backend sends detector information in 18 time-slices (TM18).
  - Algorithm at calorimeter trigger runs without any time-multiplexing (TM1).
  - Demultiplexing (TM18 => TM1) is required before GCT endcap algorithm.
- DEMUX algorithm is developed in VHDL
  - serving two time slices per SLR.
  - Reduces the utilization by half.
- Prototyping one SLR can easily scale to one board
  - One board can easily scale to 6 boards.
  - Make prototyping faster.
- Floor planned in two separate regions to reduce the net delays
  - DEMUX: 2 clock regions
  - Jet algorithm: 6 clock regions
- Bitfile is tested for multiple LHC events.
- Latency: 661 ns



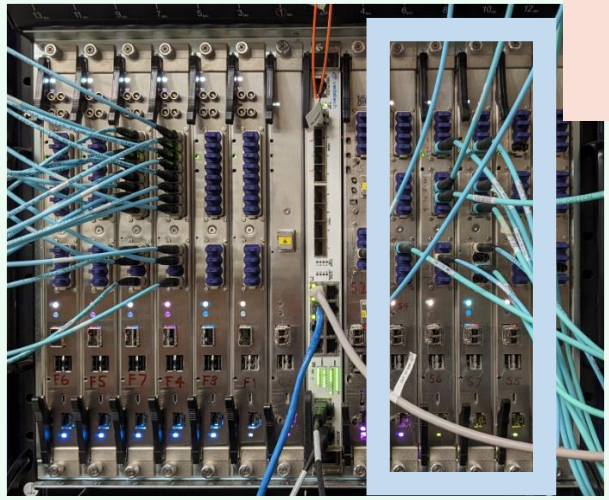


DEMUX Jets and taus

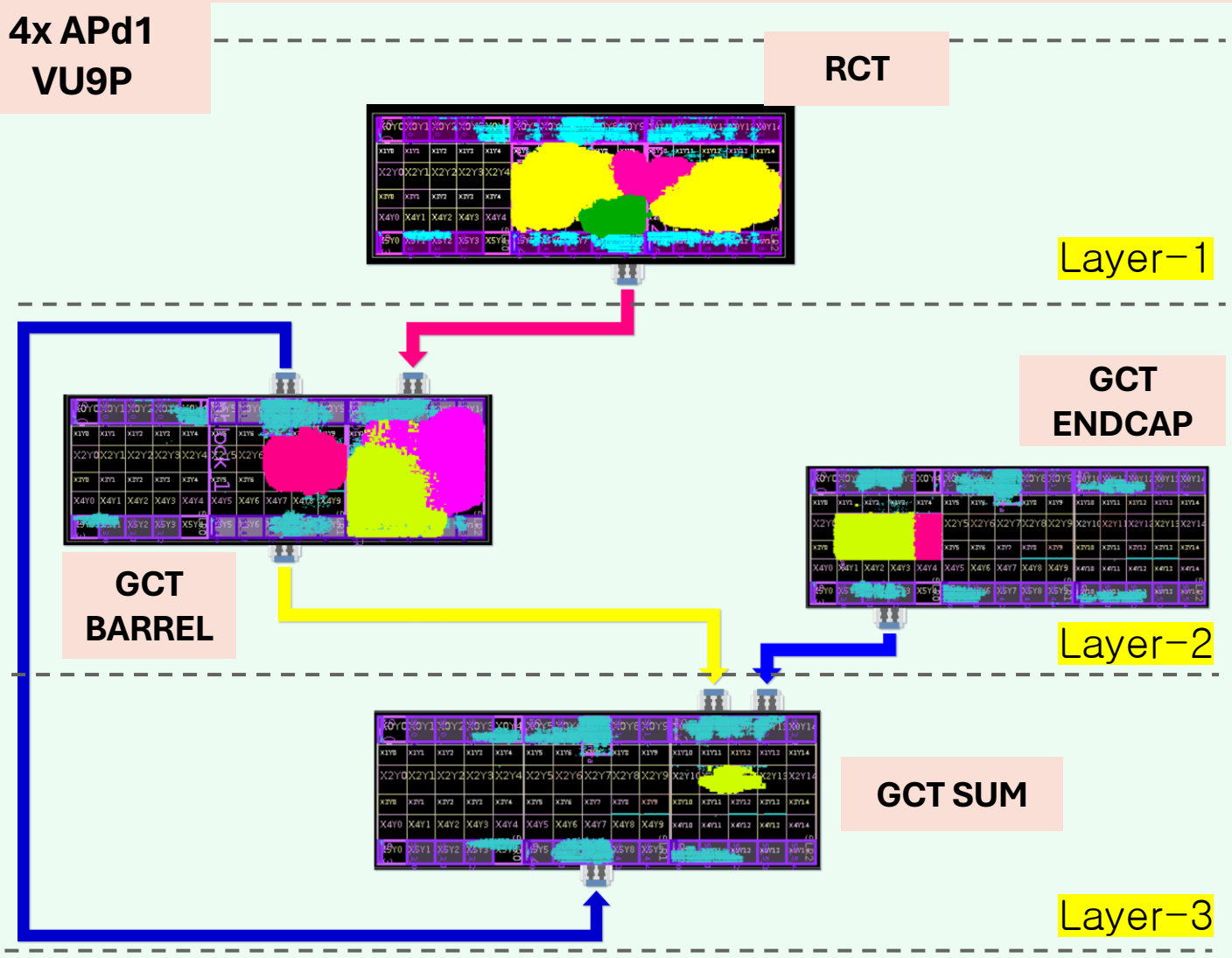
Algorithm post Prototyping	Utilization and F_{MAX}
LUT	6%
FF	7%
F_{MAX}	360 MHz

Prototyping Calorimeter Trigger System

Board to Board	Latency in µS (budget)
RCT => GCT barrel	1.8 (3)
RCT => GCT barrel, endcap => GCT SUM	2.4 (4)



- Prototyping of the complete CALO system using 4 APd1 board.
- The boards are aligned with MC input pattern filled at
  - ECAL Crystals and HCAL towers: input buffers of RCT board
  - HGCAL tower and clusters: input buffers of GCT endcap board.
- Output is captured at GCT SUM and matches with
  - MC == HLS == RTL == Bitfile



Summary

- An architecture of Phase-2 calorimeter trigger is proposed which uses 46 APx FPGA boards.
- The architecture comprises two level and further sub-divided in three layers.
- Algorithms are developed for all board flavors which satisfies the main constraint of latency and utilization.
- Algorithms are tested and validated on APd1 board.
  - MC == HLS == RTL == Bitfile
- Following are the multi-board tests are performed and validated successfully.
  - 2 board test: RCT v2.0 => GCT barrel
  - 3 board test: GCT barrel, GCT endcap => GCT sum
  - 4 board test: RCT, GCT barrel, GCT endcap, GCT sum.
- With availability of algorithms prototyped at each layer and input test vectors, entire Phase-2 calorimeter trigger is prototyped using 4 APd1 boards and 16 optical links.

References

- [1] The High-Luminosity upgrade of the LHC: Physics and Technology Challenges for the Accelerator and the Experiments. J. Phys.: Conf. Ser., 706(2):022002, 2016. doi: 10.1088/1742-6596/706/2/022002. URL https://cds.cern.ch/record/2263093.
- [2] The Phase-2 Upgrade of the CMS Level-1 Trigger. (2020). [Techreport]. CERN. https://cds.cern.ch/record/2714892.
- [3] Dris, Stefanos & Foudas, C & Troska, J.. (2010). Performance of the CMS Tracker Optical Links and Future Upgrade Using Bandwidth Efficient Digital Modulation.
- [4] Julia Handl. Jet Energy Calibration of the CMS Detector with Z(→e+e) + Jet Events at $\sqrt{s}$ = 13 TeV, 2016.
- [5] https://home.cern/resources/image/experiments/cms-images-gallery
- [6] https://en.wikipedia.org/wiki/Large_Hadron_Collider
- [7] https://www.picmg.org/openstandards/advancedtca/
- [8] https://docs.xilinx.com/v/u/en-US/wp380_Stacked_Silicon_Interconnect_Technology

THANK YOU…

BACKUP...

GCT sum Prototyping

- Final layer of the calorimeter trigger
- Combine all the information of the calorimeter trigger.
- Re-assemble the data according to the global trigger requirements and send it in six time slices (TM6).
- 32 input links
  - 8 x Three GCT barrel board.
  - 8 from GCT endcap board.
- Calculate the final MET
  - Using CORDIC algorithm.
    - cosϕ
    - sinϕ
- 6 output links.
- Latency: 178 ns

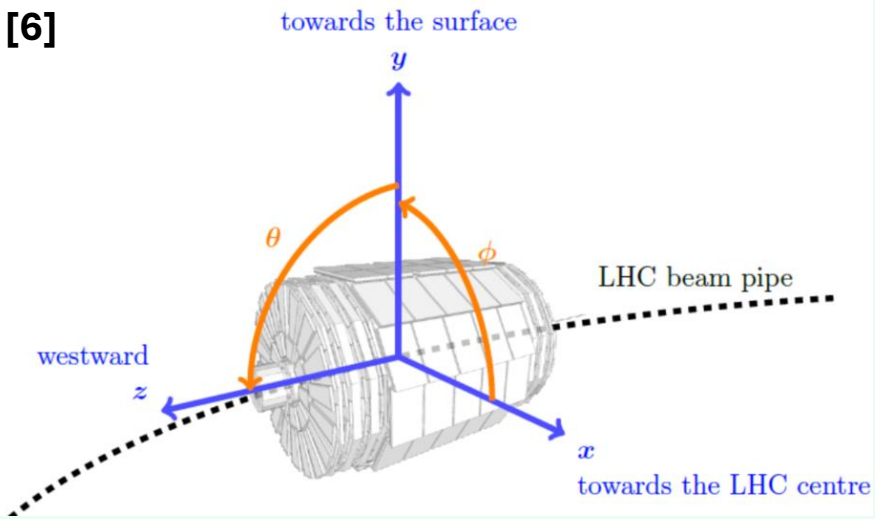
Algo component	Latency (clock cycles)
CORDIC	29

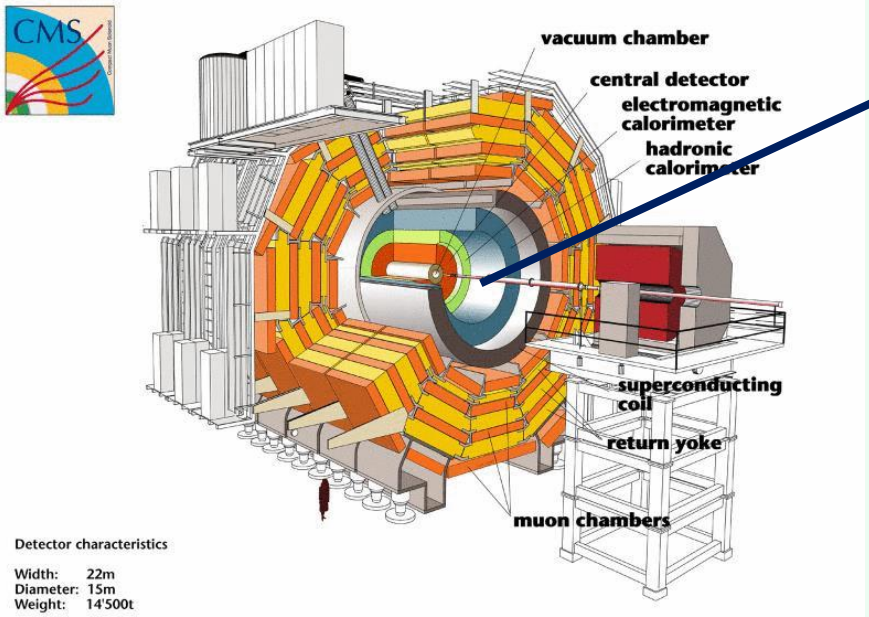
	Utilization and F_{MAX}
LUT	5%
FF	4%
DSP	4%
F_{MAX}	365 MHz

GCT Sum including CORDIC

RCT and GCT barrel region coverage

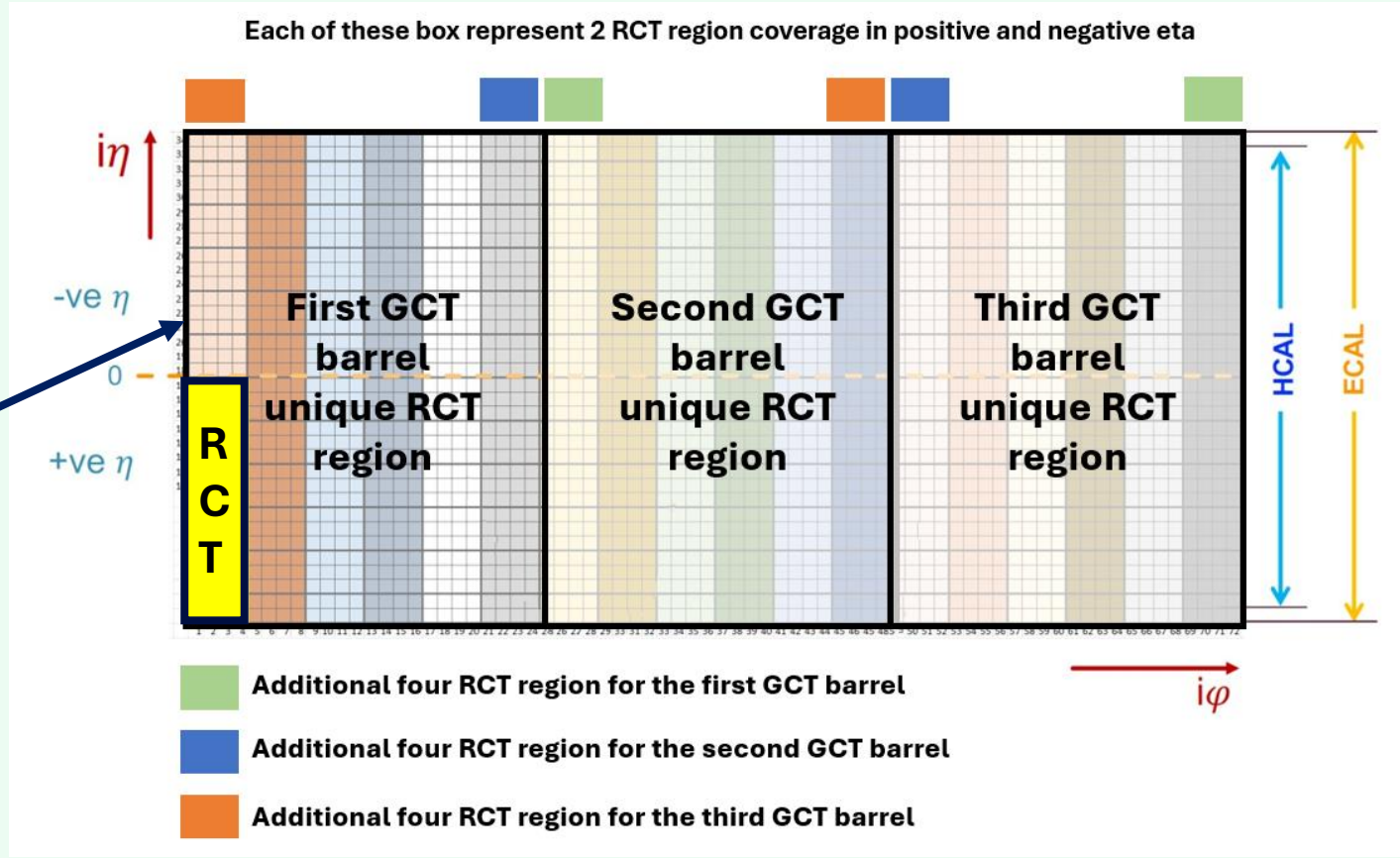
[6]





Pseudorapidity, η = -ln(tan(θ/2)), θ is the polar angle

Φ is the azimuthal angle



Design flow

First step
- ❑ Defining the physics performance and requirements
- ❑ MC simulation

Monte-Carlo

Second step
- ❑ Developing code
- ❑ C simulation
- ❑ Optimize it for
  - ❑ Latency, utilization, and F_{MAX}
- ❑ C Synthesis: C to RTL conversion.

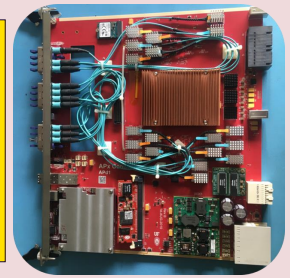
HLS DEV, SIMULATION and SYNTHESIS

Third step
- ❑ RTL simulation
- ❑ Integration of the RTL with the APd1 transceivers.
- ❑ Floorplanning, and IO planning to achieve best F_{MAX}

RTL INTEGRATION, SIMULATION and IMPLEMENTATION

Fourth step
- ❑ Final deployment of the bitfile in the APx board
- ❑ Testing the bitfile

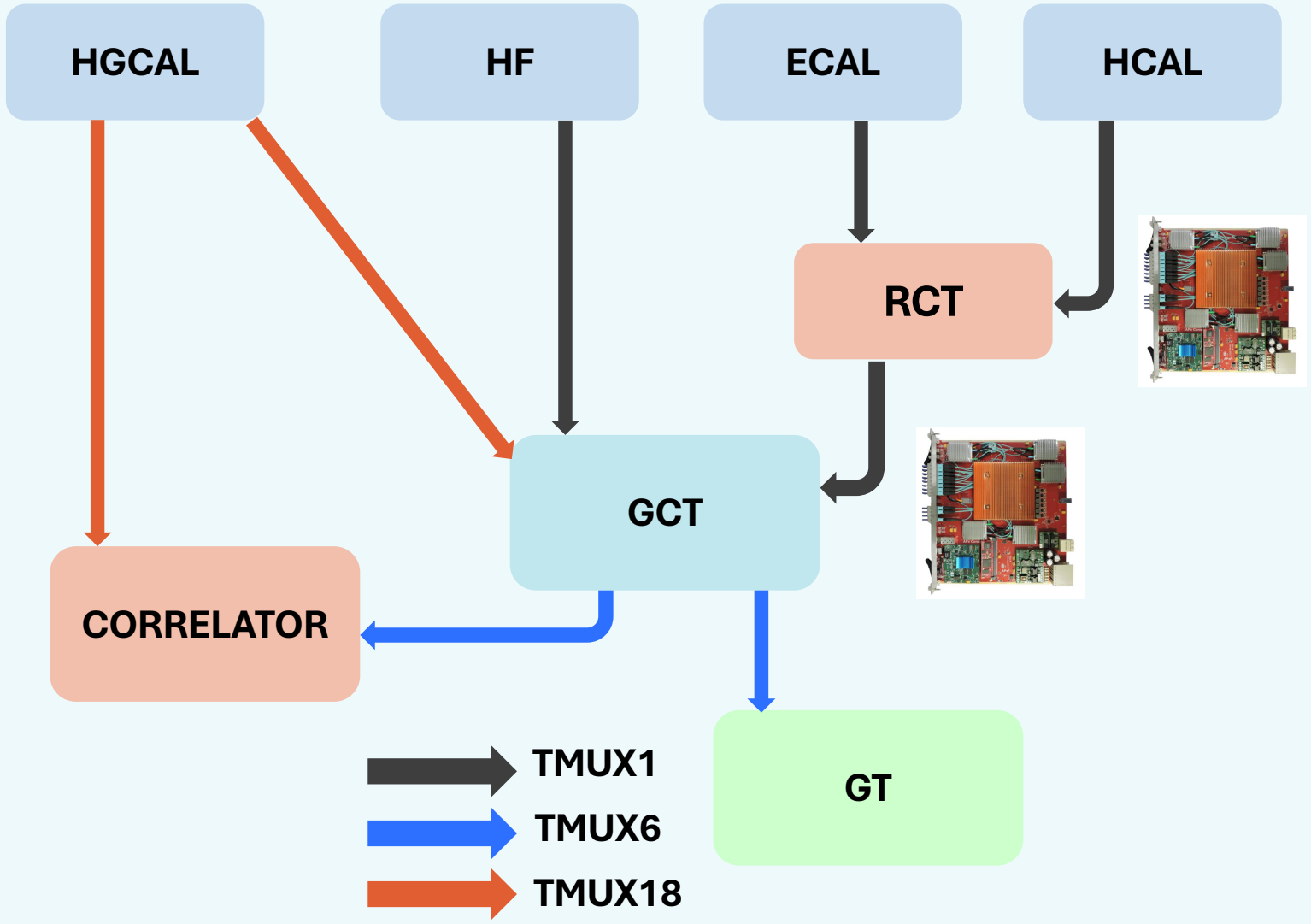
ON BOARD BITFILE TEST



CHAIN TESTED

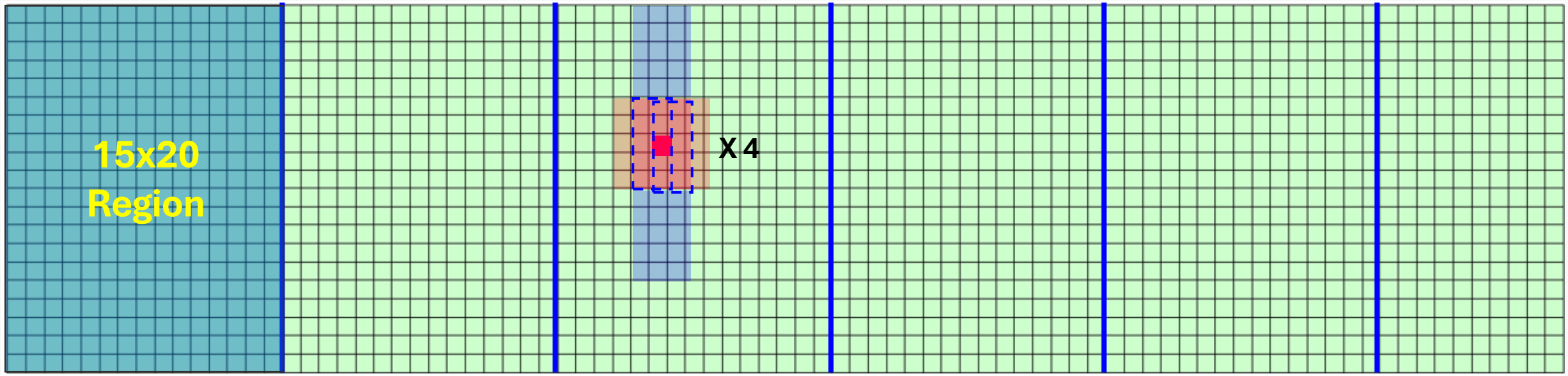
CMS Phase-2 L1 Calorimeter trigger

- Processing four calorimeter sub-system
  - Electromagnetic calorimeter (ECAL).
  - Hadronic calorimeter (HCAL).
  - Forward hadronic (HF).
  - High-granularity calorimeter (HGCAL).
- Implemented in two level
  - Regional calorimeter trigger (RCT)
  - Global calorimeter trigger (GCT).
- Further sub-divided in three layers.



Regional Calorimeter Trigger (RCT)

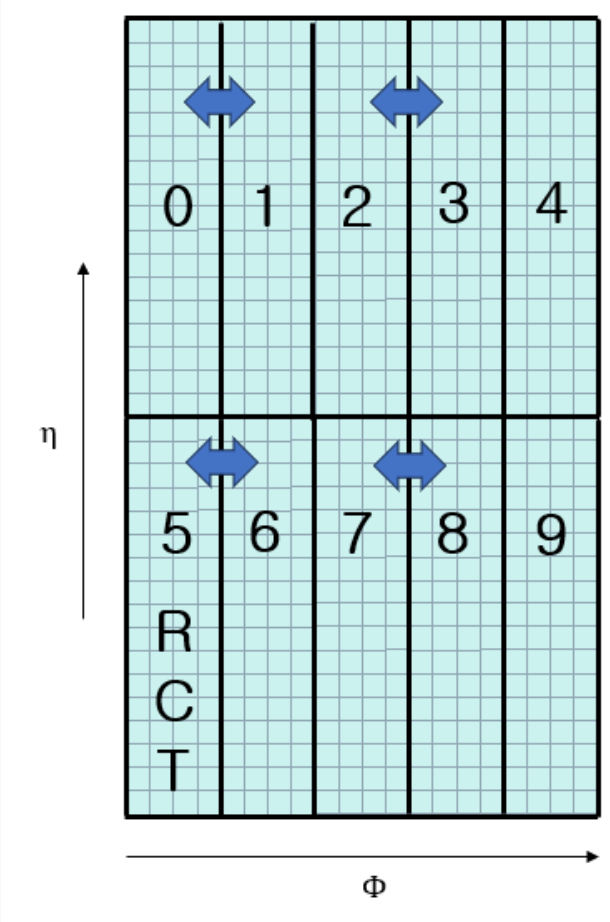
- Algorithm summary:
  - IP1:
    - Prepare clusters and towers
  - IP2:
    - Cluster merging
    - Sorting of clusters
  - IP3
    - Final stitching
    - Final sorting
    - ECAL and HCAL merging.



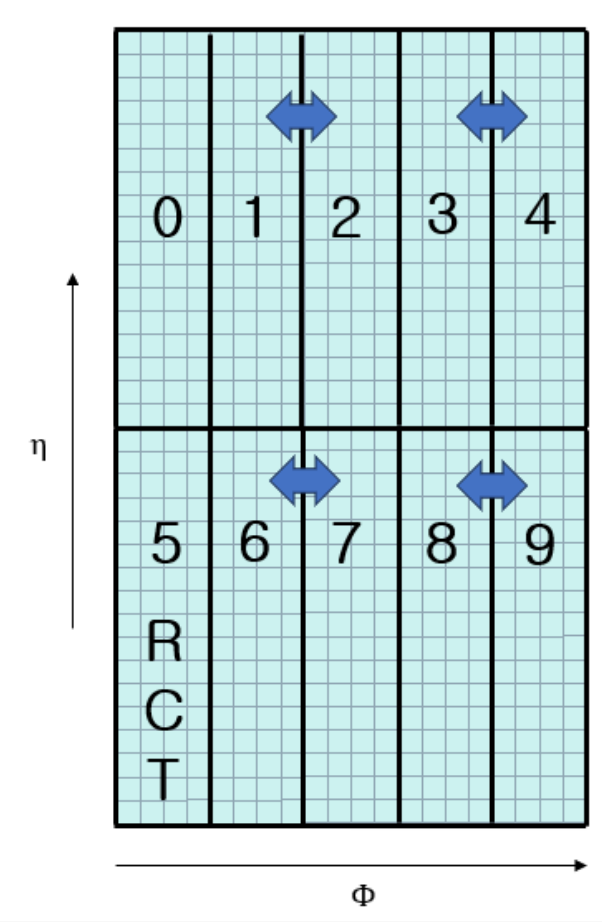
One RCT region

IP1

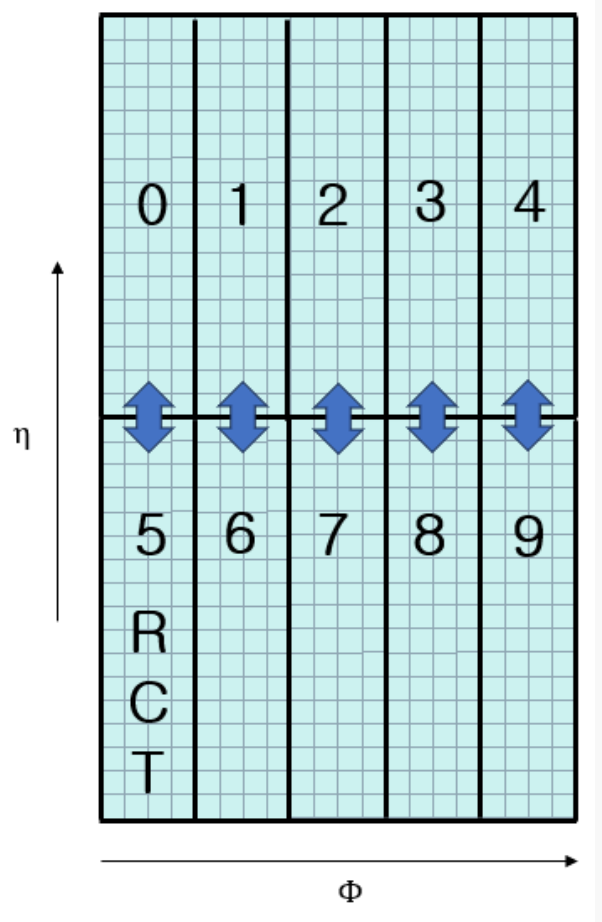
- IP1 performs the stitching of the RCT region
- Latency of the algorithm in all the direction
  - 3 clock cycles
- Create full tower information.
  - Cluster + tower
- Full tower latency: 2 clock cycles.



Direction-1
Latency 3 clock cycles



Direction-2
Latency 3 clock cycles



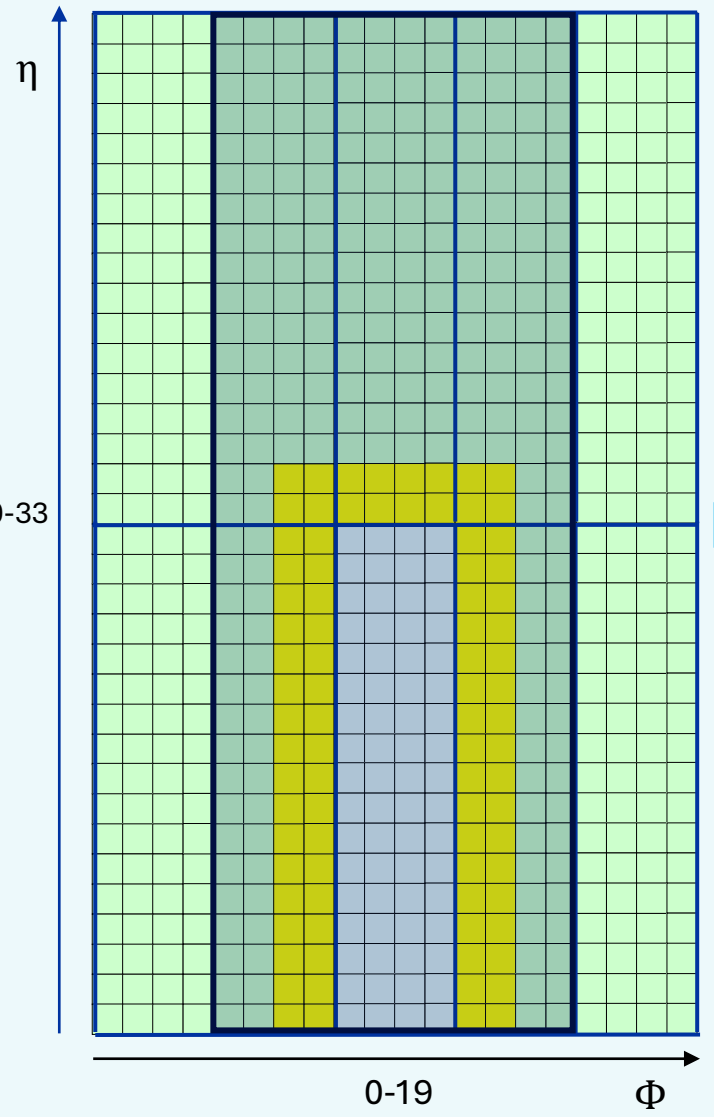
Direction-3
Latency 3 clock cycles

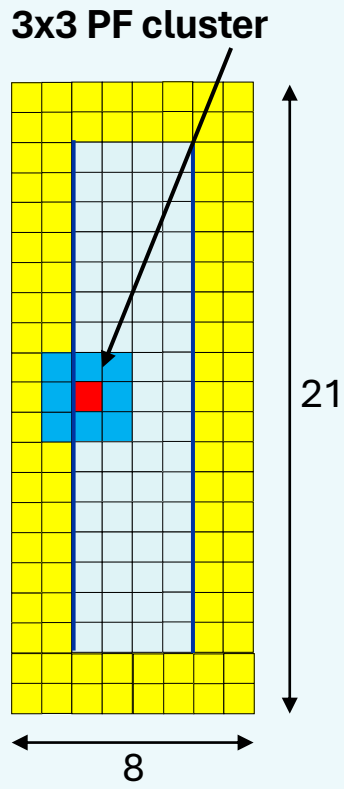
IP2: PF Clustering

- Input: Full tower of 10 RCT region.
- Procedure:
  - Creating overlapping region
    - 17x4 -> 21x8
  - Finding peak tower in 21x8 region.
  - Calculating 3x3 PF cluster energy.
  - Removing the peak tower for next iteration
  - Repeating the steps eight times.
- Output: 48 PF cluster in 6 RCT boards.
- Latency of making eight PF cluster: 80 clock cycle.

Algo component	Latency (clock cycles)
Stitching in eta	3
Stitching in phi	3
Full towers	2
48 PF clusters	80
Total latency	114

	Utilization and F_{MAX}
LUT	30%
FF	18%
F_{MAX}	360 MHz



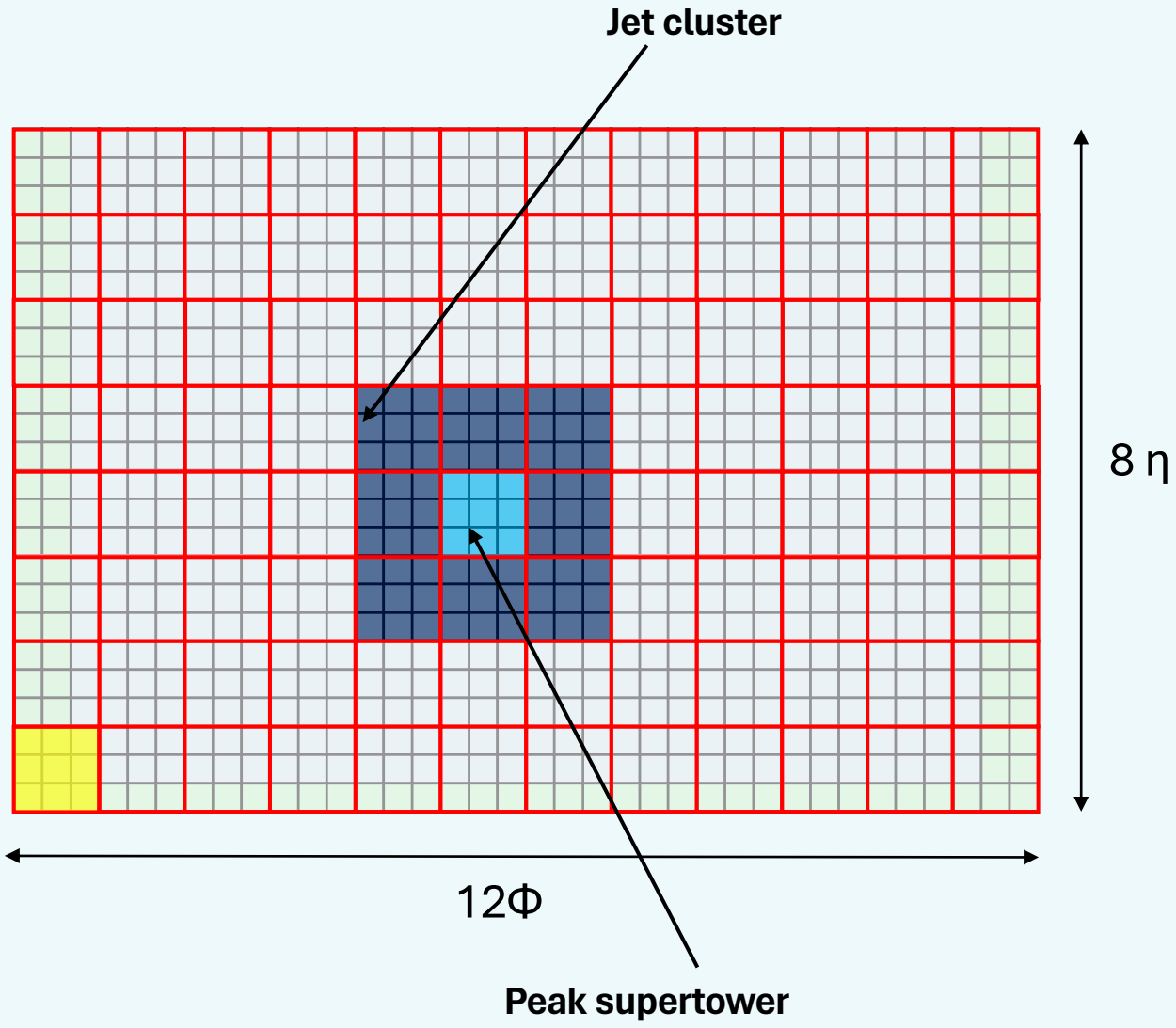


Jet and tau algorithm

- Input: Full tower of 16 RCT region (34 x 32).
- Subdivided in two half (positive and negative eta).
- Uses supertower methodology to reduce the geometry in three-fold.
  - Supertower: group of 3x3 tower.
- 34x32 tower region =>:
  - + η: 12 x 8 supertowers: 6 jets
  - - η: 12 x 8 supertowers: 6 jets
- One jet region: 9x9 in tower
  - 3x3 in supertower.

Algo component	Latency (clock cycles)
Making two 8x12 supertower	2
Finding peak supertower in the bin of 12	3
Making 3x3 jet around the peak	3
Total latency	99

	Utilization and F_{MAX}
LUT	7%
FF	5%
F_{MAX}	367 MHz



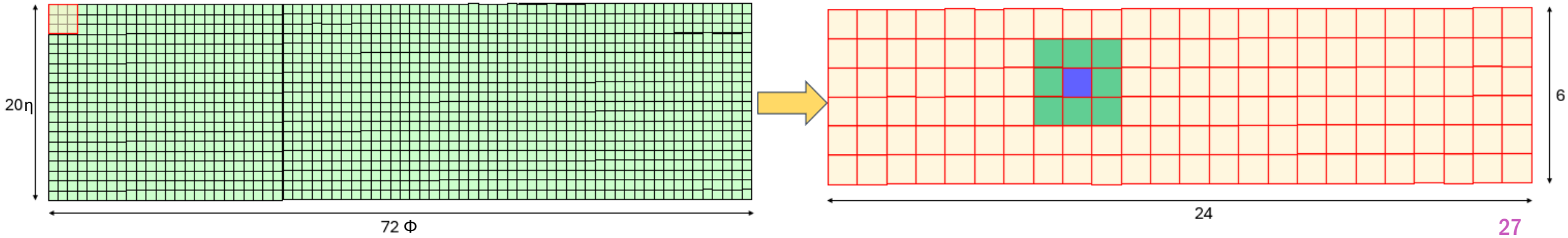
Latency one Jet:12 clock cycles

GCT Endcap

- Prepare jet and taus cluster.
- Internal input links: 108
- Geometry: 20 x 72 endcap towers
- Create supertower for jet calculation
  - 20x72 => 6x24
- Jet calculation step
  - Finding peak in the region of 6x24
  - Calculating jet cluster of size 3x3 around the peak
  - Removing the peak for next iteration
- Total 6 jets
- Output: 4 links

Algo component	Latency (clock cycles)
Making 6x24 supertower	9
Making jet and removing the peak	20
Total latency of Jet and taus algorithm	146

DEMUX + Jet	Utilization and F_{MAX}
LUT	6%
FF	8%
$F_{MAX, DEMUX}$ $F_{MAX, Jet}$	384 MHz 361 MHz



- The SSI technology integrate multiple Super Logic Region (SLR) components placed on a passive Silicon Interposer (fig 3).

- Each SLR contains the active circuitry common to most Xilinx FPGA (Field programmable gate array) devices. This circuitry includes large numbers of:
  - 6-input LUTs (Look-up tables)
  - Registers
  - I/O components
  - Gigabit Transceivers (GT)
  - Block memory
  - DSP blocks
  - Other blocks

- The device we are using for our synthesis and implementation is based on Xilinx SSI technology and support three SLRs.
  - Xilinx Virtex UltraScale+ xcvu9p flgc2104-1-e FPGA

Xilinx Stacked Silicon Interconnect (SSI) Technology

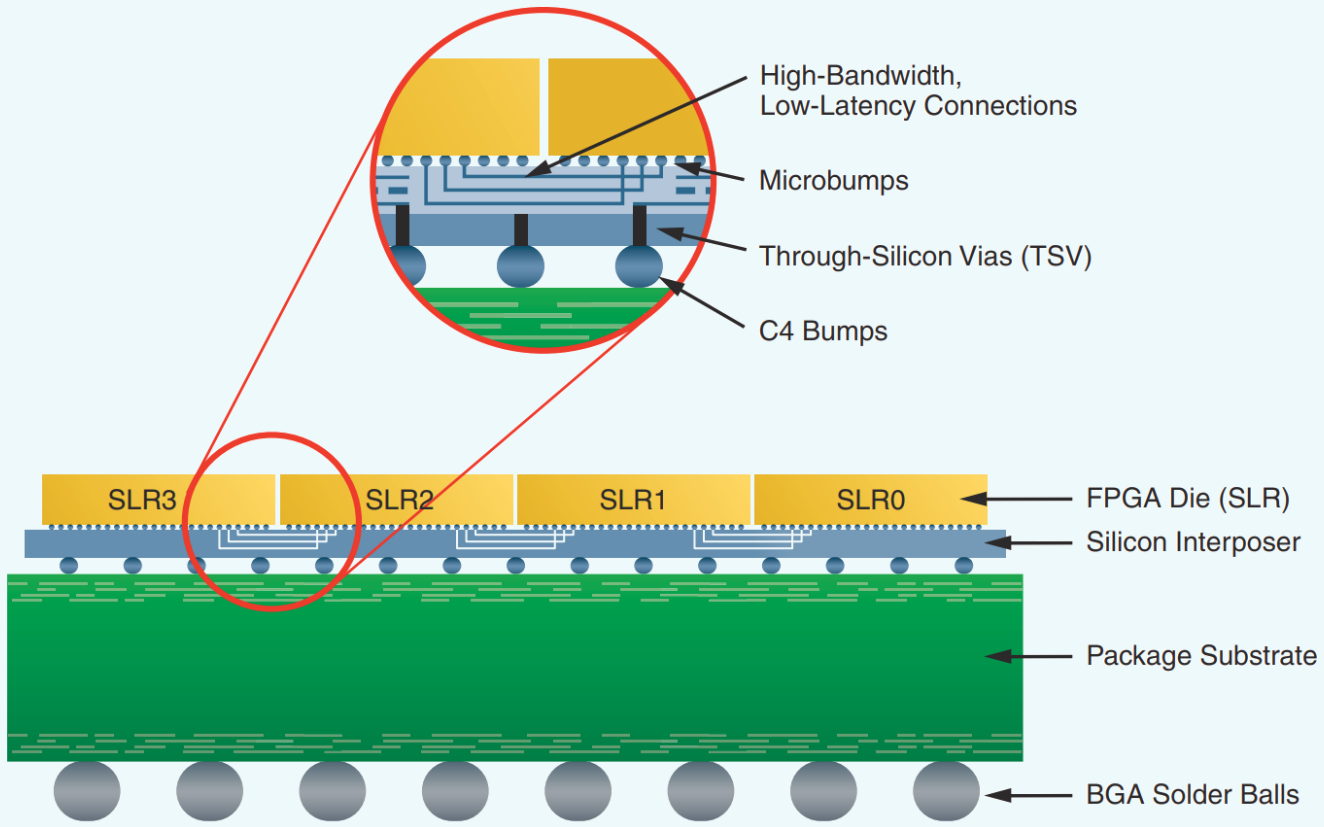


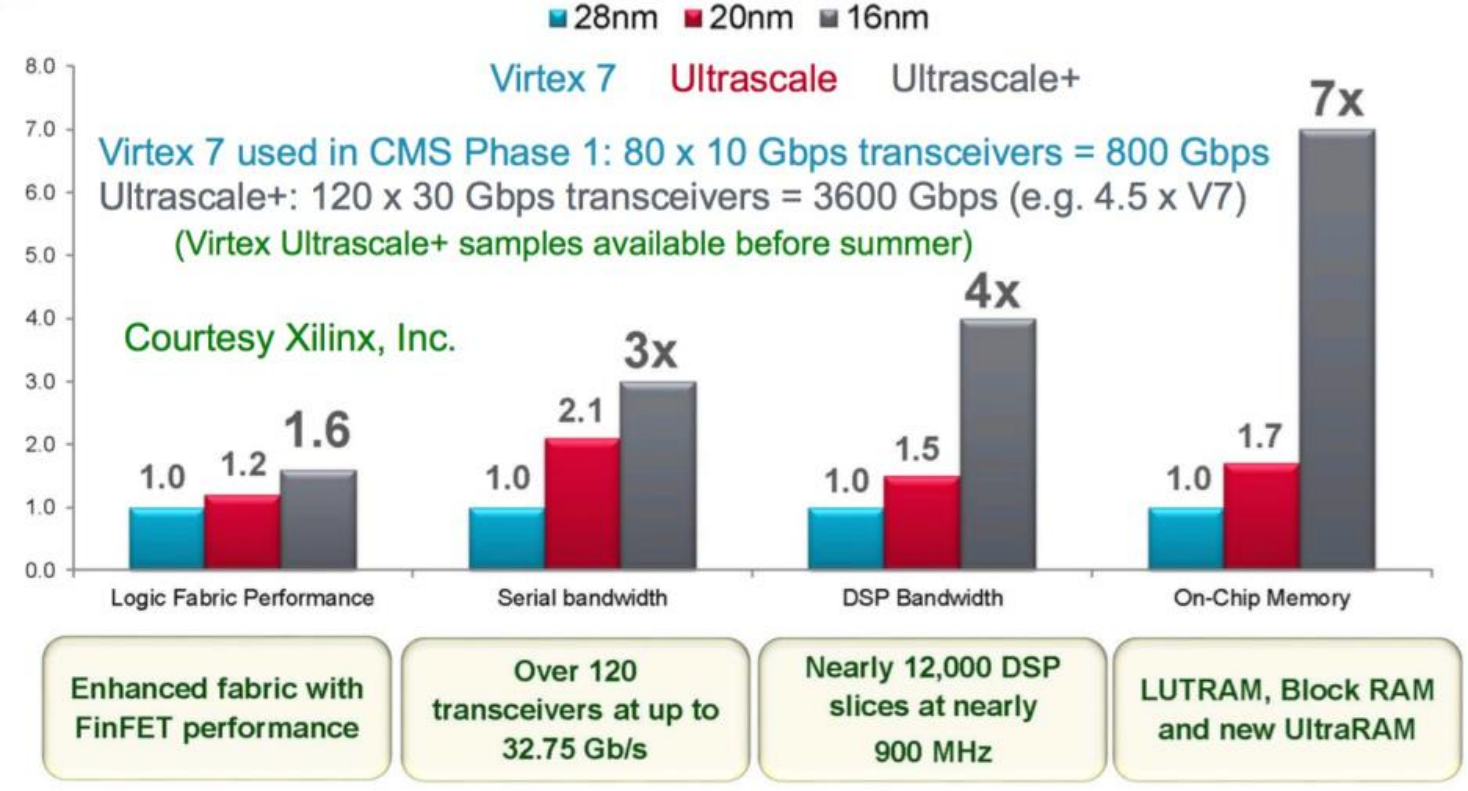
Fig 3: Xilinx FPGA Enabled by SSI Technology*

*: *UG872 Large FPGA Methodology Guide*

Key design challenges...

- Throughput is increasing almost 9 times (0.28 to 2.41 Tbps) per board compared to the Phase-1 system.
  - Tackled by employing high-end FPGA devices such as XCVU9P: can handle 3.93 Tbps of bandwidth.

- However, the device capability in terms of logic performance, serial bandwidth, and on-chip memory are not scaling in the same fashion.



ATCA

- Board total Area ~140 in^2 (~12.68” x 11.02”)
- Size advantage over microTCA
  - 50% more area, 100% more front panel
- Power and associated Cooling advantage over microTCA
  - 400% more available power.

- Crate: the 12U (U is rack unit equivalent to 1.75 inches) tall chassis delivers power, backplane connectivity, cooling, and the slots to maintain up to 16 boards.

- Rack: A rack (generally 46U high) delivers a rigid framework abiding up to three shelves.

APd1

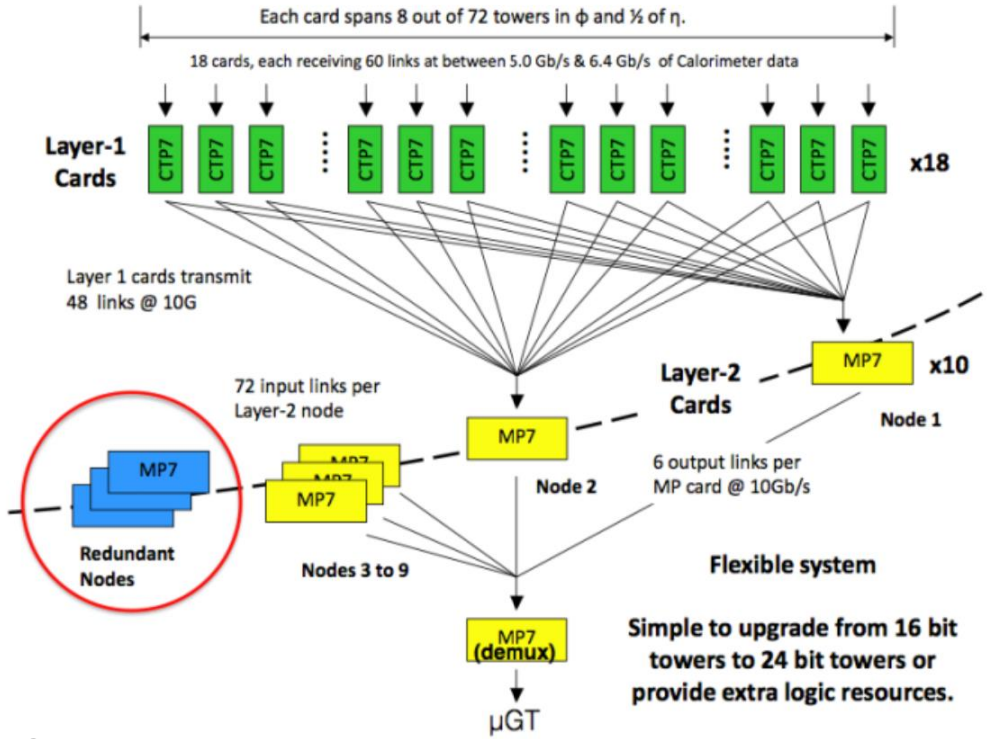
- Controls in the APx are provided by the IPMC and the ELM. The IPMC board is responsible for crate power on/off control
- IPMC also communicate with the crate IPM controller, known as the Shelf Manager.
- Once booted, the ELM Linux system provides configuration and operational support for the platform. This includes initialization of FPGAs
- (bitfile loading and register/memory initialization) and configuration of support devices such as Firefly optical modules

Phase-1 Architecture and its Drawback

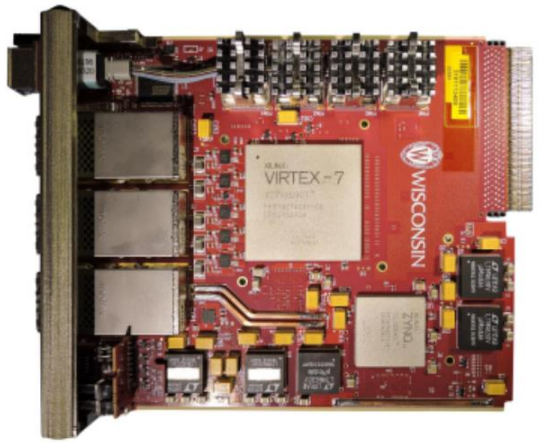
- Current architecture support 6.4 Gbps of link bandwidth which is insufficient to handle the 25 times increase in input granularity.
- The current architecture lack the support for the new radiation hardened HGCAL trigger.
- The FPGA in CTP7 board viz. Xilinx Virtex-7 is unable to satisfy the demand of the Phase-2 calorimeter trigger
  - which requires additional MGTs with high bandwidth
  - more logic capacity in terms of
    - LUTs
    - FF and
    - DSPs
- On the algorithm side, the current system works over the tower's granularity
  - requires redesigning to work on more precise input, such as ECAL crystals.
  - The current doesn't support the particle-flow (PF) clustering vital for the PF algorithm at the correlator trigger.

Phase-1 Architecture and its Drawback

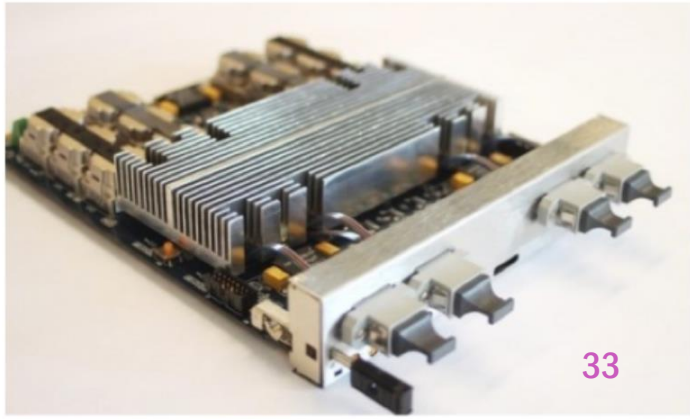
- Input primitives: ECAL, HCAL, and HF tower
- Input bandwidth of 6.4 Gbps.
- Organized in two layer
  - Calo Layer-1 using 18 Calorimeter Trigger Processor board (CTP7).
  - Calo Layer-2 using 10 Master Processor (MP7) board.
- Layer-1 adopted the regional architecture approach
  - Each board process one phi segment of the detector.
  - Employs identical algorithm.
- Layer-2 adopted the TM approach and works in TMUX9 scheme.
  - One MP7 board for demultiplexing before sending the final output to GT.



CTP7 board



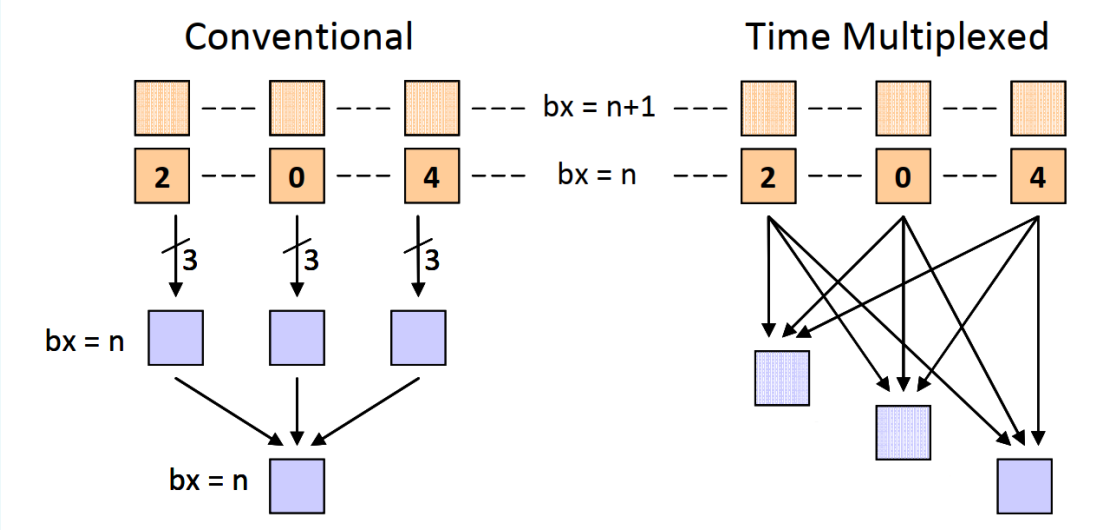
MP7 board



Architecture choices

Regional approach

- FPGA boards parallelly process the detector geometry (a segment of the detector) to every bunch-crossing.
- Each board employ similar algorithms.
- May require sharing of data between the FPGAs to process the overlapping region.



Time-multiplexing (TM)

- FPGA boards run identical/different algorithms on different time slice.
- The TMUXN (where N is a natural number) denotes the round-robin scheduling interval of the trigger processing board.
- Requirement for data duplication can be eradicated.
- The data arrive and are processed over a more extended time than the regional approach.

Design flow – from emulator to hardware

- The trigger algorithms are implemented by using a high-level synthesis tool
  - Rapid prototyping
  - Codes are written in C++
  - HLS Synthesis: generate the HDL
- Provide of latency and very early estimate of resource utilization
- Can implement (place and route) the design without any pin constraint.

Integration of the algo with the APx firmware shell (FS) that provides

- Serial link instantiation (MGT hard block).
- LHC clock connectivity
  - Trigger timing and control distribution (TCDS)
- AXI interface to the controlling system
- Support to test and ILA debug the design
  - Playback (input) and capture (output) long buffer
  - Able to emulate 113 bunch-crossing of LHC data.

ALGO

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	4.17	2.917	1.25

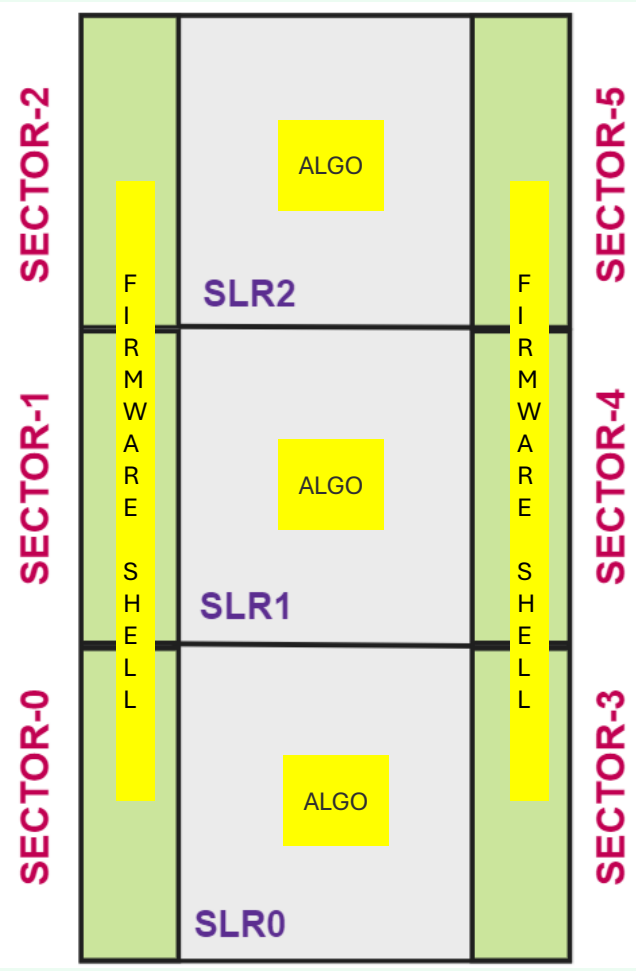
Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
158	158	6	6	function

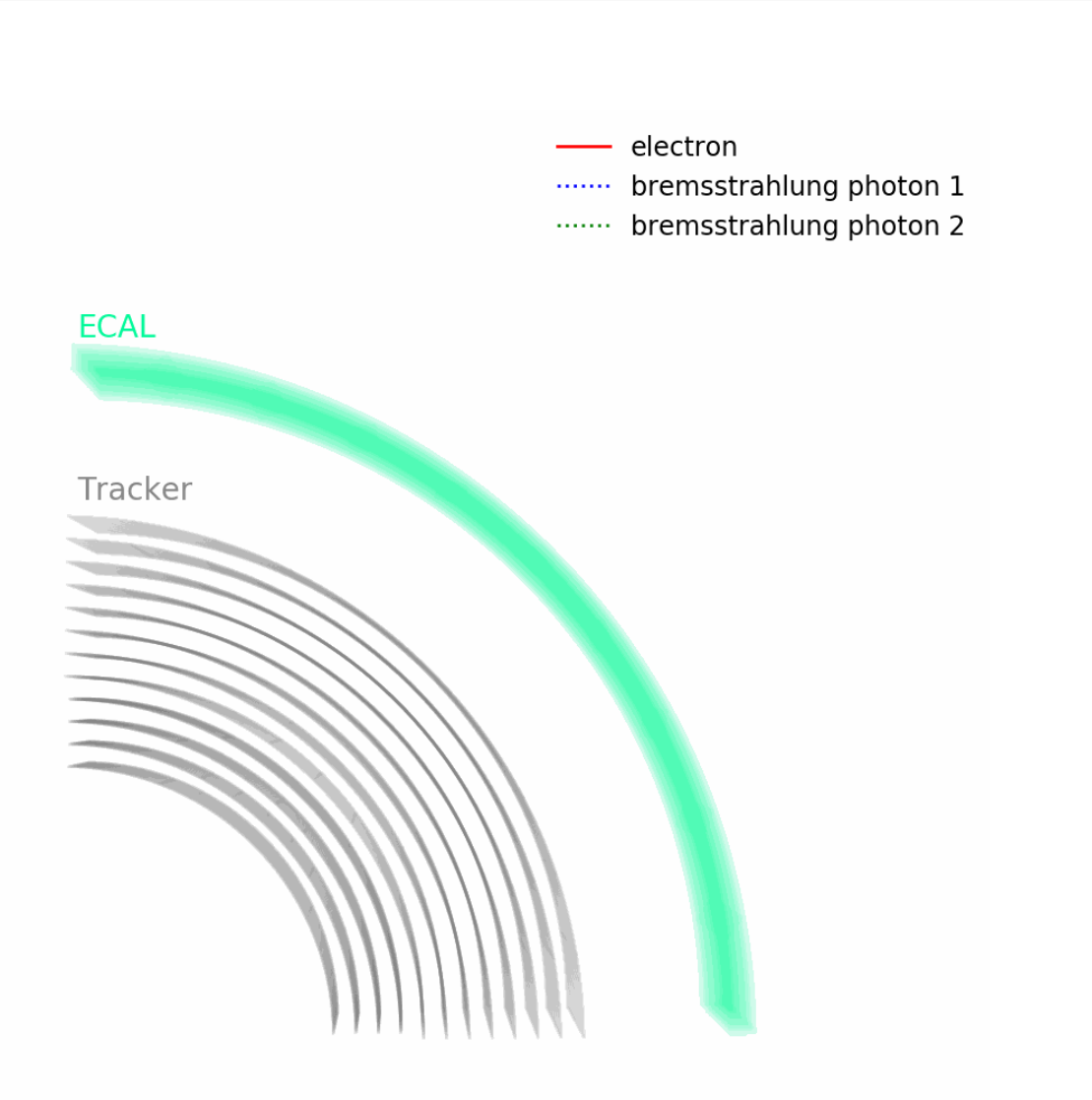
Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	520	-
FIFO	-	-	-	-	-
Instance	0	0	280881	397283	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	12656	-
Register	0	-	7808	512	-
Total	**0**	**0**	**288689**	**410971**	**0**
Available	4320	6840	2364480	1182240	960
Available SLR	1440	2280	788160	394080	320
Utilization (%)	**0**	**0**	**12**	**34**	**0**
Utilization SLR (%)	**0**	**0**	**36**	**104**	**0**



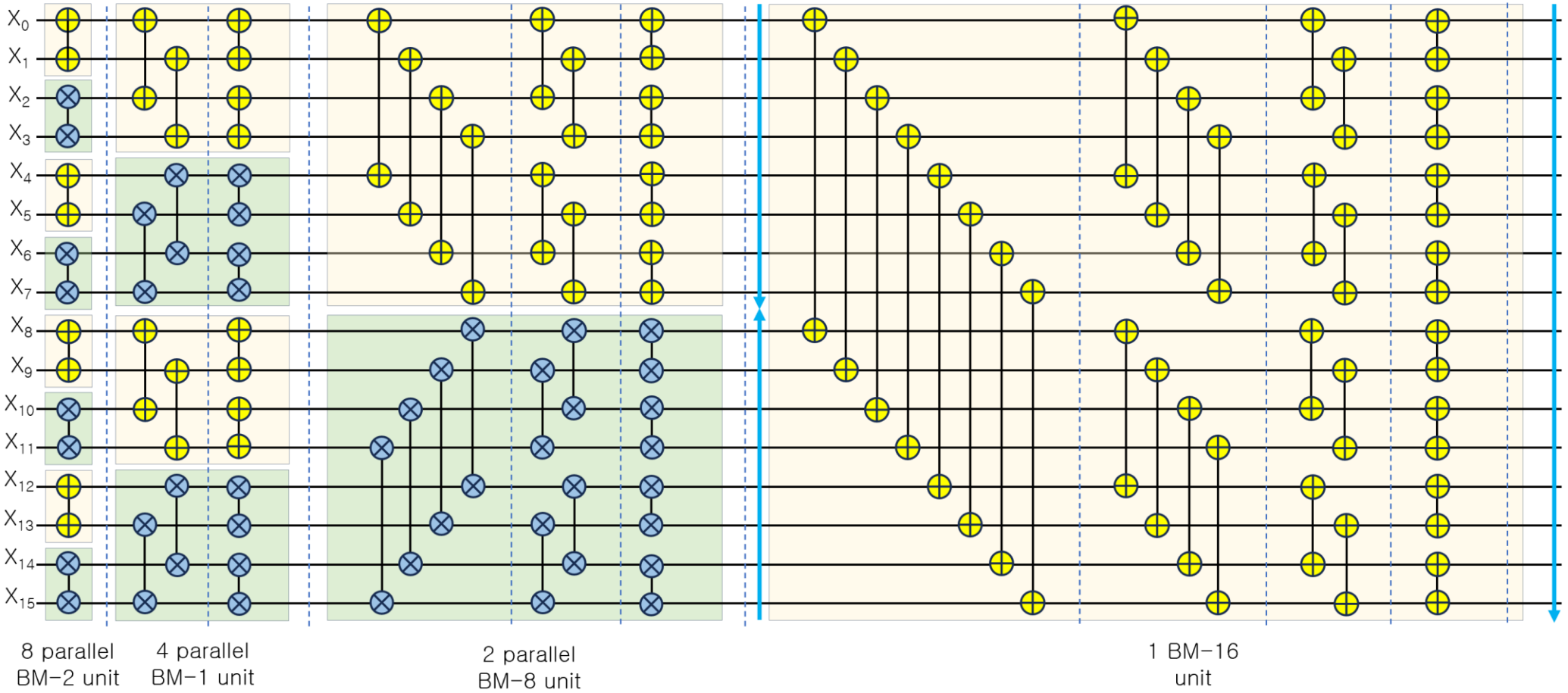
RCT v2.0 IP1

- Primary cluster function
  - Region: 19x24
  - Creating 3x5, 2x5, and 5x5 cluster
  - This computation is done by calculating the energy of the five strips in the eta direction
  - As the peak position can be arbitrary in the crystal space
  - The overall latency is 6 clock cycles.



RCT v2.0 IP2

- A 16-input bitonic sorting unit is used.
- 10 CAE level.
- Considering the unit is pipelined such that the individual stage takes one clock cycle, it can render the sorted results in 10 clock cycles and can initiate a new sort each cycle



IP2

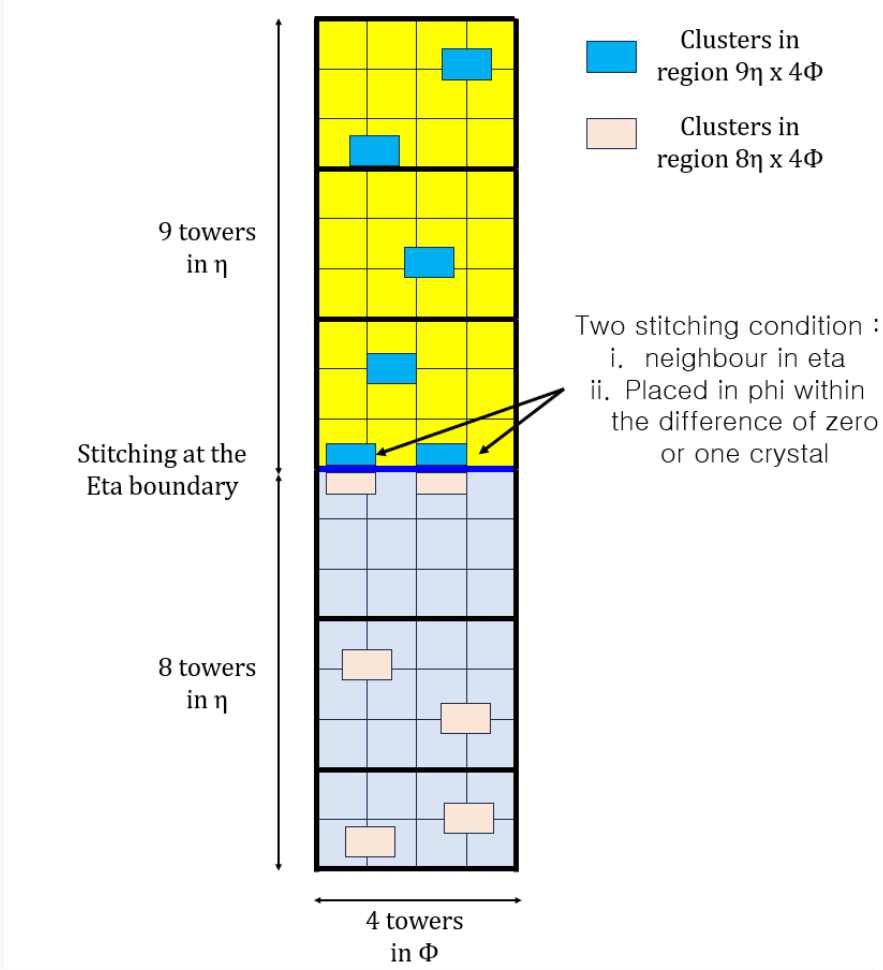
- Two output links
- Each output link carries
  - 18 towers and
  - 3 cluster information
- The latency measured for IP2 is 62 clock cycles.
- Standalone implementation results
  - F_{MAX} : 368 MHz
  - LUTs: 3%
  - FFs: 2%

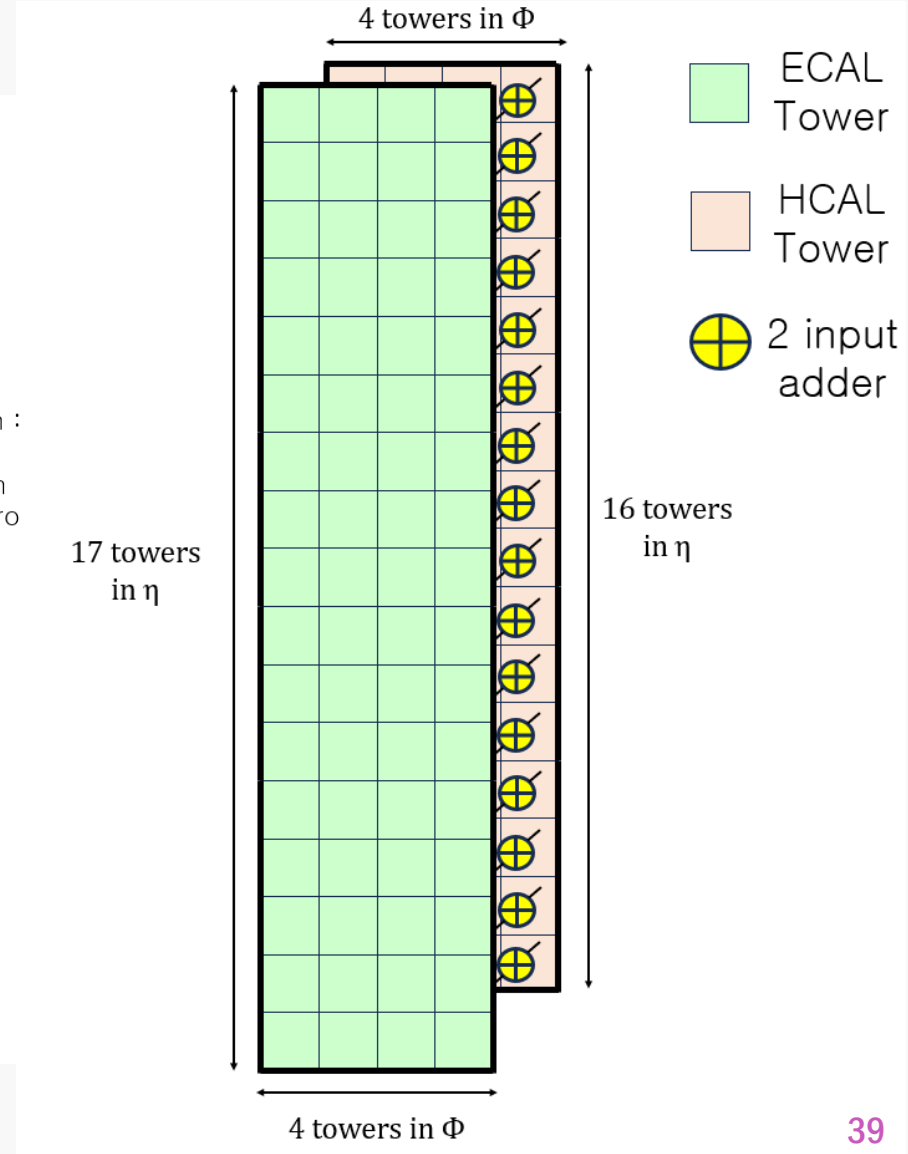
Algo component	Latency (clock cycles)
Stitching clusters	4
16 input bitonic sort	9
Total latency	62

Algorithm post place and route	Utilization and F_{MAX}
LUT	3%
FF	2%
F_{MAX}	368 MHz

IP3

- Receives the information from the IP2 of both the subregions and HCAL towers.
- Perform the stitching of the clusters at the central eta boundary
- Sort the 12 clusters from both the sub-regions using the *bitonic sort* algorithm.
- The final merging of the ECAL and HCAL tower is
- Packs 4 output links to the GCT. With 17 towers and 2 clusters of information per link.





RCT v2.0 IP3

- The merging of ECAL and HCAL also includes the calculation of H/E.
  - HCAL and ECAL energy ratio.
- The H/E calculation is stored in 4-bit.
- The LBS bit indicates the possibility that either the ECAL or HCAL energies are zero or
  - HCAL energy is greater than or equal to the corresponding ECAL tower energy.
- A logarithmic scale is employed
  - cover a wide range of differences between the HCAL and ECAL energy profiles
- Packs 4 output links to the GCT. With 17 towers and 2 clusters of information per link.

Algorithm post place and route	Utilization and F_{MAX}
LUT	5%
FF	4%
F_{MAX}	364 MHz

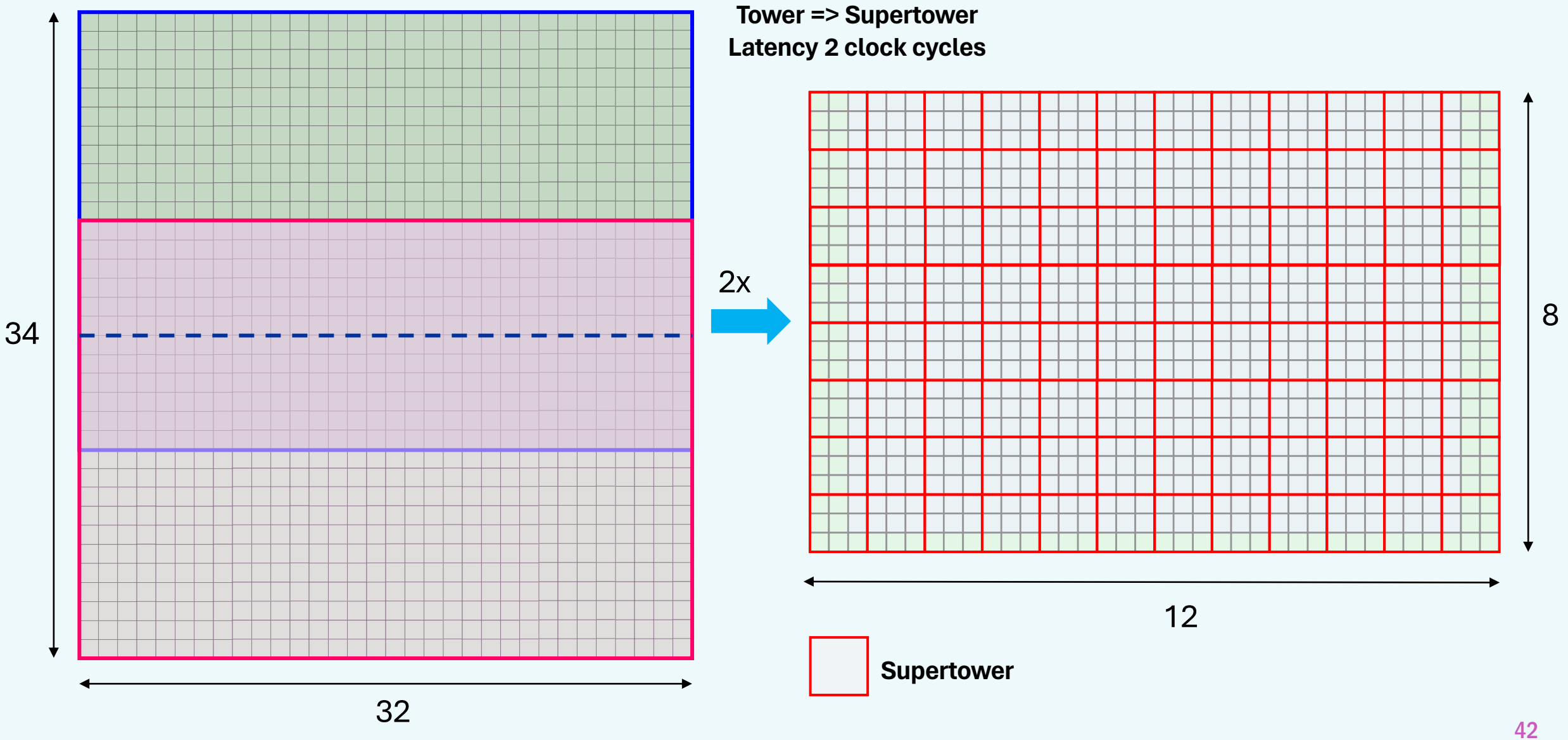
Algo component	Latency (clock cycles)
Stitching clusters	23
Cluster merging with tower	72
Bitonic sorting	9
HCAL and ECAL merging with H/E calculation	8
Total latency	125

RCT v2.0 Summary

Algo component	Latency (clock cycles) and F_{MAX}
IP1 F_{MAX}	152 364 MHz
IP2 F_{MAX}	64 368 MHz
IP3 F_{MAX}	125 364 MHz

Algorithm post place and route	Utilization
IP1 LUTs FFs	 24% 14%
IP2 LUTs FFs	 3% 2%
IP3 LUTs FFs	 5% 4%

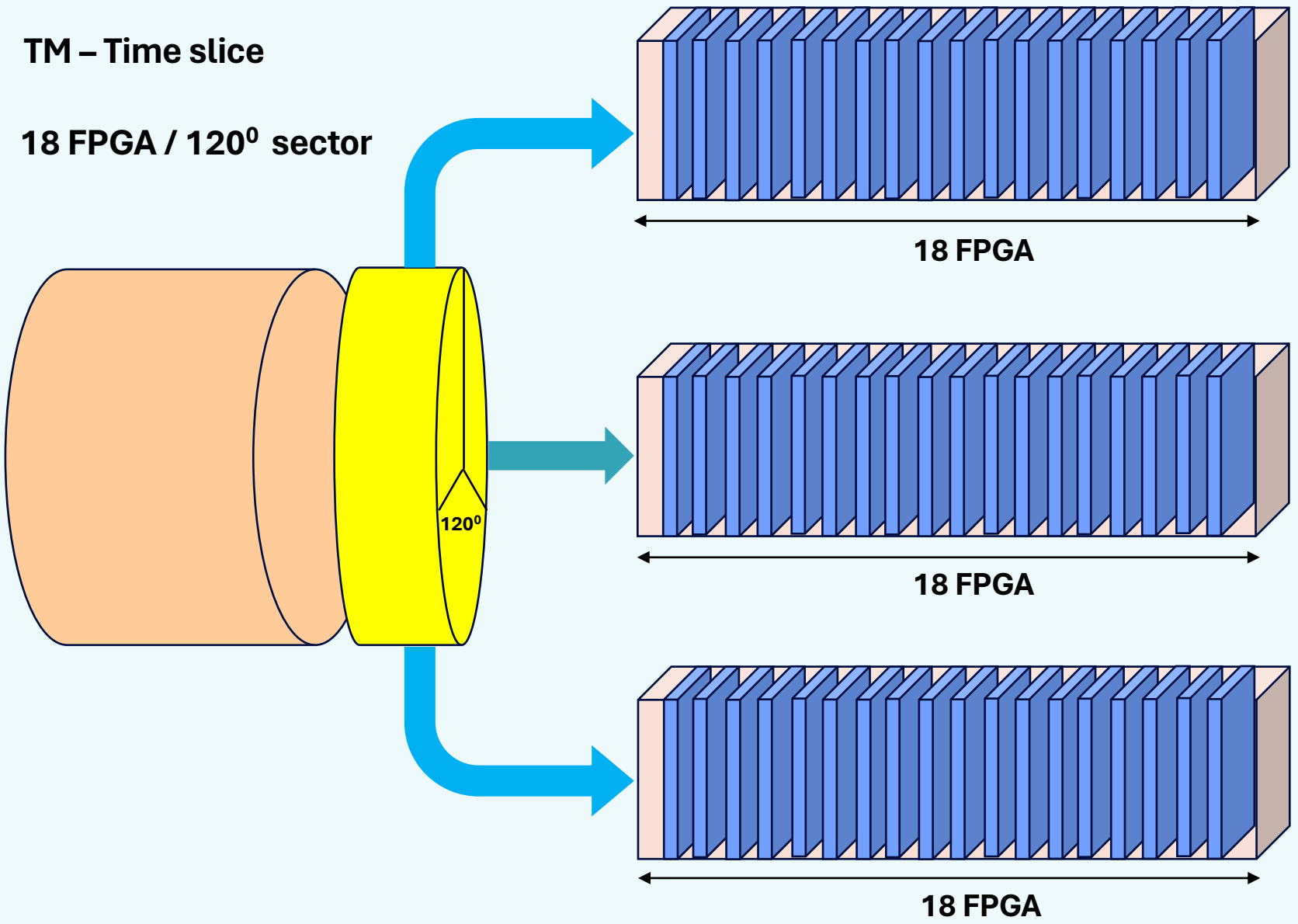
Global Calorimeter Trigger (GCT) Barrel



Global Calorimeter Trigger (GCT) Endcap

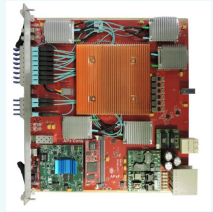
TM – Time slice

18 FPGA / 120^0 sector



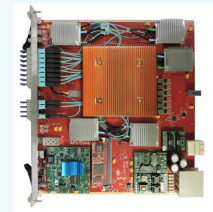
CONNECTIONS

TM 0	SLR3	TM 9
TM 1	SLR2	TM 10
TM 2	SLR1	TM 11
	SLR0	

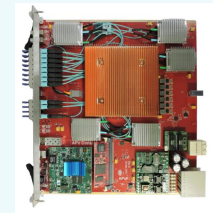


3 APx FPGA

TM 3	SLR3	TM12
TM 4	SLR2	TM13
TM 5	SLR1	TM 14
	SLR0	



TM 6	SLR3	TM15
TM 7	SLR2	TM16
TM 8	SLR1	TM17
	SLR0	



Continue...

VHDL based design

360 MHz clock with
9 words / BX

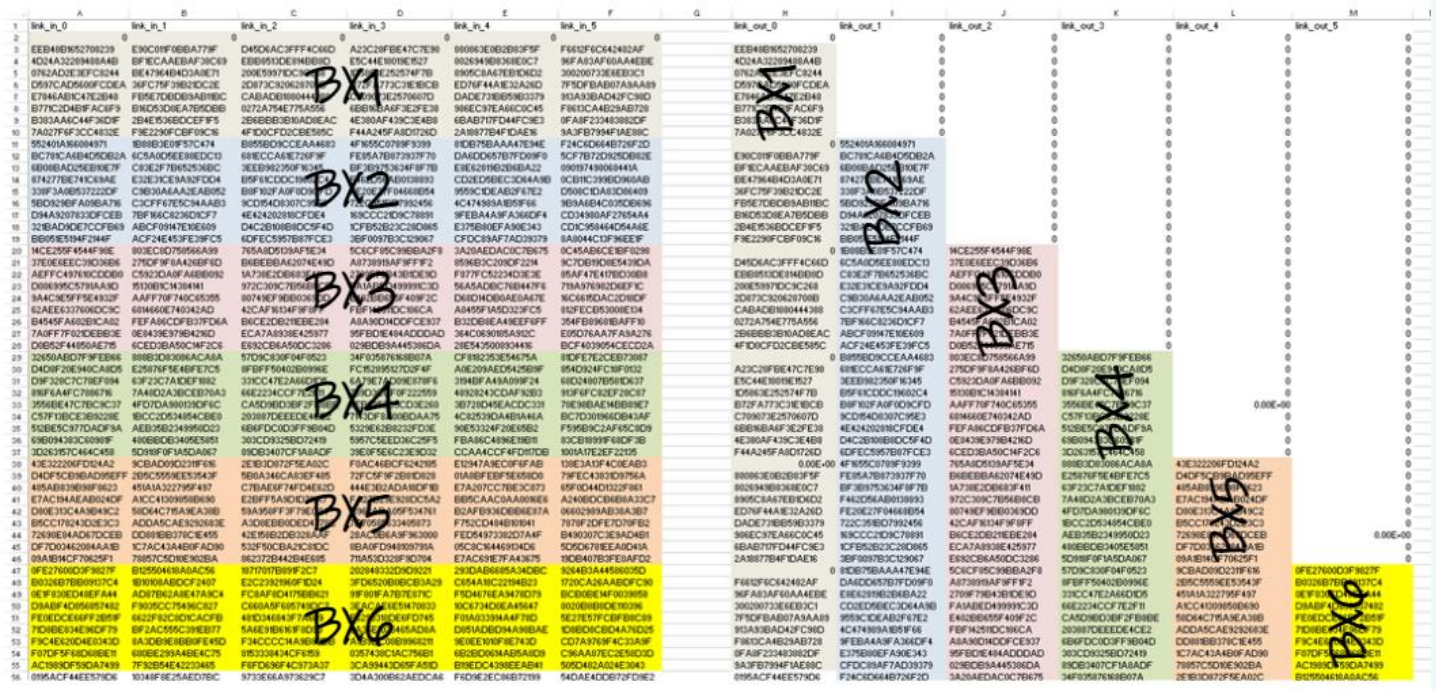


Fig 2: RTL simulation

Latency: 2 clock cycle

Utilization Post-Synthesis | **Post-Implementation**

Graph | **Table**

Resource	Utilization	Available	Utilization %
LUT	6592	1182240	0.56
FF	21162	2364480	0.89

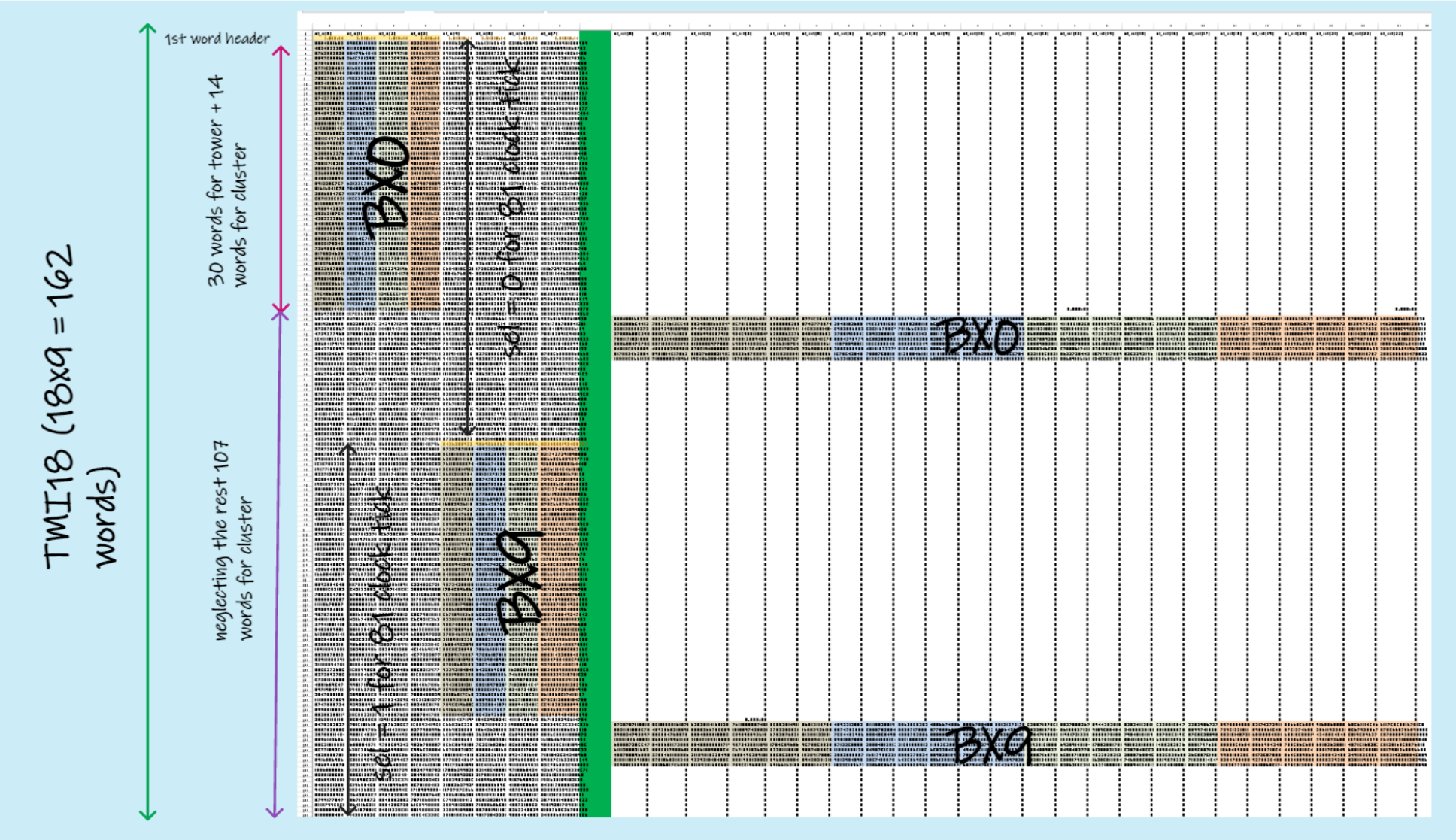
Timing **Setup** | Hold | Pulse Width

Worst Negative Slack (WNS):	0.154 ns
Total Negative Slack (TNS):	0 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	21549

Implemented Timing Report

Fig 3: synthesis and implementation results

Continue...


1st word header
30 words for tower + 14 words for cluster
TMI18 (18x9 = 162 words)
neglecting the rest 107 words for cluster
8x0
8x0
8x0

Continue...

- DEMUX code is developed in VHDL
  - 4 input links
  - 24 output links
  - Clock: 360 MHz
- A 2x1 MUX is used to select the input (BX0 and BX9) for the DEMUX IP using a “sel” signal
  - Sel 0: BX0
  - Sel 1: BX9