A Real-time An FPGA-based ADC for PET module applications

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INTRODUCTION

Positron emission tomography (PET) is an imaging technique that detects the distribution of positron drugs in the body through electron pair annihilation. The traditional circuit design around analog-to-digital conversion (ADC) chips is usually complex and the circuit size is relatively large. The FPGA-based ADC (FPGA-ADC) is a soft-core ADC implemented in an FPGA. Based on the consideration of high integration, it is a good choice to use the FPGA-ADC to achieve a waveform digitizer. The FPGA-ADC can greatly reduce the size of front-end electronic if applied in data acquisition (DAQ) systems.

STRUCTURE OF PET MODULE

The block diagram of the PET detector evaluation based on the FPGA-ADC technology is shown in Fig. 1.

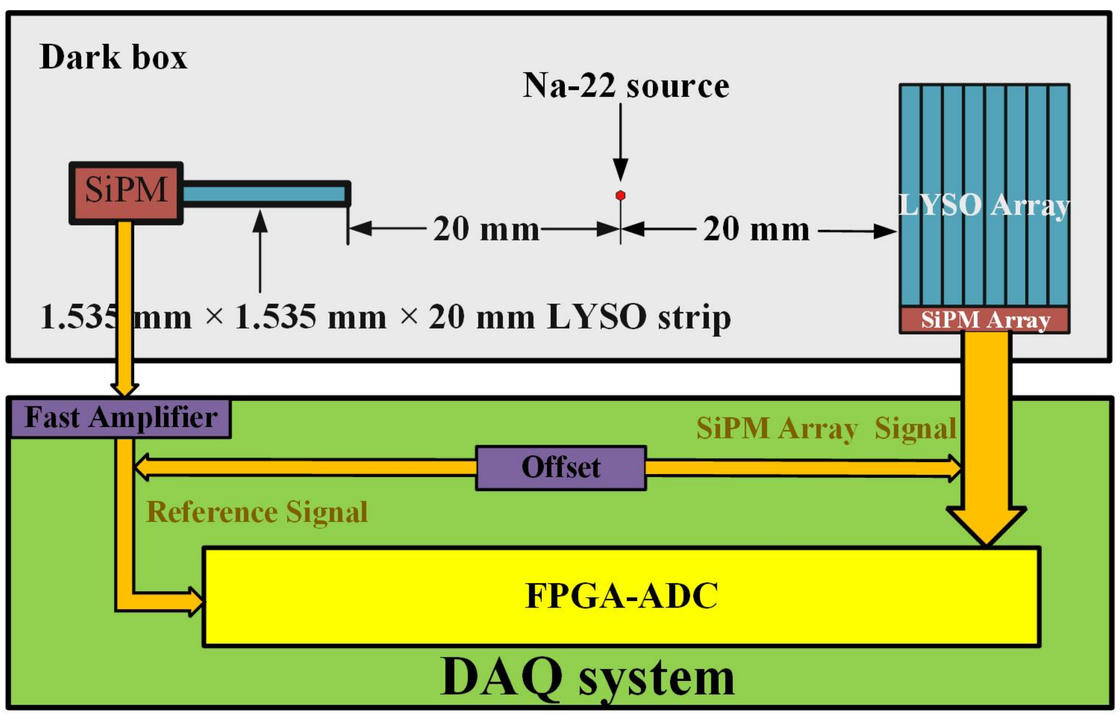

Figure. 1. The block diagram of PET module.

The PET Prototype consists of two parts:

a) the PET detector module as shown in the dark box.

b) the DAQ system based on FPGA-ADC technology.

The PET detector consists of a SiPM array and a LYSO array. In addition, a reference detector with a good timing performance is used for timing measurement of the PET detector module. Signals of the PET detector is sampled by 16 FPGA-ADCs channels while the signal of the reference detector is obtained using only one channel. Totally, 17 FPGA-ADCs channels are developed in the DAQ system. Note that all processing units such as trigger and data buffering are implemented in the FPGA.

FPGA-ADC

The basic block diagram of the FPGA-ADC scheme is shown in Fig. 2. The hardware of the FPGA-ADC consists of an external clock generator, an external resistor RREF and an FPGA.

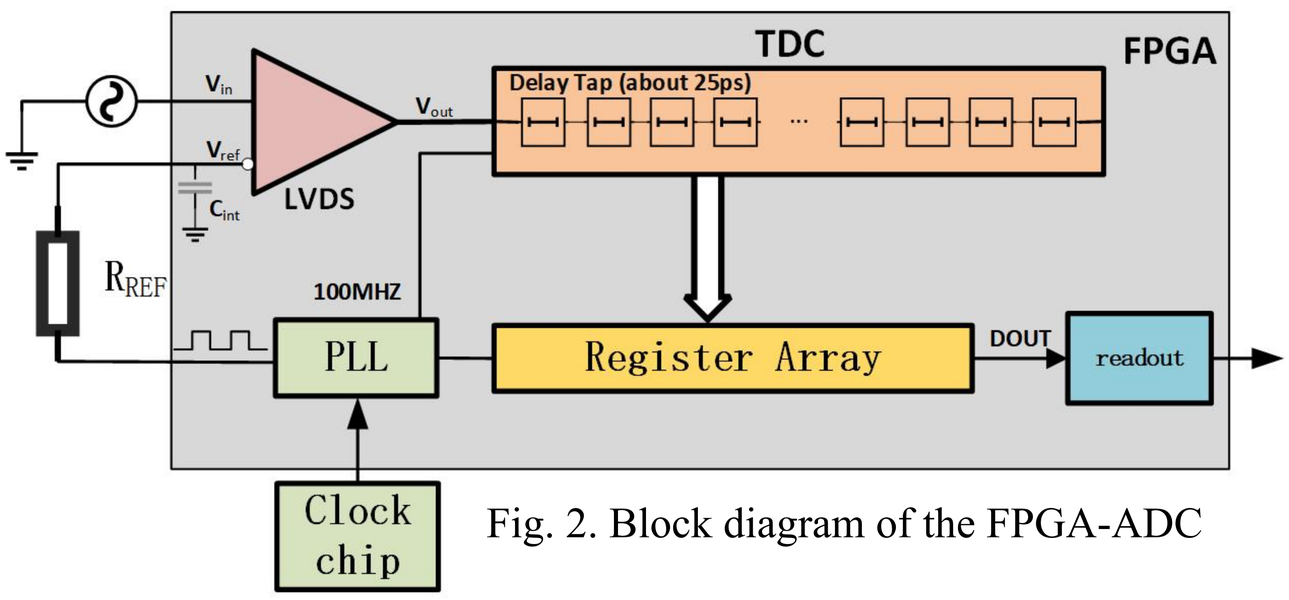

Fig. 2. Block diagram of the FPGA-ADC

All the modules of the FPGA-ADC are implemented in the FPGA, which include a LVDS receiver, a TDC and a phase-locked loop (PLL).

A. PLL

The PLL receives the reference clock and generates another clock signal that is sent to the RC filter network.

B. LVDS receiver

The external resistor R_{REF} and the parasitic capacitance C_{INT} of a LVDS receiver in the FPGA constitutea RC filter network. The ramp waveform V_{REF} is generated at the inverting input when the clock signal is input into the RC filter.The LVDS receiver that serves as a comparator is applied to compare an analog signal with the ramp waveform and output a pulse signal.

C. TDC

The time pulse is approximately proportional to the sampled voltage value. The delay tap based TDC is used to achieve a fine-time interpolation, corresponding to amplitude quantization of the ADC. After calibration, the time information is ultimately converted into the voltage of the sampling point.

PET DETECTOR

In this PET module, detector part will use a 15×15 LYSO array coupled with an 8×8 SiPM (J-series, from ON Semiconductor) array as shown in Fig.3 (a). Between crystals are the enhanced specular reflector (ESR).

A row/column summation-based signal multiplexing method is applied to reduce the pressure on readout electronics. Taking the anode signal as an example, SiPM anodes located in the same column are summed to form eight-column signals, which is shown in Fig.3 (b).

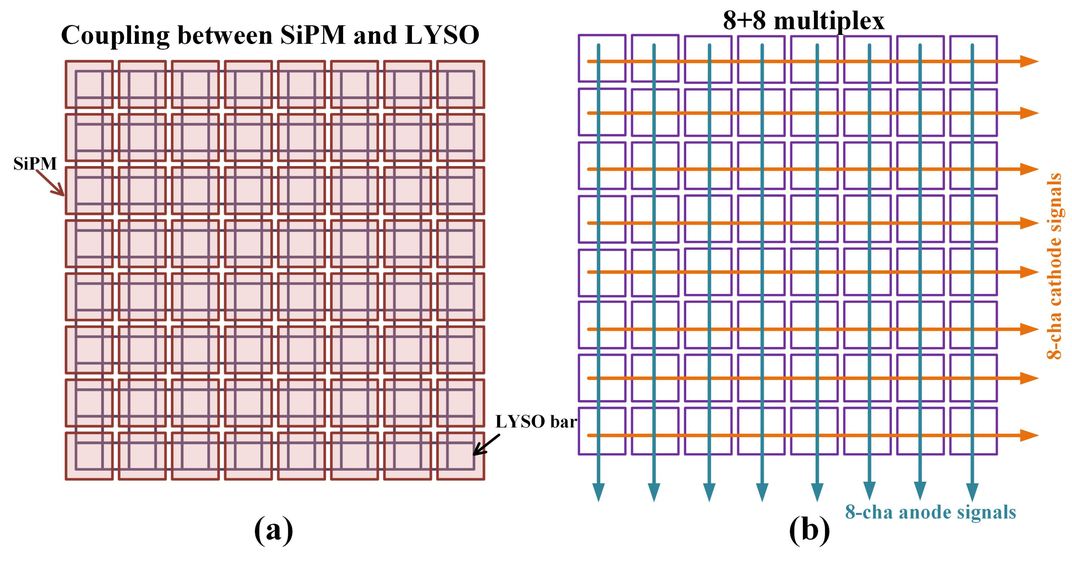

Figure. 3. (a) Coupling and (b) 8+8 multiplex of the PET detector

FPGA-ADC PERFORMANCE

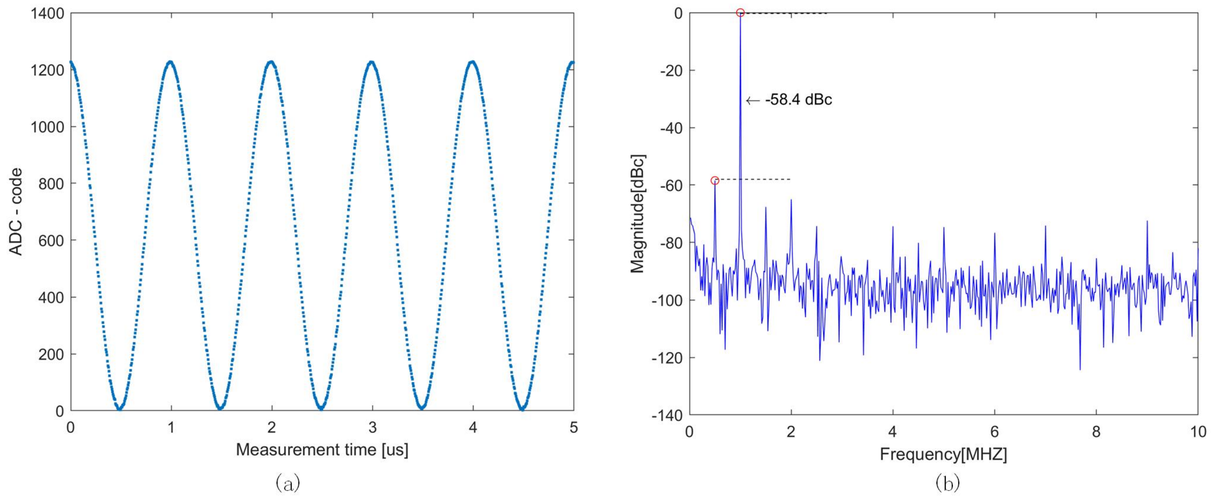

Figure. 4. (a) 1 MHz sinusoid sampled at 200 MS/s (b) the sinusoid in frequency domain.

The plot in frequency domain that corresponds to the sine wave signal in time domain shown in Fig. 4 (a) is obtained using a fast fourier transform (FFT) as illustrated in Fig. 4 (b). In the Fig. 4 (b), the spurious-free-dynamic-range (SFDR) is indicated. At low frequencies, the ENOBs are close to 7 bits.