Study on Readout Electronics of CEPC Scintillator Analog Hadronic Calorimeter Prototype

Zhongtao Shen, Shubin Liu, Anshun Zhou, Hao Liu, Yukun Shi and Yunlong Zhang

***Abstract*—Circular electron positron collider (CEPC) is proposed to research Higgs and particle flow algorithm (PFA) is expected to be adopted to get a high energy resolution. As a PFA calorimeter, CEPC hadronic calorimeter (HCAL) features fine granularity, which necessitates high integration, low noise and low power consumption in readout electronics. The scintillator-based analog hadronic calorimeter (AHCAL), one of the PFA HCAL technical approaches, has been studied.**

In this paper, a readout system of CEPC AHCAL prototype is designed and implemented. The system can not only read the signals of high-density SiPMs, but also calibrate SiPM gain and monitor temperature. Testing of the electronics demonstrates that the noise and dynamic range performances meet the requirements.

Following mess production and prototype integration, cosmic ray tests and beam tests are conducted, with all results verifying the functionality and performance of the readout system.

***Index Terms*—Readout electronics, CEPC, AHCAL, SiPM.**

I. Introduction

As a Higgs and Z factory, circular electron positron collider (CEPC) has been proposed to precisely measure Higgs and Z bosons and study their properties [1]. For high-resolution energy measurement, the detector incorporates the particle flow algorithm (PFA) [2 – 4] with a precision vertex detector, a time projection chamber, a silicon tracker, a high-granularity electromagnetic calorimeter (ECAL), a high-granularity hadronic calorimeter (HCAL) and a muon detector. This paper discusses the scintillator-based analog hadronic calorimeter (AHCAL), a type of PFA HCAL, and especially its prototype readout electronics.

As shown in Fig. 1, the AHCAL prototype is a 40-layer calorimeter and each layer contains an absorber sub-layer and a sampling sub-layer. Each sampling sub-layer consists of 324 plastic scintillators as sampling materials, each measuring 40 mm × 40 mm × 3mm plastic, giving a total active area of 720 mm × 720 mm [5, 6]. At the bottom of each scintillator, there is a silicon photomultiplier (SiPM), responsible for light-to-charge conversion. As shown in Fig. 2, in the sampling sub-layer, scintillators and SiPMs are mounted on one side of a PCB board, while the readout electronics of SiPMs are mounted on the other side.

Manuscript received in May 20, 2024, revised XXX.

This work was supported in part by National Key Program for S&T Research (Grant NO.: 2018YF0404303), in part by the National Natural Science Foundation of China (Grant NO.: 12025504) and in part by the State Key Laboratory of Particle Detection and Electronics (Grant No. SKLPDE_ZZ_202019).

The main function of readout electronics is to measure the signals from SiPMs. According to the Monte-Carlo simulation, the range of energy deposition in one scintillator is 1 – 240 MIPs [6] and testing results indicate the light yield is about 17 p.e./MIP [7 - 9]. With an SiPM gain of 3.6×10^5 (S14160-1315 from Hamamatsu [10]), the dynamic range is 980 fC to 235 pC, and the electronics noise should be lower than 980/3 fC.

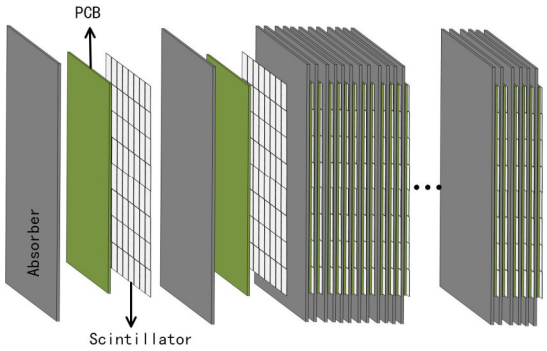

Fig. 1. Perspective view of CEPC AHCAL prototype

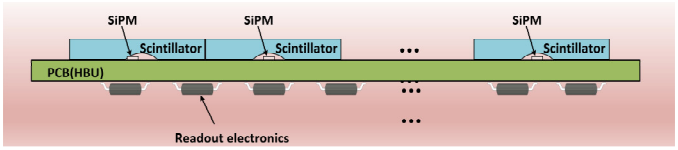

Fig. 2 Cross section of one sampling sub-layer

II. System Architecture of Readout Electronics

The readout structure of the AHCAL prototype is shown in Fig. 3. The system consists of 40 HCAL Basic Units (HBU), 40 Data Interface Boards (DIF), a Data Acquisition Board (DAQ) and a data server. The HBU, shown in Fig. 2, is the PCB board discussed before, which carries SiPMs and scintillators on one side and readout electronics on the other. The DIF board, which interfaces between the HBU and the DAQ, contains an FPGA chip for controlling the readout electronics on HBU and communicating with DAQ. Additionally, each DIF includes a high-voltage (HV) supply circuit to provide bias voltages for the SiPMs on the corresponding HBU. The DAQ board, which connects to all DIFs, is responsible for powering, sending commands to and receiving data from the DIFs.

Corresponding author: Shubin Liu.

Zhongtao Shen, Shubin Liu, Anshun Zhou, Hao Liu, Yukun Shi, Yunlong Zhang and Jianbei Liu are with State Key Laboratory of Particle Detection and Electronics, and Department of Modern Physics, University of Science and Technology of China, No.96, Jinzhai Road, Hefei, 230026, China (e-mail: liushb@ustc.edu.cn; henzt@ustc.edu.cn).

A USB type-C cable is used for scientific data transmission and power supply between the one DIF board and the DAQ board. It is important to note that the type-C cable is only used for physical connecting and the type-C protocol is not adopted in the AHCAL readout system. In the type-C cable, power supply wires are used for powering the DIF, two data lanes for data and command transmission, and four differential lanes are used for clock, trigger, hit and busy signals.

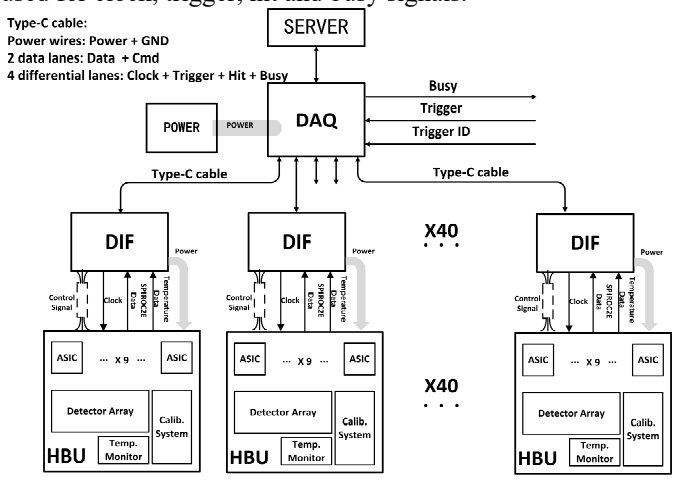

Fig. 3. Readout structure of the CEPC AHCAL prototype

III. Front-end Electronics Design

The main function of the front-end electronics is to read out signals from a single sampling layer. Due to the basic structure of the sampling layer, one DIF and one HBU board complete the front-end readout, as shown in Fig. 4.

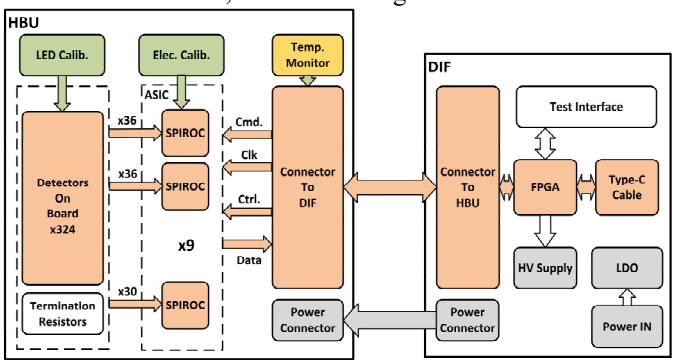

Fig. 4 Structure of HBU coupled with DIF

A. HBU design

The sensitive area of the HBU is 720 mm × 720 mm, which is too large to be manufactured as a single unit. Therefore, it is divided into three sub-HBUs, each measuring 240 mm × 720 mm, connected via high-density connectors and flexible printed circuits (FPC) [11], as shown in Fig. 5. Based on the distance from the DIF board, the sub-HBUs are categorized as C (Close to the DIF), F (Far from the DIF), and VF (Very Far from the DIF).

As mentioned before, the HBU carries SiPMs and scintillators on one side and electronic circuits on the other. Considering the demands of high integration, an Application-Specific Integration Circuit named SPIROC [12] is selected for reading the SiPM signals. Each sub-HBU board is integrated with 3 SPIROCs to cover 108 channels of SiPM, resulting 9 SPIROCs per sampling sub-layer. Besides the SPIROC-based readout circuits, the board also includes electronic calibration circuits, LED calibration circuits, and temperature monitoring circuits. Details on the LED calibration and temperature monitoring are provided in Section V in this paper.

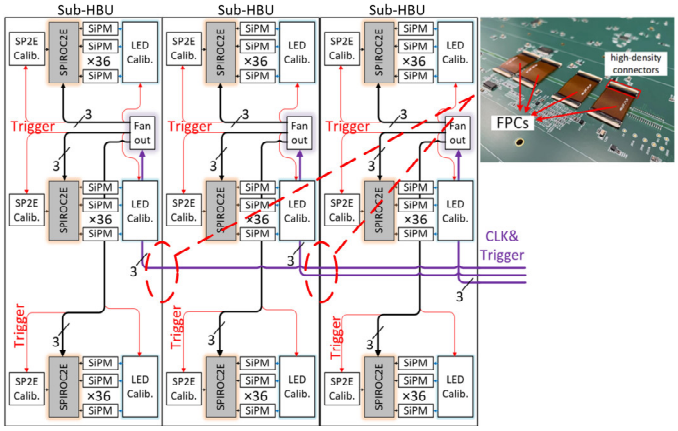

Fig. 5 The structure of the sub-HBUs.

B. DIF design

The primary functions of the DIF board are to analyze the received commands, control the HBU board in real time, readout the Spiroc2Es and to supply power to the HBU board. The DIF board integrates an FPGA, a USB2.0 interface, a type-C interface, an HV chip, four low-dropout regulators (LDOs) and four high-density connectors. The FPGA analyzes commands and configures the various functional circuits on the HBU board. The USB 2.0 interface is used for single-board testing, while the Type-C interface uses a USB 3.1 cable for data transmission and power supply. The LDOs power the HBU board, and the HV chip can be modified in real-time through configuration commands. The high-density connectors facilitate data transmission and power supply to the HBU board.

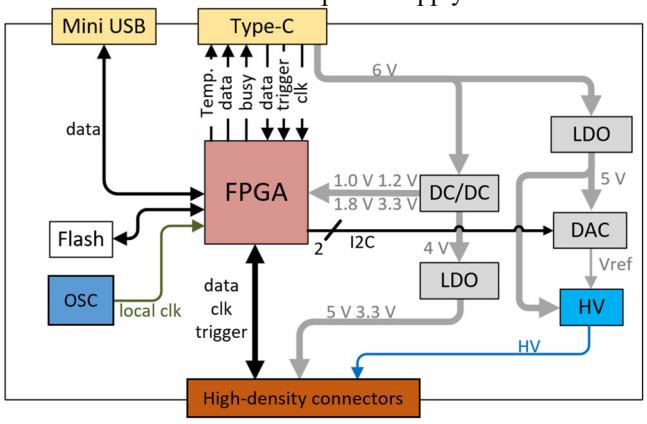

Fig. 6 The strucure of DIF board.

C. Electronics tests

Electronics test are conducted to evaluate the performance of the HBU board. Eech SPIROC chip is integrated with 36 input channels and an Analog-to-Digital Converter (ADC), and the

test results are presented as ADC code values. Fig. 7 shows the distribution of the pedestal mean values, ranging from 360 ADC code to 480 ADC code. The saturation position of ADC in SPIROC is above 3000 codes, indicating a dynamic range greater than 2500 codes. Fig. 8 shows the Root Mean Squares (RMS) of pedestals, which is less than 5 ADC codes.

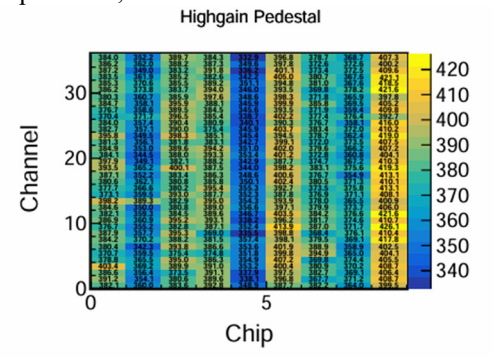

Fig. 7 Mean distribution of pedestals in one layer.

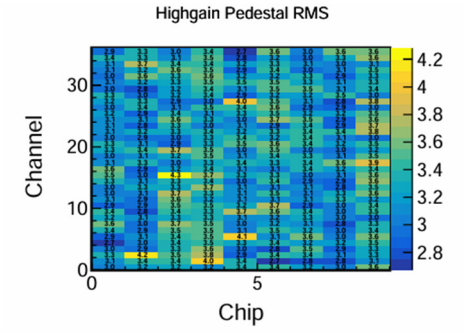

Fig. 8 RMS distribution of pedestals in one layer

Each SPIROC analog channel has two preamplifier circuits with different gains, resulting in two sets of test results correspondingly. Fig. 9 shows the calibration results of gains of all analog channels, with high gains ranging from 140 to 200 ADC code/pC (mean value ~177.4 ADC code/pC) and low gains ranging from 4.5 to 7 ADC code/pC (mean value ~6.18 ADC code/pC).

Based on these results, the performance of the HBU board is determined. The electronics noise of the HBU board is less than 5 ADC codes / 177.4 ADC code/pC = 45 fC, while the dynamic range is greater than 2500 ADC codes / 6.18 ADC code/pC = 400 pC. These results confirm that the HBU board meets the performance requirements.

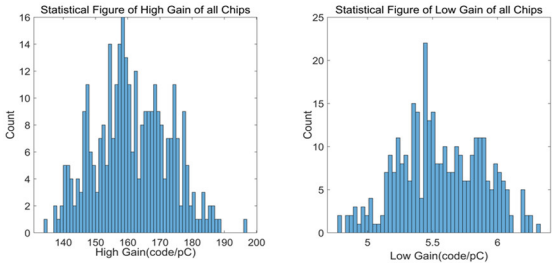

Fig. 9 Calibration result of gain of all analog channels.

IV. Data Acquisition Electronics Design

The scientific data generated by the SPIROCs will be temporarily cached in the FPGA on the DIF boards. Communication between the DIF and DAQ boards is established through USB cables, with data transmission using the AC-coupled LVDS protocol.

The DAQ board is shown in Fig. 10. Its core devices are an FPGA (Xilinx K7) and a jitter attenuator/clock multiplier chip (Si5345). It has 40 USB type-C interfaces to receive data from front-end boards. Data is aligned and packaged in DAQ and then uploaded to the server for stable storage through the optical SFP interface, and the bit rate for communication between DAQ board and the server is 4.8 Gbps.

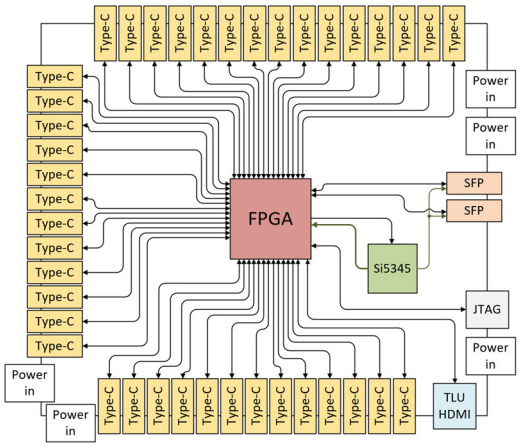

Fig. 10 Structure of the DAQ Board

V. Challenges and Solutions

The gain of SiPMs is temperature-sensitive, requiring a compensation strategy that involves both gain calibration and temperature monitoring. Since no mature solutions exist for similar prototypes, these challenges must be addressed in the electronics design.

A. SiPM calibration

The SiPM calibration is to measure the gain of single photoelectron, and this is finished by an extremely short light pulse (less than 5 ns). As shown in Fig. 11, next to each SiPM, a small LED is placed to do the calibration.

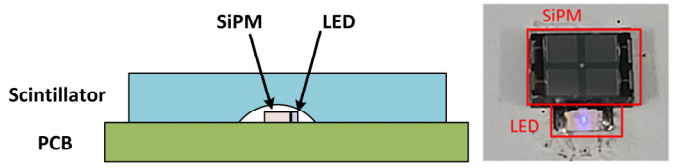

Fig. 11 High integration design of the LED: (left) Structure Diagram, (right) Photograph of the Circuit

Generating a short LED pulse is challenging, and Fig. 12 illustrates a light pulse generation circuit [13]. A quenching signal is introduced to overcome the nonlinearity of the LED. When the switch-on signal activates, the NMOS1 turns on and the LED illuminates, controlled by the DAC. And when the quenching signal activates, the LED is shorted and turns off. By this, the width of the light pulse is not sensitive to the resistor

and capacity of the LED but controlled by the delay line.

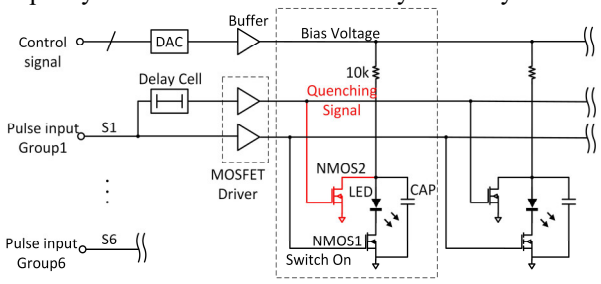

Fig. 12 Light Pulse Generation Circuit

Using this light pulse generation circuit, the single photoelectron peak spectrum (S.P.S) can be obtained. Fig. 13 shows the S.P.S of an SiPM, with peak distance indicating the SiPM gain quantitatively. Furthermore, full-channel calibration results can be obtained by extracting peak spacings from all channels.. Fig. 14 shows the distribution of SiPM gains in one layer, range from 17 ADC code/photoelectron to 35 ADC code/photoelectron.

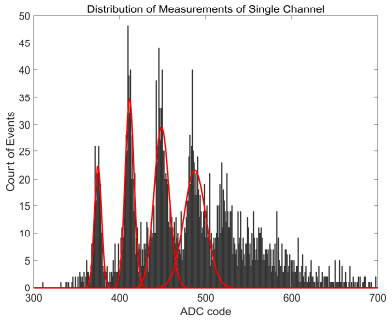

Fig. 13 Single Photoelectron Peak Spectrum of Single SiPM.

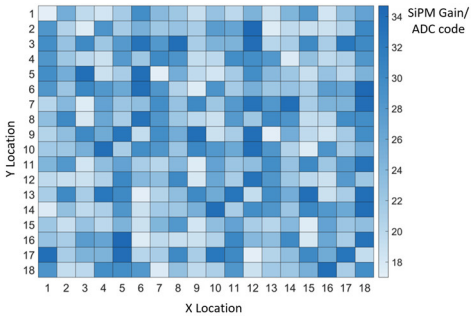

Fig. 14 Distribution of SiPM gains in one layer.

B. *Temperature monitoring strategy*

As for the solution of the SiPM operating temperature monitoring, due to the large number of the SiPMs, the strategy for full-channel temperature monitoring with sparse probes must be discussed to reduce the power consumption and the electronics cost.

In the AHCAL system, kriging interpolation method [14, 15] is adopted to reconstruct the temperature field. By this, temperatures of all SiPMs can be obtained from much fewer temperature sensors. On HBU board, 48 temperature probes are placed at key positions, such as heat sources, connectors and boundaries. Then the interpolation is conducted and the temperature filed of HBU is established, as shown in Fig. 15.

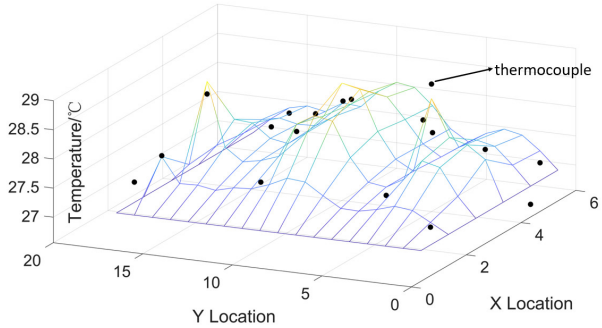

Fig. 15 Reconstruction of the temperature field on HBU and the illustration of thermocouple test.

A test is carried out to learn the performance of this method. As shown in Fig. 15, 18 additional thermocouples are attached on HBU, where there is no temperature sensor. When the HBU works, the temperatures obtained by the thermocouples and by the kriging interpolation method are compared, and the errors turn out to be less than 0.5 °C. In fact, some more experiments are performed, which put the board in different environment temperatures from 20 °C to 45 °C, and the errors are confirmed to be less than 0.5 ° C [15]. These results validate the performance of the kriging interpolation.

VI. Mass Production and Integration

A. *Mass production and electronics tests*

After the electronics design, all 40 layers of front-end boards (DIF boards and HBU boards) and the DAQ board are produced. Electronics tests are carried out to verify the functionality of the readout system, and Fig. 16 and Fig. 17 show the pedestal distribution and the high gain-to-low gain ratio distribution of all 12,960 channels, respectively. The results mean all electronics channels work normally.

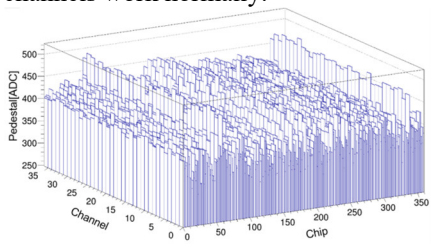

Fig. 16 The pedestal distribution of all 12,960 channels.

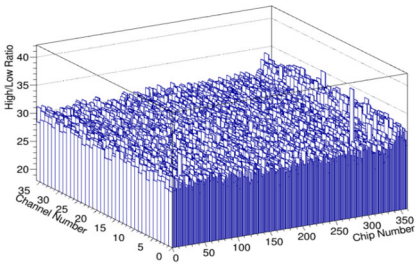

Fig. 17 High gain-to-low gain ratio distribution of all 12,960 channels

B. *Cosmic ray test*

A cosmic ray test is conducted to assess system performance.

For the absorber sub-layers is too heavy to be supported, only 40 sampling sub-layers are used in the cosmic ray test. One DAQ board connects to all 40 DIFs via 40 type-C cables, providing power, control, and data reception. Scientific data are accumulated and packaged in DAQ and then sent to the server. The system trigger is generated by the coincidence of the top and the bottom layer.

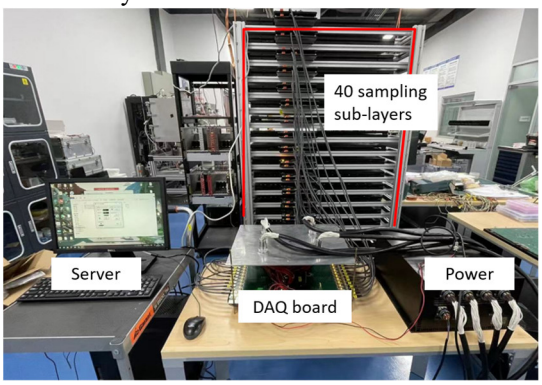

Fig. 18 Cosmic ray test site.

Fig. 19 shows some results of the comic ray test. The left figure shows the track of a cosmic ray event, which proves the data alignment method of the readout system works well. And the right figure is the hit map of one sampling sub-layer, consistent with predictions. Due to low event rates, especially at the edges, MIP calibration is not performed in the cosmic ray test.

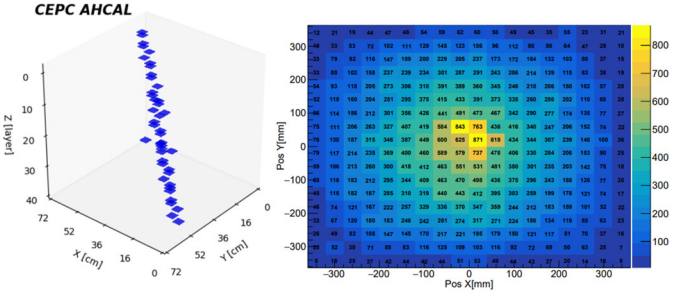

Fig. 19 The left figure shows the track of a cosmic ray event and the right figure is the hit map of one sampling sub-layer.

C. *Prototype integration*

After electronics and cosmic ray tests, all 40 absorber sub-layers and 40 sampling sub-layers are integrated into a support structure. As shown in Fig. 20, the absorber sub-layers and the sampling sub-layers are alternately arranged. The 40 DIFs, which are the main heat sources in the readout system, are placed outside the active areas of the prototype. This is helpful to maintain the SiPM temperatures, and further maintain the SiPM gains. The entire AHCAL prototype weighs about 5 tons and measures approximately 1 m × 1 m × 1.5 m.

Fig. 20 Photo of the AHCAL prototype

VII. Beam Test

To test the performances of CEPC AHCAL, beam tests combined with CEPC Sc-ECAL prototype are conducted in CERN PS and SPS and the test site is shown in Fig. 21. During these tests, pedestals, gains and MIPs of all channels are calibrated, followed by assessments of energy resolution and linearity. The results confirmed the readout system's functionality and performance. and Fig. 22 shows the showers of a 15 GeV Pion event and a 350 GeV Pion event respectively [16].

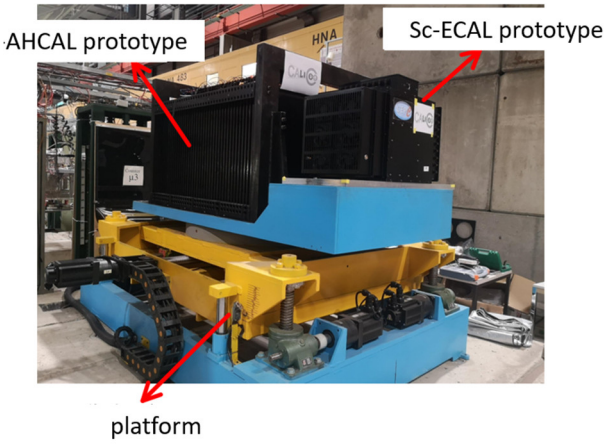

Fig. 21 The photo of beam test site.

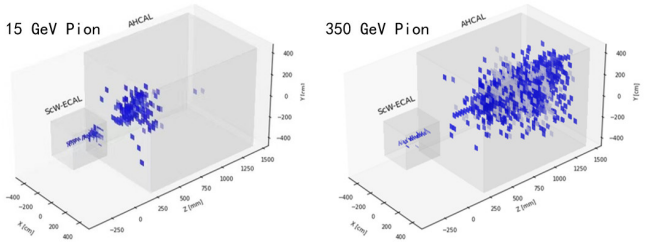

Fig. 22 The showers of a 15 GeV Pion event and a 350 GeV Pion event respectively.

VIII. Summary

This paper describes the design of readout system of CEPC AHCAL prototype, detailing the readout module, especially the readout structure, the light calibration circuit and the

temperature monitoring circuit. The system can not only readout the signals of high-density SiPMs, but also has functions of SiPM gain calibration and the temperature monitoring. The electronics test proves that the noise and dynamic range performances meet the requirements.

After mess production and prototype integration, cosmic ray tests and beam tests are conducted, and all the results confirm the readout system's functionality and performance.

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