24th IEEE Real Time Conference
2024/04/22 – 2024/04/26 – ICISE, Quy Nhon, Vietnam

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Low-power large-dynamic range readout ASIC for VLAST silicon strip detector

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Introduction

The Very Large Area Gamma-ray Space Telescope (VLAST) will be used for physical purposes such as dark matter detection, high-energy time-domain astronomy, gamma-ray horizon, and the origin of cosmic rays. Fig.1 shows the schematic of the VLAST payload, which consists of the Anti Coincidence Detector(ACD), the Silicon Tracker and low Energy gamma-ray Detector(STED), and the High Energy Imaging Calorimeter(HEIC). The primary function of STED is to measure high-energy photon (electron pair) tracks and low-energy Compton effect photons. Single STED array comprises eight super-layers, including eight CsI detection layers and sixteen large silicon strip detection layers, with 344064 channels in total. Each detector channel has a large equivalent capacitance of 100pF. Therefore, the readout chip must meet the large dynamic range, low power consumption, and low noise. Therefore, it is necessary to design a 16-channel low-power, large-dynamic range readout ASIC, named SiReadout, which has been designed for silicon strip detectors on VLAST. This paper will present the design and performance of the SiReadout.

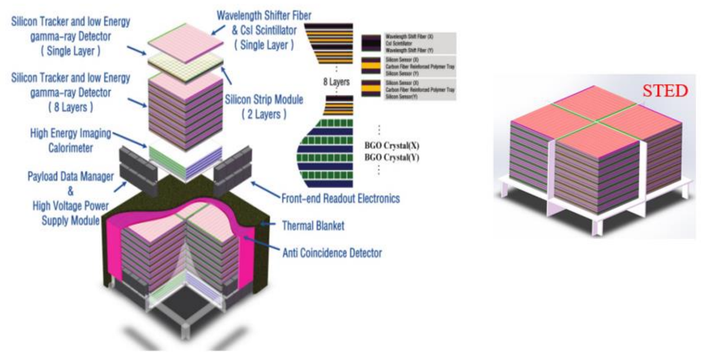


Figure.1 The schematic plot of the payload of VLAST

Overall Structure

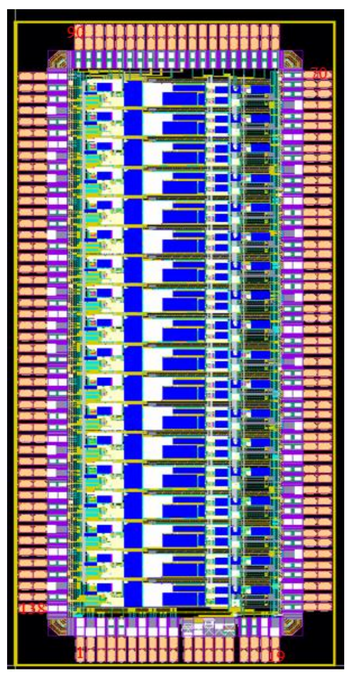


Figure.2 layout of the SiReadout

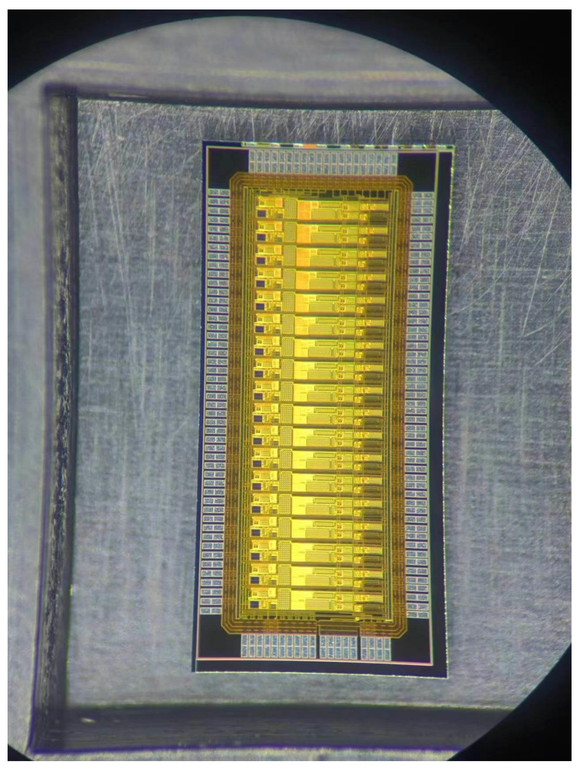


Figure.3 Microphotograph of the SiReadout

Figure.2 shows the overall layout of the SiReadout chip. It consists of 16 channels. Two dummy channels are added to ensure that the parasitic parameters around each readout channel are equal. Moreover, it prevents etching errors to improve the consistency between channels. This SiReadout has been fabricated in 180nm CMOS technology and the microphotograph is shown in Fig.3. The die size of the prototype chip is 2 mm × 4.23 mm.

Single-Channel Structure

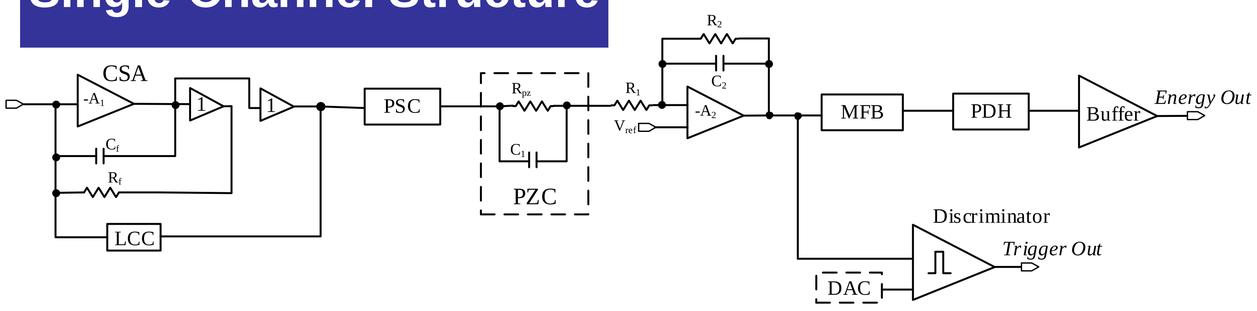


Figure.4 Single channel structure of SiReadout chip

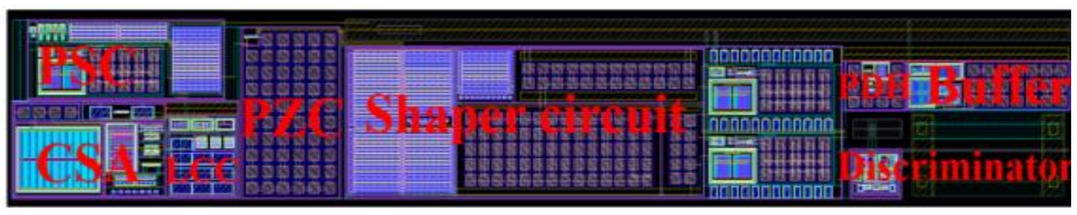
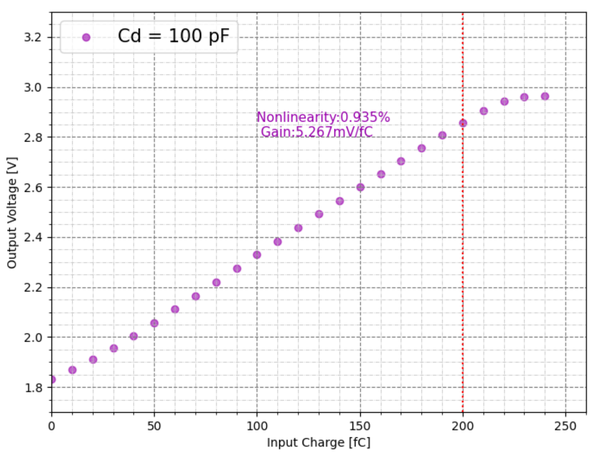


Figure.5 Single-channel layout of the SiReadout

Figure.4 shows the single channel structure of the SiReadout chip. Figure.5 shows the single-channel layout of the ASIC. The energy path is composed of the charge sensitive preamplifier(CSA), the leakage current compensation circuit(LCC), the polarity selection circuit(PSC), the pole-zero cancellation circuit(PZC), the shaper circuit, the peak detect and hold circuit(PDH), and the buffer. The output of the fast shaper circuit connects to the discriminator to output trigger information. The preamplifier using dual power supplies dramatically reduces power consumption, the large-size input device operating in the weak inversion region reduces noise, and the shaper circuit improves the signal-to-noise ratio.

Performance



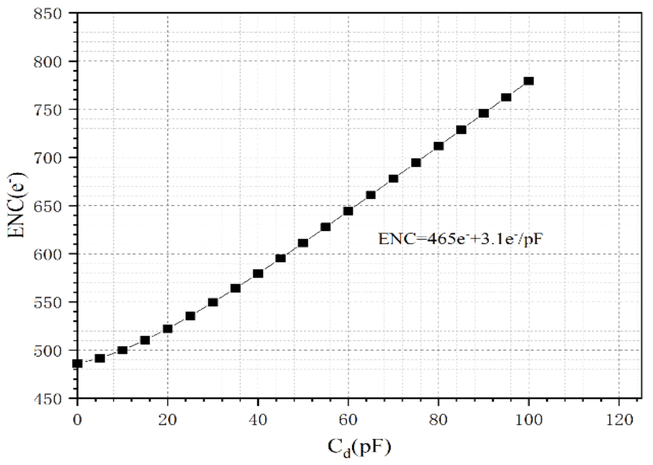


Figure.6 Left: Results of the gain and linearity; Right: ENC versus Input capacitance

Figure.6 shows the linearity and ENC of the readout channel for typical positive charge input. The system's overall gain is calculated to be 5.27 mV/fC. The maximum integral nonlinearity(INL) is less than 1%, and the ENC is 465e- at 0 F plus 3.1e- per pF.

Conclusion

This paper discusses the SiReadout for readout of the silicon strip detectors in VLAST. This ASIC can measure the energy and trigger information of the input charge signal with low-power, large-dynamic range. The input dynamic range is ±200fC, the power consumption is less than 270$\mu W/channel$, the linearity error is less than 1% for typical positive charge input, and the ENC is 779e-@100pF for positive charge input. The SiReadout fulfills the design requirement of the VLAST.

References

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