A High-Precision Two-Stage Time-to-Digital Converter in 180 nm CMOS Technology

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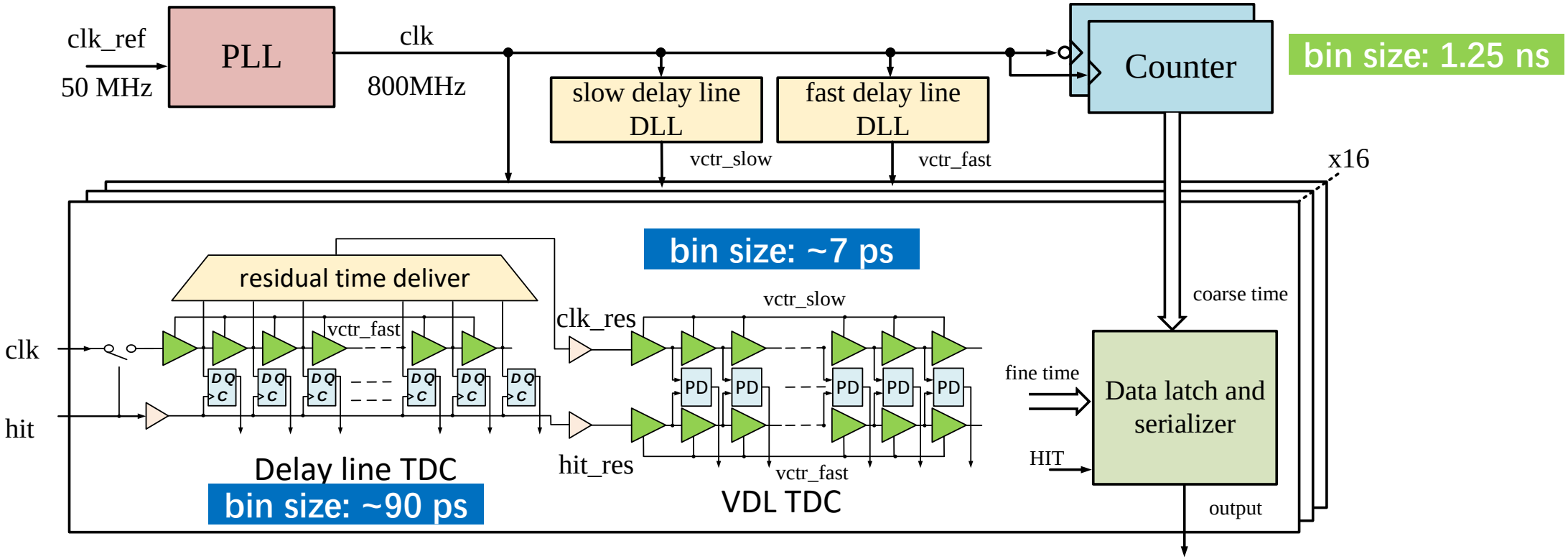
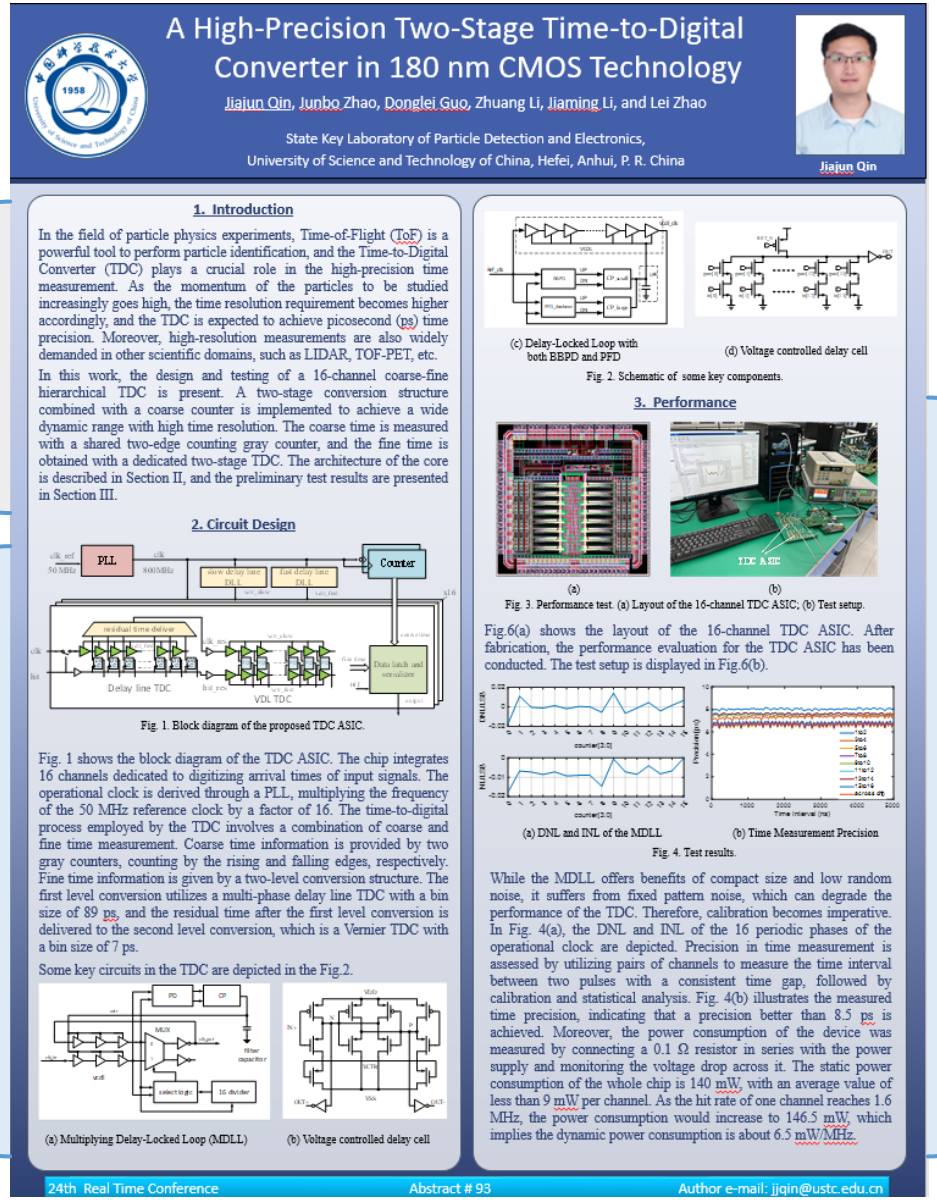


Background

Architecture & Circuit design

Performance



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1. Introduction

In the field of particle physics experiments, Time-of-Flight (ToF) is a powerful tool to perform particle identification, and the Time-to-Digital Converter (TDC) plays a crucial role in the high-precision time measurement. As the momentum of the particles to be studied increasingly goes high, the time resolution requirement becomes higher accordingly, and the TDC is expected to achieve picosecond (ps) time precision. Moreover, high-resolution measurements are also widely demanded in other scientific domains, such as LIDAR, TOF-PET, etc.

In this work, the design and testing of a 16-channel coarse-fine hierarchical TDC is present. A two-stage conversion structure combined with a coarse counter is implemented to achieve a wide dynamic range with high time resolution. The coarse time is measured with a shared two-edge counting gray counter, and the fine time is obtained with a dedicated two-stage TDC. The architecture of the core is described in Section II, and the preliminary test results are presented in Section III.

2. Circuit Design

Fig. 1. Block diagram of the proposed TDC ASIC.

Fig. 1 shows the block diagram of the TDC ASIC. The chip integrates 16 channels dedicated to digitizing arrival times of input signals. The operational clock is derived through a PLL, multiplying the frequency of the 50 MHz reference clock by a factor of 16. The time-to-digital process employed by the TDC involves a combination of coarse and fine time measurement. Coarse time information is provided by two gray counters, counting by the rising and falling edges, respectively. Fine time information is given by a two-level conversion structure. The first level conversion utilizes a multi-phase delay line TDC with a bin size of 89 ps, and the residual time after the first level conversion is delivered to the second level conversion, which is a Vernier TDC with a bin size of 7 ps.

Some key circuits in the TDC are depicted in the Fig.2.

(a) Multiplying Delay-Locked Loop (MDLL) (b) Voltage controlled delay cell

(c) Delay-Locked Loop with both BBPD and PFD (d) Voltage controlled delay cell

Fig. 2. Schematic of some key components.

3. Performance

(a) (b)

Fig. 3. Performance test. (a) Layout of the 16-channel TDC ASIC; (b) Test setup.

Fig.6(a) shows the layout of the 16-channel TDC ASIC. After fabrication, the performance evaluation for the TDC ASIC has been conducted. The test setup is displayed in Fig.6(b).

(a) DNL and INL of the MDLL (b) Time Measurement Precision

Fig. 4. Test results.

While the MDLL offers benefits of compact size and low random noise, it suffers from fixed pattern noise, which can degrade the performance of the TDC. Therefore, calibration becomes imperative. In Fig. 4(a), the DNL and INL of the 16 periodic phases of the operational clock are depicted. Precision in time measurement is assessed by utilizing pairs of channels to measure the time interval between two pulses with a consistent time gap, followed by calibration and statistical analysis. Fig. 4(b) illustrates the measured time precision, indicating that a precision better than 8.5 ps is achieved. Moreover, the power consumption of the device was measured by connecting a 0.1 Ω resistor in series with the power supply and monitoring the voltage drop across it. The static power consumption of the whole chip is 140 mW, with an average value of less than 9 mW per channel. As the hit rate of one channel reaches 1.6 MHz, the power consumption would increase to 146.5 mW, which implies the dynamic power consumption is about 6.5 mW/MHz.

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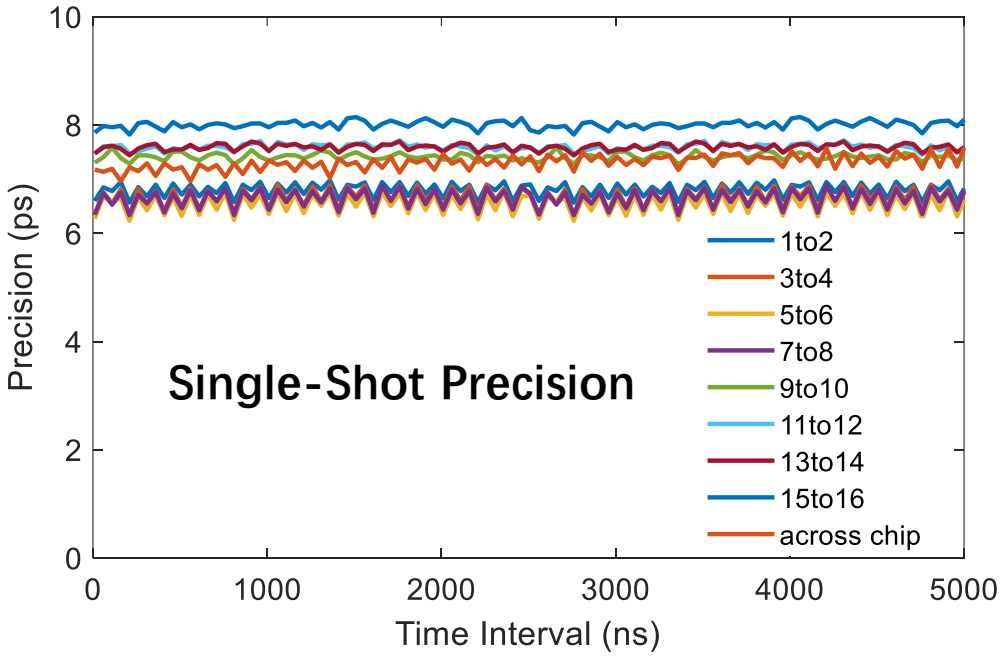
Parameters	Value
Channels	16
Bin Size	~7 ps
Dynamic Range	5120 ns
Single-Shot Precision	<8.5 ps
Power Consumption	<150 mW



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