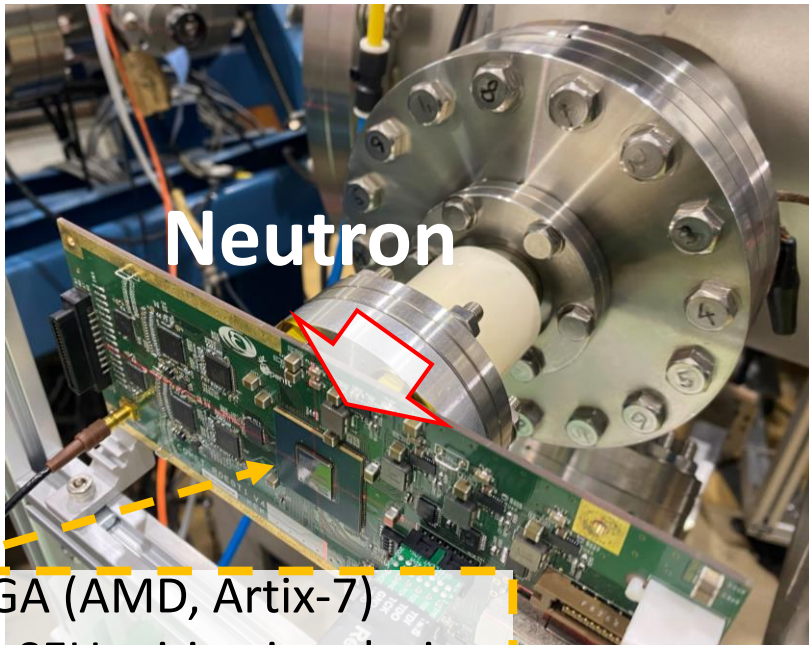# Hybrid Scrubber of SEM and Picoblaze for FPGA on COMET Read-out Electronics #104

The dead time decreased by 80%!

Neutron

FPGA (AMD, Artix-7)
The new SEU mitigation design is implemented in the FPGA.

Setup of Neutron Irradiation Test

UnRcoverable Error Rate $[[n/cm^2]^{-1}]$

$\times 10^{-11}$

URE1 'Multi-Bit Upsets'

URE2 'Other Errors'

SEM (AMD IP core for SEU Mitigation)

New SEU mitigation design

Results

Eitaro Hamada[1], Youichi Igarashi[1], Kazuki Ueno[2]

[1]High Energy Accelerator Research Organization,
[2]Osaka University

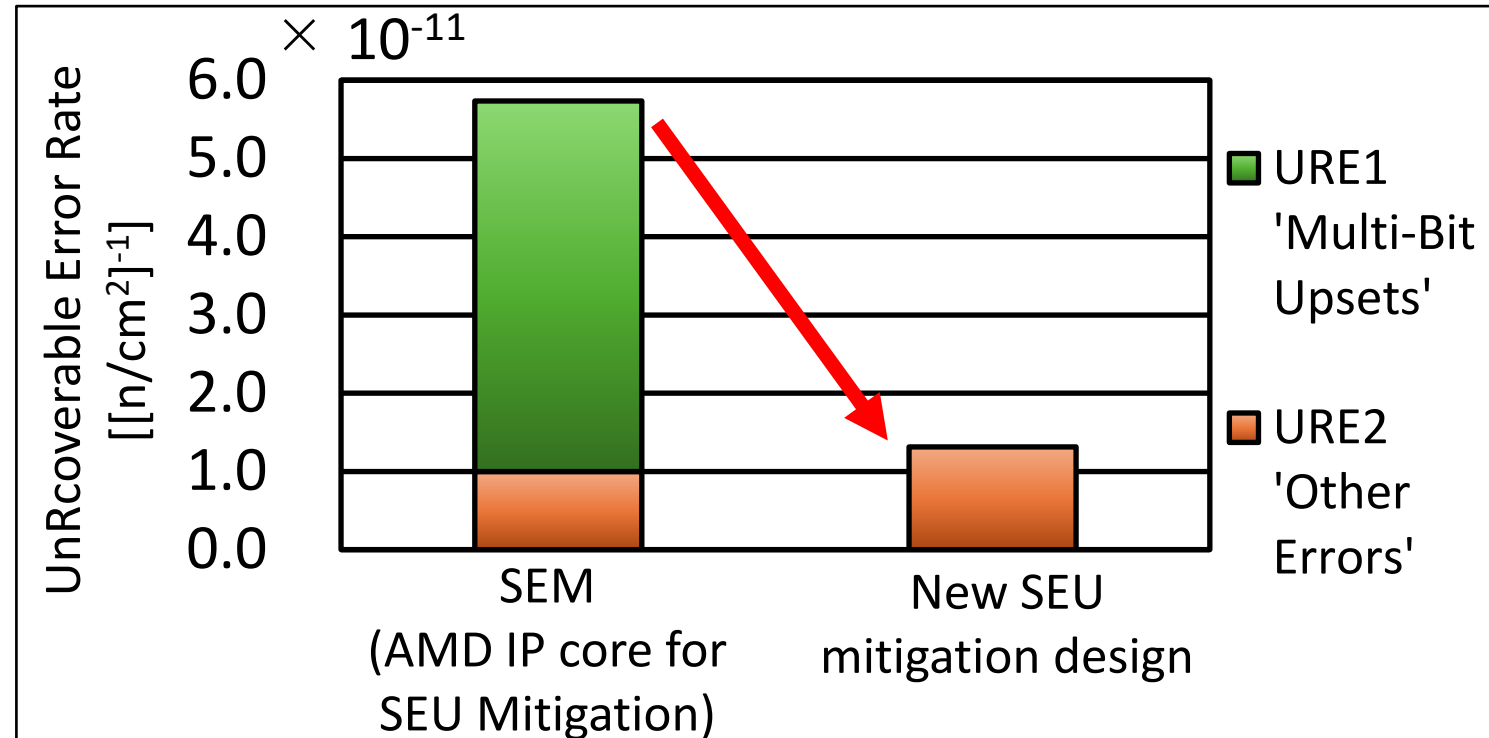# Hybrid Scrubber of SEM and Picoblaze for FPGA on COMET Read-out Electronics #104

Hybrid scrubber of the SEM and the Picoblaze
can correct not only single-bit upset but also multi-bit upsets!

Hybrid Scrubber

SEM

Picoblaze

FPGA design

digitalized data

configuration memory data

Network I/F

digitalized data and configuration memory data (Ethernet TCP/IP)

Block Diagram

SEU Mitigation Strategy
- single-bit upset

corrected by SEM

- multi-bit upsets

corrected by picoblaze and PC

Eitaro Hamada[1], Youichi Igarashi[1], Kazuki Ueno[2]

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