Implementation of the Trigger, Timing, and Control Link for Data Acquisition with the Pixie-Net XL

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Background

Large nuclear physics experiments can include hundreds or thousands of separate detector channels. They usually require synchronization of clocks of multiple digital detector readout electronics modules to ensure that data from different channels can be matched by their time stamps and that time differences can be computed to high precision. Triggers may need to be distributed to select subsets of channels to be recorded.

Such clocks and triggers are traditionally distributed through dedicated cabling, which can become quite complex [1]. Previous work described how White Rabbit (WR) [2] has been implemented on the Pixie-Net XL detector readout electronics [3] as an example of time synchronization via existing data networks. However, implementation of White Rabbit is not straightforward and its use is currently not widespread.

A different approach is the Trigger, Timing, and Control Link (TTCL) [4, 5, 6] developed for GRETINA, expanded for Digital Gammasphere, and now used by all DAQ systems at ATLAS and GRETA. Here we report the implementation of TTCL as another alternative to dedicated clock/trigger cabling. It will allow the Pixie-Net XL to be used in conjunction with Gammasphere, GRETA, and other major setups without anticipated WR infrastructure.

Pixie-Net XL Electronics

The Pixie-Net XL electronics hardware design centers on two Kintex 7 FPGAs for pulse processing. Each Kintex is connected to a high density connector for ADC daughter cards that implement multiple channels of analog signal conditioning and digitization. Each Kintex is further connected to an SFP card cage for 1G Ethernet with WR or 10G Ethernet without WR and to a variety of general purpose I/O connections and peripherals. A “CLK DB” daughtercard for each Kintex generates source clocks for FPGA processing (125 MHz), Ethernet I/O, (156.25 MHz) and ADCs (multiple of 125 MHz as needed).
The CLK DB has here been redesigned for as a TTCL interface board.

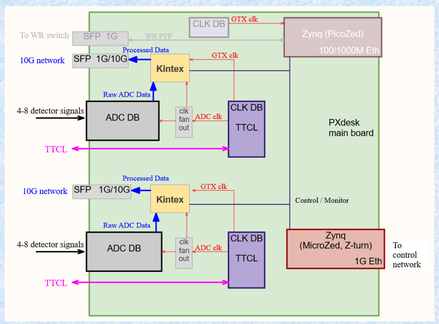

Figure 1: Block diagram of the Pixie-Net XL, showing
- **2 Kintex FPGAs (yellow) for pulse processing**
- **2 ADC daughterboards (gray).**
- **2 clocking daughterboards (purple) connected to a TTCL link**
- **1 commercial Zynq processor board (red) for setup and operation control.**

Figure 2. Picture of Pixie-Net XL, fully assembled. (Front panel varies with ADC and clocking options)

TTCL Interface Board

The Pixie-Net XL TTCL interface board provides clocks to the Pixie-Net XL motherboard synchronous to the TTCL master. It connects to digital I/O pins on the Kintex for trigger distribution and control, including a Serial Peripheral Interface (SPI). The board’s components are:
- A SFP connector for the link to the TTCL trigger distribution system. This link carries a continuous stream of data at 1Gbps with “frames” containing trigger and synchronization messages (not Ethernet),
- A serializer/de-serializer chip to reformat the TTCL data and extract the master clock.
- A Spartan 6 FPGA for decoding the TTCL data, extracting the timestamp, commands, and event accept messages from the TTCL master.
- An optional (unused) jitter cleaner chip
- A fixed clock chip for the Kintex Ethernet interface

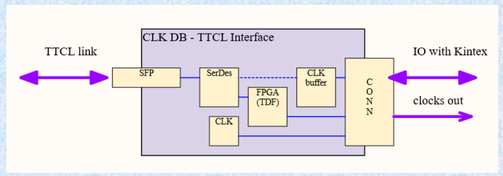

Figure 3: Block diagram of the TTCL interface board

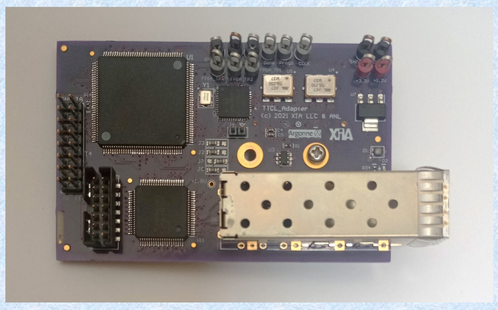

Figure 4. Picture of the TTCL interface board

About XIA LLC

XIA LLC invents, develops and produces advanced digital data acquisition and processing systems for x-ray, gamma-ray, and other radiation detector applications in university research, national laboratories and industry. Having pioneered digital detector readout electronics for over 20 years, we value collaboration with academic and industrial partners to customize solutions for challenging applications.

Firmware Implementation (TTCL Interface)

The TTCL master sends 16-bit payload words every 20ns, grouped into 5-word sets called frames to the TTCL interface card. Frame types include

- **Imperative Sync**
  Reset time stamp counters in the whole system
- **Trigger Accept**
  Based on coincidence information from key detectors, the TTCL master makes a decision if the event was acceptable. The time of acceptance is included in the frame.

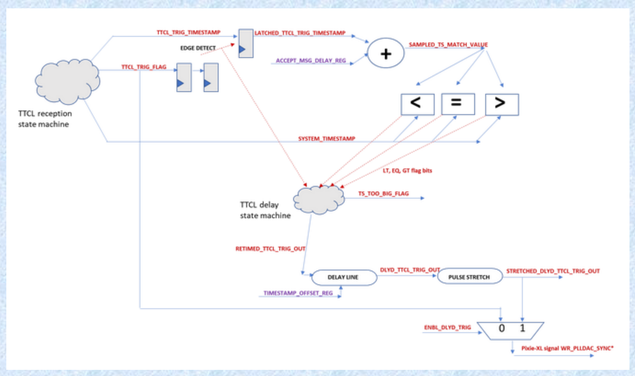

Figure 5. Trigger distribution logic in the Spartan 6 FPGA

The firmware for the interface board can decode these frames, after de-serialization, with a number of control registers configured by the Kintex via SPI. It provides the following outputs to the Kintex:
- **Clock**
  The extracted clock from the trigger system for synchronization of Pixie ADC sampling and pulse processing to the system-wide clock.
- **Trig flag (from trigger accept frame)**
  An event acceptance signal from the trigger system, resynchronized to timestamp and clock from trigger, thus arriving at fixed delay relative to timestamp contained within trigger accept message irrespective to transmission latency.
- **Sync flag (from imperative sync frame)**
  A reset signal for timestamp counter within Kintex for synchronization of event timestamping.
- **SM_LOCK**
  status signal indicative of good connection to trigger.

Firmware Implementation (Pixie-Net XL)

Besides programming user settings in the TTCL interface board via a new SPI interface, the Kintex Firmware was updated to respond to signals from the TTCL interface board as follows:

- **Imperative Sync**
  Upon receipt of the “sync” pulse, time stamp counters using the TTCL clock in the Pixie-Net XL are reset.
- **Trigger Accept**
  For each detected pulse, after applying energy filter and other pulse processing, the event data is recorded in FPGA memory IF a TTCL accept trigger occurred within a user defined time earlier. To accommodate situations where the TTCL trigger distribution takes longer than the energy filter etc, the incoming ADC data can be delayed.
- **Data Format**
  Event data is output as UDP packages over the 10G Ethernet interface in a format compatible to that of Gammasphere. Event data includes TTCL time stamps, which allowing matching this data to the output from other TTCL compatible digitizers

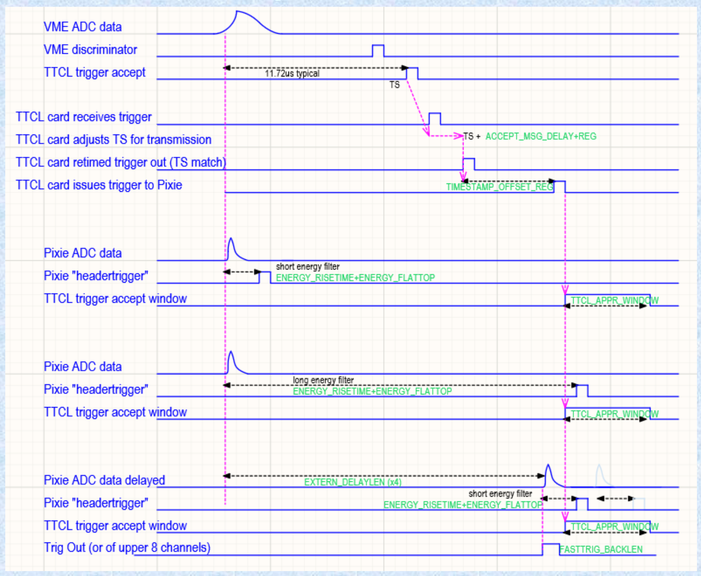

Figure 6. Timing of the trigger distribution

References and Acknowledgments

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Characterization and Test

Jitter

To verify the quality of the clock distributed via the TTCL link, we measured the clock jitter of the recovered clock on the TTCL interface board against a trigger signal generated by the TTCL master synchronous to the master trigger's clock. The time difference from trigger edge to next clock edge (red double arrow) has a standard deviation of ~111ps. The clock jitter on the interface card itself is ~17ps between 2 consecutive clock edges.

Figure 7. Clock jitter measurement. Yellow: clock on TTCL interface board, green: trigger from TTCL master.

Timestamp

To verify time stamp counters in the Pixie-Net XL are synchronized via TTCL, we acquired events in 2 units that receive the same signal (split pulser). Figure 8 demonstrates timestamps are identical.

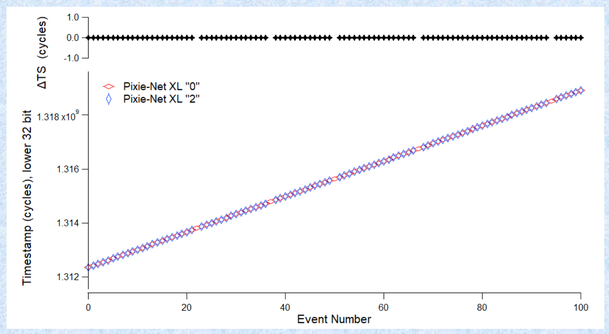

Figure 8. Time stamps of simultaneous pulses captured in two Pixie-Net XL synchronized with TTCL link. Time stamp difference is zero as expected.

Application Preview

The Pixie-Net XL with TTCL interface is used to instrument liquid scintillators for neutron detection added to the Gammasphere array, as outlined in Figure 9. Results from the setup phase are shown in Figure 10.

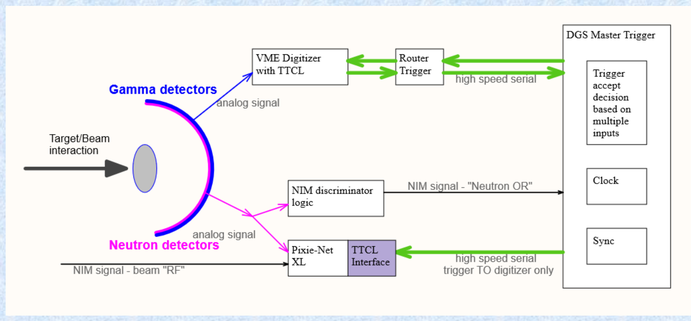

Figure 9. System setup with Gammasphere and TTCL master trigger

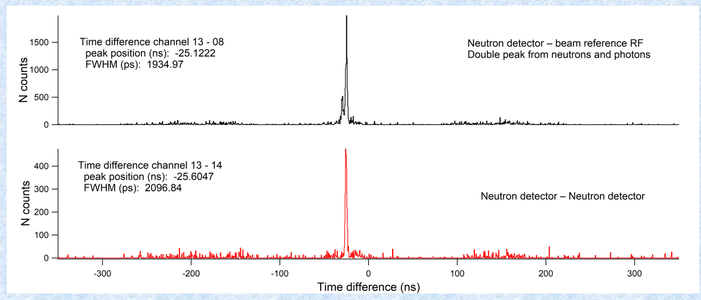

Figure 10. Preliminary timing results: Time measured between different channel pairs of the Pixie-Net XL synchronized via TTCL. The "source" is a 40Ca+40Ca reaction where one of the reaction partners is a pulsed beam (ATLAS accelerator) and the other one a target foil. The peak width of ~2ns corresponds to the FWHM of a beam pulse, the centroid of which serves as reference for measuring time of flight differences between reaction photons and neutrons.

Summary

We implemented a TTCL interface for the Pixie-Net XL detector readout electronics module. The interface board provides a low jitter clock for Pixie-Net XL digitization and pulse processing; the firmware decodes messages from the TTCL master, resets time stamp counters synchronously, and makes recording of events conditional to approval from the TTCL master.

Test measurements suggest that the clock is distributed with low jitter, time stamps are synchronized as expected, and time of arrival of detector pulses can be determined to precision better than the digitization clock rate. An accelerator experiment using the Gammasphere + neutron-detector setup confirms the test results: Neutron events read out by two Pixie Net-XL are merged according to timestamps and correlated with photon events from Gammasphere. The "correlated" gamma spectrum is enhanced in the expected photon peaks proving that the two subsystems are synchronized.

The TTCL interface is physically compatible to the “GTCL” triggering system developed for GRETA, which uses the same concept of synchronization and trigger frame messages. This allows straightforward integration of the Pixie-Net XL in GRETA experiments and related systems, for example instrumenting auxiliary detectors at FRIB [7], and greatly increases its utility for the nuclear physics community.