Implementation of the Trigger, Timing, and Control Link for Data Acquisition with the Pixie-Net XL

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Abstract— **A common problem in larger nuclear physics experiments is the distribution of clocks and triggers between multiple types and instances of detector readout electronics. Measurements of the time difference of two or more related particle or photon interactions in separate radiation detectors, to sub-nanosecond precision, require the data to be time stamped with high accuracy across the system. In addition, background events that do not fit interactions of interest may have to be suppressed to limit data acquisition to available bandwidth and storage.**

Clocks and triggers are traditionally distributed through dedicated cabling. Techniques such as the IEEE 1588 Precision Time Protocol and its high accuracy profile (White Rabbit) can distribute clocks and time/date through generic Ethernet data connections, but do not easily allow sharing of triggers for data acquisition. In contrast, the Trigger, Timing, and Control Link (TTCL) has been developed as a method to distribute both clock and trigger through generic fiber with a specific data exchange protocol. TTCL has been adopted for several experiments and facilities since 2008 and is supported by a variety of readout electronics designs. The related interface described here is compatible with Digital Gammasphere and GRETA.

We implemented TTCL for the Pixie-Net XL detector readout electronics. A TTCL interface board de-serializes the incoming TTCL gigabit data stream, extracts the embedded clock and makes it available for digitization and time stamping on the Pixie-Net XL, and decodes the TTCL messages to issue triggers to the Pixie-Net XL pulse processing logic. We describe design and testing of the interface board, show how TTCL triggers can be used to conditionally record events, and report the time resolution of coincident events acquired with multiple units.

I. INTRODUCTION

Large nuclear physics experiments can include hundreds or thousands of separate detector channels. They usually require to synchronize the clocks of multiple digital detector readout electronics modules to ensure that data from different channels can be matched by their time stamps and that time differences can be computed to high precision. The timing requirements depend on the application, and can range from hundreds of nanoseconds for covering coincidence background to tens of picoseconds for time-of-flight measurements. Such clocks and triggers are traditionally distributed through dedicated cabling, which can become quite complex [1]. Recently, high precision time synchronization through data networks has been developed, such as the IEEE 1588 precision time protocol (PTP) and its high accuracy profile, White Rabbit (WR) [2]. Since detector readout electronics are usually already connected to a data network for readout to storage, these methods can be used instead of dedicated cabling [3], though for sub-nanosecond precision, special network routing equipment is required. Attempts have been made [4] to add the distribution of triggers to WR, which would allow, for example, capturing data in "spectator channels"

without a local trigger. However, the WR implementation is not straightforward and its use is currently not widespread. A different approach is the Trigger, Timing, and Control Link (TTCL) [5, 6, 7] developed for the early implementation of GRETA (GRETINA), Digital Gammasphere, and other systems. Standard fiber is used to distribute both clock and triggers with a 1 Gbps embedded-clock data stream. TTCL as well as GTCL, the GRETA variant, also allow for synchronous commands (register I/O) to be distributed throughout the system which allows a control parameter to be changed simultaneously in all digitizers.

The challenge for the use of such techniques in detector readout electronics is to integrate the synchronization with the data capture in analog to digital converters (ADCs) and the processing of digitized detector signals in a field programmable gate array (FPGA). References [3, 8] describe how WR has been implemented for the Pixie-Net XL data acquisition electronics. Here, we report the implementation of TTCL as another alternative to dedicated clock/trigger cabling. It will allow the Pixie-Net XL to be used in conjunction with Gammasphere, GRETA, and other major setups without anticipated WR infrastructure. Its performance is characterized through timing resolution measurements.

II. SYSTEM DESCRIPTION
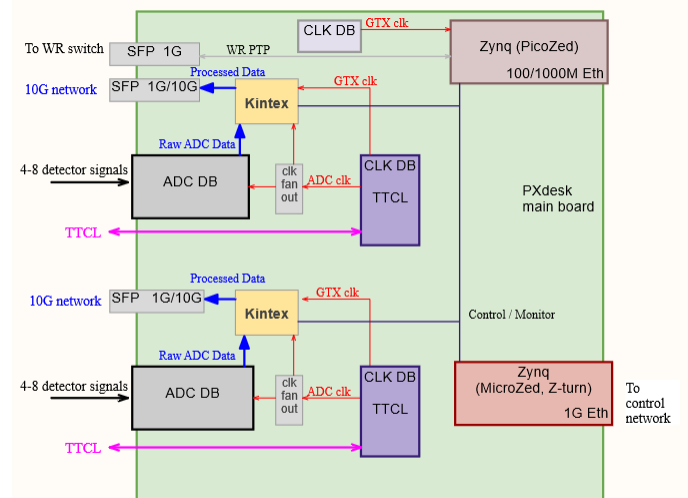
A. Pixie-Net XL Electronics

Fig. 1. Block diagram of the Pixie-Net XL. Physically separate daughterboards are shown with thick borders. Each FPGA "interfaces" with a clocking daughterboard connected to a TTCL link.

As shown in Fig.1, the Pixie-Net XL electronics hardware design centers on two Kintex 7 FPGAs. Each Kintex is connected to a high density connector for ADC daughter cards that implement multiple channels of analog signal conditioning

and digitization. Each Kintex is further connected to an SFP card cage for 1G Ethernet with WR or 10G Ethernet without WR and to a variety of general purpose I/O connections and to other peripherals. A "CLK DB" daughtercard for each Kintex generates clocks for FPGA, Ethernet I/O, and ADCs; it has here been redesigned for TTCL and is referred to below as the TTCL interface board.
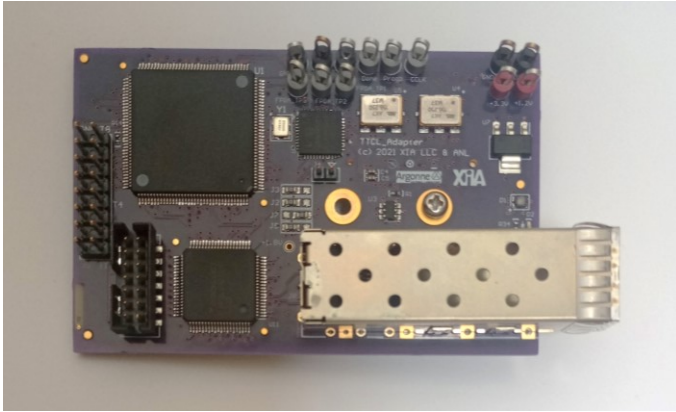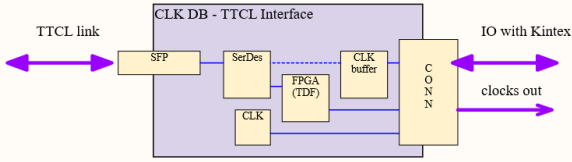
B. TTCL interface board

Fig. 2. Block diagram and picture of the TTCL interface board.

The Pixie-Net XL TTCL interface board is a roughly 5 cm x 8 cm circuit board. As indicated in Fig. 2, it provides clocks, and connects to digital I/O pins on the Kintex for trigger distribution and control, including a Serial Peripheral Interface (SPI). The board's components are:

- A SFP connector for the link to the TTCL trigger distribution system. This link carries a continuous stream of data at 1Gbps with "frames" containing trigger and synchronization messages (not Ethernet),
- A serializer/de-serializer chip to reformat the TTCL data.
- A Spartan 6 FPGA for decoding the TTCL data, extracting the timestamp, commands, and event accept messages from the TTCL master.
- A clock distribution chip (unused).
- A fixed clock chip for the Kintex Ethernet interface.

C. Pixie-Net XL Firmware

On the Pixie-Net XL, the firmware for the Kintex FPGA was updated to include a SPI interface to program registers in the firmware for the Spartan FPGA on the TTCL interface board that control TTCL decoding and triggering, a time stamp counter synchronous with the TTCL clock, logic to validate locally captured data based on TTCL triggers, and formatting of output data compatible to that of Gammasphere. In this approach, captured data is still output via the 10G Ethernet link of each Kintex; the TTCL interface provides synchronization and validation.

D. TTCL Interface Board Firmware

The TTCL master sends 16-bit payload words every 20ns, grouped into 5-word sets called frames. Frame types include distributing the system timestamp, synchronizing receivers to the frame order, and distribution of trigger accept messages [9]. The firmware for the TTCL interface board can decode these frames, after de-serialization, with a number of control registers configured by the Kintex via SPI. It currently recognizes the following frames:

- Imperative Sync: Reset time stamp counters in the whole system
- Trigger Accept: Based on coincidence information from key detectors, the TTCL master makes a decision if the event was acceptable. The message frame includes the timestamp for which events are acceptable. Logic in the TTCL interface board extracts the time stamp, and adjusts it by a user defined offset to accommodate transmission delays. When the adjusted time is equal to the local time stamp counter, a trigger flag is created, and after a further user defined delay to accommodate processing delays in the Pixie-Net XL, the trigger flag is issued to the Pixie-Net XL. The Pixie-Net XL logic then opens an acceptance window of user defined length. (In case Pixie-Net XL processing is shorter than decision making and message delay, an input delay of user defined length can be added to the Pixie-Net XL, which acts like an analog delay cable.)

Signals issued from the TTCL interface board to the Kintex pulse processing FPGA on the Pixie-Net XL thus include the clock for ADC operation, a trigger flag (from the trigger accept frame), a sync flag (from the imperative sync frame) and also a lock flag indicating that the clocks in the TTCL interface FPGA are locked to the TTCL link.

III. CHARACTERIZATION MEASUREMENTS

Fig. 3. Clock jitter measurement: Delay of TTCL master trigger (green) against clock on TTCL interface board (yellow).

To verify the quality of the clock distributed via the TTCL link, we measured the clock jitter of the recovered clock on the TTCL interface board against a trigger signal generated by the TTCL master that is synchronous to the master trigger's clock. As shown in Fig. 3, measuring the time difference from trigger edge to next clock edge with a fast oscilloscope (red double arrow) leads to a standard deviation of that difference of ~111ps. The clock jitter on the interface card itself, measured between 2 consecutive clock edges, is ~17ps. Earlier tests measured the

jitter at various points within a Pixie-Net XL clock circuitry at ~50ps. In a WR setup, the jitter between a trigger generated by the WR master and the recovered clock on the Pixie-Net XL was ~100ps.

To verify that time stamp counters in the Pixie-Net XL are synchronized via TTCL, we acquired events in 2 units that receive the same signal (split pulser). Figure 4 demonstrates that the timestamps from each unit are identical.
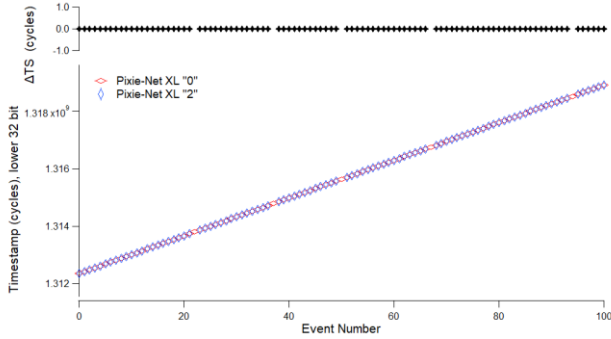

Fig. 4. Time stamps of simultaneous pulses captured in two Pixie-Net XL synchronized with TTCL link. Time stamp difference is zero as expected.
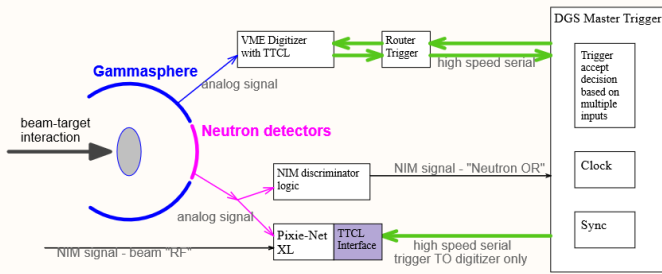
IV. APPLICATION PREVIEW

Fig. 5. System setup with Gammasphere and TTCL master trigger.

The Pixie-Net XL with TTCL interface was used to instrument an array of liquid scintillators for neutron detection that are added to the Gammasphere array, as outlined in Figure 5. In this case, the accept/reject decisions are based on the "VME digitizers", plus an "OR" of all neutron detectors. The Pixie-Net XL additionally captures the "RF" signal whenever any neutron detector triggers locally, to be able to compute the time between RF and detector pulse. Results from the setup phase are shown in Figure 6.
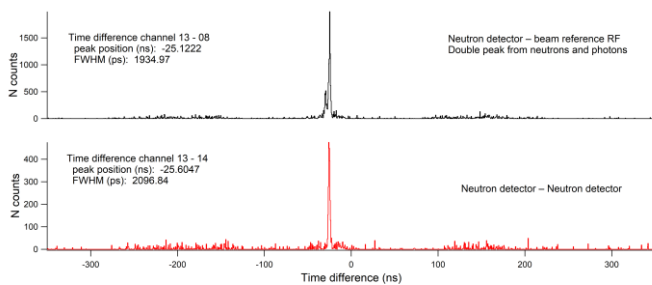

Fig. 6. Preliminary timing results: Time measured between different channel pairs of the Pixie-Net XL synchronized via TTCL. The "source" is a 40Ca+40Ca reaction where one of the reaction partners is a pulsed beam (ATLAS accelerator) and the other one a target foil. The peak width of ~2ns corresponds to the FWHM of a beam pulse, the centroid of which serves as reference for measuring time of flight differences between reaction photons and neutrons..

V. SUMMARY

We implemented a TTCL interface for the Pixie-Net XL detector readout electronics module. The implementation consists of an interface board, and firmware for the FPGAs of the Pixie-Net XL and TTCL interface. The interface board provides a low jitter clock for Pixie-Net XL digitization and pulse processing; the firmware decodes messages from the TTCL master, resets time stamp counters synchronously, and makes recording of events conditional to approval from the TTCL master.

Our test measurements suggest that the clock is distributed with low jitter, time stamps are synchronized as expected, and time of arrival of detector pulses can be determined to precision better than the digitization clock rate. An accelerator experiment using the Gammasphere + neutron-detector setup confirms the test results: Neutron events read out by two Pixie Net-XL are merged according to timestamps and correlated with photon events from Gammasphere. The "correlated" gamma spectrum is enhanced in the expected photon peaks proving that the two subsystems are synchronized.

The TTCL interface is physically compatible to the "GTCL" triggering system developed for GRETA, which uses the same concept of synchronization and trigger frame messages. This allows straightforward integration of the Pixie-Net XL in GRETA experiments and related systems, for example auxiliary detectors at FRIB [10], and greatly increases its utility for the nuclear physics community.

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