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The HIPA radio frequency control system application

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Abstract

For the upgrade of the High Intensity Proton Accelerator at PSI of injector cavities 2 and 4, a new digital radio frequency control system was developed using the IFC 1210 VME board. This system comprises three components: A single-board computer running the control system software and the real- time application, both running on a dual core P2020 PowerPC, as well as the FPGA Design utilizing a Virtex 6. The real-time application (RTAPP) covers three use cases: "Cavity Tuning", "Startup FSM", and "Calculate Statistics". "Cavity Tuning" implements the controller for the cavity's tuning system, which consists of two controllers. One controls the physical position of the two tuners within the cavity, and the other one provides the setpoint for the tuner controller and controls on the phase error between forward power and cavity pickup, ensuring minimum reflected power during operation. The "Startup FSM" governs the radio frequency control system during the startup procedure. Here, the cavity must overcome the multipactoring zone while minimizing reflected power and without overstressing the amplifiers. Finally, "Calculate Statistics" performs computations on measurement data from high resolution ADC RAW values, reducing the data load before forwarding them to the control system. The software design is split into four layers: Common, hardware, service and application layer. These layers cover 13 different components which are each assigned a dedicated thread. The update frequency of the components varies between 25 and 50Hz, real-time behavior is given if a deadline of 20ms or 40ms respectively can be guaranteed.

Introduction and Requirements

Digital radio frequency control systems (also called Low Level Radio Frequency = LLRF systems) control the RF field in accelerating cavities. The objective of the present application is to operate a tuning feedback at 25Hz repetition rate and at the same time calculate signal statistics of down sampled data at 50 and 25Hz. In addition, an automated start-up procedure has been implemented to switch on the cavity.

Requirements briefly summarized:
- Sample **8 ADC** channels, demodulate, down sample signal and calculate signal statistics at **50** and **25Hz**
- Implement scope recorder functionality triggered by threshold value
- Tuning feedback operation at **25Hz** with exception and fault handling
- Implement operation modes: valve, position and phase controlled (phase tuning)
- Amplitude and Phase feedback operation at **8MHz** (FPGA)
- Start-Up procedure to bring up the high-power RF without too big reflections

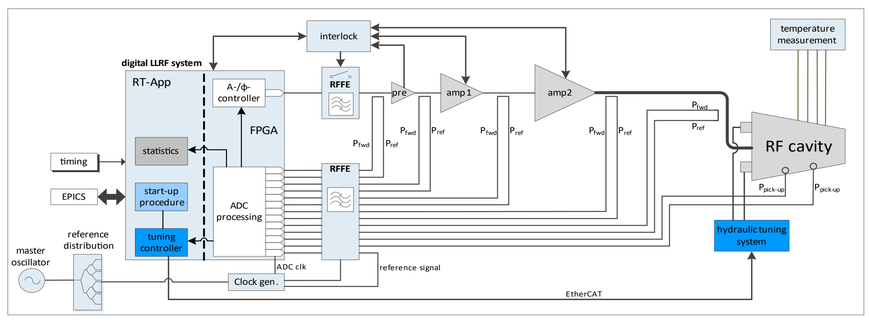


Figure 1: Overview of the entire RF system consisting of accelerating cavity, amplifiers, couplers, analog pre-processing units, interlock unit, temperature measurement unit, hydraulic tuning system and the two tuners. Particularly noteworthy is the dark blue tuning controller, which is in the lower left-hand corner of the figure. Control signals are sent to the hydraulic tuning system via the EtherCAT bus. Currently the cavity tuning feedback runs at 25Hz. Because the bandwidth of the hydro-mechanical system is around 3Hz. A faster control loop would not improve the control quality. Rule of thumb is to sample with ten times the plant bandwidth. Measurements on the system also showed that it was sufficient.

Cavity characteristics:
- Built from pure aluminum
- Resonance : **50.6328MHz**
- Quality factor Q ~ **25'000**
- Dissipated power **45kW@ 400kV**
- Operation at 60kW
- Vacuum pressure 1e-6mbar
- Water flow 15m³/h
- Tuning range ~ 200kHz
- Weight 7.6t , Volume 55m³

Figure 2: As part of the HIPA upgrade the installed 150MHz 3rd harmonic cavity will be replaced with a 50 MHz cavity. In further steps all the remaining three cavities of injector 2 will be replaced. The picture shows the 50 MHz accelerating cavity with hydraulic tuners. The whole cavity was built entirely from aluminum. Ideally copper is used due to better conductivity. But the cost of producing such cavities is much higher.

Architecture and Implementation

Our approach was to divide the LLRF system into two parts: the processing system and a programmable logic. The main task of the processing system is to provide the control interface for the entire RF station and in particular for the cavity. It also provides measurement and control of cavity signals via EtherCAT bus and provides this data to clients via EPICS. The programmable logic (implemented in FPGA) has to perform signal pre-processing such as IQ-demodulation, down sampling and coordinate system transformation. It must also stabilize the amplitude and phase of the cavity signals using PI control.

Hardware/Software briefly summarized:
- Single board computer from IOxOS IFC1210
- FMC-ADC3110 and FMC-DAC3114 @253MHz
- Linux with PREEMPT_RT patch running on PPC P2020
- EPICS is the control interface and EtherCAT master
- EtherCAT master stack from IgH
- Beckhoff EtherCAT IO terminal
- Application logic and time critical tasks in the RTAPP
- Programmable Logic (FPGA) for signal processing

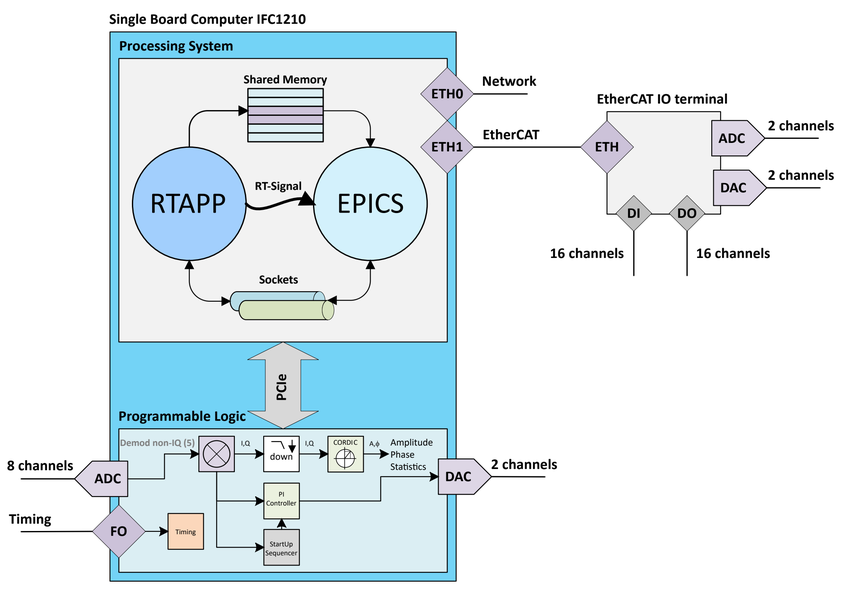
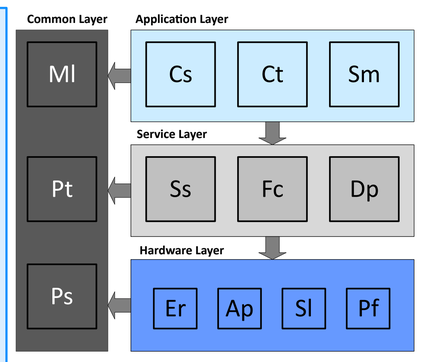


Figure 3: Shows the two relevant processes and the IPC mechanisms for event and data exchange. Three different mechanisms are in use: Shared Memory to move the big data blocks like waveforms, Unix domain sockets for application settings and data forwarded to the EtherCAT bus like the tuner control signal and RT-Signals to trigger shared memory access of EPICS.

RTAPP characteristics:
- Layered architecture
- Layer contains components
- Every component is an actor, implementation of the **actor model**
- Event-driven interaction
- Client server principle
- Component interfaces abstract event generation and reception
- Every component can have **reactive** and **proactive** interfaces



Er : *EventReceiver*
Ap : *AdcProcessor*
Sl : *StartUpLogic*
Pf : *ParameterForwarding*
Ss : *SystemService*
Fc : *FlowController*
Dp : *DataPresentation*
Cs : *CalculateStatistics*
Ct : *CavityTuning*
Sm : *StartUpFsm*
Ml : *MessageLogger*
Ps : *ParameterStorage*
Pt : *ParameterTransmission*

Figure 4: The RTAPP is a strictly layered architecture. Responsibilities were divided into four layers, hardware abstraction, service, common and application layer. Every layer includes components with specific responsibilities that are consistent with the layer's abstraction level. The component dependencies are organized so that they always point downwards. From higher to lower (or same) levels of abstraction. The common layer can be used by all other layers.

Measurements and Results

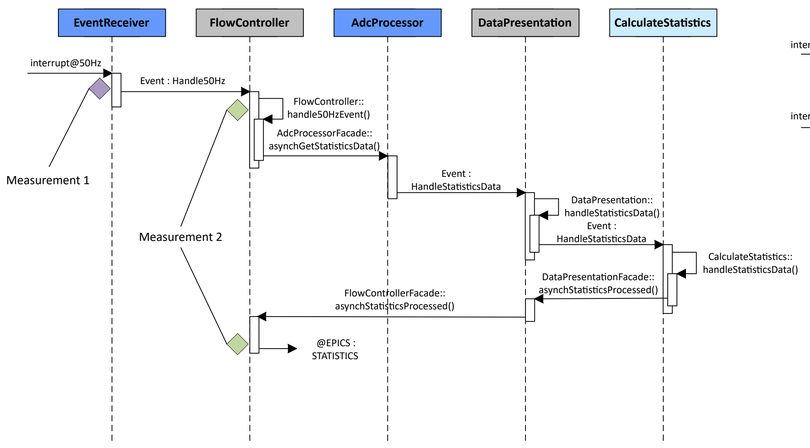


Figure 5: Sequence diagram of use case: calculate statistics. *Measurement 1* determines how periodically the interrupt is received. *Measurement 2* records the execution time for statistical calculations across all channels.

Measurement	Average [µs]	Standard Deviation [µs]	min [µs]	max [µs]	# of events
1	20013	37.15	5017	29888	50000
2	4441.8	627.41	3759	6354	200000

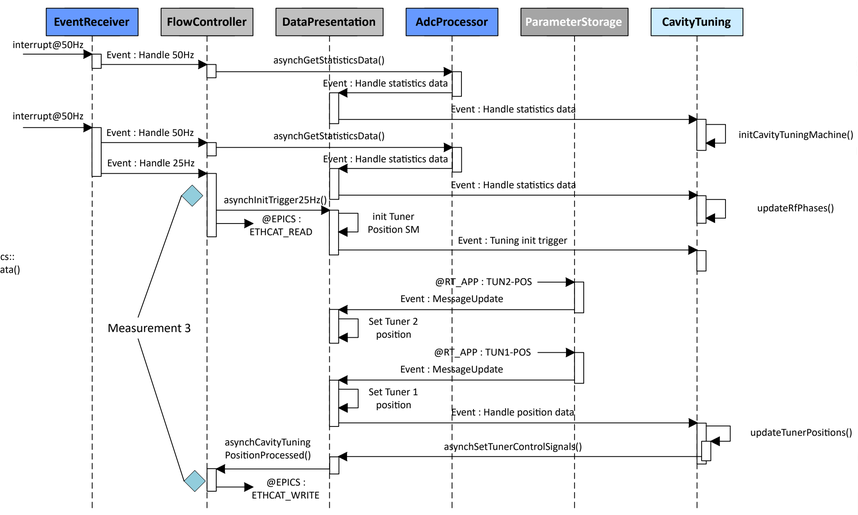


Figure 6: Sequence diagram of use case: cavity tuning. *Measurement 3* determines the time required to handle the tuner positions, feedback controller and set new control signals.

Measurement	Average [µs]	Standard Deviation [µs]	min [µs]	max [µs]	# of events
3	790.21	100.6	714	6219	160000

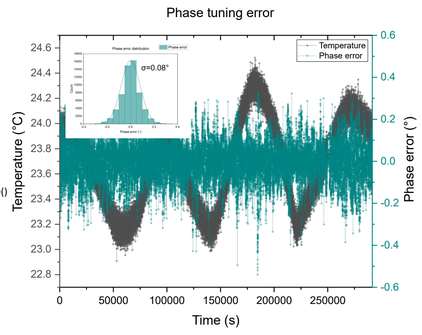


Figure 7: Long-term behavior of the phase tuning error over approximately three days.

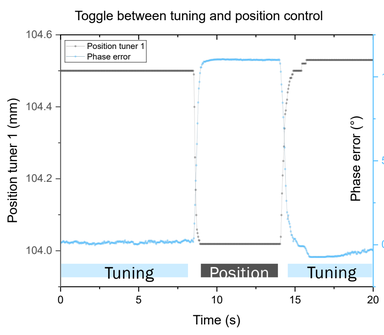


Figure 8: Phase error when transitioning between two operating states. A smooth transition is crucial for operations.

Conclusion

All requirements have been met with this design. The test run has shown stable and smooth operation over several days. The *Measurement 2* shows that the statistics are calculated after 4.4ms. This is done every 20ms, so there is a large time margin. *Measurement 3* shows that cavity tuning takes 0.79ms and this is performed every 40ms. There is also a significant time reserve. The communication overhead resulting from the implementation of the actor model can be ignored.

Grundfarben PSI

Wahlfarben Grafiken: 1. Wahl

Wahlfarben Grafiken: 2. Wahl