# a Prototype of the Timing Electronic System for the CALICE SDHCAL

Yongqi Tan, Yihan Guo, Imad Laktineh, Yang Liu, Qiuping Shen, Jiannan Tang, Mingxin Wang, Wei Zhi, Zhizhen Zhou, and Weihao Wu

***Abstract*—The CALICE Semi-Digital Hadronic Calorimeter (SDHCAL) concept is designed to be a high-granularity hadronic calorimeter for the future high-energy colliders such as the International Linear Collider (ILC) and the Circular Electron-Positron Collider (CEPC). A technological SDHCAL prototype was built with 48 layers, each equipped with 1 m $\times$ 1 m Glass Resistive Plate Chamber (GRPC) and its readout electronics featuring 1 cm $\times$ 1 cm pickup pads. It was successfully tested in several beam tests and excellent hadronic energy resolutions were obtained. However, it was found that very close-by showers can raise confusion in jet energy reconstruction, which is based on the Particle Flow Algorithm (PFA). To address this issue, the Timing-SDHCAL concept has been introduced. This approach involves replacing GRPC layers with Multi-gap Resistive Plate Chamber (MRPC) layers with high-resolution timing electronics. Timing-SDHCAL intends to exploit the precise time information provided by MRPC to efficiently separate close-by showers. It also intends to discriminate the neutron components of the hadronic showers to better estimate their energy. Here we present a timing electronic system based on Petiroc2B ASIC, along with its Data Acquisition (DAQ) system based on Zynq UltraScale+ SoC. The system demonstrates a satisfactory timing resolution of better than 100 picoseconds and could therefore equip the future Timing-SDHCAL prototype.**

***Index Terms*—Calorimeters, Gaseous Detectors, High-resolution Timing Techniques**

## I. Introduction

THE CALICE Semi-Digital Hadronic Calorimeter (SDHCAL) prototype [1], developed in 2011, is the first technological prototype in the family of high-granularity calorimeters developed by the CALICE Collaboration which satisfies the requirements of the future International Linear Collider (ILC) [2] and Circular Electron-Positron Collider (CEPC) [3]. Beam tests showed that the efficiency of the GRPC layers of SDHCAL prototype exceeds 95% and excellent energy reconstruction resolution were obtained [4]–[6].

While the primary purpose of a calorimeter is to measure the overall event energy of both neutral and charged particles, high-granularity calorimeters like SDHCAL, incorporate systems allowing for event reconstruction and particle identification to fully exploit the potential of the future $e^+e^-$ high-energy colliders. The use of MRPC layers and timing electronics in the SDHCAL calorimeter will allow the exploitation of high-resolution timing information to improve on the event reconstruction which will be very important for the future colliders [7], [8].

In Section II, a prototype of the timing electronics is introduced. It is designed to work with MRPC layers to measure the precise time of the charged particles crossing these detectors. The timing electronic system presented here, contains 2 Petiroc2B ASICs [9]. To control and receive data from the Front-End Board (FEB), we designed a Data Acquisition (DAQ) system based on Zynq UltraScale+® System-on-Chip (SoC) [10], which consists of two parts: Programmable Logic (PL) and Processing System (PS). Compared to traditional FPGA, Zynq offers the advantage of integrating hardware and software components in a single chip, providing high performance and flexibility for designers, and significantly reducing the complexity of hardware system design and layout. However, the requirement on the developers is considerably increased, for the need of both FPGA hardware design and embedded software development [11]. Further details regarding the usage of Zynq is explained in Section II-C. The PC software is developed and implemented using Python and Qt5. The host computer communicates with the PS of Zynq via Gigabit Ethernet, functioning in both control and data acquisition.

The test results are presented in Section IV. To ensure the threshold uniformity of each channel of the Petiroc2B, calibration is operated before each test experiment, using its internal pre-amplifier baseline and individual threshold adjustment function. Injection tests have been carried out to evaluate the timing resolution within a single ASIC and between two ASICs, respectively.

## II. Design of Electronic System

The electronic system consists of the FEB, the DAQ system and PC. A block diagram is shown in Fig. 1. The FEB is in charge of detecting signals and transferring data to the DAQ system. The DAQ system is based on Zynq UltraScale+® SoC, and is connected to PC via Gigabit Ethernet.

### A. Front-End Board

The electronics developed for high resolution time measurement is very sensitive to noise and crosstalk, which can lead to fake hits. To get better signal quality, the FEB is designed

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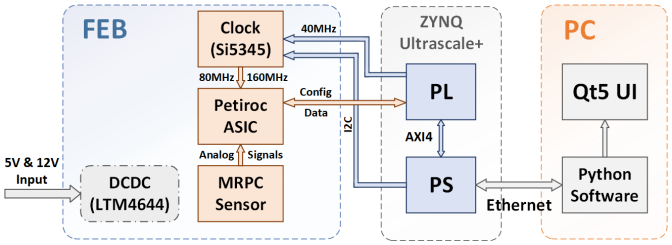



Fig. 1: Block diagram of the electronic system.


Fig. 2: Stack-up structure of the FEB layers.

to be a 10-layer board. The stack-up structure is shown in Fig. 2. Analog signals and power rails are designed to be well shielded from the other signals and the outside electromagnetic fields. It is achieved by putting both layers (one for analog signals and the other for power rails) between 3 ground layers and form a sandwich structure, while digital signals and power rails which have lower requirements for signal quality are designed in two close-by layers. Thanks to this design, no crosstalk is observed in any of our tests. A picture of the FEB is shown in Fig. 3, as well as the annotations of main components.

Power for the system is supplied by an external DC power source, which is connected to a quad DC/DC regulator LTM4644. In order to get higher power quality for analog circuits, The input power rail has two channels, 5V and 12V. 5V power rail is specified for Petiroc ASICs and 12V power rail is used for other parts such as clocks and translators.

The clocks are generated by a jitter attenuating clock multiplier Si5345. This component is capable of providing up to 10 programmable low-jitter clocks, ensuring stable and precise clocks for the system's operation [12]. Three sources are available to Si5345, clock from Zynq, onboard crystal oscillator, and external clock source.

SMA connectors are designed for injection tests and debug signal monitoring. Each ASIC has a few channels which are AC coupled to these SMA connectors. In addition, 4 SMA connectors are connected to Si5345, to allow for differential external input clock source and output clock, so that the clock can form a daisy chain between multiple boards to guarantee the synchronization.

To interface with the DAQ system, which is based on ZCU102 evaluation board [13], two FMA connectors are mounted to the back side of the board. There are also 64 1cm

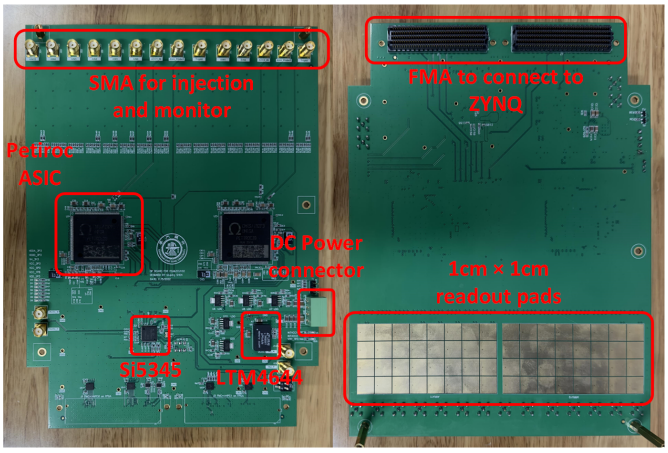



Fig. 3: Picture of both sides of the FEB.

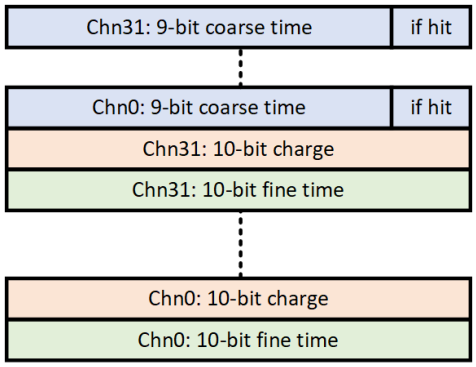



Fig. 4: Structure of the output data of Petiroc2B.

× 1cm copper pads on the back side for picking up MRPC signals.

### B. ASIC

Petiroc2B is a 32-channel front-end ASIC designed for particle time-of-flight measurement applications. The power per channel is 6 mW, and the readout is fully digital with 960-bit length, indicating four sets of information of each channel: 9-bit coarse time, 10-bit fine time, 10-bit charge and 1-bit if hit, as shown in Fig. 4. This work focuses on timing information.

The signal path for each of the 32 channels is composed of a preamplifier, a discriminator, and timing circuits. Timing of the signals involves two steps: Coarse timing and fine timing. Coarse timing is performed by a counter running at an input 40 MHz clock, resulting in the coarse bin size of 25 ns. Fine timing is performed by a Time-to-Amplitude Converter (TAC), converting time information to amplitude before digitizing. The time measurement process is demonstrated in Fig. 5. The equation for calculating time information is determined by ASIC architecture:

$$\begin{aligned}\text{event time} &= (\text{coarse time} + 1) \times (\text{coarse bin size}) - \\ &\quad (\text{fine time}) \times (\text{fine bin size}).\end{aligned}$$

fine bin size is approximately 37 ps, and can be precisely determined through periodic injection tests.

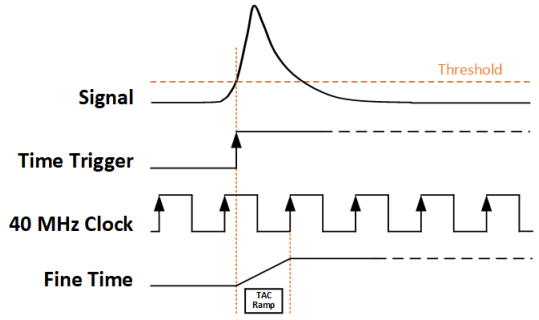



Fig. 5: A demonstration of time measurement.

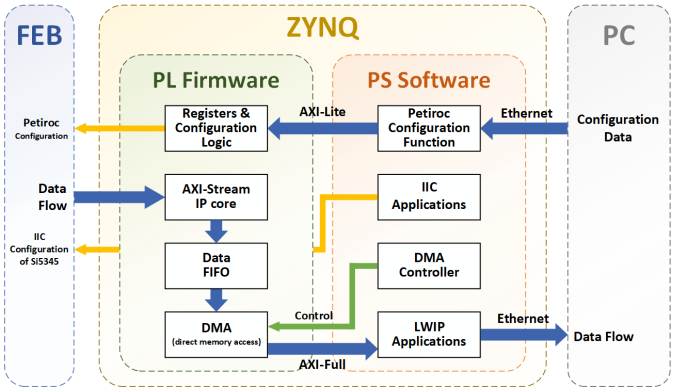



Fig. 6: Block diagram of the functions of Zynq.

### C. Zynq

The design of DAQ system is based on a ZCU102 evaluation board, populated with the Zynq UltraScale+® XCZU9EG-2FFVB1156E MPSoC. Zynq is composed of two parts: programmable logic and processing system. PL part is similar to a Kintex FPGA, and PS features the Arm® flagship Cortex®-A53 64-bit quad-core processor and Cortex-R5 dual-core real-time processor. The special structure of Zynq allows us to put some of the functions, such as Inter-Integrated Circuit ($I^2C$), Lightweight IP (LwIP), etc. from PL to PS, which is easier to use and saves the complexity of the hardware. The functions of Zynq in our electronic system is illustrated in Fig. 6, which can be divided into two parts: PL firmware and PS software.

*1) Programmable Logic:* PL is directly connected to the FEB, controlling Petiroc2B and receiving data from it. PL contains First-In-First-Out (FIFO), Advanced eXtensible Interface (AXI) logic cores, Direct Memory Access (DMA), configuration logic core, readout logic core and other customized logic cores designed especially for Petiroc2B.

The configuration data flow and received data flow run through different paths. Configuration data is generated by PC software, sent by PS via AXI-Lite protocol, and then transferred to a customized AXI-Lite logic core, which turns AXI-Lite data flow into 32 32-bit registers. When these registers are updated, the configuration logic will be triggered and shift the values of the registers into Petiroc2B's flip flops in order to configure the ASIC.

The receiving logic is triggered by a flag signal, which is generated by Petiroc2B and synchronized with the data. The receiving logic includes triggering logic, serial to parallel converter, data FIFO, AXI-Stream logic core and DMA. After triggering, the received data will be first sent to serial to parallel converter, in order to use AXI protocol which is a parallel on-chip communication bus protocol. Then it is input to a data FIFO to synchronize with the PS clock, followed by a logical DMA to store and be prepared for the PS to read.

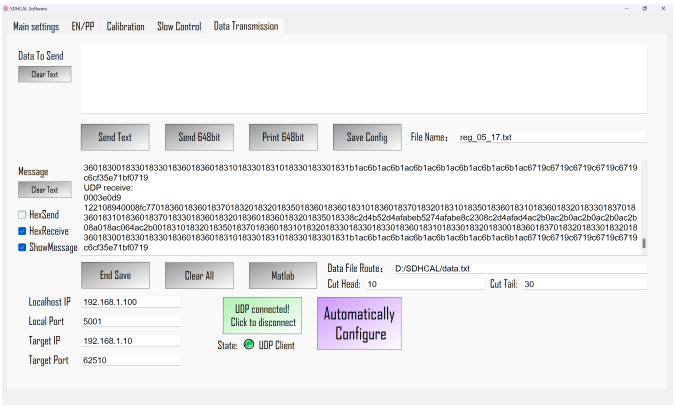



Fig. 7: Data transmission tab of the software UI.

*2) Processing System:* PS is operated on an ARM Cortex-A53 CPU, which is integrated on Zynq. The software we design is composed of $I^2C$ applications, LwIP applications, DMA controller and other user-defined functions.

Zynq provides $I^2C$ buses that are fully controlled by PS, so Si5345 is configured and controlled by software-based $I^2C$ applications in Zynq SoC. Using PS $I^2C$ applications gives us the flexibility to modify the clock configurations, in order to switch the clock source, without fully restart of the hardware system.

LwIP is a widely used TCP/IP stack for embedded systems [14]. Zynq SoCs have separate PL and PS Ethernet connection pins, which allows users to operate Ethernet applications only in PS and significantly reduces the complexity of hardware, resulting in saving a large amount of resources of PL.

PL-PS communication is performed by AXI-Full protocol, which requires a memory space to store the data from AXI-Stream data flow. Thus, a DMA is instantiated in PL, and is controlled by a DMA controller in PS via AXI-Lite protocol. Besides providing memory space, DMA can also free the main processor unit when operating reading or writing, improving the efficiency of the PS. The maximum transmission rate of DMA depends on the memory hardware, which is DDR4 RAM sticks on ZCU102 evaluation boards.

## III. PC Software

The software is designed using Python and Qt5, with main functions including generating configuration data, communicating with PS via Ethernet, controlling the FEB, performing "S-curve" tests, and implementing calibration. To include all the functions, the software User Interface (UI) is divided into 5 tabs. A screenshot of software UI is shown in Fig. 7.

### A. Configuration

Each Petiroc2B ASIC is configured by a 648-bit configuration data stream. The most fundamental function of the

software is generating this configuration data.

First three tabs are used for the configuration of Petiroc2B, where individual masks, charge and time thresholds, variable capacitors can be set. And in "Calibration" tab, users can control individual 6-bit threshold DACs, which are crucial for the threshold calibration.

### B. Calibration

To ensure the uniformity of the thresholds of all the channels, calibration needs to be done before each test experiment. The time threshold of each channel can be calculated by the following equation:

$$\begin{aligned}\text{Time Threshold} &= 0.89\ \text{V} + [(\text{10-bit DAC value} * 0.92\ \text{mV}) \\ &\quad - (\text{6-bit DAC value} * 1.5\ \text{mV})].\end{aligned} \tag{1}$$

10-bit DAC is the common time threshold, 6-bit DAC is the individual threshold of each channel. Calibration is performed by adjusting individual 6-bit DACs in order to make time threshold of all the channels as close as possible [15].

Before proceeding with the calibration, it is essential to first obtain the "S-curves". Thanks to the pre-amplifier baseline, "S-curve" tests can be performed on the pedestal, not depending on injection signals, which is crucial in future applications with a large number of channels. To obtain the "S-curves", we need to scan through the 10-bit time threshold DAC. For each channel, the trigger rate should be 100% when threshold is lower than pre-amplifier baseline and 0 when higher, theoretically. And in application, the trigger rate vs. threshold DAC curve is similar to the shape of inverted letter "S", which is why it is called "S-curve". If the all channels thresholds have a good uniformity, "S-curves" of the channels should be close to each other. The calibration is intended to reduce the separation of the "S-curves" through adjusting the individual 6-bit DACs.

Firstly, the pre-amplifier baseline is about 1.15 V, which indicates that the 10-bit time threshold DAC should be around 330 to start triggering on the baseline, giving that the 6-bit DACs are set to 32 (half of the maximum) by default to get maximum adjustment range, referring to "(1)".

Then the first "S-curve" test is performed. A figure of original "S-curves" will be plotted, which is usually dispersive. From the first "S-curves", average 50% trigger rate threshold DAC can be obtained by "(2)", in which $Th_{50\%}$ stands for average 50% trigger rate threshold, $S$ stands for "S-curve", or trigger rate as a function of threshold and $Th$ stands for threshold.

$$Th_{50\%} = \frac{\sum_{\text{chn}} \int S(Th)dTh}{\text{Chn Num}} \tag{2}$$

The calibration process is operated after the "S-curve" test. Set the 10-bit time threshold DAC to be the average 50% trigger rate threshold DAC, and start the iteration for finding individual 6-bit DAC for each channel to make the trigger rate as close as possible to 50%. The iteration is implemented by bisection method, which means the target settings are reached after five iterations (starts with 16).

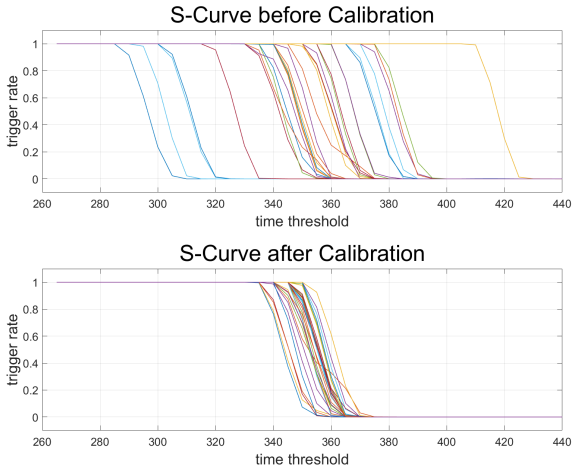



Fig. 8: Calibration result of ASIC1. The figure on the top panel shows the S-curves before calibration. The spread of the S-curves is over 100, with the RMS of 25.25 DAC. The figure on the bottom panel shows the S-curves after calibration. The spread is reduced to about 20, with the RMS of 4.56 DAC.

After the individual 6-bit DACs reach the target setting, another "S-curve" test is performed. The uniformity of the thresholds is guaranteed by checking that the "S-curves" after calibration are well aligned.

### C. Data transmission

For the data transmission, users need to input the local and target IP and port number according to PC and Zynq settings. Data transmission is operated by Gigabit Ethernet protocol. The software can generate and send the Petiroc2B configuration data, specified by the settings of previous tabs, to the FEB, and save the data from the FEB to user-defined file routes. It also integrates MATLAB® engine for data decoding and analyzing.

## IV. Results of Laboratory Commissioning

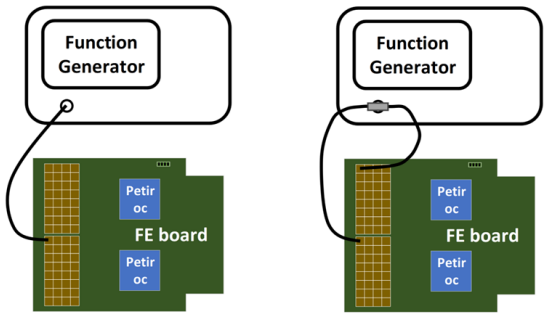
Calibration tests and injection tests are carried out to validate the electronic system. Calibration tests are intended to compare the S-curves before and after the calibration, to validate the calibration procedure and make sure that the system is properly set. The injection tests are performed to evaluate the timing resolution of the electronic system.

### A. Calibration tests

The "S-curves" before and after calibration are shown in Fig. 8. The RMS of the 50% trigger rate thresholds before calibration is 25.25 DAC (23.23 mV), and reduced to 4.56 DAC (4.20 mV) after calibration. The obvious reduction of separation of the "S-curves" validates the calibration.

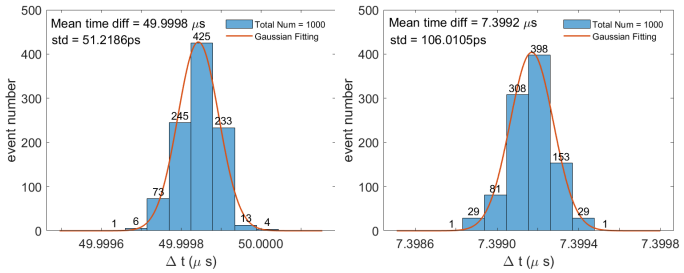
### B. Injection tests

The timing performance of the system was evaluated by injection tests. Periodic pulse waves of frequency 20 kHz are




(a) single channel injection (b) coincident signal injection

Fig. 9: Sketch of injection tests: (a): Single channel injection: Inject a periodic pulse signal into one channel; (b): Coincident signal injection: Inject the same periodic signal into two ASICs via a two-way splitter and identical wires.




(a) Single channel hits (b) Coincident hits

Fig. 10: Results of injection tests: (a): Timing between neighbor hits of the injected signal of one channel; (b): Timing of coincident hits between two ASICs.

injected to the ASICs. The pulse is generated by a Tektronix® AFG 31000 function generator with negative amplitude of 30.0 mVpp, leading edge of 1.000 $\mu$s, trailing edge of 2.00 ns and duty of 95%.

Two tests were performed to evaluate the timing performance: One is to evaluate the time resolution of events within one ASIC, by injecting the signal into one channel, and measuring time differences between every two neighbor events. The other is the Coincidence Time Resolution (CTR) test, which is performed by injecting the same signal into one channel of each ASIC using a two-way splitter, and measuring the difference of times of the same event between two ASICs.The results of timing performance are shown in Fig. 10.

The RMS of the time differences between neighbor events is 51.2 ps, so the intrinsic time resolution of one channel is about 36 ps (divided by $\sqrt{2}$). The RMS of the CTR test result is 106 ps, so the overall timing resolution of the electronic system is about 75 ps.

It is hard to ignore that the time resolution of events between different ASICs is considerably less precise than intrinsic time resolution of one channel. We believe that this difference is due to the jitter of the clocks, which can be eliminated within one ASIC by taking the difference and shows up when two ASICs are compared.

## V. Discussion and Conclusion

A prototype of low-power high-resolution timing electronic system for MRPC readout is introduced in this paper. The design of the front-end electronic system is based on Petiroc2B ASIC, and the DAQ system is based on Zynq SoC and PyQt5 software. The prototype reaches the resolution of better than 100 ps, which is expected to be an important information for the energy reconstruction.of hadronic showers and their separation in future high-energy colliders.

Comparing to traditional RPC readout electronics, this design has the advantages of high timing resolution, low power consumption and high channel density, which gives it the potential for large detectors in the future colliders. It was originally designed to be used in CALICE T-SDHCAL, and can potentially be used as readout electronics for other (M)RPCs too.

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