Prototype Design of Data Converter Module for LLRF Applications

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***Abstract*—In this paper, a mezzanine card is designed based on high speed ADC and DAC for particle accelerator field. FPGA firmware was built to realize high-speed A/D conversion and D/A conversion. The performance of the ADC on the board was tested. The experimental results show that the ENOB of the ADC with a sampling rate of 125MSPS can be as high as 12.96.**

***Index Terms*—A/D converter, Circuit boards, D/A converter, Data conversion**

I. Introduction

IN modern accelerator applications, stringent requirements are placed on the noise performance of digital converters. The noise from the digital converter will become part of the field noise seen by the beam, thus necessitating a low-noise, low-crosstalk digitizer. In response to this demand, this paper presents the design of a digital converter circuit board with 8 analog-to-digital converter (ADC) channels and 2 analog-to-digital converter (DAC) channels, which has been subjected to testing. The test results indicate that the circuit board possesses low noise and low crosstalk characteristics, rendering it suitable for reading accelerator signals.

II. Hardware Design

Figure 1 shows the design of the mezzanine card. The main functional components include two quad 125MSPS 16bit ADCs, one dual 500MSPS 16bit DAC, a clock distributor, trigger function circuit, FMC connectors. The PCB has 8 layers and can be divided into ground, power and signal layers. The design needs to pay attention to impedance matching and data line length processing. The actual weld of this mezzanine card is shown as Fig. 2.

The ADC is ADI's AD9653. The AD9653 is a 4-channel, 16-bit, 125 MSPS ADC with conversion rates up to 125 MSPS, outstanding dynamic performance and low power consumption.

The DAC is ADI's AD9783. The AD9783 is a pin-compatible, high-dynamic-range, 16-bit resolution, dual-channel DAC with sampling rates up to 500 MSPS.

The clock distributor is TI's LTC6953.The LTC6953 is a 11-channel high-performance, ultra-low jitter clock distribution. The additive output jitter < 6fsRMS when integration BW = 12kHz to 20MHz and f = 4.5GHz.

The digital signals from the ADCs and DACs interact with the FPGA using an LVDS interface. the FPGA can control these chips via the SPI protocol.

Other features include current monitoring, temperature monitoring, RMS detector, etc. These functions can be interfaced with FMCs via the IIC protocol, which allows the use of FPGAs or MCUs to interact with these chips. This design uses an external 1.25V reference voltage.

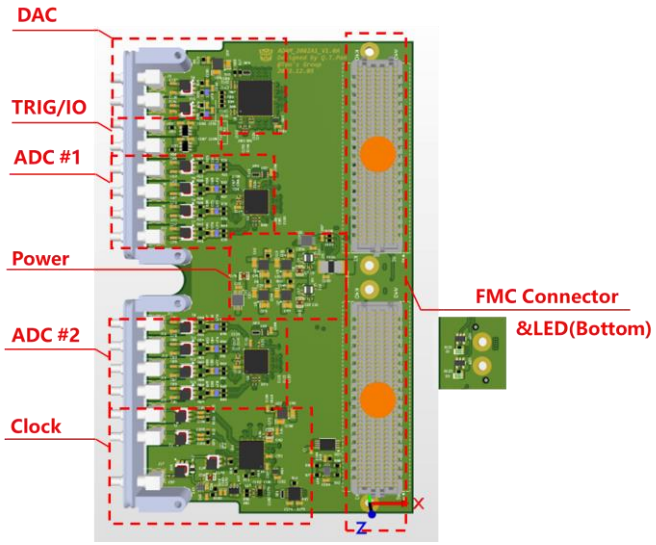

Fig. 1 High-speed PCB design.

Fig. 2 High-speed mezzanine card.

III. Firmware Design and Experiment

The FPGA readout firmware is designed refer to the timing diagram in the AD9653's and AD9783's datasheet. The ADC readout firmware logic block diagram is shown in Figure 3. The figure shows the readout logic for only one channel; the other channels are similar. The DAC firmware logic block diagram is shown in Figure 4.

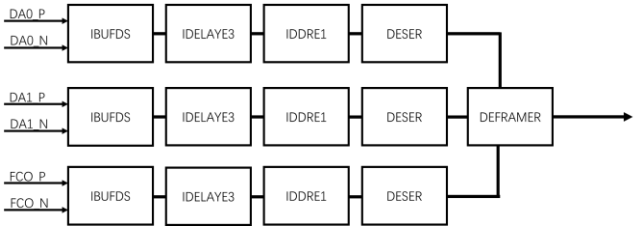

Fig. 3 AD9653 Readout Logic Block Diagram

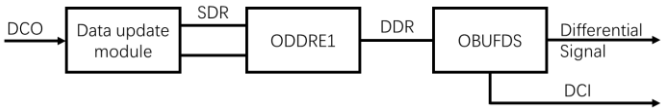

Fig. 4 AD9783 Logic Block Diagram

The experiment uses the SMA100B signal source to generate a sine wave signal and 500MHz clock. The 500MHz clock can be divided by the LTC6953 to provide a 500MHz clock for the AD9783 and a 125MHz clock for the AD9653.

Change the registers of AD9653, AD9783, and LTC6953 through SPI protocol, is they work in the appropriate state. The FPGA used for data readout is XCKU060-FFVA1156-2. The output of the ADC is read and analyzed by ILA. Current monitoring, temperature monitoring, and RMS detector values can be read via the IIC.

IV. RESULT

The ADC's ENOB can be as high as 12.96 when using an external 1.25V reference voltage. Part of the waveform and the SNR analysis are shown in the right figure. The experimental conditions for the figure on the right are an ADC sampling rate of 125 MHz and a sine wave signal source frequency of 10MHz.

After testing, the supply voltage of this circuit is 12V, the current is about 0.45A, and the power is about 5.4W.

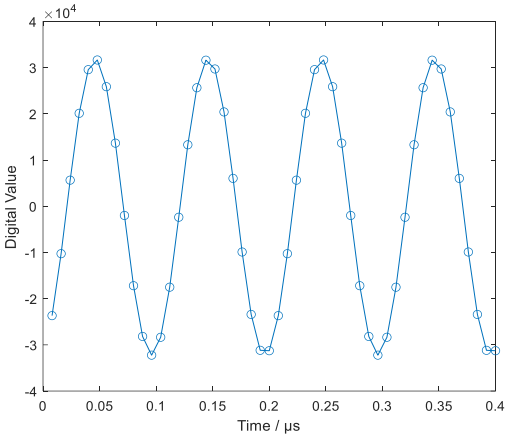

Fig. 5 Waveform

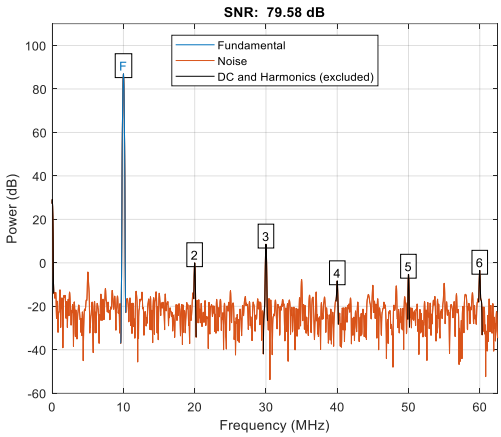

Fig. 6 SNR analysis

V. CONCLUSION

This paper designs a low noise data conversion module for LLRF applications. The ENOB of the ADC can be tested up to 12.96.

REFERENCES

[1] Huang, G., Doolittle, L., Xu, Y. L., & Yang, J. (2016). Low noise digitizer design for LCLS-II LLRF. NAPAC2016, Chicago, IL.