Preliminary Design of Data Exchange Module with USB and QSFP Interface for Test of Readout Electronics

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***Abstract*—The FT601 is a high-performance USB3.0 to FIFO bridge chip, which can be utilized in applications that require high data throughput, such as multi-channel FIFO ADC or DAC devices. This paper presents the design of a circuit board that enables the transmission of data from a QSFP interface to a PC via a Type-C interface, based on the FT601 and Xilinx Artix-XC7A35T FPGA. The design of the data transmission board and its performance test results are discussed in this paper.**

***Index Terms*—Enter key words or phrases in alphabetical order, separated by commas. For a list of suggested keywords, send a blank e-mail to keywords@ieee.org or visit http://www.ieee.org/organizations/pubs/ani_prod/keywrd98.txt**

I. Introduction

When exploring scientific problems related to nuclear physics, there is usually a large amount of data transfer involved. The design of this paper can realize the data transmission from QSFP to USB, so as to realize the fast data transmission to PC. This design can simplify the link of collecting data, and can realize the data transmission speed of USB3.0, which brings higher operability and convenience for the experiments with the transmission speed under 300MB/s.

II. Hardware Design

Figure 1 shows the design of the adapter board. The main functional components include the QSFP cable, the FPGA (XC7A35T), the FT601, the MUX chip and the USB3.0 cable. The PCB has 8 layers and can be divided into ground, power and signal layers. The design needs to pay attention to impedance matching and data line length processing. The actual weld of this PCB is shown as Fig. 2.

The XC7A35T contains a set of GTP and three low-speed banks. during design, the high-speed data lines of the QSFP need to be connected to the GTP, and the data lines and clock lines of the FT601 need to be connected to the same low-speed banks. during PCB design, attention needs to be paid to the equalization of the differential lines as well as the equalization of the clock lines of the data lines of the FT601.

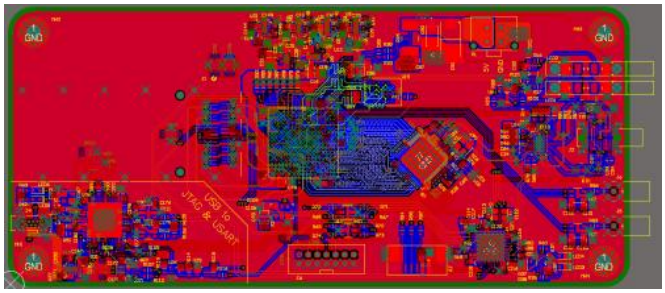

Fig. 1 PCB design

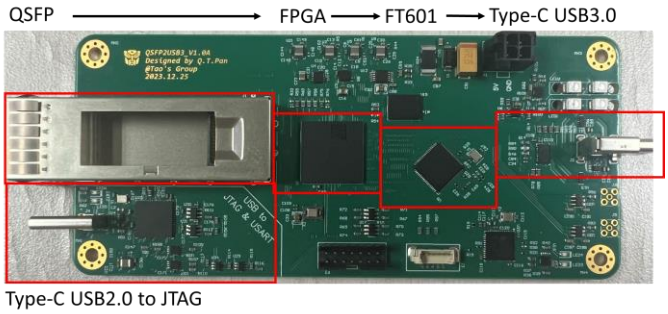

Fig. 2 PCB

III. Experiment

The logic block diagram of the firmware design for the FPGA is shown in Figure 3. Data transfer was tested by using Aurora64B/66B's external self-loopback mode. The Data Generation Module generates continuously growing data, which is subsequently sent to the Optical Module via Aurora 64B/66B, looped back within the Optical Module, and then Aurora 64B/66B reads the data and sends it to the Data Transmission Module. The data is sent in the timing sequence required by the FT601 and then sent to the PC via Type-C using the USB3.0 protocol.

In this paper, we designed the software to read and store data based on the driver and function library provided by FTDI. The software needs to cooperate with hardware and firmware to realize the reading and storing of data. In the software, you can set the size of the word storage file, which is limited by the computer's own memory. In the software, you can set the size of the word storage file, which is limited by the computer's own memory. When data is read from the computer's external circuitry, it is stored as a file in binary format. The reading of the file is easily accomplished using MATLAB, which facilitates the processing of the data.

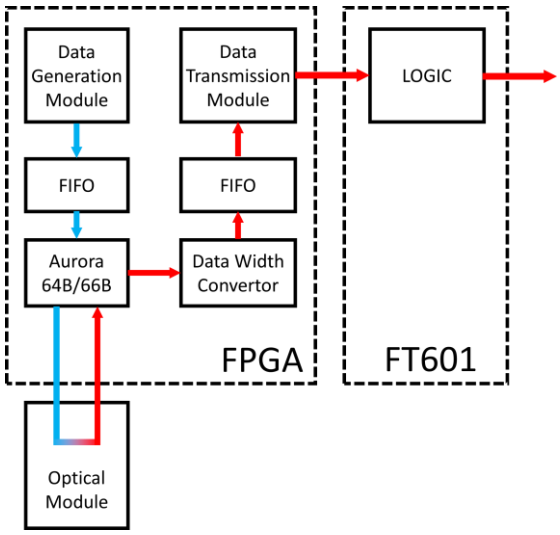

Fig. 3 logic block design

The FT601 has specific timing logic requirements for data interaction with the FPGA, which need to be accomplished by referring to the datasheet. The FT601 receives data from the FPGA and transmits it to the PC via Super Speed USB.

The data link can be speed tested using the scripting software provided by FTDI. Theoretically the fastest write speed can reach 400MB/s, the actual test write speed is about 350MB/s, which is enough for experiments with data streaming speeds below 300MB/s.

IV. Result

PC reads the data and stores the data as a file in .bin format. In this study, MATLAB is used to read the data in the file in degrees and do the analysis.

The data read by MATLAB is shown on the right, and it is the same as the preset values, with an error rate of 0% for all 100 transmission results.

The number of bytes transferred and stored can be rewritten by the driver. The size of a single .bin file in this experiment is about 8192kB, which can store 100 files in a few seconds. Faster storage can be achieved if larger files are stored.

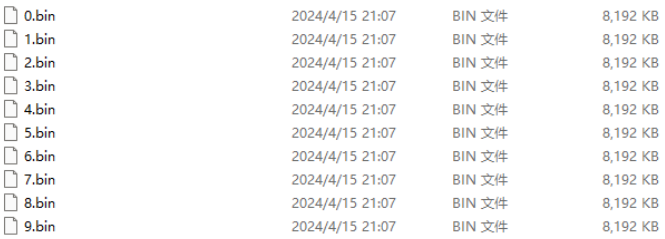

Fig. 4 Data storage as binary files

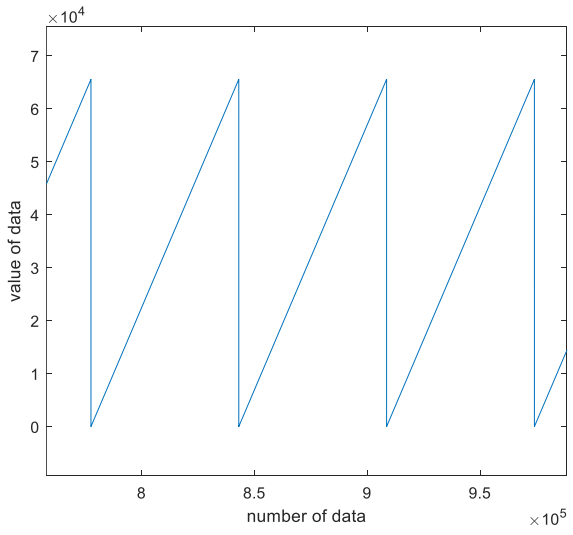

Fig. 5 Read-out data

V. Conclusion

This paper designs a QSFP to USB 3.0 data conversion module for readout electronics testing. The module is realized based on XC7A35T FPGA and FT601, which can realize up to 300MB/s data transfer speed, and can meet most of the experimental tests and preliminary tests of complex experiments.