Design of a 11-bit column-parallel ADC for Monolithic Active Pixel Sensor


Weijia Han

Yongsheng Wang[1], Chengyou Xia[1], Weijia Han[2,], Yuhao Wen[1], Boxuan Li[1], Jiarui Wang[1], Fangfa Fu[1], Jinxiang Wang[1], Weijia Han[2], Chengxin Zhao*,[2,3]

[1]Department of Electronic Science and Technology, Harbin Institute of Technology, Harbin, China

[2]Institute of Modern Physics, Chinese Academy of Sciences, Lanzhou, China

[3]School of Nuclear Science and Technology, University of Chinese Academy of Sciences, Beijing, China

E-mail: chengxin.zhao@impcas.ac.cn

Introduction

- The various physics and applications at the Heavy Ion Research Facility in Lanzhou (HIRFL) and the High-Intensity Heavy-ion Accelerator Facility (HIAF) require **MAPS** to measure particle hit's position, energy deposition, and arrival time.
- An 11-bit column-parallel ADC has been designed to serve the pixels in every two adjacent columns.
- This ADC uses **cyclic architecture** to meet the strict requirements of the area.
- This ADC uses **SHA-less** architecture to reduce the power consumption.
- A novel MDAC architecture **with two residue generators** is proposed to reduce the power consumption **without additional area**.

Overall architecture

The simplified cyclic ADC architecture is shown in Figure 1, mainly consisting of a multiplying digital-to-analog converter (MDAC), a sub-ADC, and a digital correction circuit.

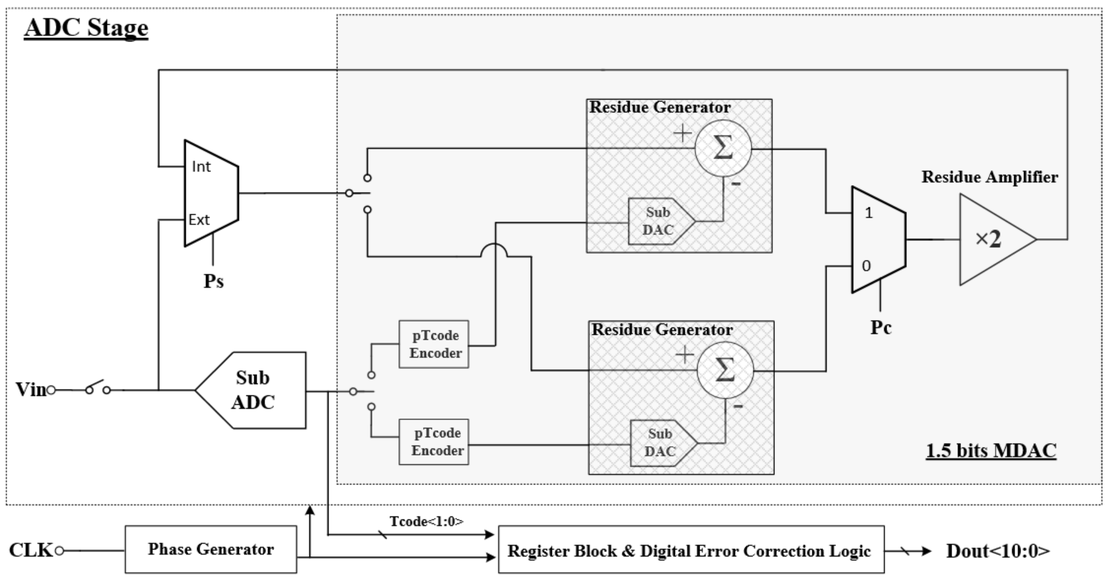

Fig. 1. Architecture of proposed Cyclic ADC

MDAC implementation

As seen in Figure 2, two RG are used in the MDAC.

- Allowing the amplification and sampling process to operate in the same time.
- The area remains unchanged by reusing the Sampling cap as load cap.

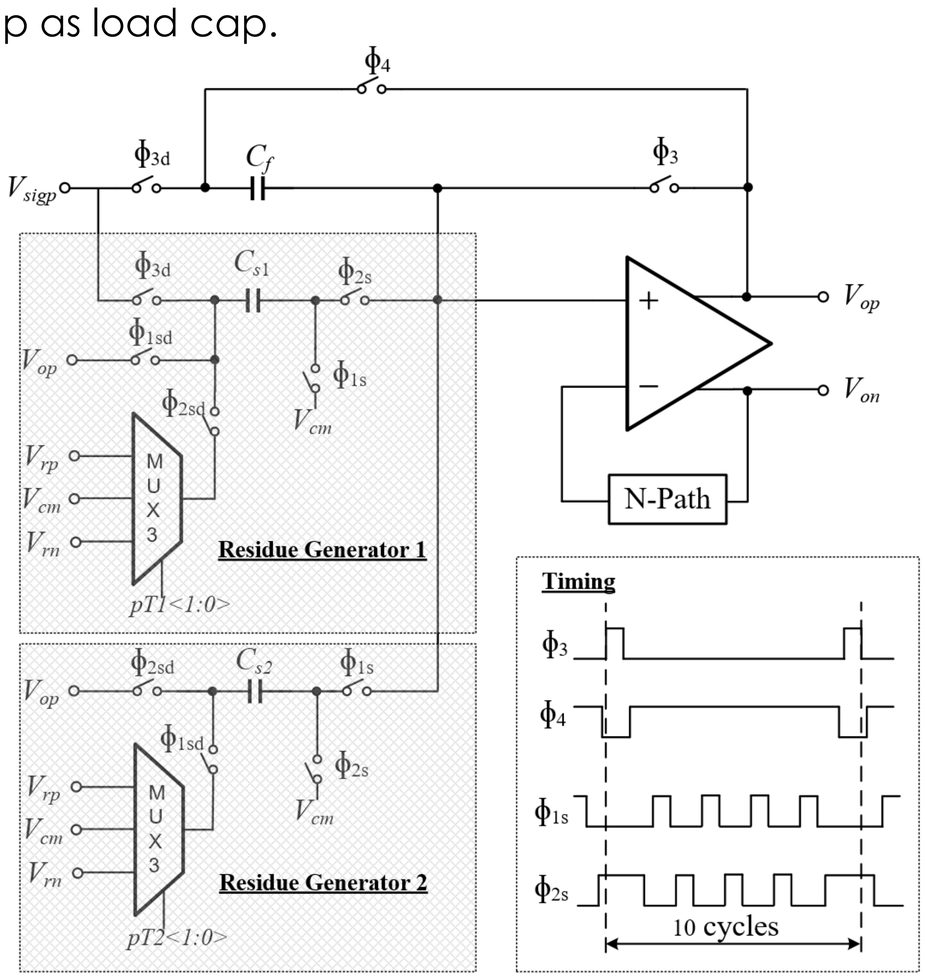

Fig. 2. Schematic of the MDAC

Amplifier implementation

The core amplifier of the MDAC is shown in Figure 3.

- This amplifier uses a **two-stage structure** to meet the requirements of high gain, high speed, and high output swing.
- This amplifier uses two kinds of cascode compensation.
- A PMOS input pair and an NMOS input pair are placed parallelly to achieve a **wide input common mode range** close to rail-to-rail.

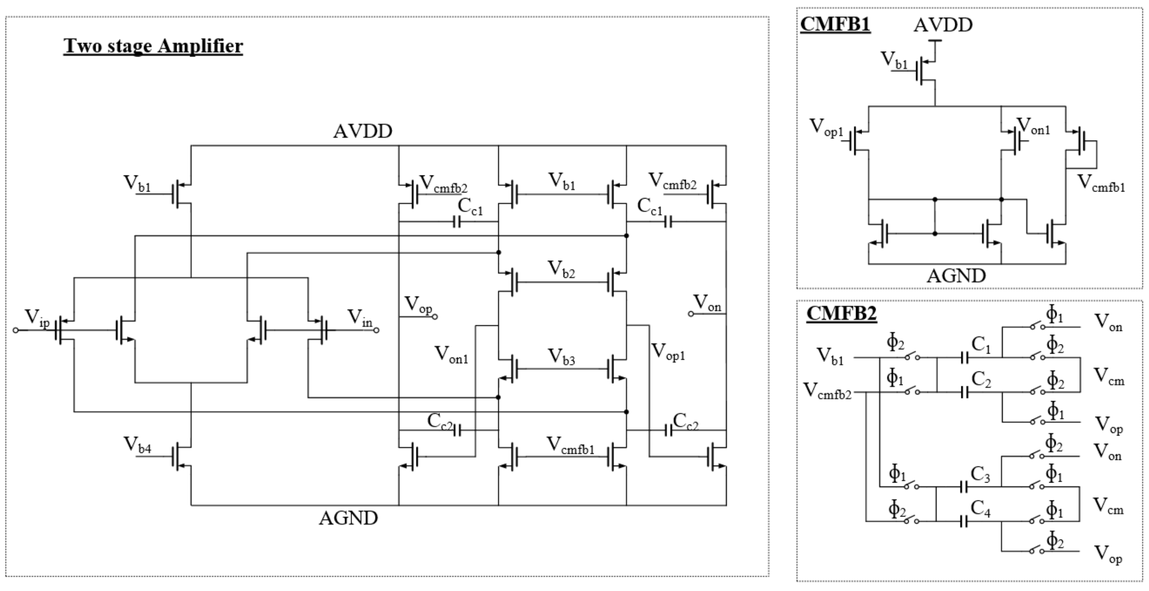

Fig. 3. Schematic of the core amplifier

Measurement Results

The measured performance of the ADC is shown in Figure 5 and the Layout of the ADC is shown in Figure 6. The **signal-to-noise and distortion ratio (SINAD) is 57.71 dB,** and **the effective number of bits (ENOB) is 9.3 bits**. The **area** of the ADC is **60×670 μm²**.

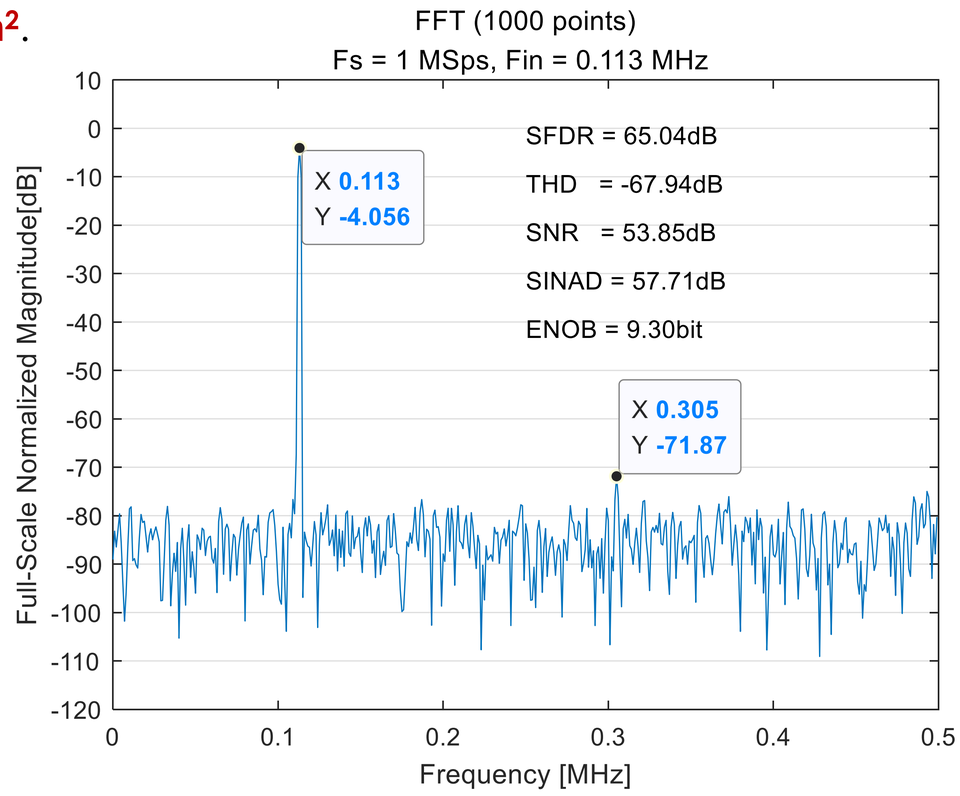

Fig. 5. Spectrum for 113 kHz input sampled at 1 MS/s

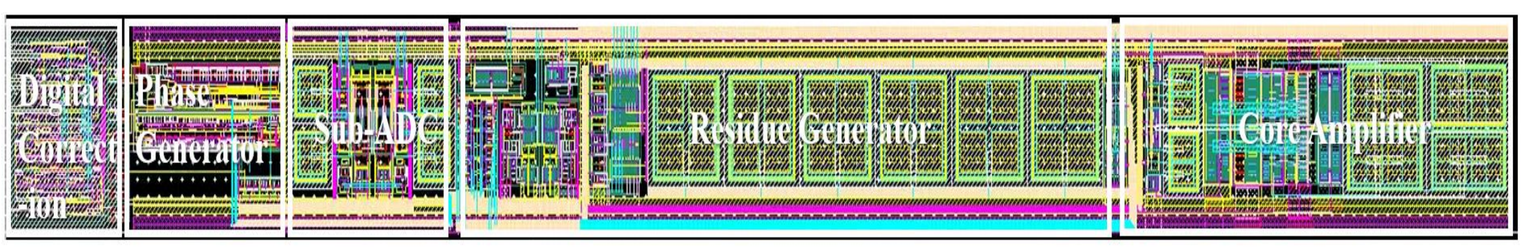

Fig. 6. Layout of this column-parallel ADC

哈爾濱工業大學 HARBIN INSTITUTE OF TECHNOLOGY

中国科学院近代物理研究所 Institute of Modern Physics, Chinese Academy of Sciences