Development of a High-Bandwidth Waveform Processing System using RFSoC for RI Beam Experiments

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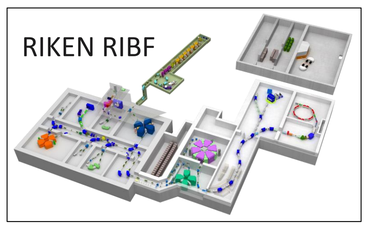
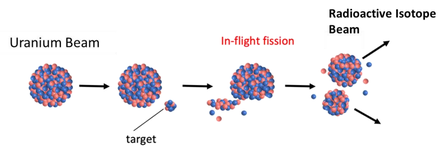
Introduction:RIKEN RI Beam Factory(RIBF)

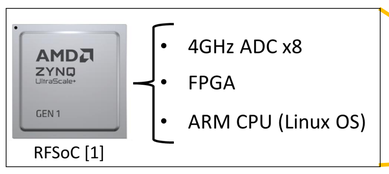


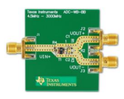
We are working on a data acquisition system for RIKEN RIBF that is a RI beam facility in Japan. various RI beams are produced via fission or projectile fragmentation reaction with heavy-ion beams such as uranium.
TOF measurements at high rate and high time resolution are required for particle identification of RI beams.
Goal of this development is : it can process more than 100kHz trigger rate with better than 25ps timing resolution in σ.

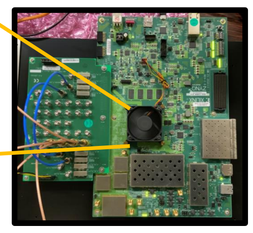


AMD RFSoC

We have been developing a new system based on **AMD RFSoC** [1]. The RFSoC device includes 4GHz ADC, FPGA, and CPU, so it **includes all necessary functions** for the data acquisition.
In this development, we use ZCU111 Evaluation kit [2].
In order to input differential signals to the ZCU111, a wideband balun board (ADC-WB-BB [3]) with a frequency range of 4.5-3000 MHz is used.



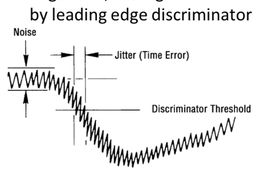

balun board (ADC-WB-BB[3])


ZCU111 Evaluation kit [2]

Timing Resolution

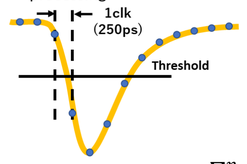
In general, the timing information is determined by the leading edge timing. However, this method is not suitable for waveform processing. Therefore, we have studied timing determination methods of extrapolation of the rising slope, zero-cross timing, and centroid calculation.

- In general, Timing determined by leading edge discriminator



$$\text{Timing Jitter} = \frac{\sigma_{noise}}{\left|\frac{dV}{dt}\right|}$$

- In case of FADC, apply waveform processing



⇨ **Centroid Calculation** $G = \frac{\sum_i^n v_i \times i}{\sum_i^n v_i}$

Here, **Centroid Calculation** was adopted.
The centroid calculation is independent of the slope form and can be applied to any waveforms.
Furthermore, in this equation, G is timing, and the denominator is charge, so **time and charge information can be obtained simultaneously**.

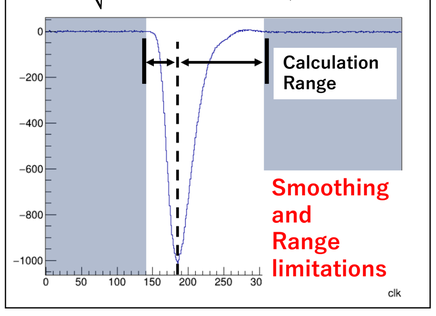
The signal-to-noise ratio is important to obtain high time resolution.For denominator, the white-noise component is cancelled by simple integration.
On the other hand, we have to consider the error propagation of the numerator g.

The effect of noise becomes very large due to each dv is multiplied by the clock number i.
To minimize effect of noise, first, white noise is canceled by **smoothing** as far as possible. In addition, by **limiting the calculation range**, low-frequency noise that cannot be removed by smoothing is reduced.

$$G = \frac{g}{\frac{\sum_i^n v_i \times i}{\sum_i^n v_i}}$$

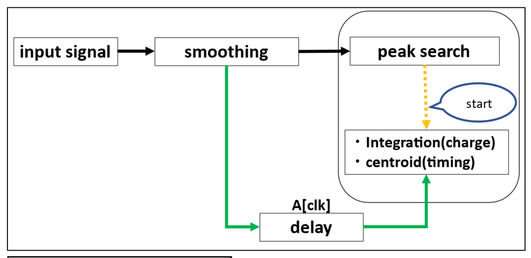
v_i: i th signal value

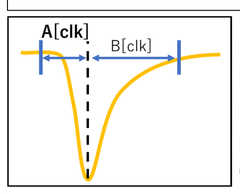
$$\text{error of } g \quad dg = \sqrt{\sum \left(\frac{\partial g}{\partial v_i} dv_i\right)^2} = \sqrt{\sum (i \times dv_i)^2}$$



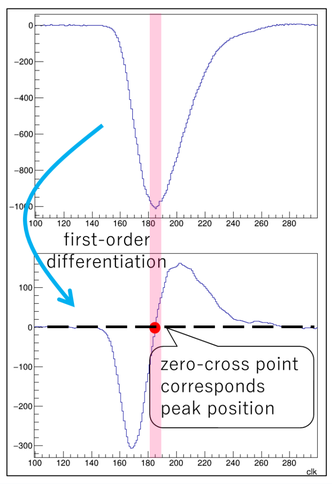
Waveform processing

We developed an algorithm for waveform processing that performs centroid calculations.This figure is the outline of waveform processing.
1st, the input signal is smoothed to reduce white noise.
2nd, peak detection circuit is implemented to determine the calculation range.
3rd, Using delayed waveform, the integration and centroid calculation is started after the peak position is detected.



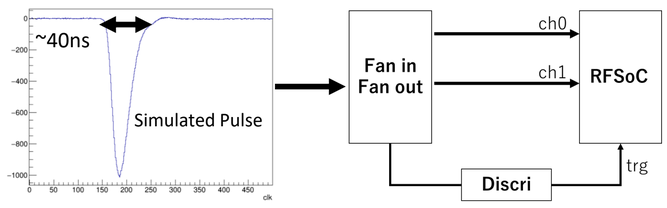


Determined calculation range based on peak position.
Manually set A and B as parameters.
(Calculate range = A+B)

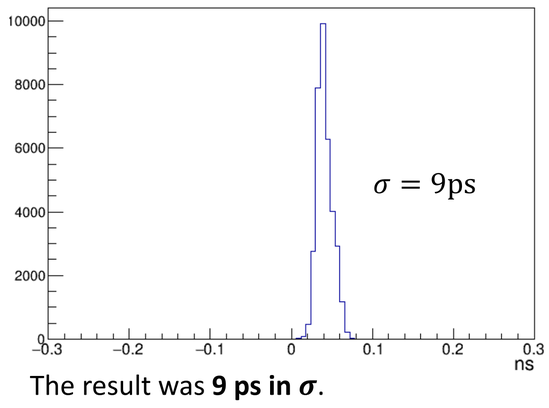


Timing resolution with centroid calculation

The timing resolution obtained by centroid calculations is shown. In this case, a pulse that simulated a plastic scintillator signal was used.
Distribute pulse signals with a Fan in Fan out module. The signals are input to ch0 and 1 of RFSoC.
Timing information is obtained by centroid calculation for each channel. The timing resolution of RFSoC is obtained from the time difference between the two channels.



circuit diagram



The result was **9 ps in σ**.
Very good timing resolution was achieved.

Algorithm of centroid calculation

To perform the real-time waveform processing in FPGA, centroid calculation is described as recurrence formula.
By adding the result of the denominator q to numerator g recursively, g can be described by recurrence formula.

numerator : $g_i = g_{i-1} + q_i$

denominator : $q_i = q_{i-1} + v_i$

$i = 1$ as the starting point of calculation

v_i : i th signal value
g_i : i th numerator value
q_i : i th denominator value

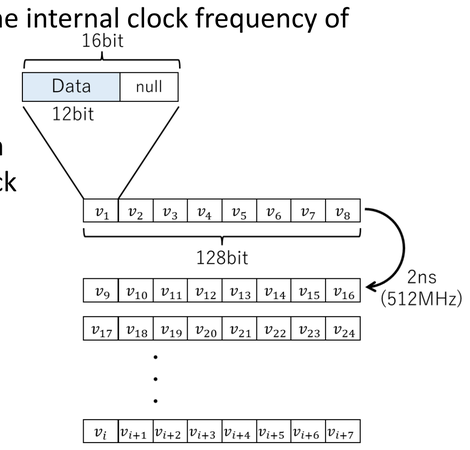
$$G = \frac{\sum(v_i \times i)}{\sum v_i} \longrightarrow \begin{cases} g_1 = 0 + q_1 = v_1 \\ g_2 = \underbrace{q_1}_{g_1} + q_2 = 2v_1 + v_2 \\ g_3 = \underbrace{q_1 + q_2}_{g_2} + q_3 = 3v_1 + 2v_2 + v_3 \\ \vdots \\ g_i = q_1 + q_2 + \cdots + q_{i-1} + q_i \\ \quad = \underbrace{iv_1 + (i-1)v_2 + \cdots}_{g_{i-1}} + v_i \end{cases}$$

Issue of algorithm implementation

There is an issue in implementing the developed algorithm to RFSoC. The sampling rate of ADC-block installed in the RFSoC is 4.096GSPS. On the other hand, the internal clock frequency of FPGA-block is 512MHz.

Hence, 8 data points of waveform are packed and sent to FPGA-block every 1clk.

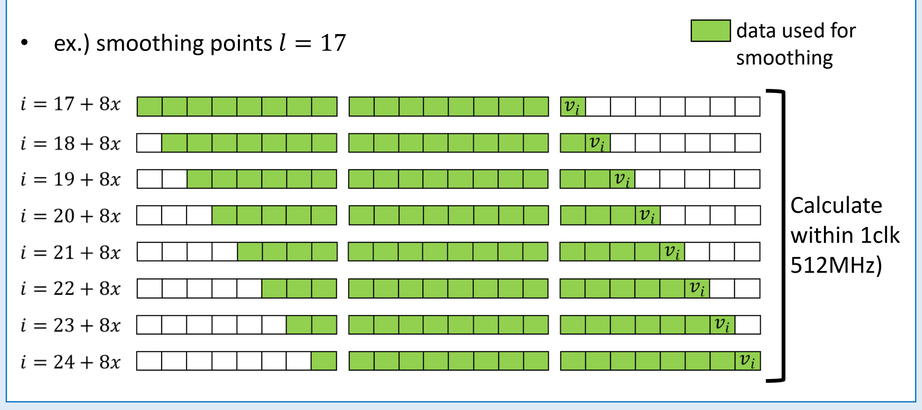
Therefore, Requires processing 8 data simultaneously.



Simultaneous processing of 8 data in smoothing

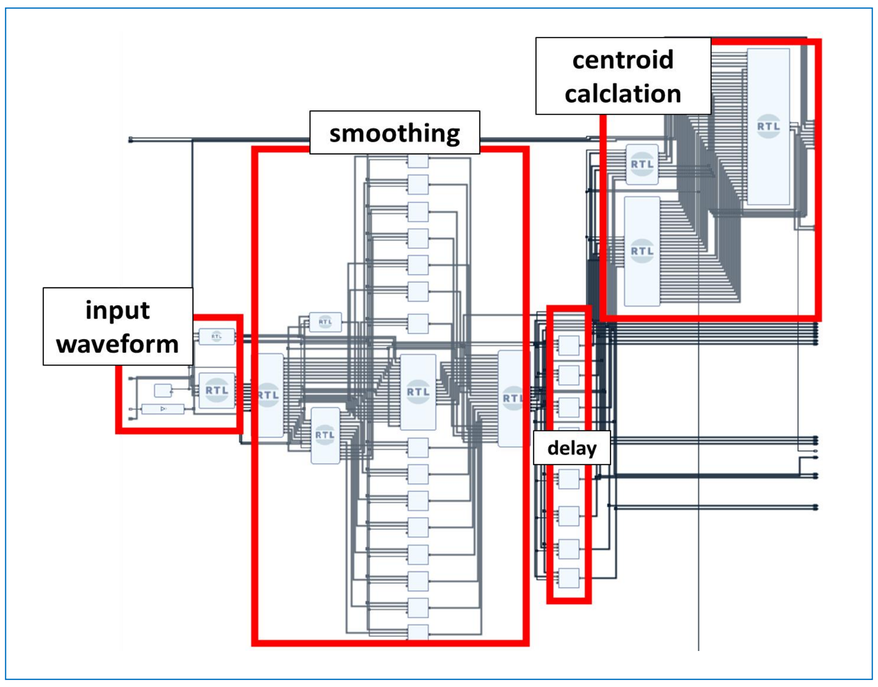
8 formulas are calculated in parallel within 1clk of FPGA(512MHz).
The data corresponding to 8 clk of 4GHz is always calculated in parallel.
For example, if the smoothing points $l = 17$, the calculation is performed as shown in the figure.
Thus, a circuit that calculates 8 formulas is implemented in the FPGA.

- ex.) smoothing points $l = 17$

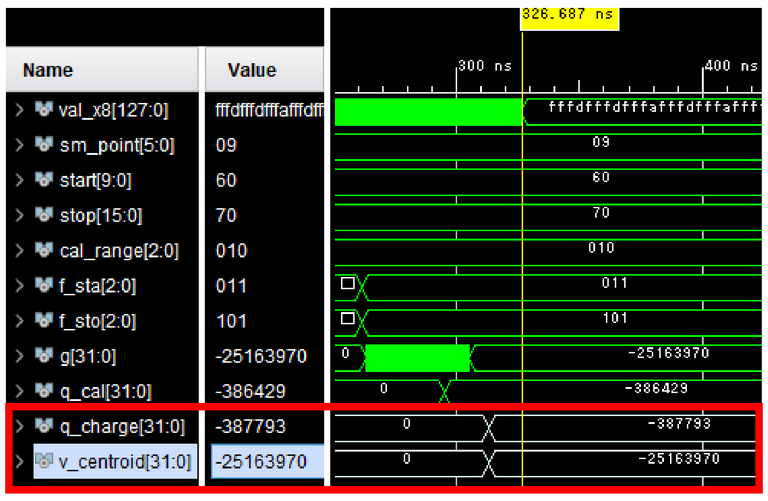


Result : Simultaneous processing of 8 data in smoothing

Simulation of the actual implementation of the developed algorithm on FPGA was performed. The implemented block diagram is shown below.



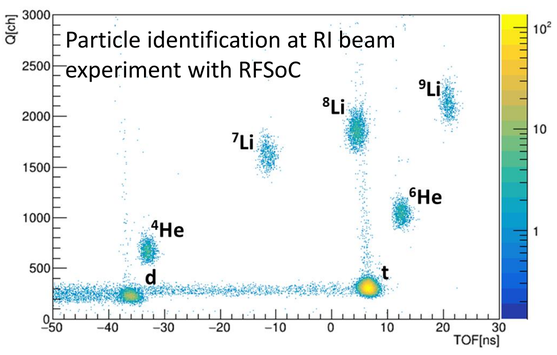
This figure shows simulation results for smoothing point $l = 9$.
It was confirmed that the simultaneous smoothing calculation of 8 data could be implemented correctly by the simulation.

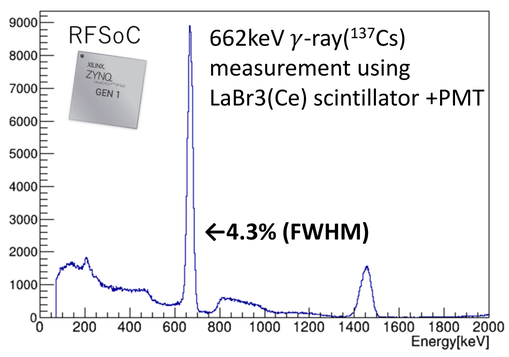


Summary

We have been developing next generation data acquisition system using RFSoC device. We adopted centroid calculation for waveform processing method. A very good timing resolution of σ=9ps was obtained.
Successfully developed an algorithm for 8 data simultaneous processing for smoothing and centroid calculation.
We plan to conduct a commissioning measurement using RI-beam in 2024.

Appendix





In the future development, Vadatech AMC573 board is used.
Frequency range : 10-4000 MHz


Vadatech AMC573

Reference

[1] AMD, Zynq UltraScale+ RFSoC
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