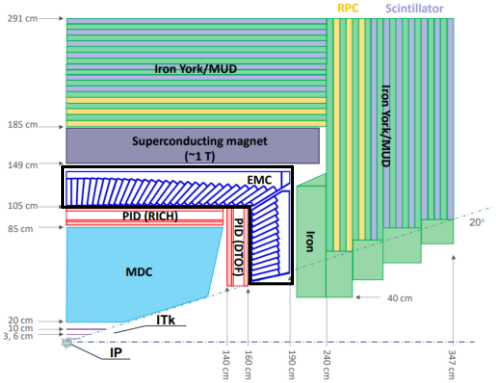
The Design of an 8-channel, 41.7-ps Resolution Time-to-Digital Converter for STCF ECAL

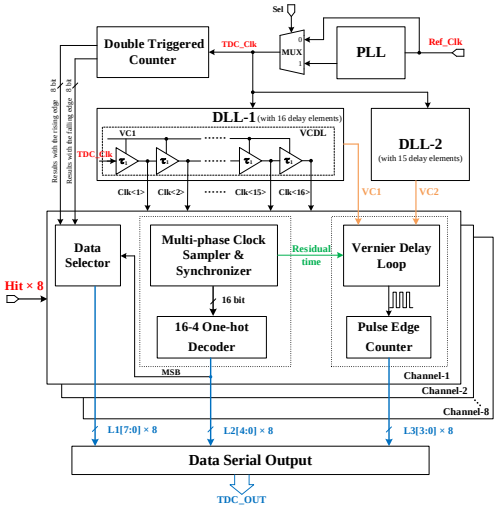
Introduction



To realize background suppression and events identification in the electromagnetic calorimeter (ECAL) of STCF, a time resolution better than 100-ps is required.

An 8-channel vernier delay loop (VDL) based TDC ASIC is proposed. The 3-level quantization topology is employed to get a wide dynamic range and a high resolution.

TDC Architecture

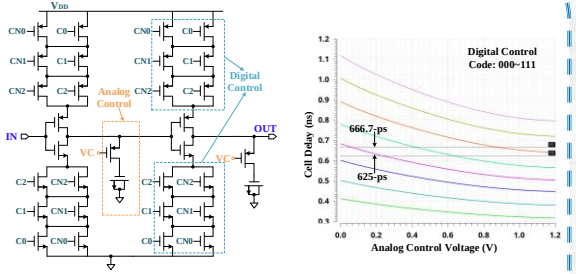


The 1st level: A global dual-edge triggered counter. (8-bit, LSB_1 = 10 ns)

The 2nd level: poly-phase interpolators. (4-bit, LSB_2 = 625 ps)

The 3rd level: vernier delay loop implemented with two DLLs. (5-bit, LSB_3 = 41.7 ps)

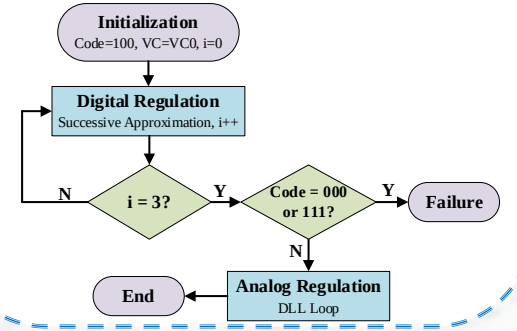
Low-Jitter DLL



K_{VCDL} ↓ → Voltage-Delay ↓ → Jitter ↓

Analog controlled shunt capacitor: To get a smooth, linear voltage-delay conversion curve.

Digital controlled current starve: To expand locking range of DLL with good linearity.



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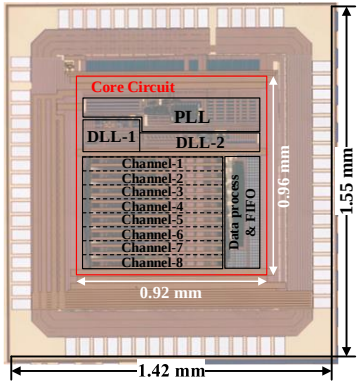
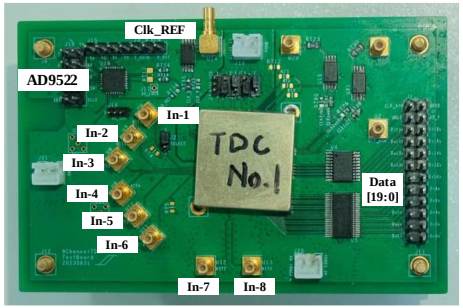
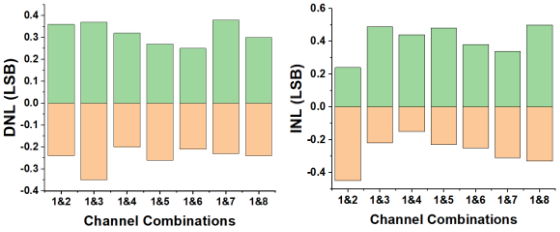
ASIC Prototype & PCB



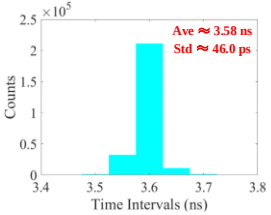


Test Results

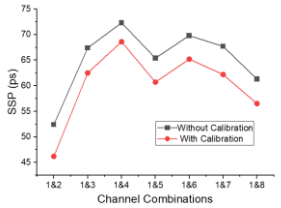
Linearity



Single Shoot Precision



Ch1 vs Ch2 (best case)



Ch1 vs other channels

Calibration: $TDC_{CAL} = TDC_{RAW} + INL[TDC_{RAW}]$

Conclusion

Parameters	[1]	[2]	[3]	This work
Process (nm)	130	110	180	180
Type	Delay line	Counter	VCRO	Vernier
Channels	1024	17	1024	8
Dynamic range (ns)	100	3400	2100	2560
SSP (ps)	78.5	104	62.1	46.0
DNL/INL (LSB)	0.4/1.2	0.3/2.5	0.5/2.2	0.4/0.5
Conversion Rate (MS/s)	500	/	/	22.2
Power (mW)	90	188.8	>1200	93.6*

* The presented power dissipation of proposed chip is obtained with the conversion rate of 4-MS/s.

An 8-channel, high precision TDC ASIC has been shown.

The TDC features with a single-shoot precision of 46-ps for the best case, the DNL and INL both better than 0.5-LSB and good consistency among all channels.

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