A fast front-end readout design for NICA-MPD shashlik electromagnetic calorimeter

Xinchi Ran[1], Zhi Deng[1,*], Fule Li[2], Tao Xue[1], Yi Wang[1], Yi Wang[2], Qiutong Pan[1], Lin Jiang[1], and Haoyan Yang[1]

[1] Key Laboratory of Particle and Radiation Imaging, Department of Engineering Physics, Tsinghua University, Beijing 100084, China
[2] Institute of Integrated Circuit Design and Electronic Design Automation, School of Integrated Circuits, Tsinghua University, Beijing 100084, China
*Correspondence: dengz@mail.tsinghua.edu.cn

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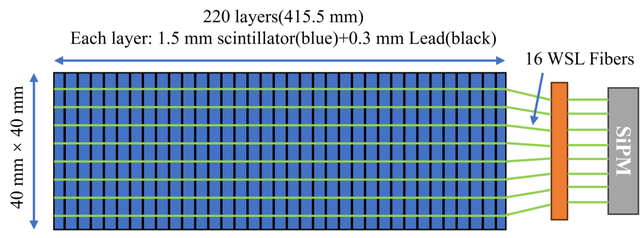
INTRODUCTION

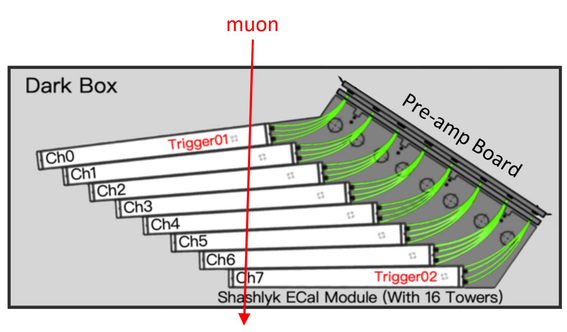
Electromagnetic Calorimeter (ECal)

- Shashlik sampling structure
- Bremsstrahlung photons collected through optical wavelength shifter (WLS) fibers
- Coupled with Silicon photomultipliers (SiPMs) readout



SiPM Readout

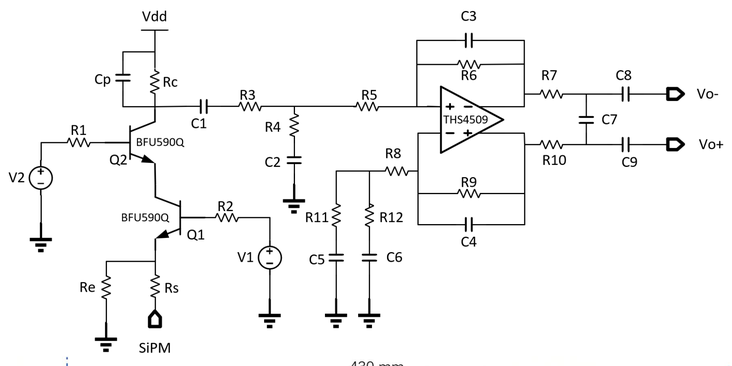
- Large terminal capacitance detector (> 100 pF)
- Nonlinear behavior arises with a finite input impedance amplifier
- Readout structure: trans-impedance (TIA) or common-base amplifier
- Unfavored effects: gain peaking and ringing of the output



READOUT DESIGN

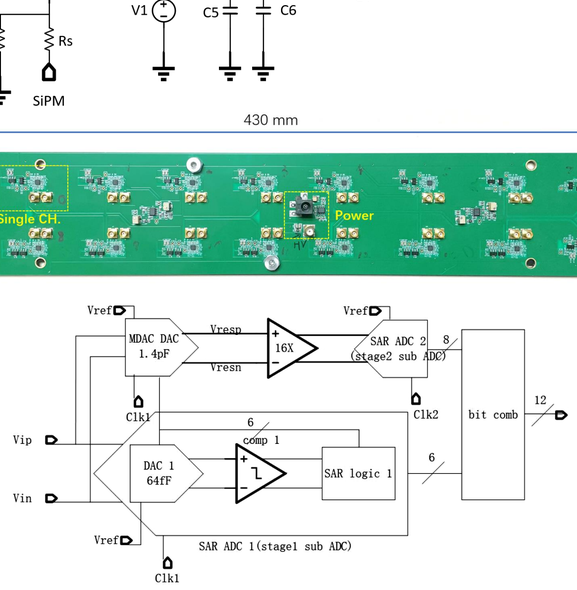
Preamplifier

- Detector: Hamamatsu multi-pixel photon counter (MPPC) S13360-6025 (typ. 1280 pF/ch)
- Circuit: a RF transistor current follower with a differential op-amp
- Working scenario: with an incident of 2000 photons, the output is ~750 mV (Vcom), ~1.5 V (Vdiff)
- PCB: 16 channels offers dual outputs



ADC

- 12bit 200MS/s pipeline SAR ADC architecture
- Two-step conversion process (6+7 bits), DAC1 with a smaller capacitance (64fF) while the MDAC DAC (1.4pF)
- A redundancy design is employed to effectively mitigate the Vref buffer requirements



Main Design Specifications				
Process Technology	Input Range	Power	ENOB @fin=100 MHz	SFDR @fin=100 MHz
TSMC65nmLP	± 600 mV	≤ 17 mW	≥ 10 bit	≥ 75 dBC

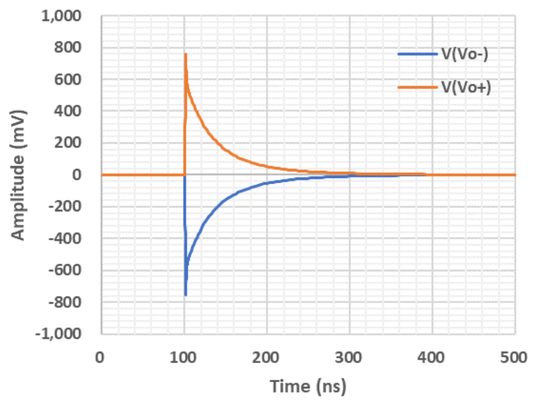
SPICE SIMULATION

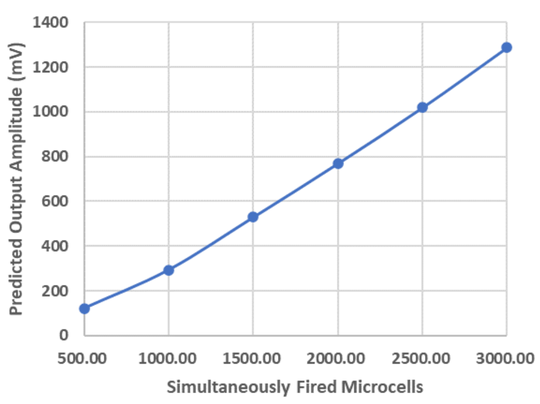
Preamplifier SPICE results

- **Software:** LTspice XVII
- **SiPM Model:**

Hamamatsu S13360-6025 Parameters							
G (10^5)	N_{cells}	C_d (fF)	C_g (pF)	R_q (kΩ)	C_q (fF)	V_{bias} (V)	M (ph)
7.13	57600	20.84	41.1	794	1.6	-56.9	2000

- **Preamplifier SPICE results:**

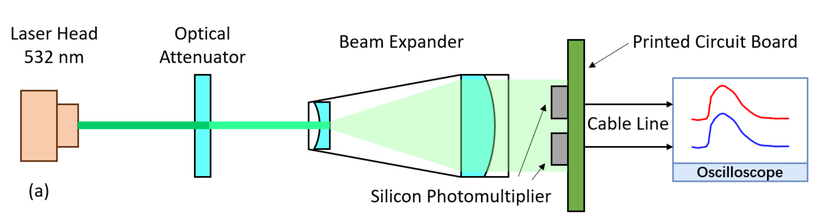


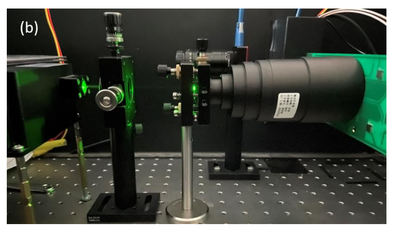


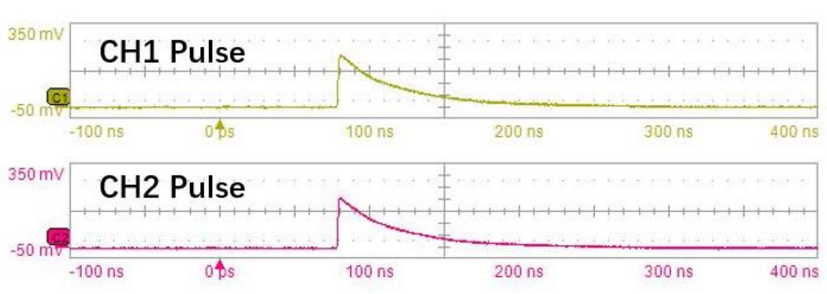
PRELIMINARY TEST

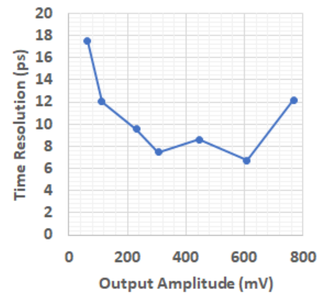
Laser test for preamplifier

- Signal rise time ~1.4 ns, giving the estimation of an expected bandwidth of roughly 250 MHz
- Single-channel time resolution performance better than 20 ps (samping rate @10GS/s)



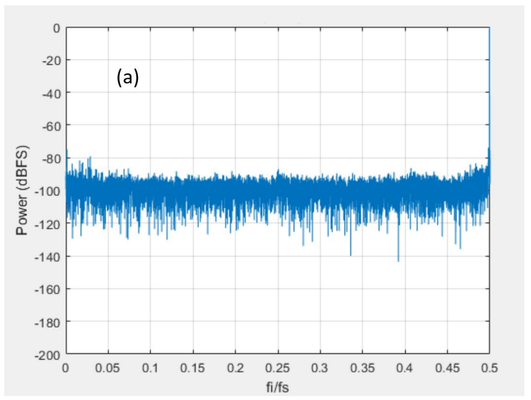


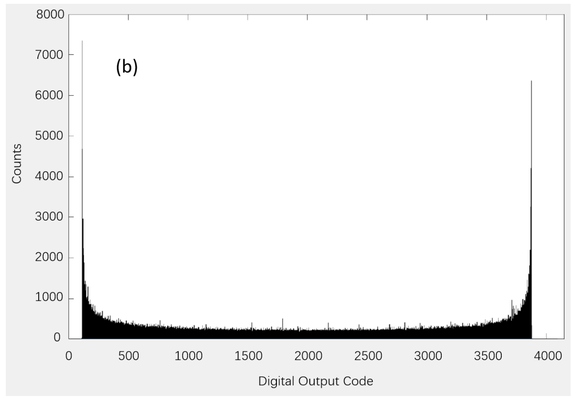




Chip test for ADC

- Maximum sampling rate ~160MHz
- Input a sine wave with a frequency of 80 MHz and an amplitude of -1dBFS, the effective number of bits (ENOB) is 9.34, the spurious-free dynamic range (SFDR) is 73.8 dBc

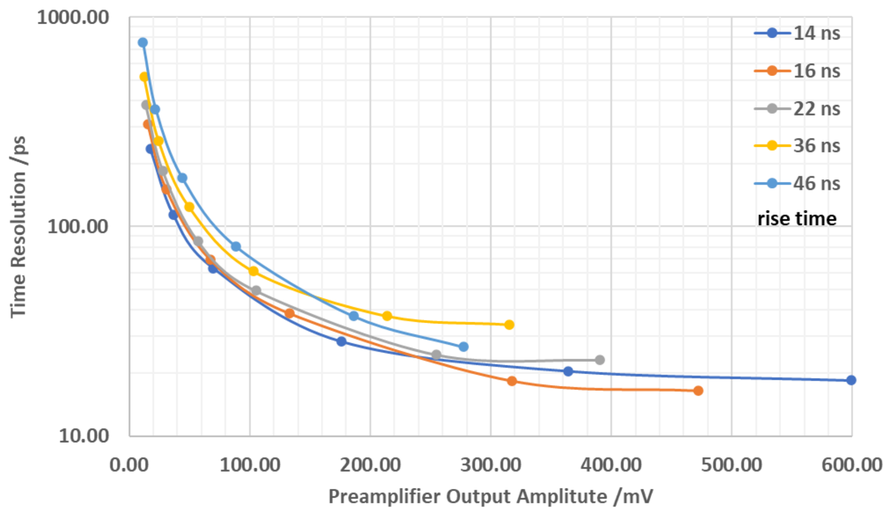




SYSTEM PERFORMANCE TESTING (PROOF OF CONCEPT)

Electrical test

- Preliminary system-level time response assessments were performed using an established 14-bit 1 GHz acquisition card (called WRX0608A1, Vpp=1.6 V)
- Preamplifier configuration was changed for different output rise time test
- A square wave signal was generated by an arbitrary function generator (Tektronix AFG3102C)
- Data processing includes sparse sampling, with an equivalent sampling rate of 200 MHz
- Waveforms with 3~4 sampling points (rise time at 15~20 ns for 200 MHz sampling rate) on the rising edge has better time resolution ~20 ps (@output ≥250mV)



SUMMARY

- A fast front-end readout design was designed and developed. The prototype preamplifier and ADC chip performance were evaluated.
- Preliminary system time response assessments were performed. Verification had shown that good time resolution performance can still be achieved at low sampling rates (200MHz).