PAUL SCHERRER INSTITUT

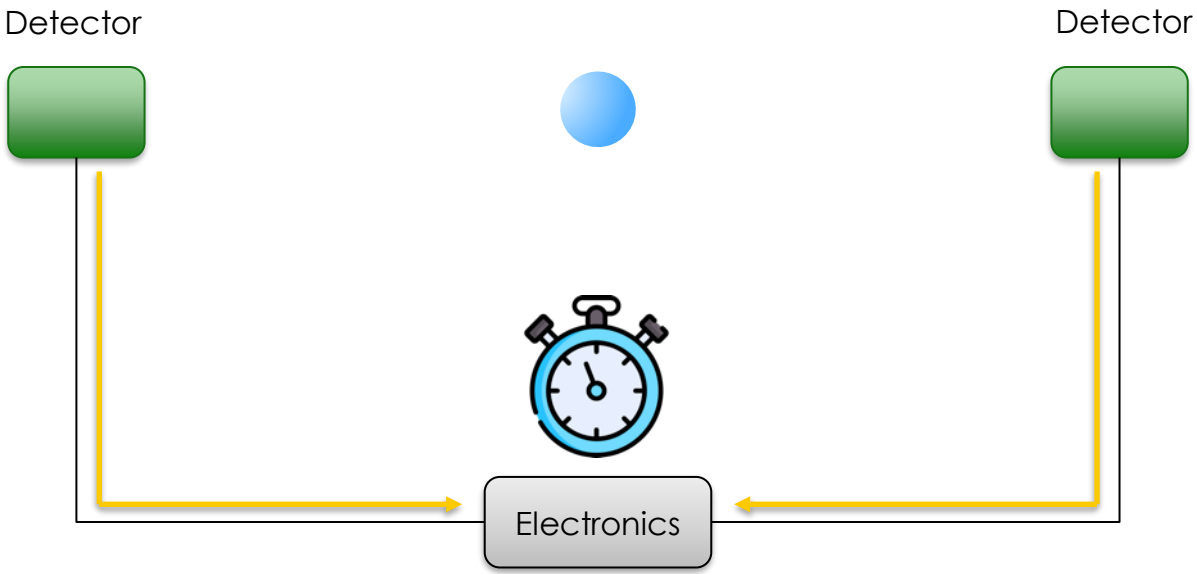
PSI

Stefan Ritt :: Head of Muon Physics Group :: Paul Scherrer Institute

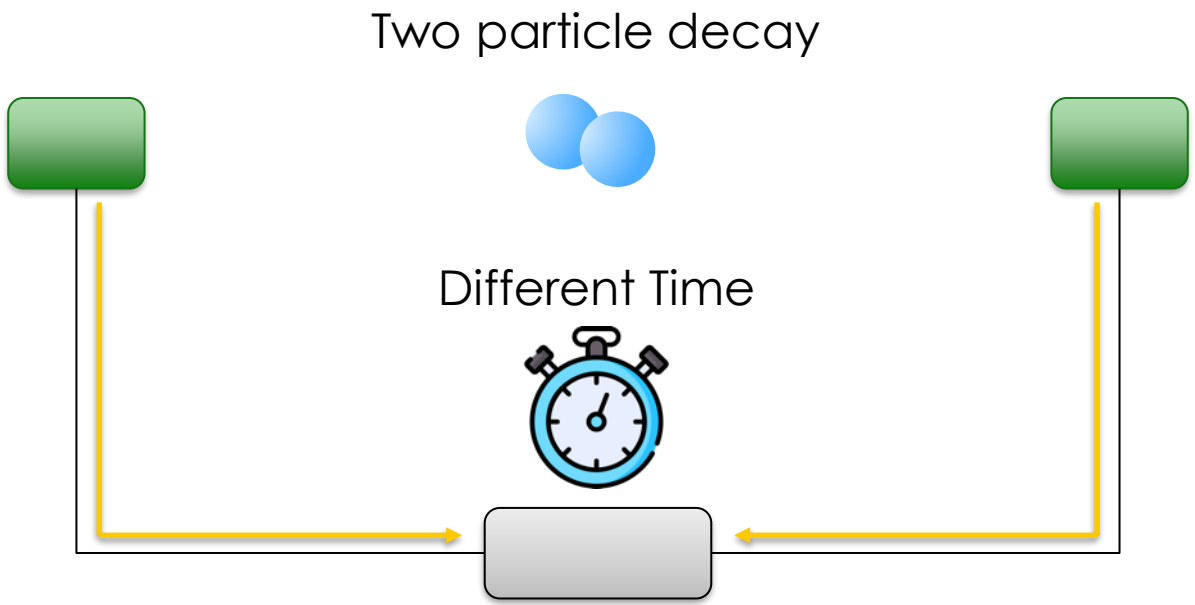
Mastering Picosecond Precision: Lessons learned from Large-Scale Timing Systems

IEEE NPSS Real Time Conference, Qui Nhon, Vietnam, April 26, 2024

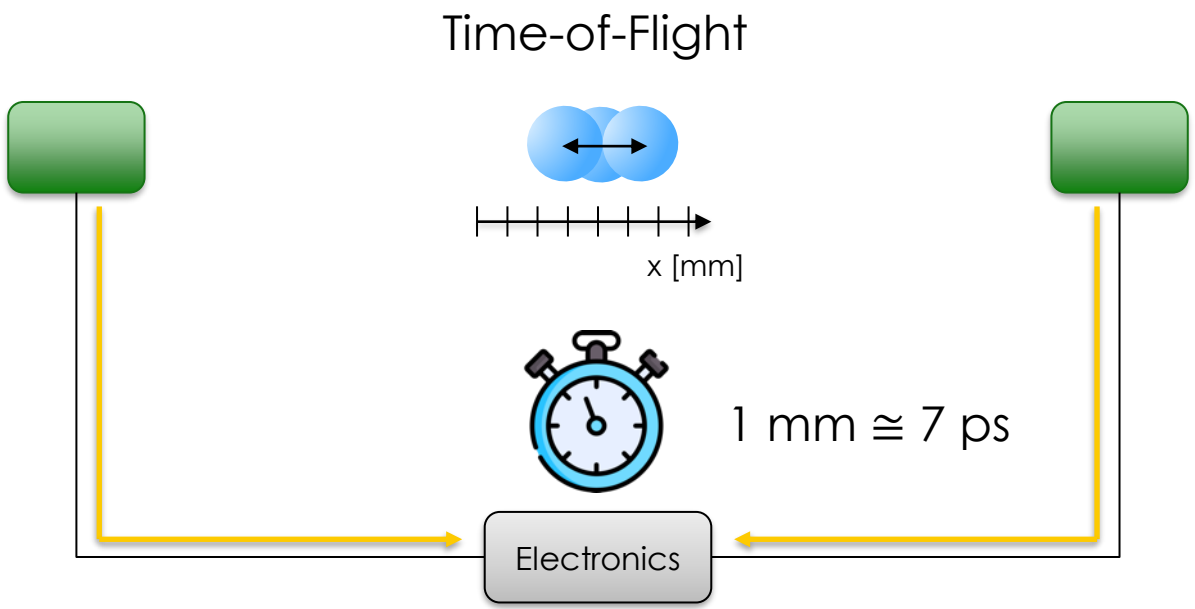
Measuring precision timing



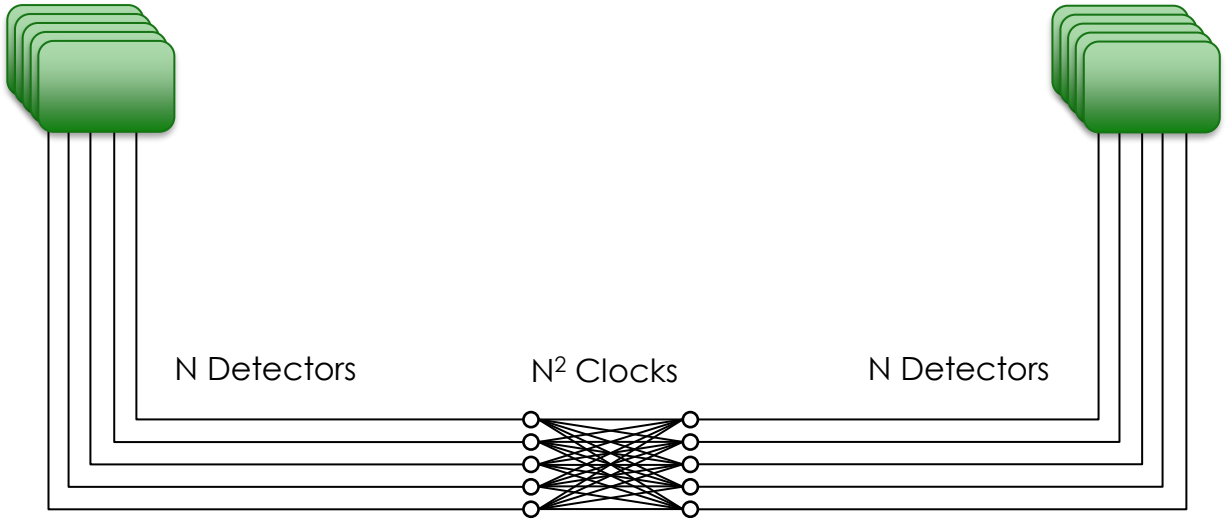
Measuring precision timing



Measuring precision timing

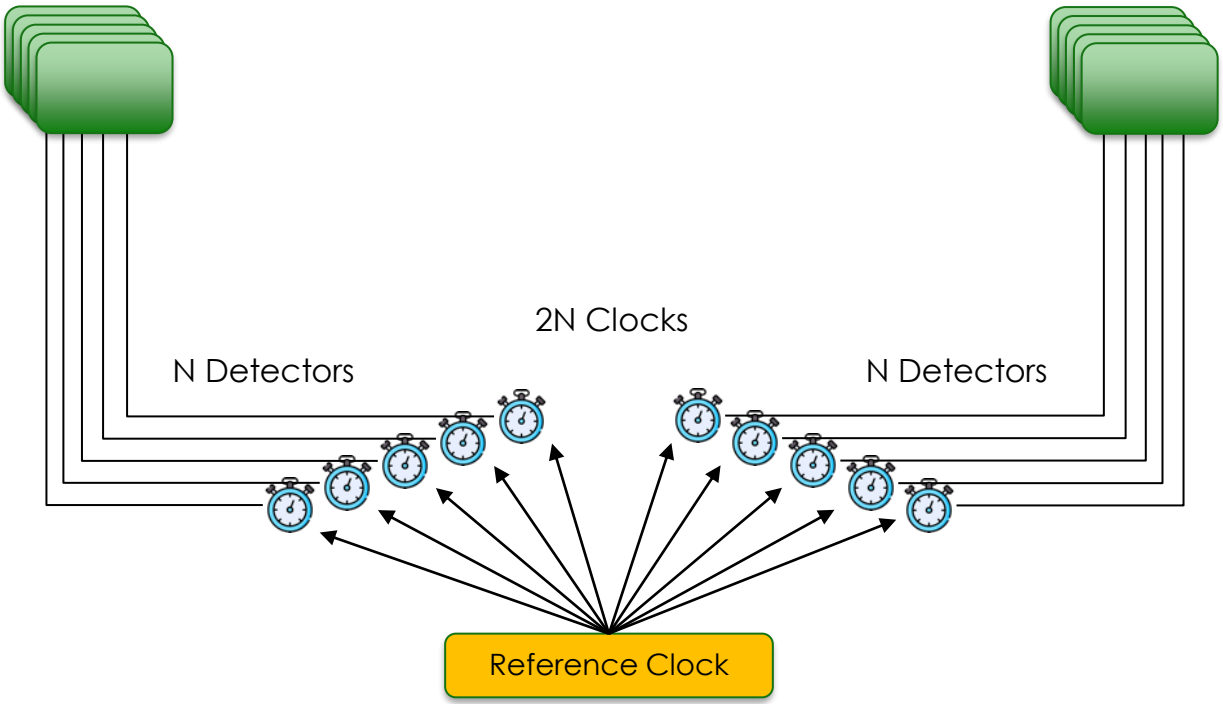


Large systems

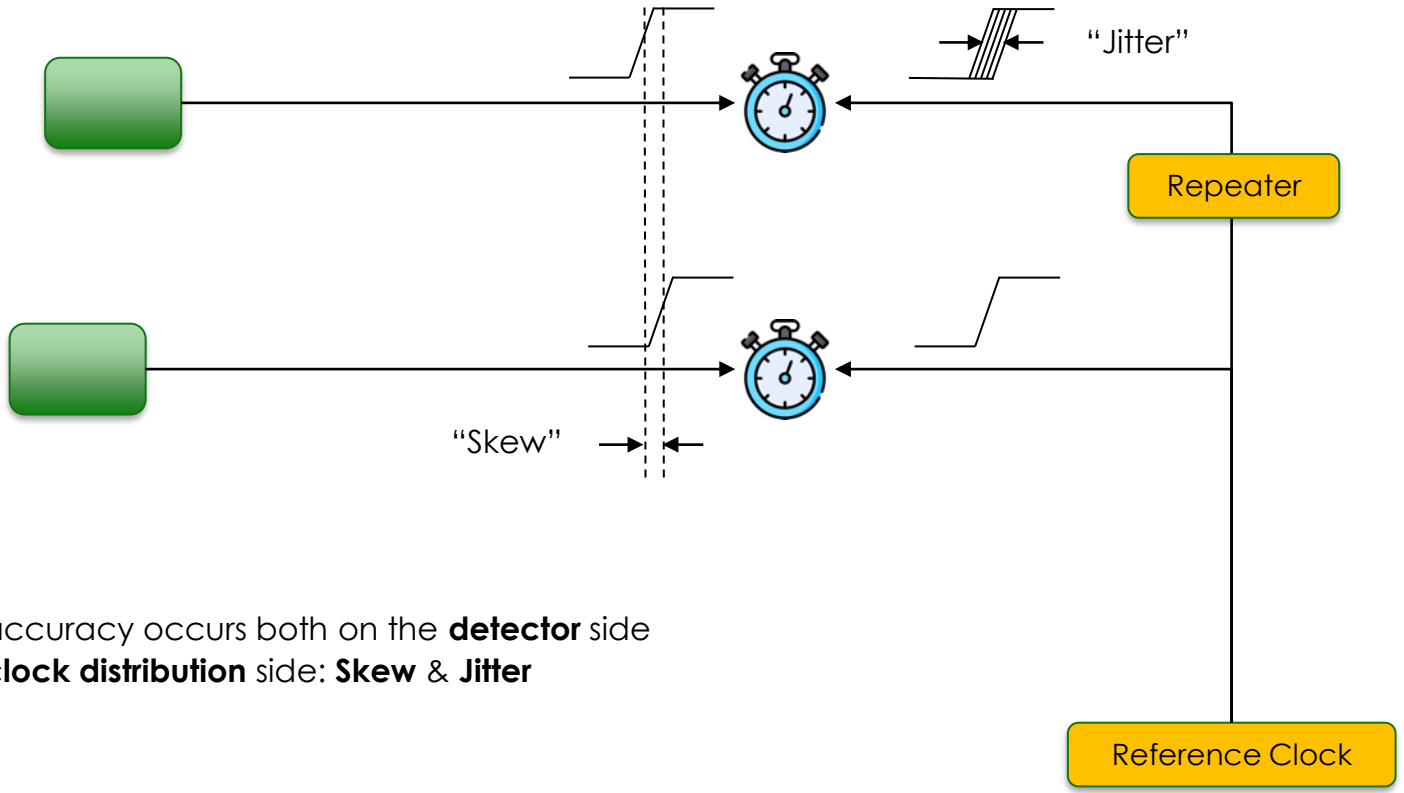


N=1000 → 1,000,000 Clocks

Large systems with reference clock

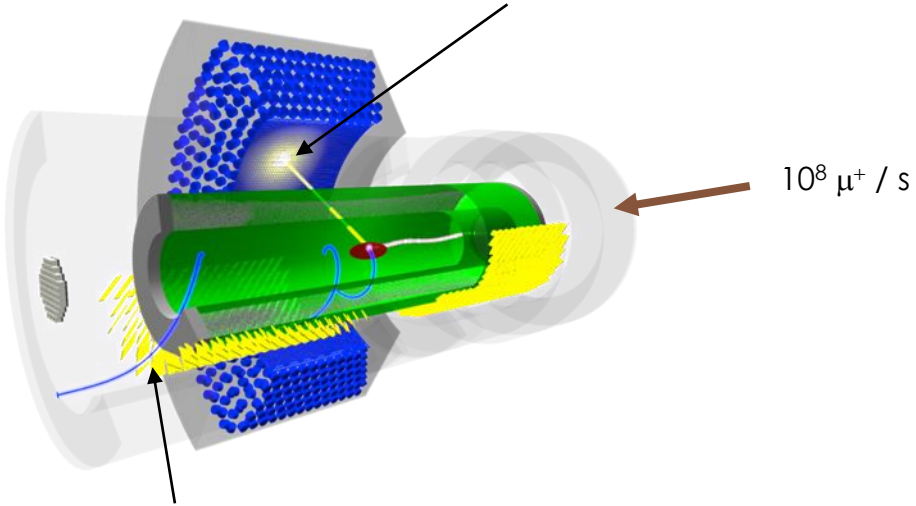


Time inaccuracy



Timing inaccuracy occurs both on the **detector** side and the **clock distribution** side: **Skew** & **Jitter**

MEG II Experiment at PSI



Normal μ decay
(Standard Model):

$$\mu^+ \rightarrow e^+ \nu_e \nu_\mu$$

Lepton-Flavor Violating Decay
(New Physics):

$$\mu^+ \rightarrow e^+ \gamma$$

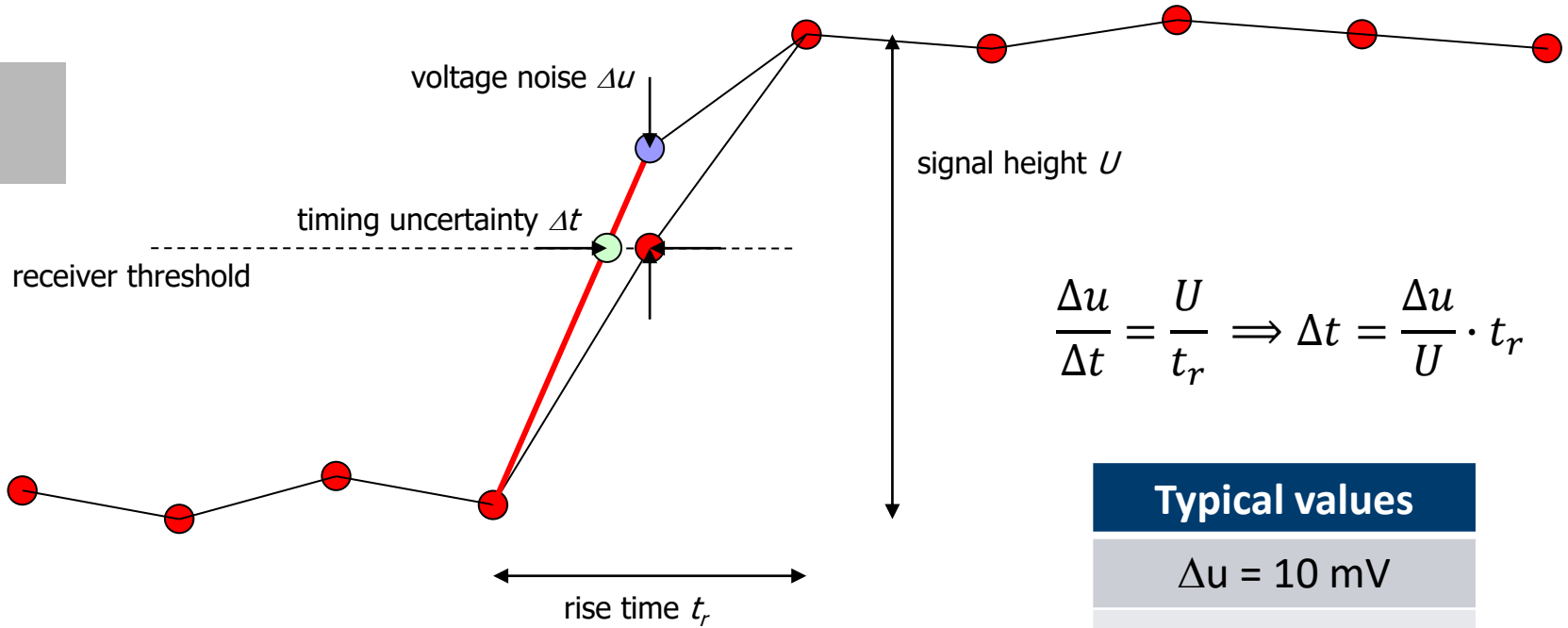
MEG II Experiment requires

~10 ps at electronics level

How to achieve timing at the Pico second level?

- Sources of timing jitter: **Single ended** lines, **PLL jitter**
- Clock **stability**
- **Noise reduction** strategies
- Timing **calibration**
- **Lessons learned** from the MEG II system

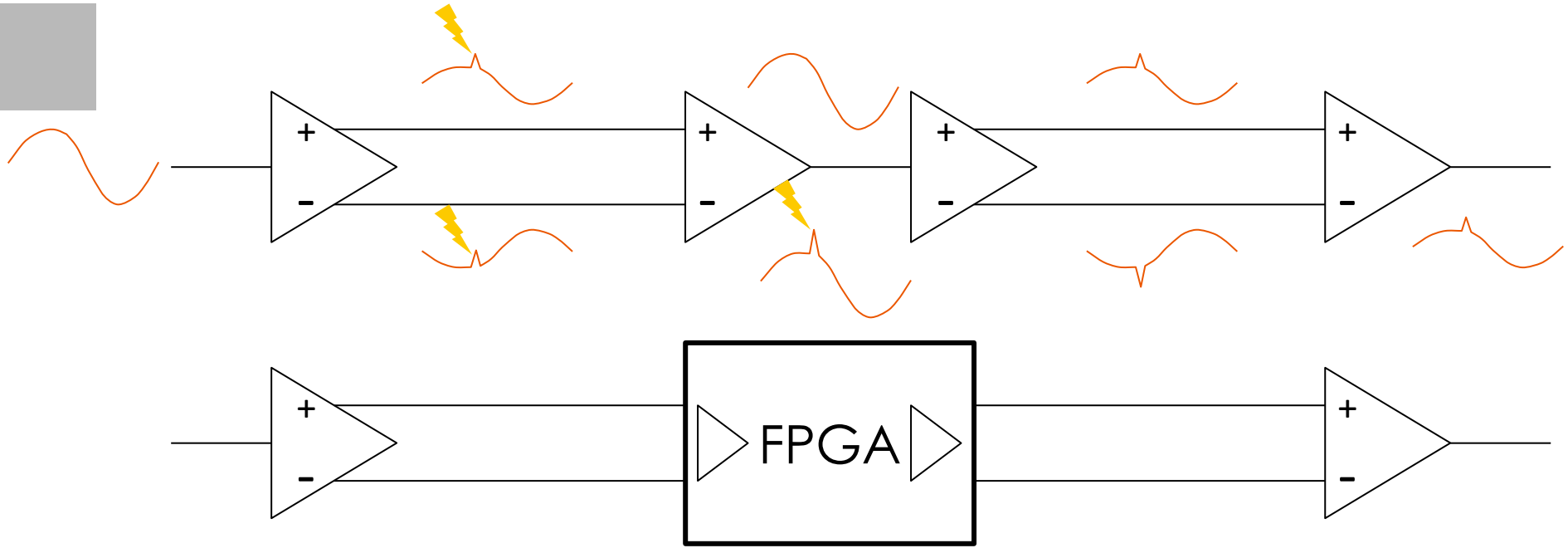
Jitter caused by voltage noise



$$\frac{\Delta u}{\Delta t} = \frac{U}{t_r} \Rightarrow \Delta t = \frac{\Delta u}{U} \cdot t_r$$

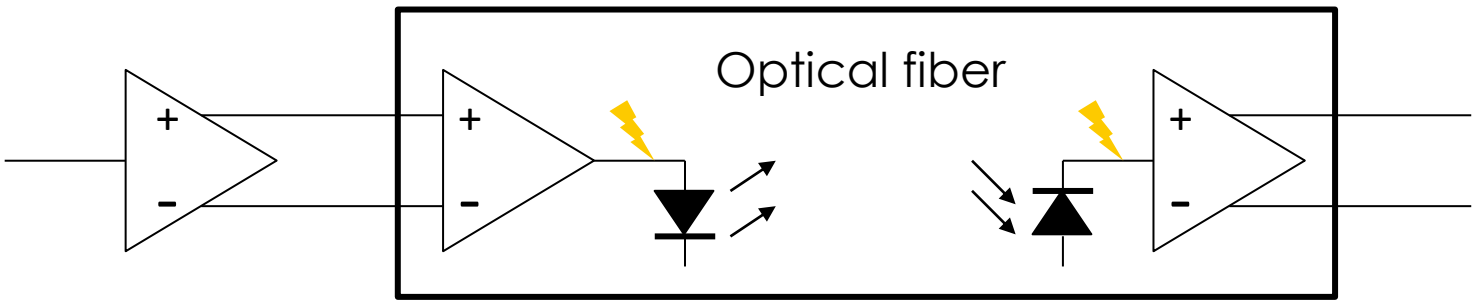
Typical values
Δu = 10 mV
U = 3.3 V
t_r = 1 ns
Δt = 3 ps

Differential Signals e.g. LVDS



Do not send low-jitter clocks through FPGAs!

Optical Signals



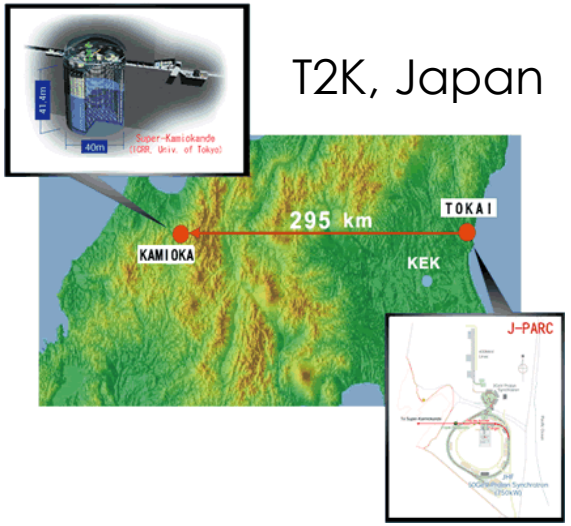
Careful with optical clock distribution!

Clock stability

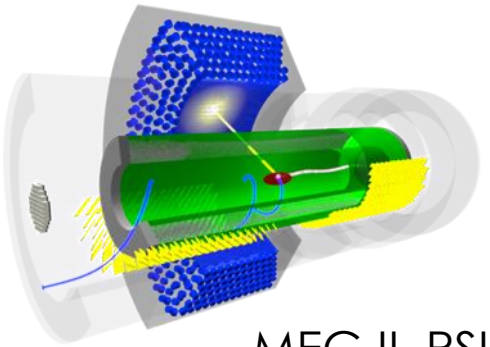
- **GPS** clock for measurements **far apart**
- **Atomic** clock for **long term** measurements
- Particle physics:
  Measurement periods **O(10 ns)**

  → Frequency stability of **10^{-4}** is enough
  10 ns * 10^{-4} = 1 ps

  → Excellent **low-jitter** clock distribution to all detector channels needed



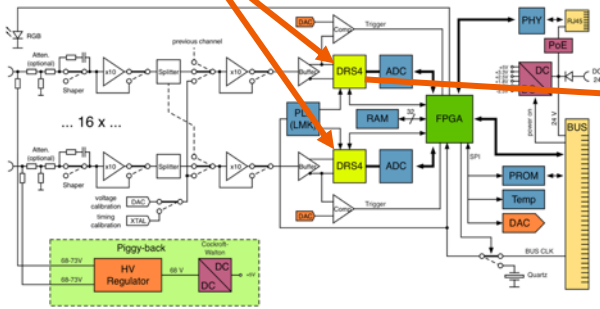
T2K, Japan



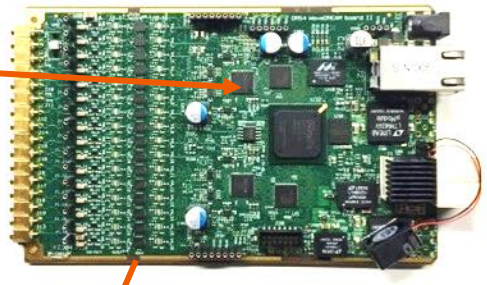
MEG II, PSI

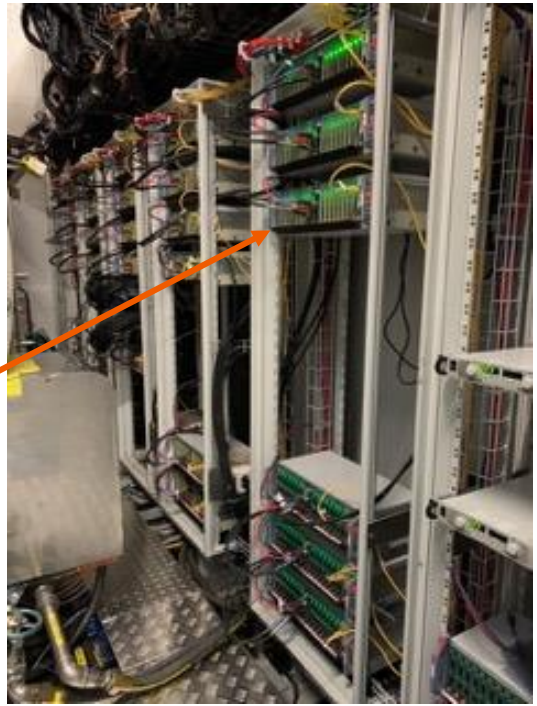
WaveDAQ system for MEG II @ PSI

DRS4 chip



WaveDREAM Board





WaveDAQ Crate

9000+ channels 5 GSPS / 12 bit

Low-jitter quartz

MEMS CLOCK OSCILLATOR

ASEMP

RoHS/RoHS II compliant

Moisture Sensitivity Level – MSL 1

Life Size 3.2 x 2.5 x 0.85 mm

FEATURES:

- Low Power Consumption for high speed communication
- Exceptional Stability Over Temp. at -40 to +85°C, ±15ppm
- Extended Automotive Grade Temp. stability at -55 to +125°C, ±25ppm
- MIL-STD-883 shock and vibration compliant
- Durable QFN Plastic Compact Packaging
- Standby or Disable Tri-state function
- Low jitter (Period jitter RMS and Phase jitter RMS)

APPLICATIONS:

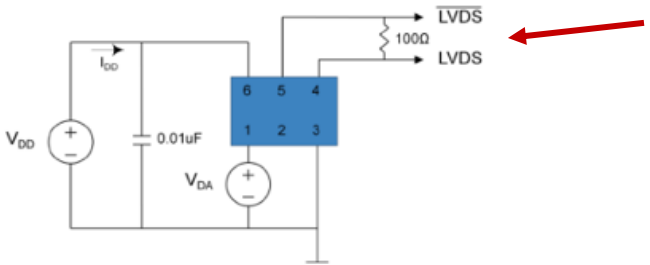
- Storage Area Networks (SATA, SAS, Fiber Channel)
- Passive Optical Networks (EPON, 10G-EPON, GPON, 10G-PON)
- Ethernet (1G, 10GBASE-T/KR/LR/SR, FCoE
- PCI Express
- Display port

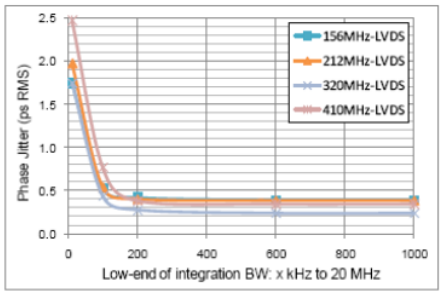
Common Key Electrical Specifications – CMOS, LVPECL, LVDS, and HCSL

Parameters		Minimum	Typical	Maximum	Units	Notes
Frequency Range	CMOS	2.3000*		170.0000	MHz	-20 ~ +70°C -40 ~ +85°C
	CMOS	3.3000*		170.0000		-40 ~ +105°C -55 ~ +125°C
	LVPECL	2.3000*		460.0000		Commercial, Industrial temp. range
	LVDS	2.3000*		460.0000		Commercial, Industrial temp. range
	HCSL	2.3000*		460.0000		Commercial, Industrial temp. range
Operating Temperature		-20		+70	°C	See options
Storage Temperature		-55		+150	°C	
Overall Frequency Stability		-50		+50	ppm	See options
Supply Voltage (Vdd)		+2.25		+3.6	V	
Startup Time				5	ms	
Enable Time				20	ns	STD (Tri-state)
				5	ms	PD option (Power Down)
Disable Time				5	ns	
Disable Current			20	22	mA	STD (Tri-state)
				0.095		PD option (Power Down)
Tri-state Function (Standby/Disable)		"1" (VIH≥0.75*Vdd) or Open: Oscillation "0" (VIL<0.25*Vdd) : Hi Z			V	40kΩ pull-up resister embedded
Aging		-5.0		+5.0	ppm	First year

Key Electrical Specifications – LVDS

Parameters		Minimum	Typical	Maximum	Units	Notes
Supply Current (I_{dd})			29	32	mA	RL=100Ω
Output Offset Voltage (V_{OS})		1.125		1.4	V	RL=100Ω differential
Delta Offset Voltage (ΔV_{OS})				50	mV	
Peak to Peak Output Swing (V_{PP})			350		mV	Single ended
Rise Time	Tr		200		ps	RL=50Ω , CL=2pF 20% to 80%
Fall Time	Tf		200			
Duty Cycle		48		52	%	Differential
Integrated Phase Jitter (J_{PH})			0.28	2	ps	200kHz ~ 20MHz @156.25MHz
			0.40	2		100kHz ~ 20MHz @156.25MHz
			1.70	2		12kHz ~ 20MHz @156.25MHz
Period Jitter RMS (J_{PER})			2.5		ps	





Phase jitter (integrated phase noise)

LVDS clock distribution

TEXAS INSTRUMENTS

CDCLVD110A

SCAS841D – FEBRUARY 2007 – REVISED DECEMBER 2016

CDCLVD110A Programmable Low-Voltage 1:10 LVDS Clock Driver

1 Features

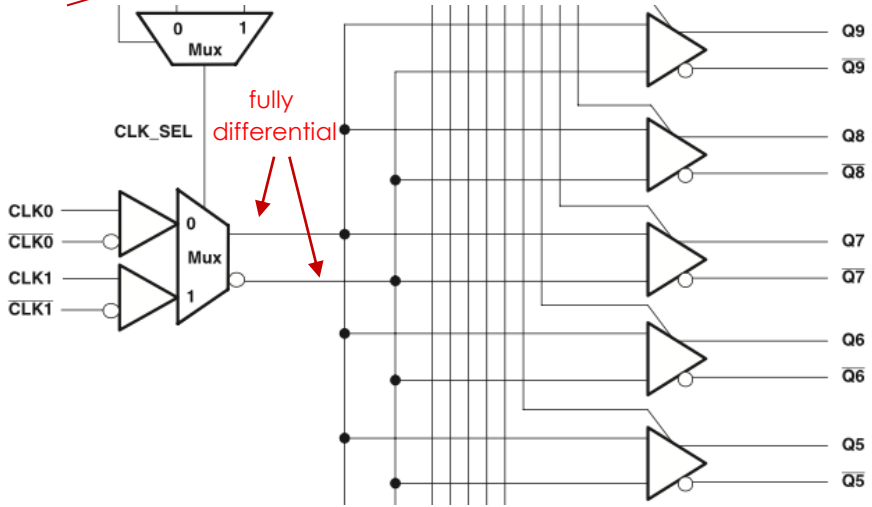
- Low-Output Skew <30 ps (Typical) for Clock-Distribution Applications
- Distributes One Differential Clock Input to 10 LVDS Differential Clock Outputs
- V_{CC} Range: 2.5 V ±5%
- Typical Signaling Rate Capability of Up to 1.1 GHz
- Configurable Register (SI/CK) Individually Enables Disables Outputs, Selectable CLK0, $\overline{CLK0}$ or CLK1, $\overline{CLK1}$ Inputs
- Full Rail-to-Rail Common-Mode Input Range
- Receiver Input Threshold: ±100 mV
- Available in 32-Pin LQFP and VQFN Package
- Fail-Safe I/O-Pins for V_{DD} = 0 V (Power Down)

3 Description

The CDCLVD110A clock driver distributes one pair of differential LVDS clock inputs (either CLK0 or CLK1) to 10 pairs of differential clock outputs (Q0 to Q9) with minimum skew for clock distribution. The CDCLVD110A is specifically designed to drive 50-Ω transmission lines.

When the control enable is high (EN = 1), the 10 differential outputs are programmable in that each output can be individually enabled or disabled (3-stated) according to the first 10 bits loaded into the shift register. Once the shift register is loaded, the last bit selects either CLK0 or CLK1 as the clock input. However, when EN = 0, the outputs are not programmable and all outputs are enabled.

The CDCLVD110A has an improved start-up circuit that minimizes enabling time in AC- and DC-coupled systems

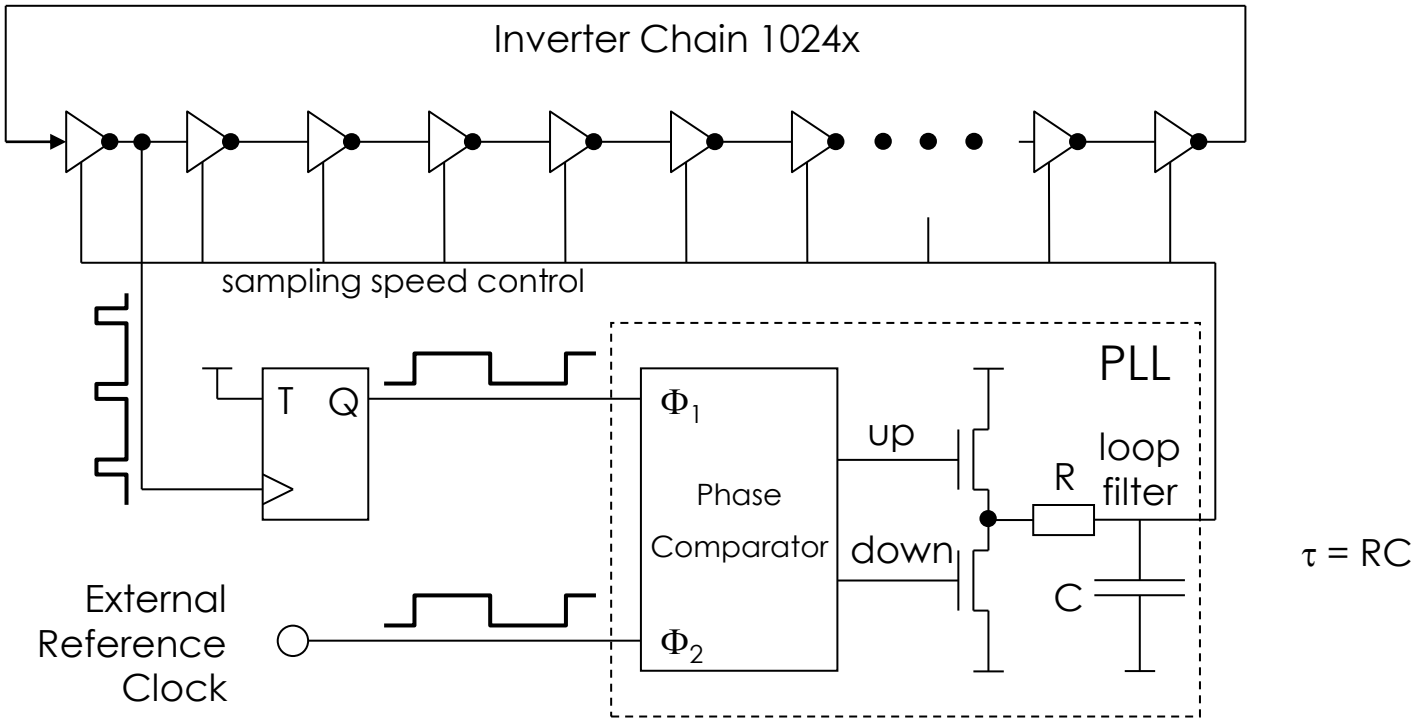


6.7 Jitter Characteristics

characterized with CDCLVD110 performance EVM, V_{DD} = 3.3 V, outputs not under test are ter
otherwise noted)

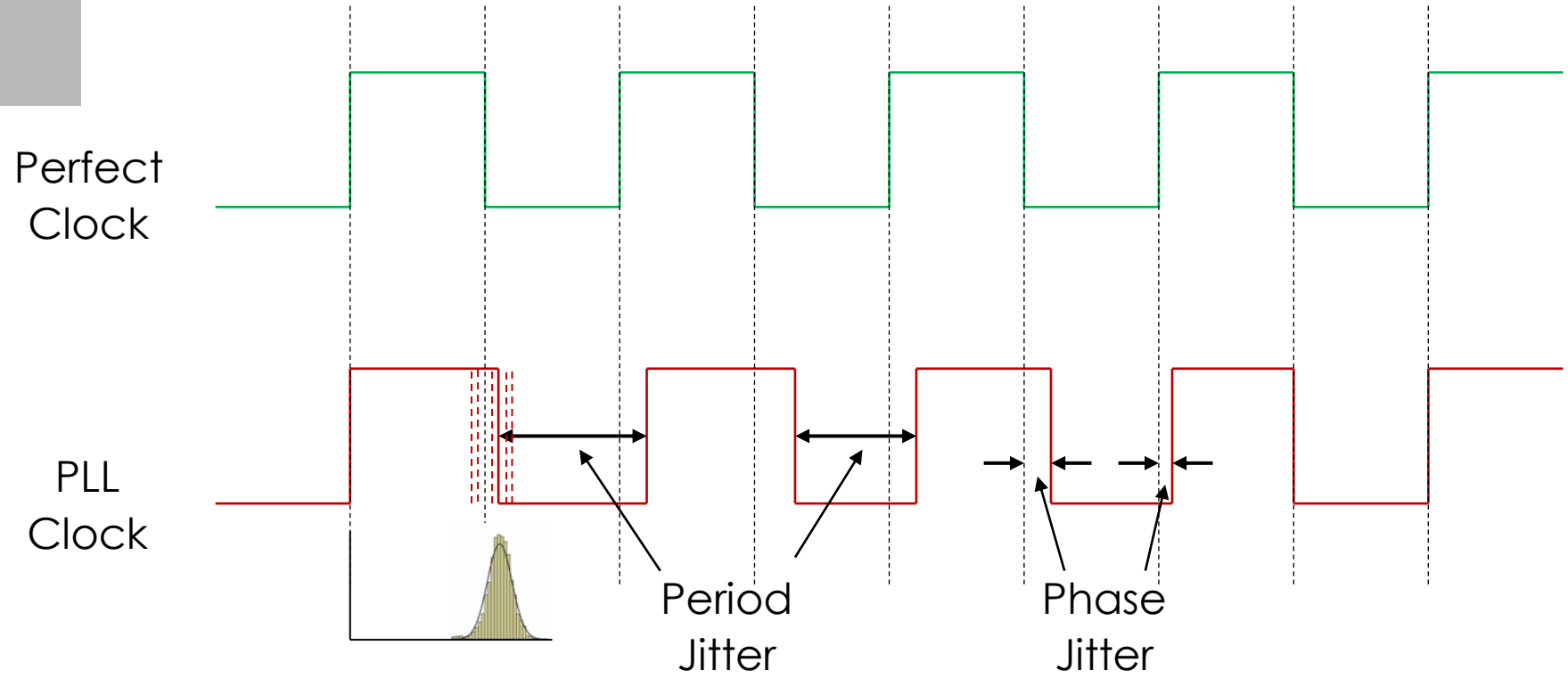
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{jitterLVDS}$	Additive phase jitter from input to LVDS output Q3 and $\overline{Q3}$	12 kHz to 5 MHz, f_{out} = 30.72 MHz		281		fs rms
		12 kHz to 20 MHz, f_{out} = 125 MHz		111		

DRS4 Phase Locked Loop

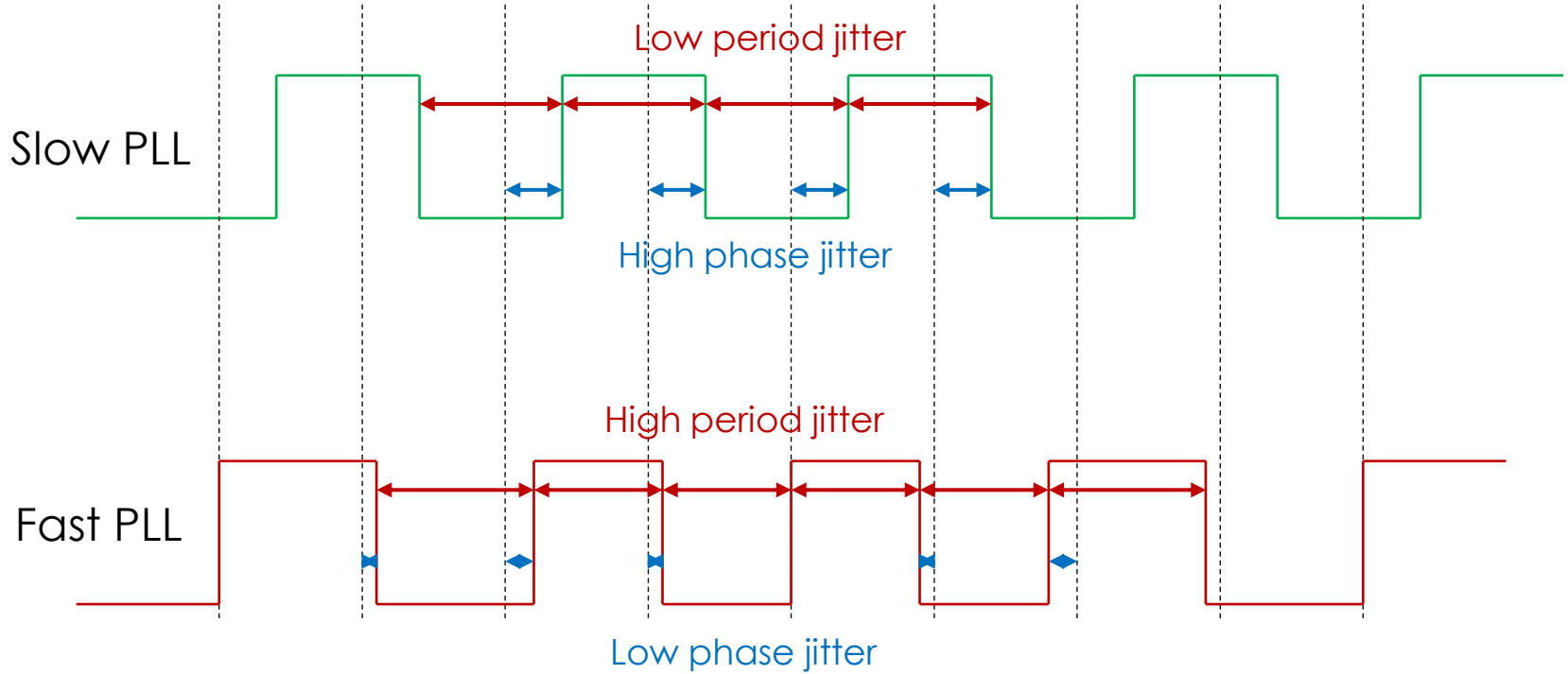


$\tau = RC$

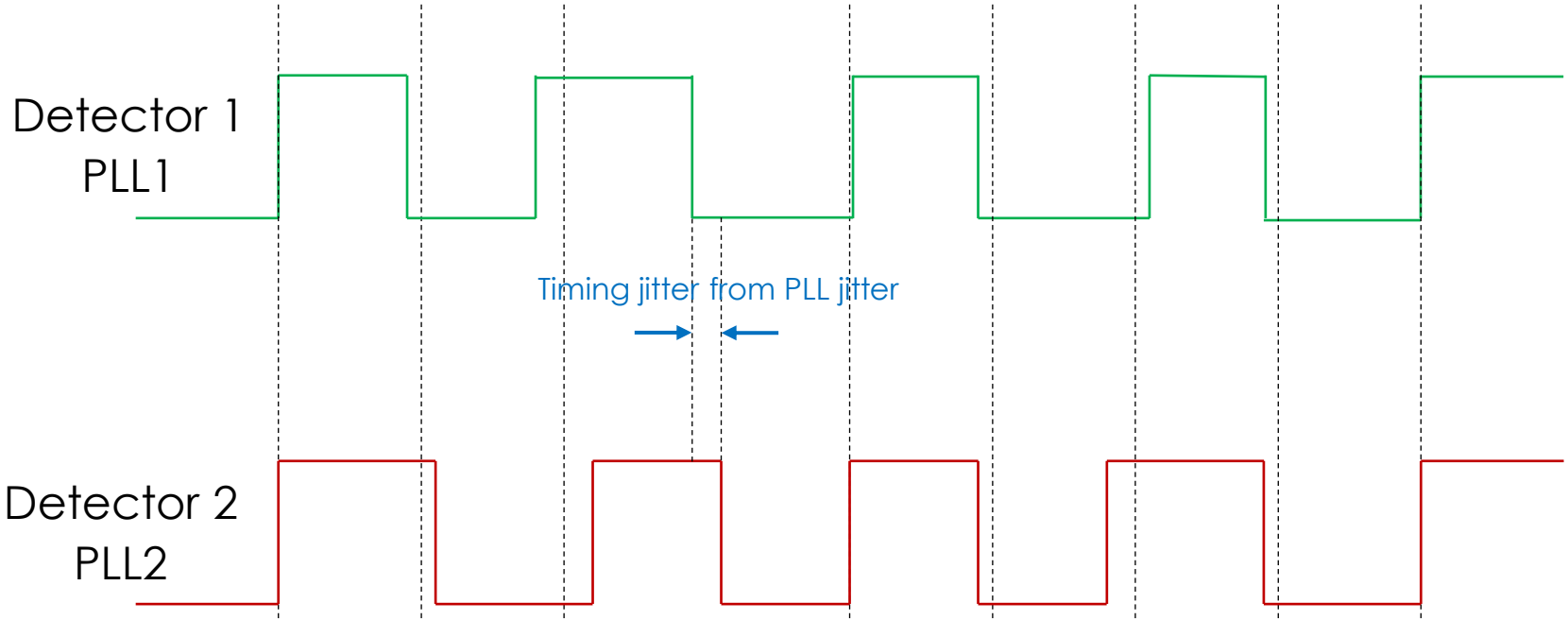
PLL Jitter



PLL Jitter

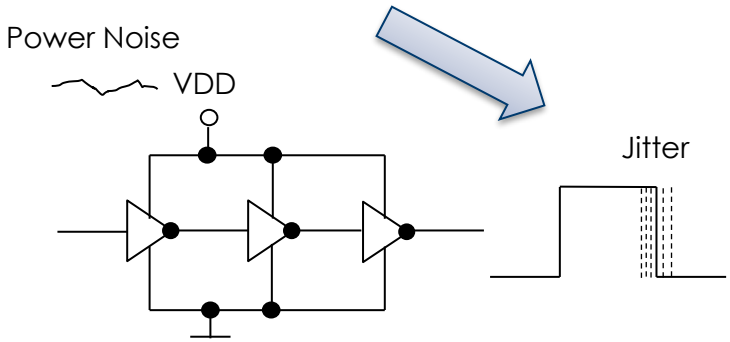

Low period jitter
Slow PLL
High phase jitter
High period jitter
Fast PLL
Low phase jitter

Jitter between two PLLs



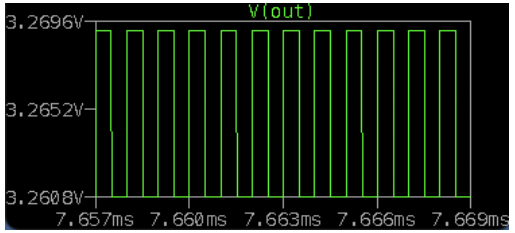
To achieve minimal timing jitter, PLL **phase jitter** must be **minimized**

PLL jitter from power supply noise

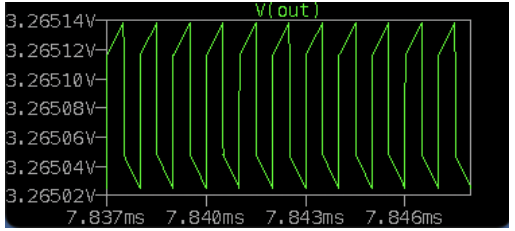


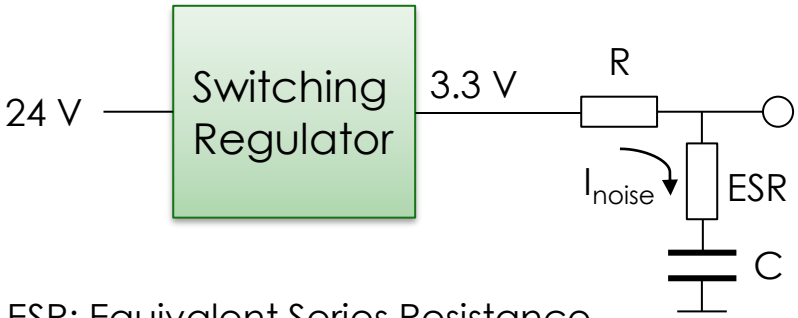
DRS4 chip: 1 mV noise → 10 ps jitter

ESR = 1 Ohm

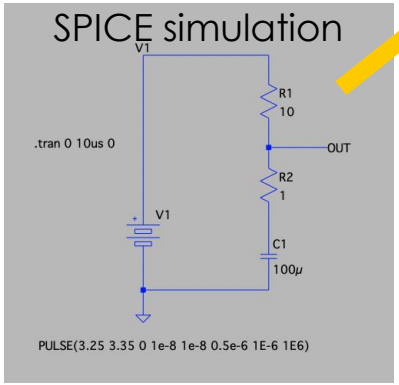


ESR = 0.01 Ohm





ESR: Equivalent Series Resistance



Use **low-ESR** capacitors for power supply filtering

Used filter components

CONDUCTIVE POLYMER ALUMINUM SOLID ELECTROLYTIC CAPACITORS nichicon

CK Chip Type, Ultra-low ESR series

For SMD · High Ripple Current · Low Impedance · For High Frequency · Anti-Solvent Feature

- Ultra-low ESR, Higher Capacitance, High ripple current.
- Load life of 2000 hours at 105°C.
- SMD type : Lead free reflow soldering condition at 260°C peak correspondence.
- Compliant to the RoHS directive (2002/95/EC).

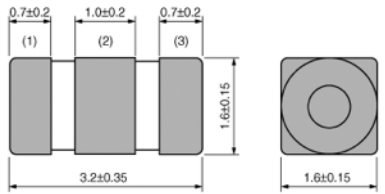
CJ → Low ESR → CK

■Standard Ratings

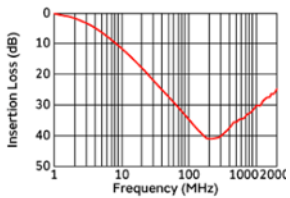
Rated Voltage (V)(code)	Surge Voltage (V)	Rated Capacitance (μF)	Case Size φD x L (mm)	tan δ	Leakage Current (μA)	ESR (mΩ) (at 100kHz 20°C)	Rated Ripple (mArms)	Part Number
2.5 (0E)	2.8	390	6.3 x 6	0.12	293	10	3900	PCK0E391MCO1GS
		560	8 x 7	0.12	420	9	4500	PCK0E561MCO1GS
		680	8 x 7	0.12	510	9	4500	PCK0E681MCO1GS
		1200	10 x 8	0.12	900	9	5000	PCK0E122MCO1GS
		2200	10 x 10	0.12	1650	8	6000	PCK0E222MCO1GS

560 μF / 9 mΩ

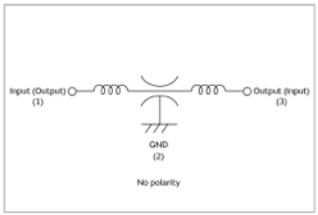
LC combines EMI Suppressor Filter
NFE31PT222Z1E9



R = 100 mΩ

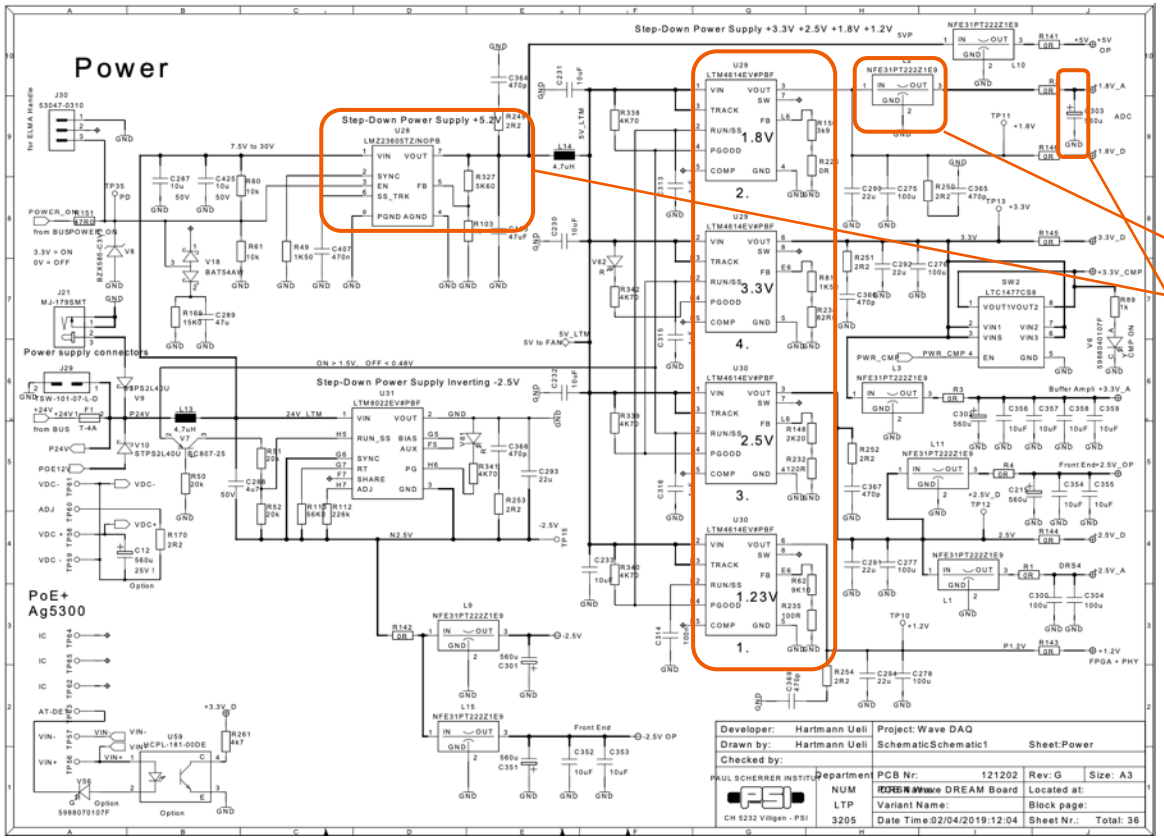


Insertion Loss Characteristics

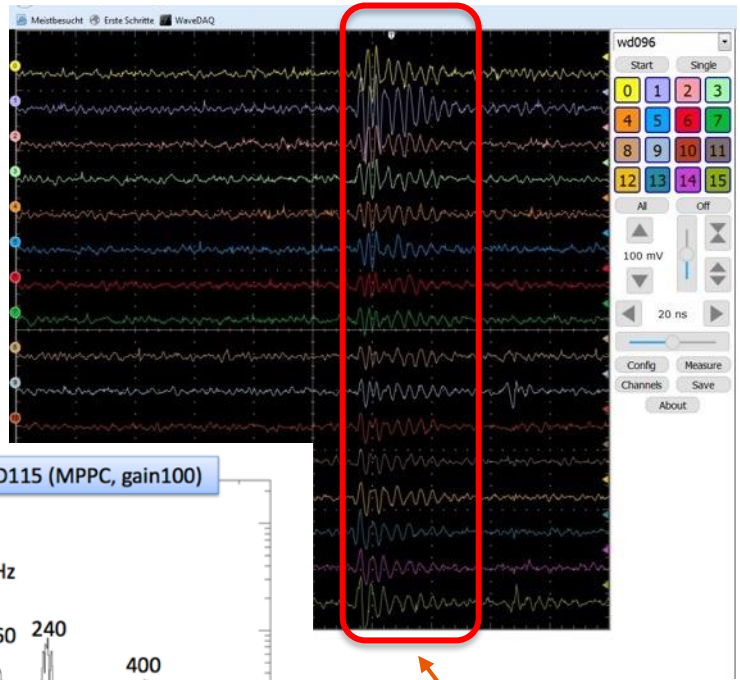


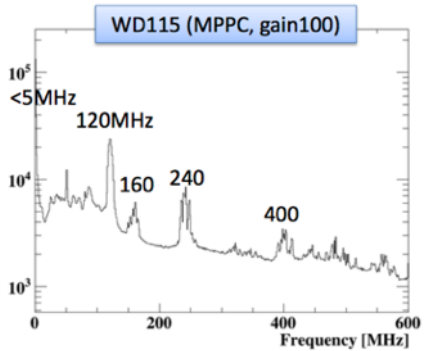
Equivalent Circuit

Power section WaveDREAM board



Electromagnetic Interference (EMI)

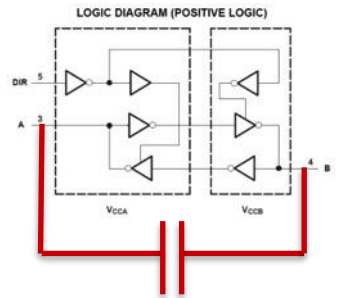


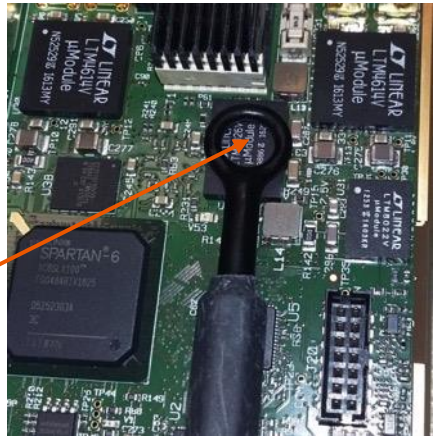


EMI pulse from switching converter

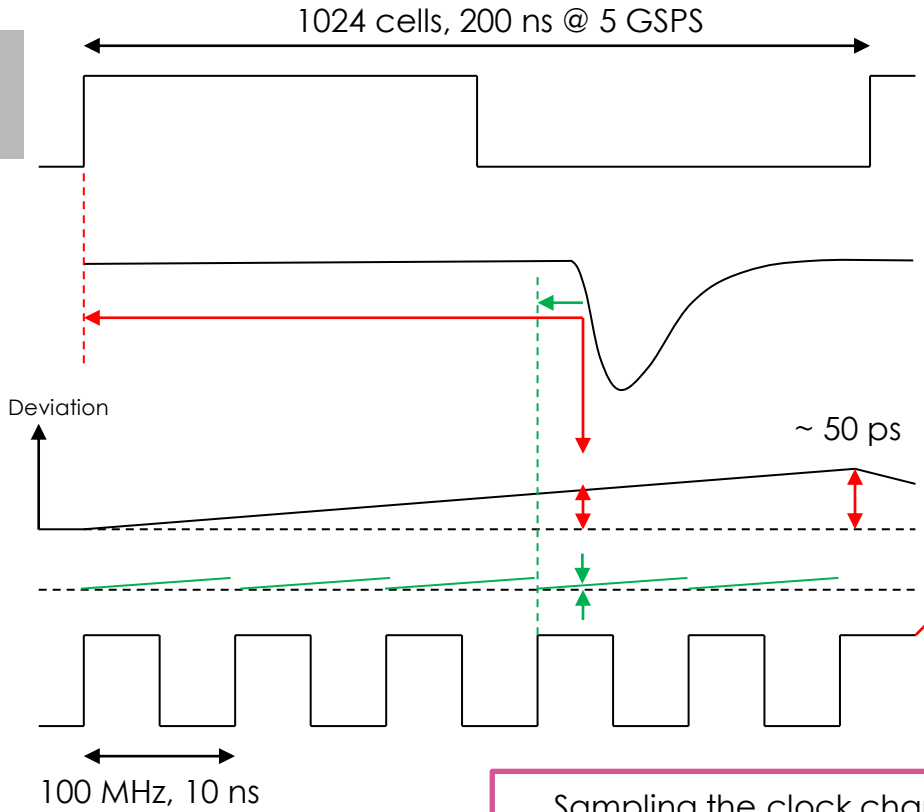
Shielding

Slew rate limiter

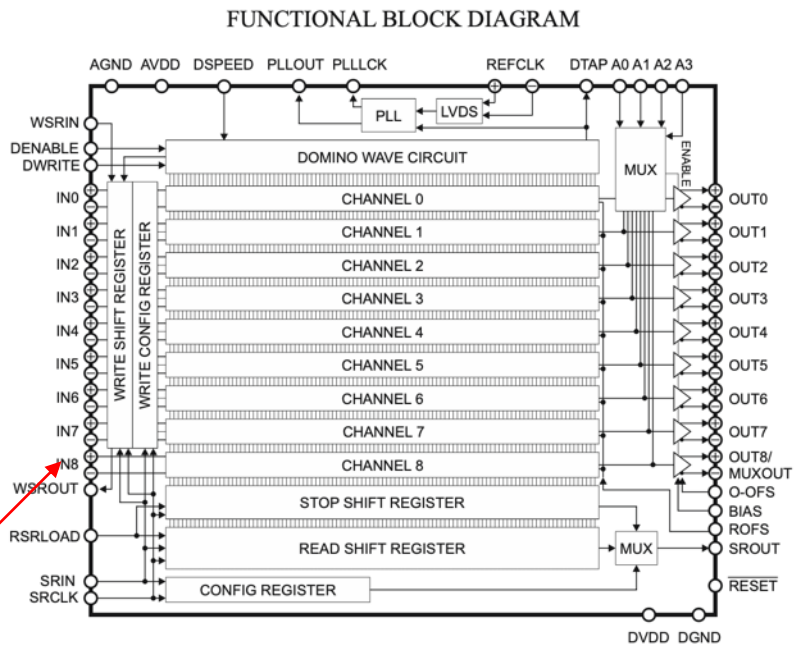




Use of DRS4 clock channel



DRS4



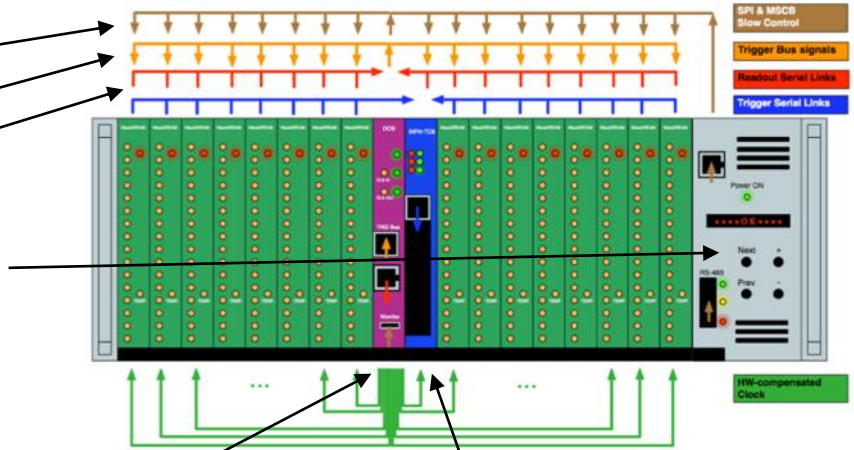
Sampling the clock channel reduces uncertainty from ~25 ps to <2 ps

PAUL SCHERRER INSTITUT

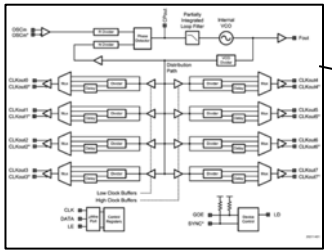
The WaveDAQ system

Custom Design “WaveDAQ”

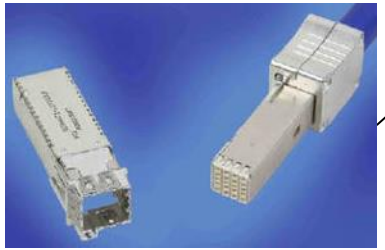
- Standard 19” crate + **custom backplane** (no VME, no xTCA)
- Idea: Not only a solution for MEG II, but **more general** “crate standard”
- Features:
  - Serial bus (**SPI**) for configuration
  - **Trigger / Busy signals** in **backplane**
  - “**Dual Star**“ Serial gigabit links
  - **Hot-swap** functionality
  - Low jitter (**<5 ps**) clock
  - **Shelf management** with Ethernet and power



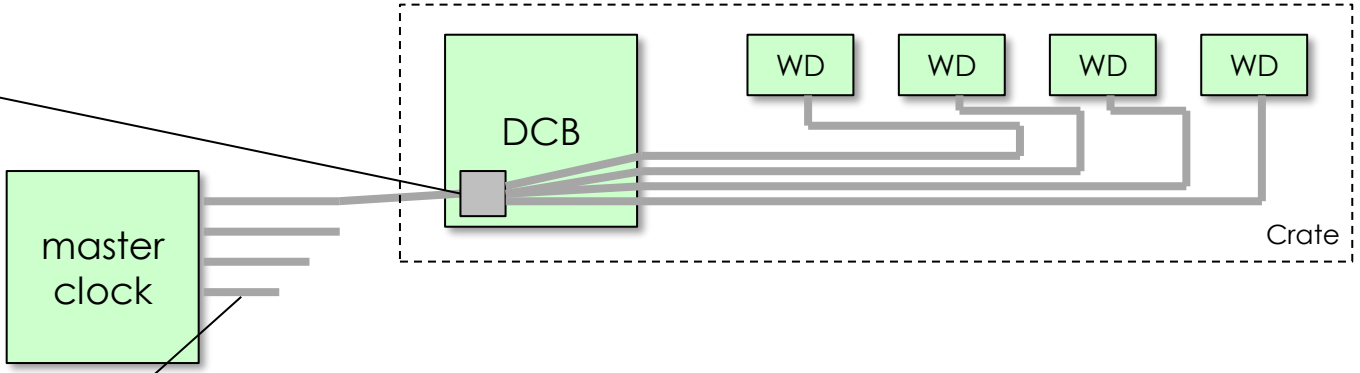
WaveDAQ Backplane



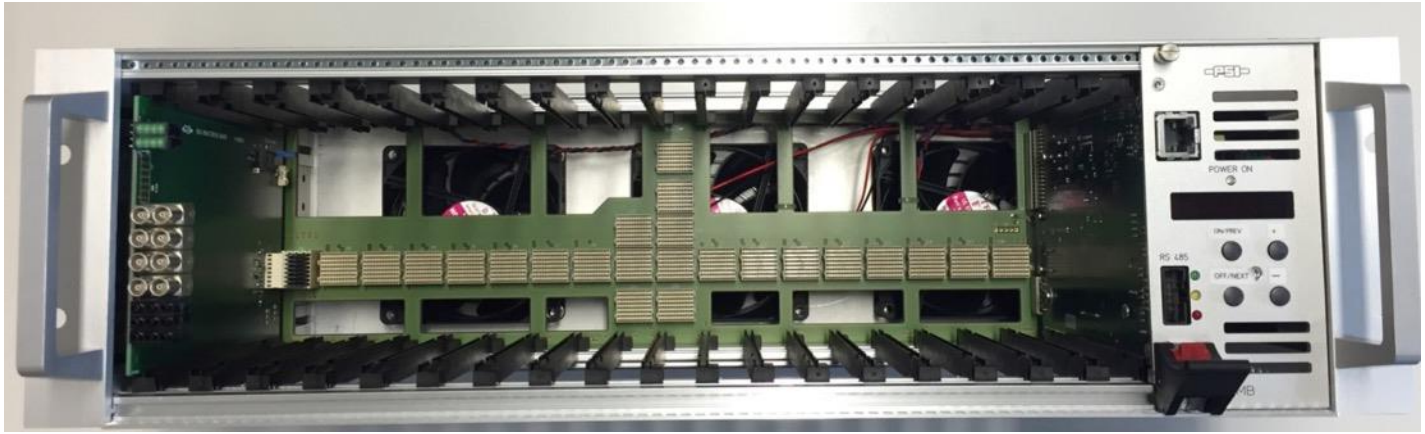
LMK03000 Jitter Cleaner



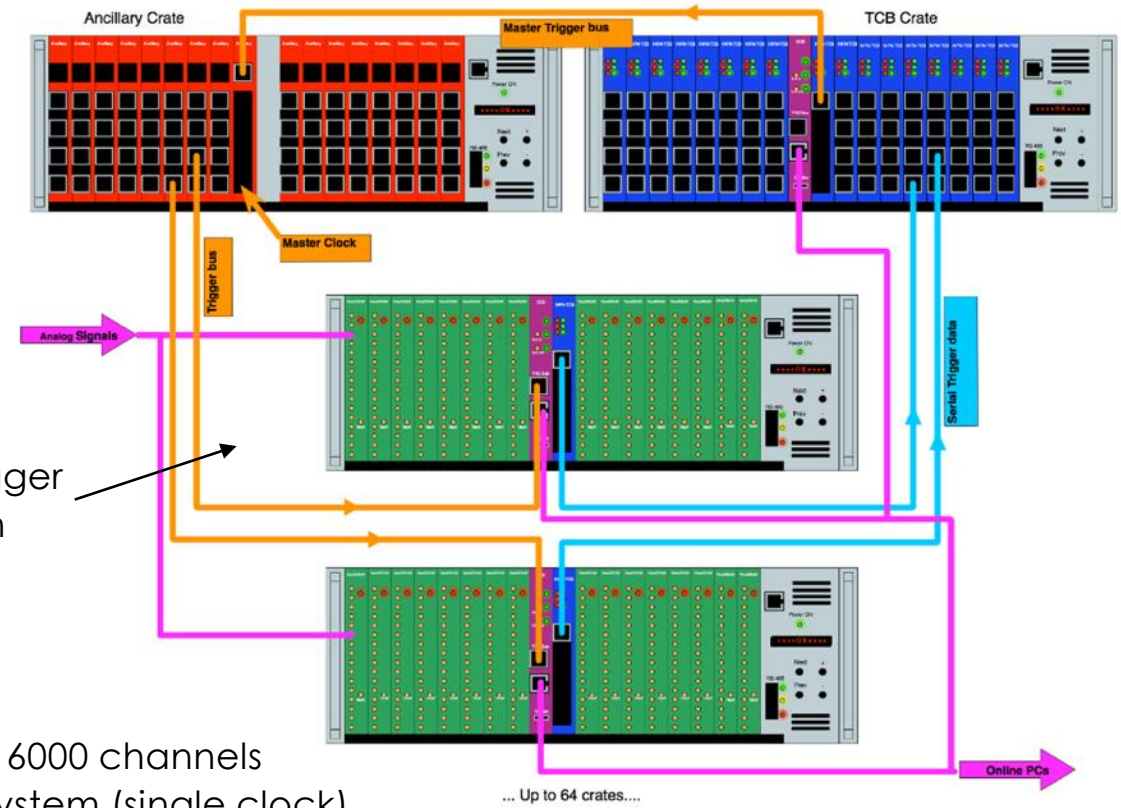
FCI Densishield Cable



Half Height Backplane

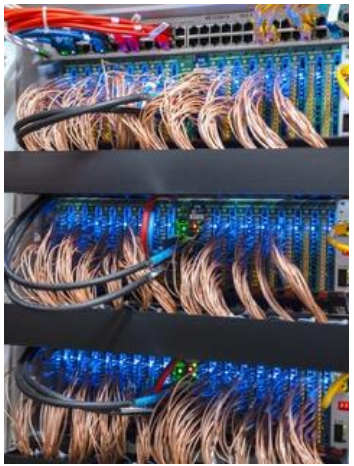


MEG II System

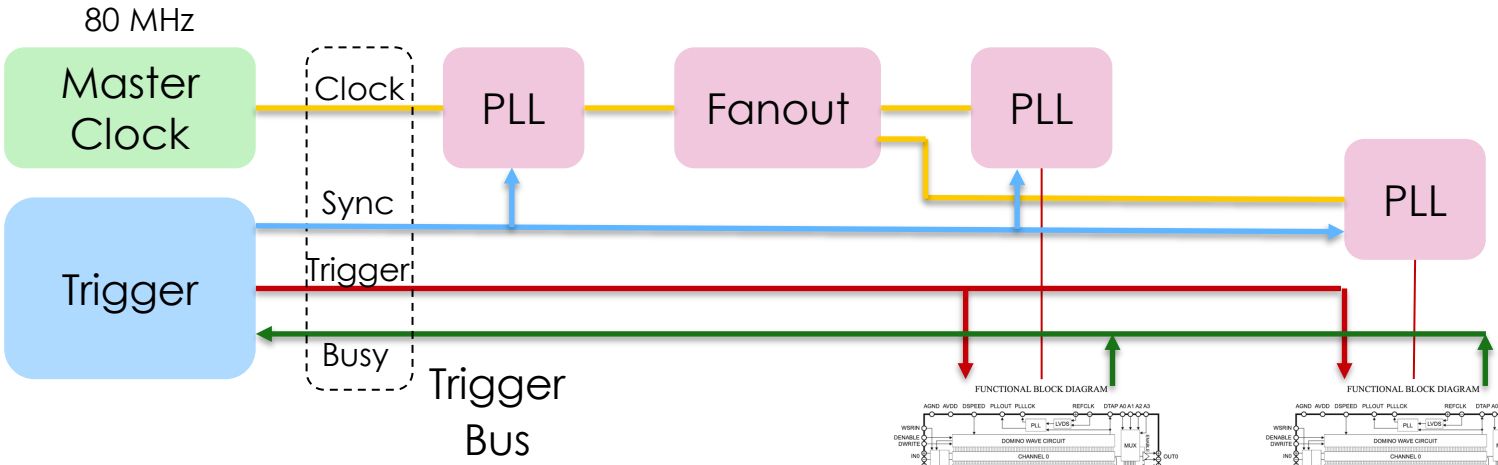


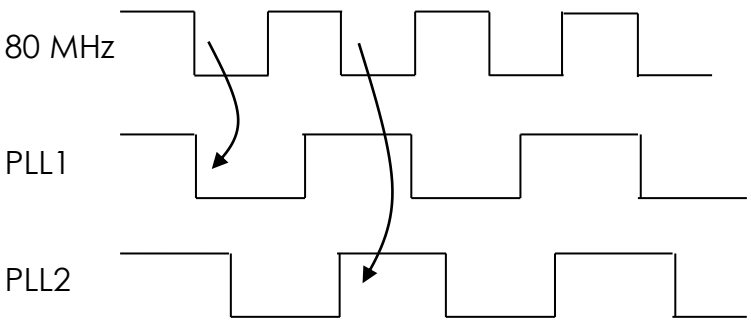
Clock and Trigger distribution

Scaling up to 16000 channels
Synchronous System (single clock)



Synchronization

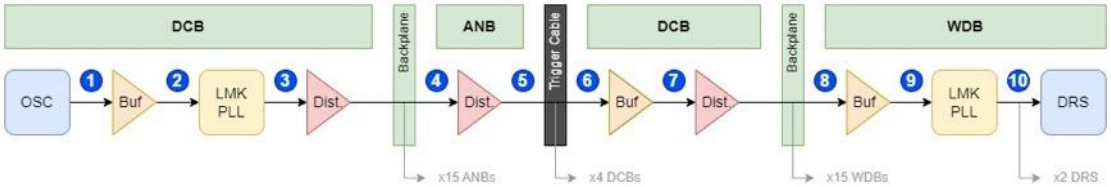


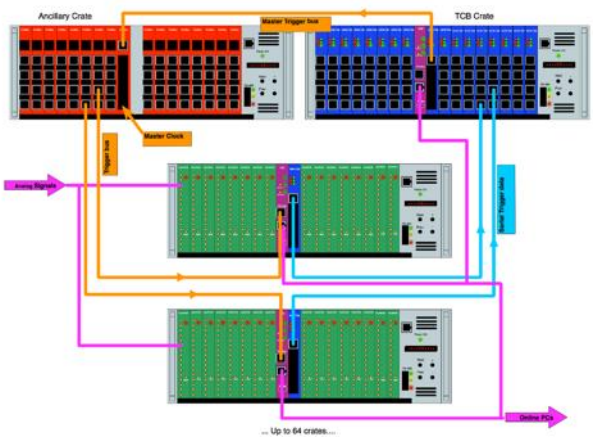


Lesson learned: Make all **PLL frequencies integer multiples** of each other

Jitter measurements

courtesy E. Schmidt, PSI

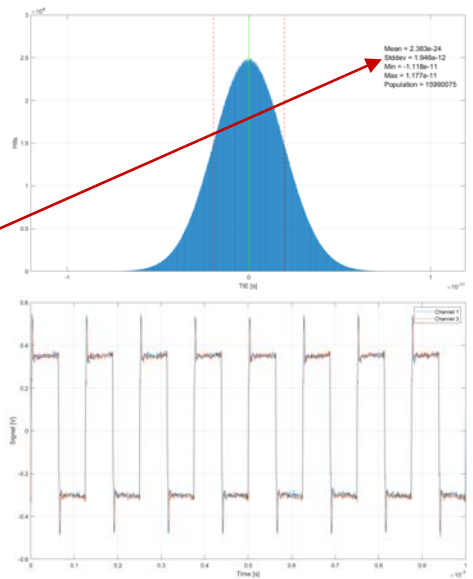




Filename + ToDo	Signal Probe Location	Signal	Ref Probe Location	Ref Signal	Jitter Std Dev	Jitter Min	Jitter Max
27_4_Crate190_AnbDistIn_vs_3_DcbDistIn Switch scope to refclk setup.	4	ANB Distributor Input (Soldered)	3	DCB Distributor Input (Soldered)	10.8 ps	-63.7 ps	53.2 ps
28_7_Crate196_DcbDistIn_vs_Crate192_DcbDistIn Solder 2 Probes to DCB02/DCB07 distributor input from Cable.	7 Crate196	DCB Distributor Input (Soldered)	7 Crate192	DCB Distributor Input (Soldered)	7.3 ps	-39.7 ps	45.5 ps
29_7_Crate196_DcbDistIn_vs_ScopeRef Switch to scope reference setup.	7	DCB Distributor Input (Soldered)	None	Scope Constant Clock	3.9 ps	-23.4 ps	31.0 ps
30_9_Crate196_Slot15WdbLmkIn_vs_ScopeRef Solder 2 Probes to 2 WDB280/WDB317 LMK inputs.	9	WDB LMK Input (Soldered)	None	Scope Constant Clock	2.0 ps	-10.9 ps	12.3 ps
31_9_Crate196_Slot15WdbLmkIn_vs_Slot1WdbLmkIn Switch scope to refclk setup.	9 Slot15	WDB LMK Input (Soldered)	9 Slot1	WDB LMK Input (Soldered)	1.9 ps	-11.1 ps	11.8 ps
32_9_Crate196_Slot15WdbLmkIn_vs_Crate192_Slot15WdbLmkIn	9 Crate196	WDB LMK Input (Soldered)	9 Crate192	WDB LMK Input (Soldered)	3.0 ps	-16.4 ps	16.8 ps

Tektronix MSO64B
8 GHz, 50 GSPS
soldered diff. probes!

σ_{jitter} = 1.9 ps

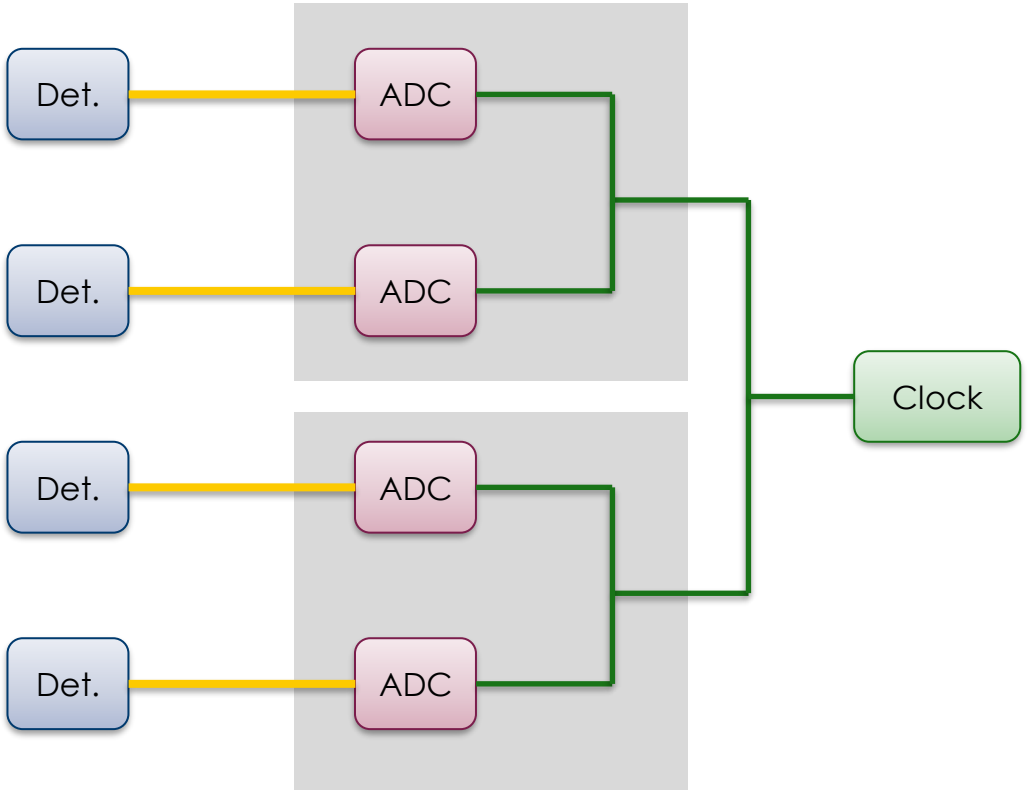


Slot - Slot

Crate - Crate

Global calibration

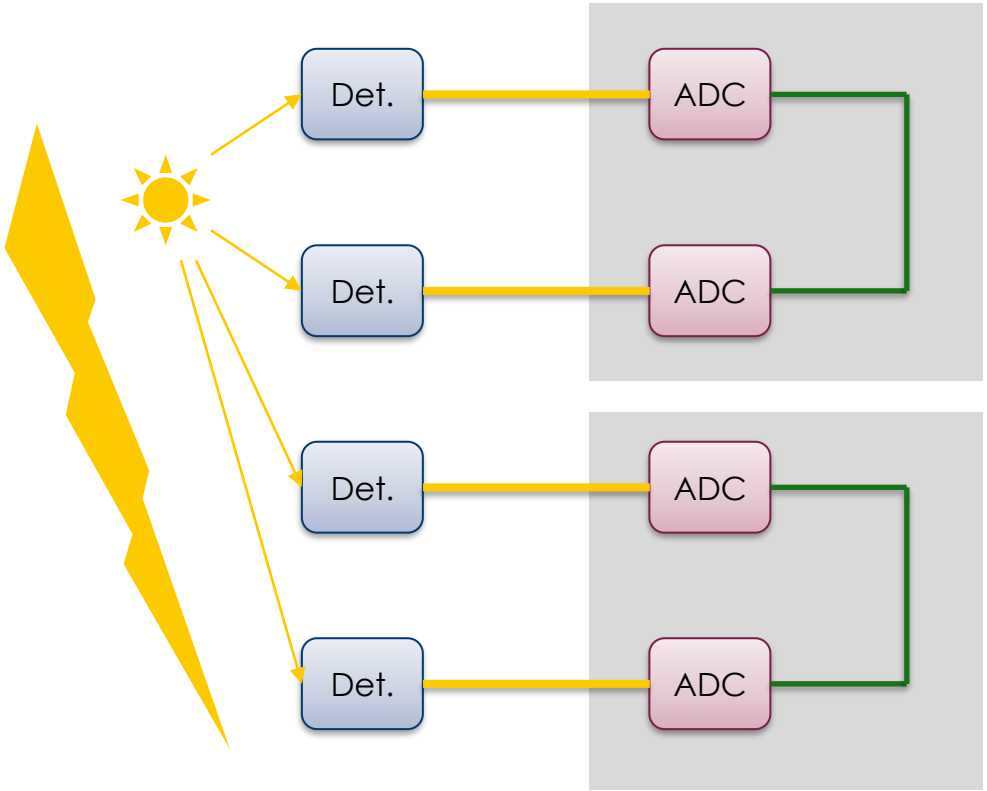
- Clock distribution is **never perfect** to the ps level
- Global sync injection at ADC does not calibrate **different cable lengths**
- Signal **injection** at detector can be **difficult**



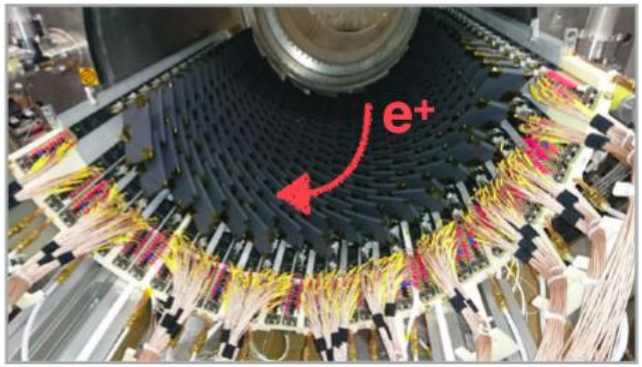
Global calibration

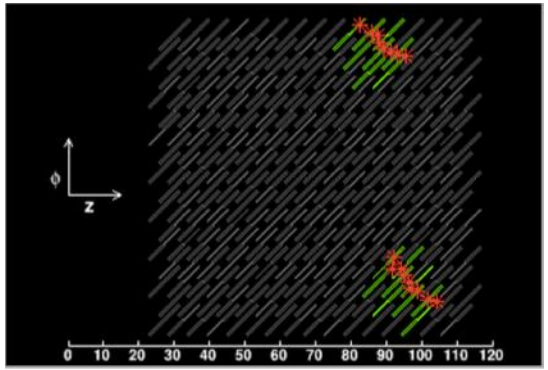
Solution: Use a **physics event** which is seen by all detectors:

- **LED** flash in calorimeter
- **Cosmic** traversing many channels
- **Correct** for different light path

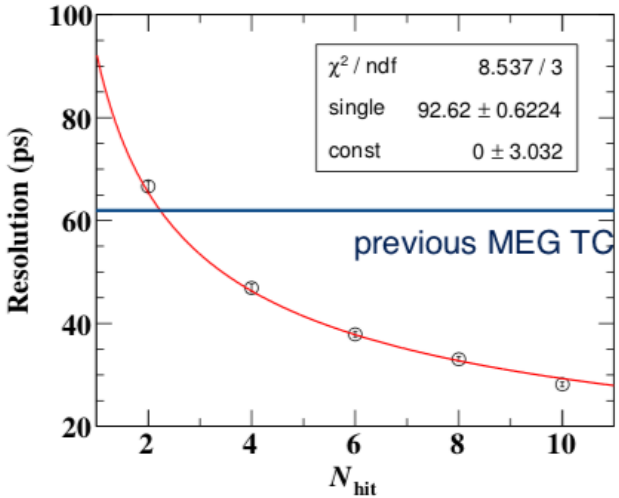


MEG II Timing Counter





- 8 x 10^8 μ/s
- 256 scintillating tiles 4x6 cm, **512 WDB chan**nels (2 crates)
- Resolution scales with sqrt(N)
- **35 ps** reached with 8 hits



Lessons learned (so far…)

DALL-E

- Designing a **crate standard** is **easier** than anticipated (if no committee is involved 😉)
- Distributing a **5 ps** jitter clock is not so hard
- Doing everything **from scratch** can **simplify** things
  - **shelf manager** with 8-bit uC with few 100 lines of code
  - crate costs **~ 2k$** including power supply
- Mixed signal board with **40 µV** of noise (gain=100 !) is **tough**
  - whole project took **6 years** from first idea with ~2 FTE
  - analog front-end took **1.5 years**, FW ~2 years
  - careful selecting and shielding **DC-DC** converter, needed **4 revisions**
  - the more noise you fix, the more new sources you find
  - Lots of **experience** obtained often missing in textbooks

Conclusions for precision timing in large systems

- Use end-to-end **differential** clock distribution
- Careful **filter** power for all PLLs with **low-ESR capacitors**
- Identify and remove **EMI sources**
- Large systems with **<5 ps** timing can be built
- This talk:
  IEEE NPSS **Educational Video** at **https://ieee-npss.org/videos/**