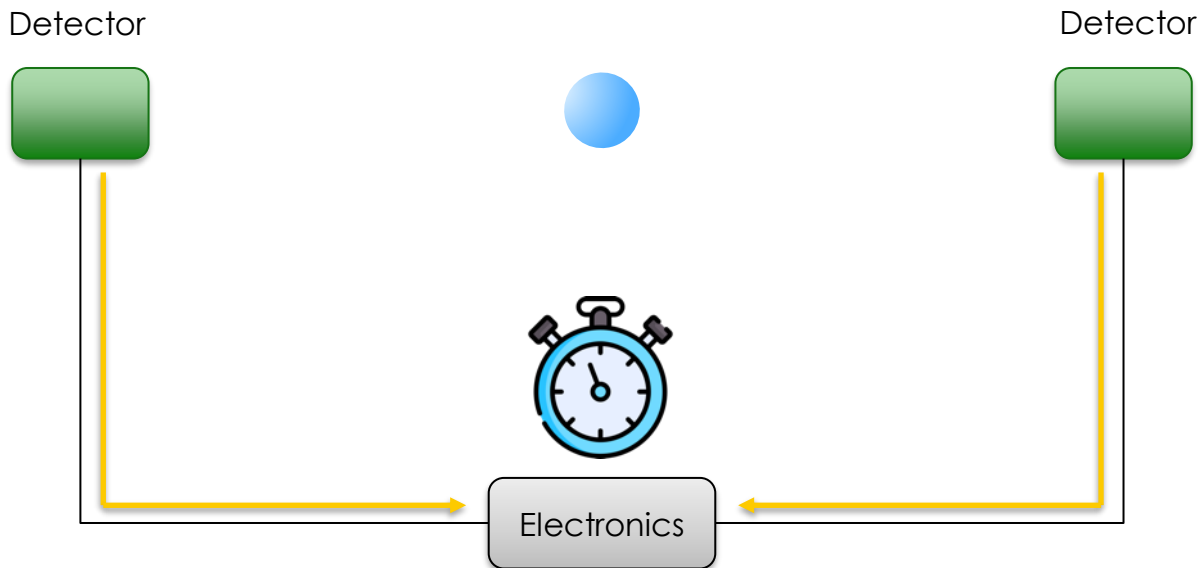**Stefan Ritt :: Head of Muon Physics Group :: Paul Scherrer Institute**

Mastering Picosecond Precision:
Lessons learned from Large-Scale Timing Systems

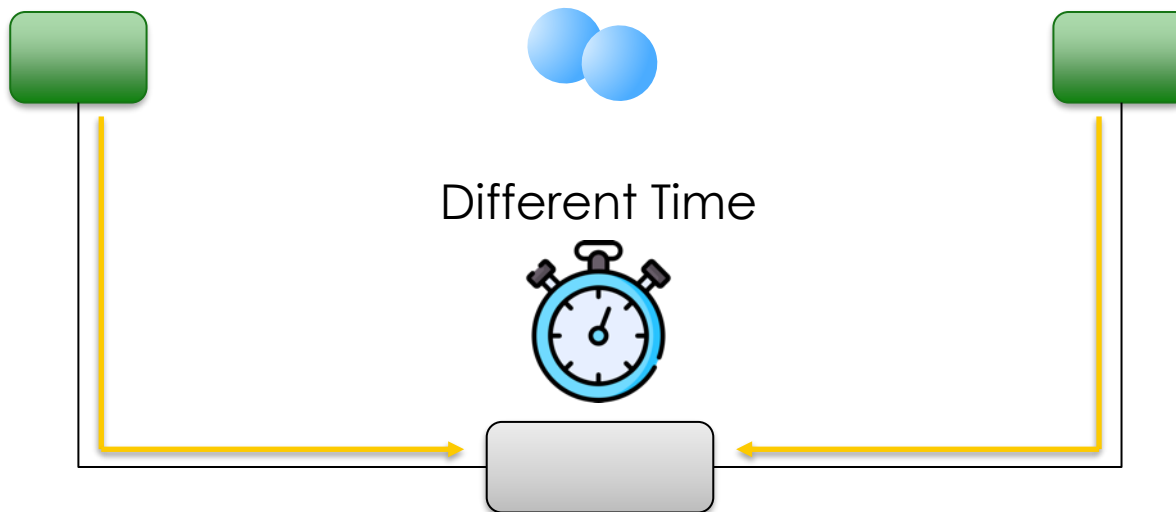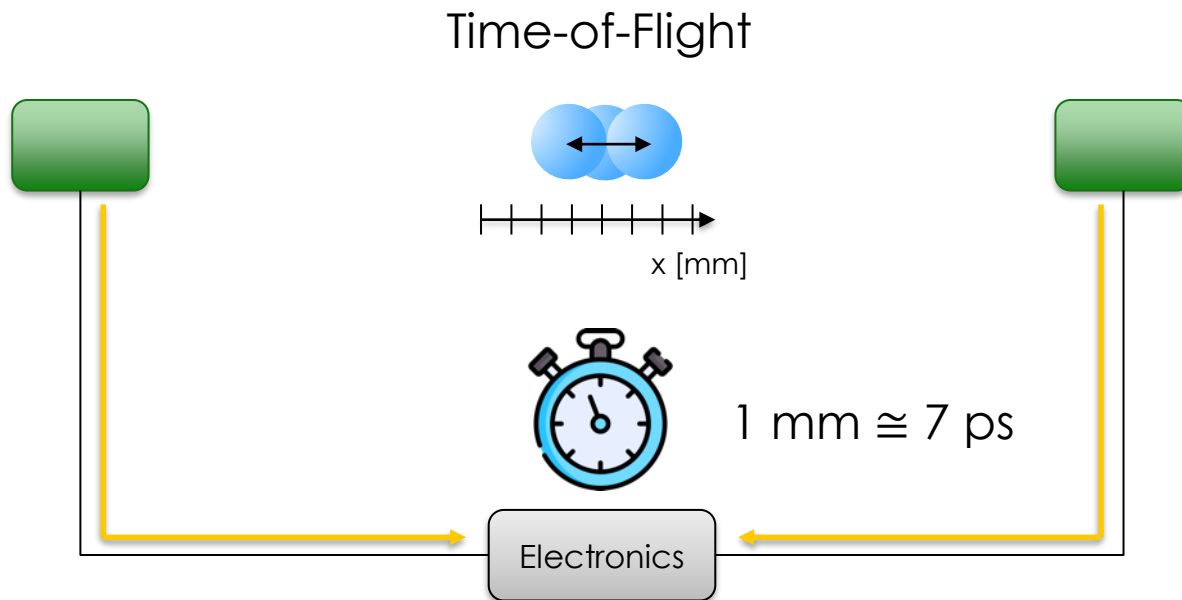**IEEE NPSS Real Time Conference, Qui Nhon, Vietnam, April 25, 2024**

Detector

Detector

Electronics

Two particle decay

Different Time

Measuring precision timing

Time-of-Flight

x [mm]

1 mm ≅ 7 ps

Electronics

N Detectors N^2 Clocks   N Detectors
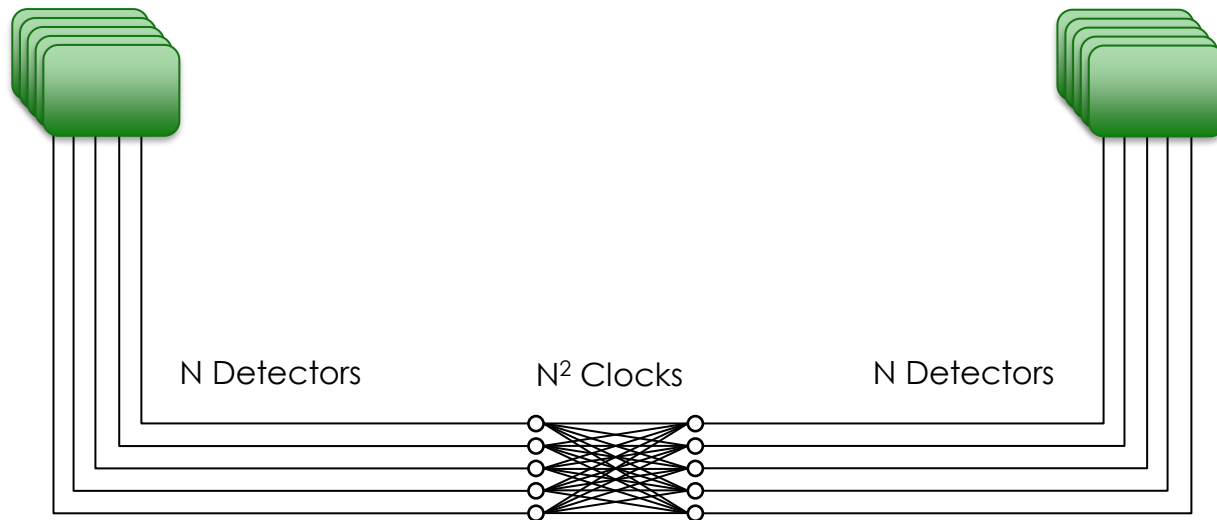
N=1000 → 1,000,000 Clocks

2N Clocks

N Detectors

N Detectors

Reference Clock

Time inaccuracy

"Jitter"

Repeater

"Skew"

Reference Clock
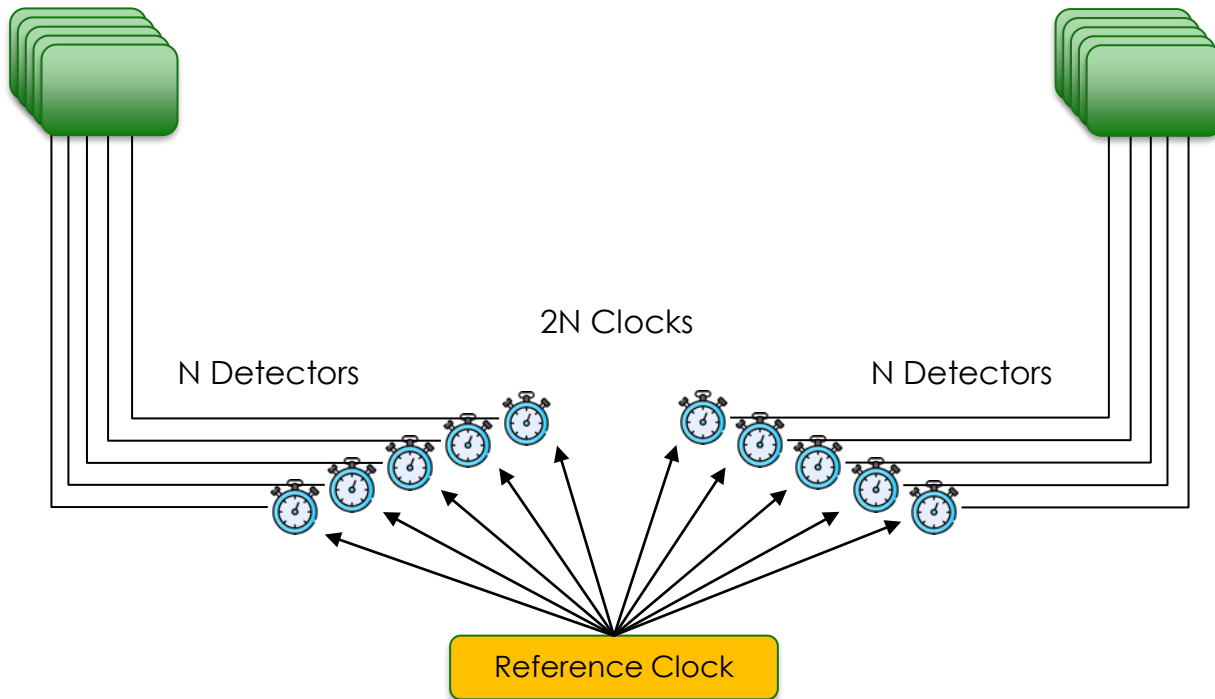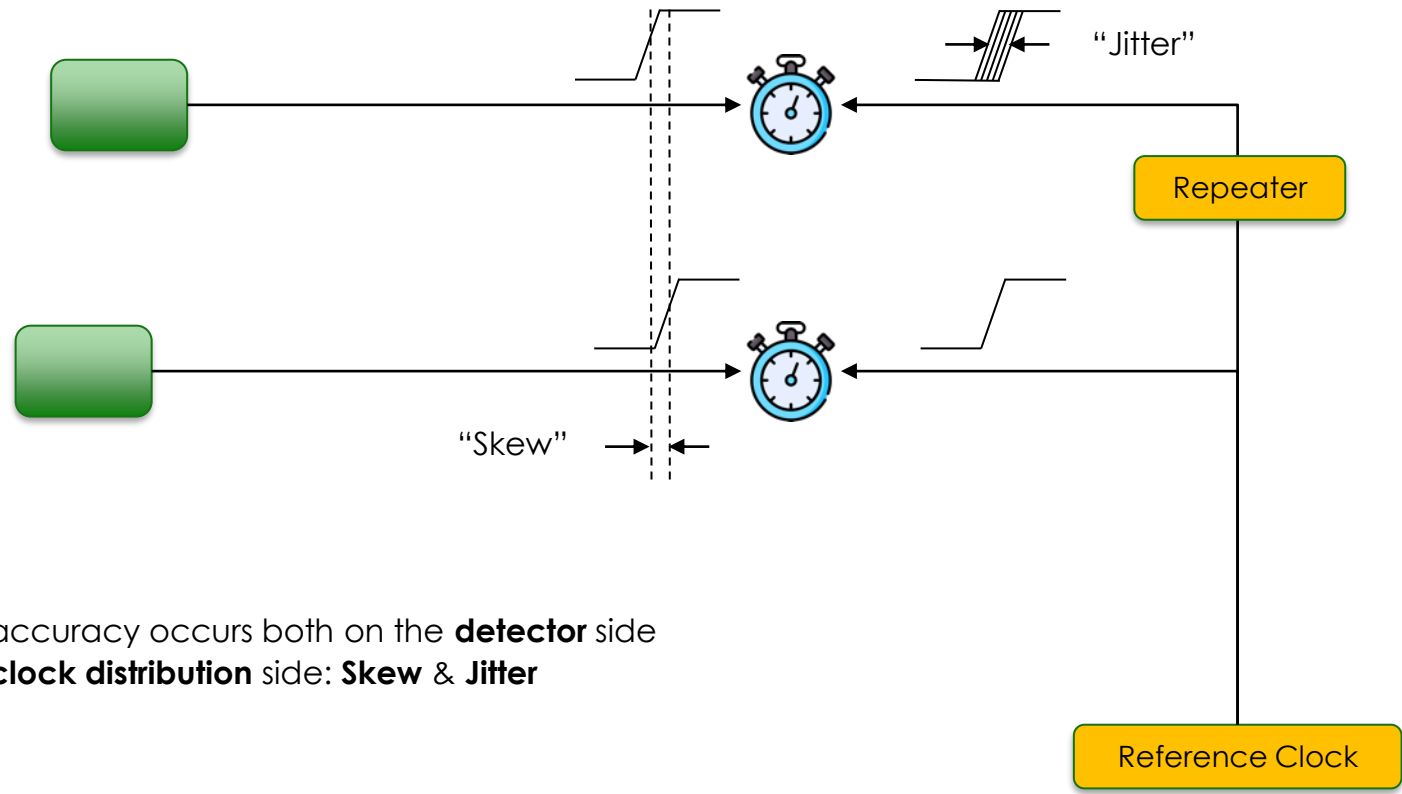
Timing inaccuracy occurs both on the **detector** side
and the **clock distribution** side: **Skew** & **Jitter**

MEG II Experiment at PSI

γ detection in liquid
Xenon Calorimeter: 4760 channels
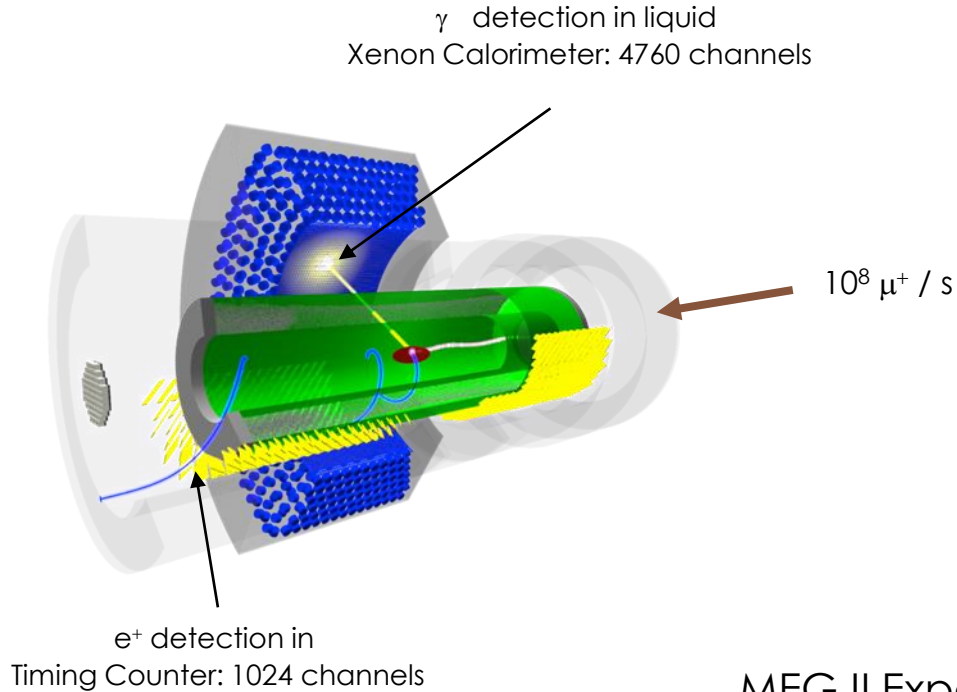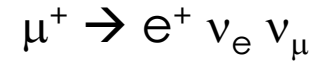
Normal μ decay
(Standard Model):

$$\mu^+ \rightarrow e^+ \, \nu_e \, \nu_\mu$$

$10^8 \, \mu^+$ / s

Lepton-Flavor Violating Decay
(New Physics):

$$\mu^+ \rightarrow e^+ \, \gamma$$

e⁺ detection in
Timing Counter: 1024 channels
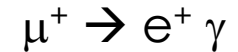
MEG II Experiment requires

~10 ps at electronics level

How to achieve timing at the Pico second level?

- Sources of timing jitter: **Single ended** lines, **PLL jitter**

- Clock **stability**
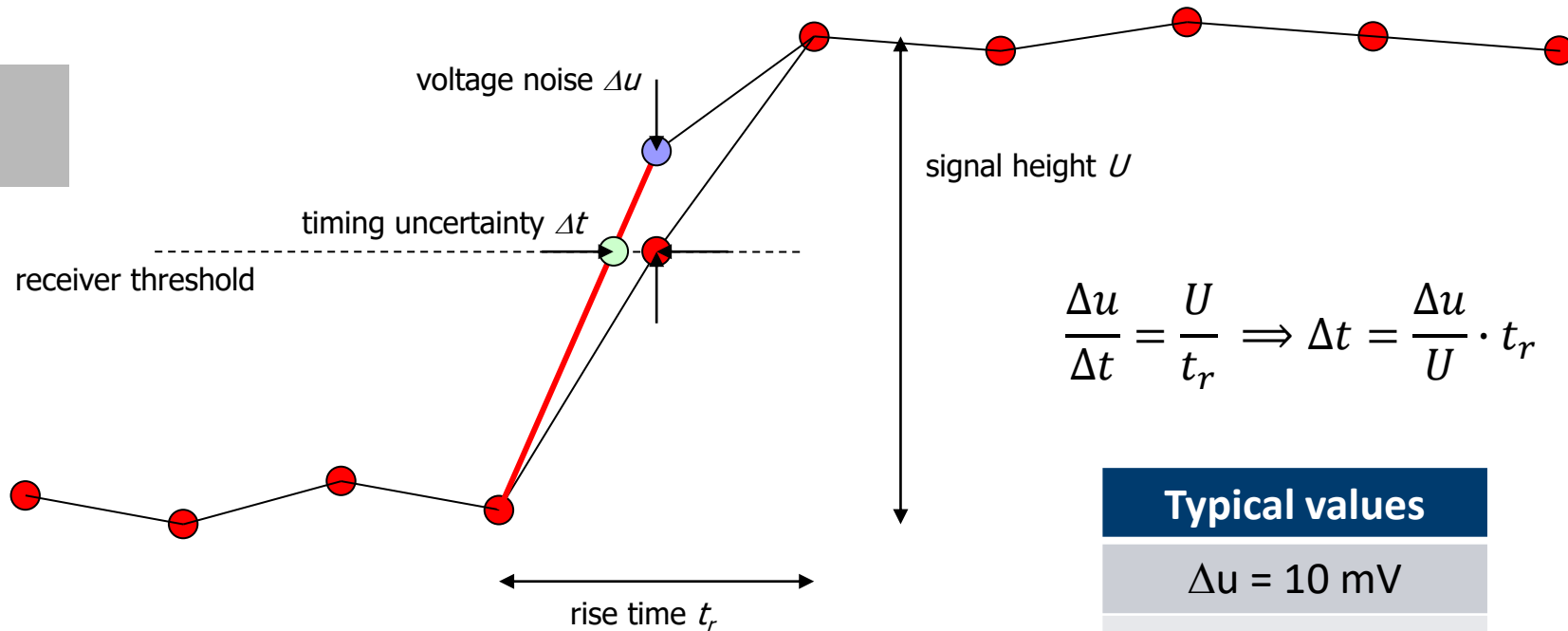
- **Noise reduction** strategies

- Timing **calibration**

- **Lessons learned** from the MEG II system

Jitter caused by voltage noise

voltage noise Δu

signal height U

timing uncertainty Δt

receiver threshold

rise time t_r

$$\frac{\Delta u}{\Delta t} = \frac{U}{t_r} \implies \Delta t = \frac{\Delta u}{U} \cdot t_r$$

Typical values
Δu = 10 mV
U = 3.3 V
t_r = 1 ns
Δt = 3 ps
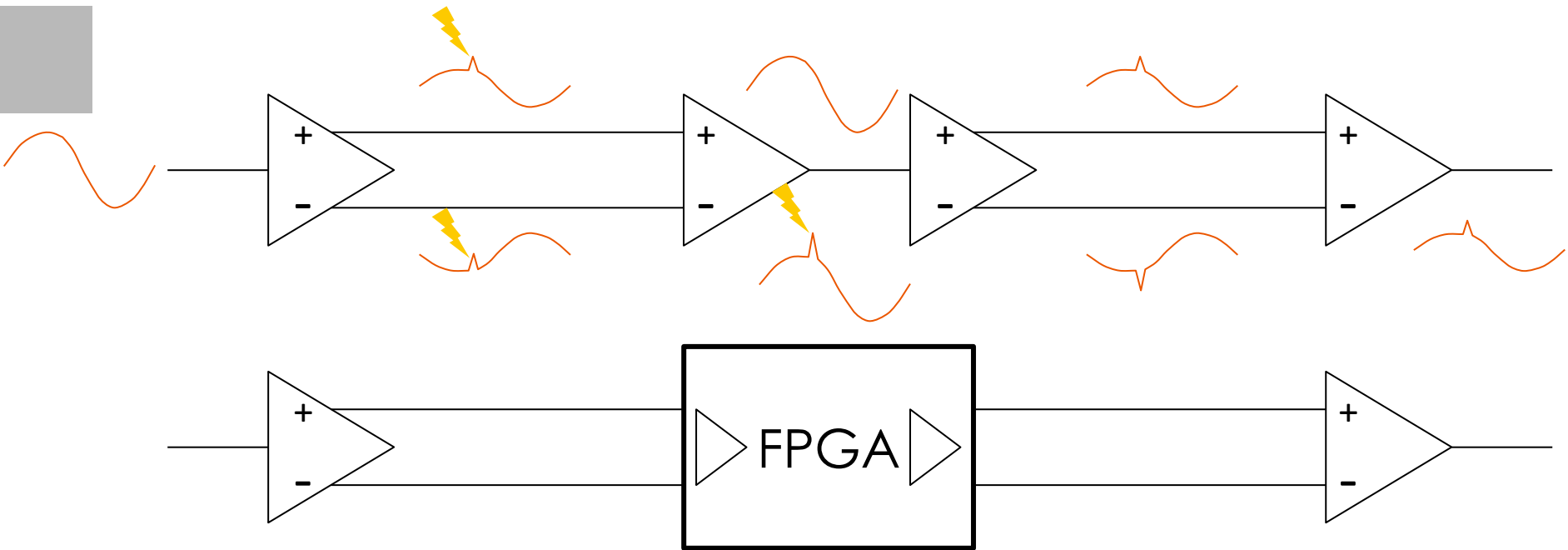
Do not send low-jitter clocks through FPGAs!
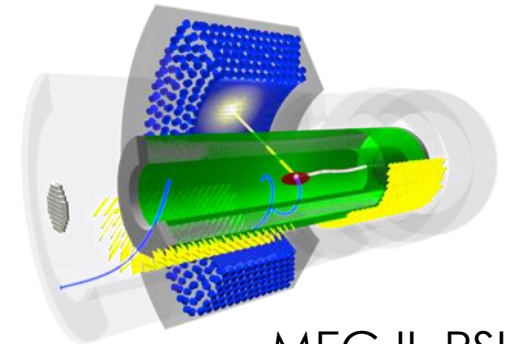
Optical fiber
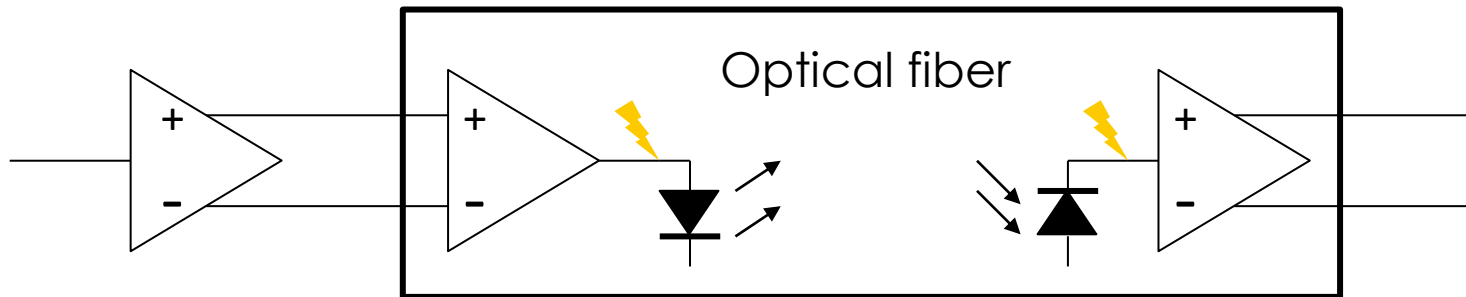
Careful with optical clock distribution!
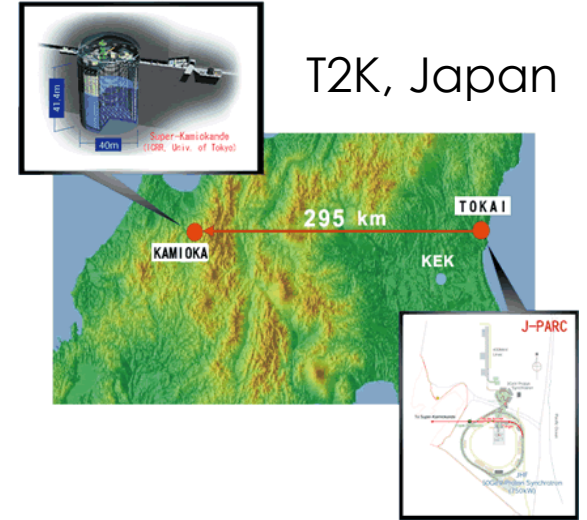
Clock stability

T2K, Japan

- **GPS** clock for measurements **far apart**

- **Atomic** clock for **long term** measurements

- Particle physics:
  Measurement periods **O(100 ns)**

  → Frequency stability of **10^{-5}** is enough
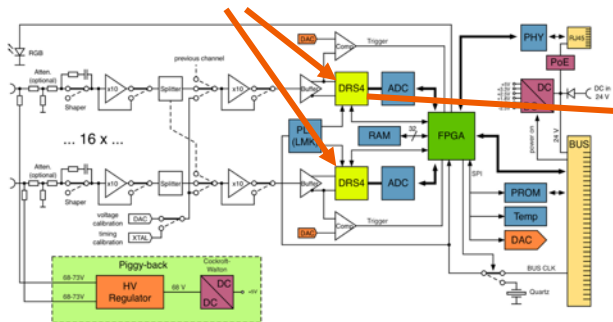 $$100 \text{ ns} * 10^{-5} = 1 \text{ ps}$$

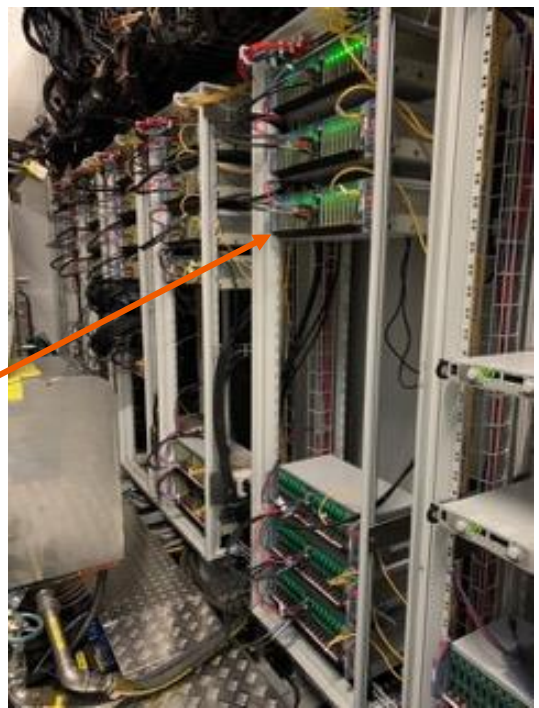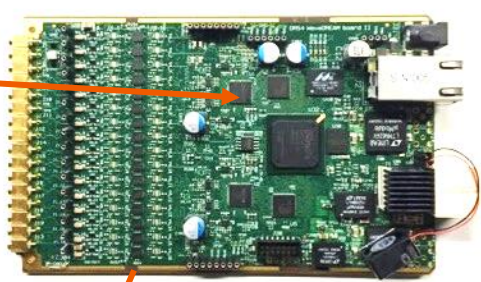 → Excellent **low-jitter** clock distribution to all detector channels needed

MEG II, PSI

WaveDAQ system for MEG II @ PSI

DRS4 chip

WaveDREAM Board

WaveDAQ Crate

9000+ channels 5 GSPS / 12 bit

PAUL SCHERRER INSTITUT

MEMS CLOCK OSCILLATOR

ASEMP

ASEMP

Pb **RoHS/RoHS II compliant**

Life Size ▦▦▦
3.2 x 2.5 x 0.85 mm

Moisture Sensitivity Level – MSL 1

▷ **FEATURES:**
- Low Power Consumption for high speed communication
- Exceptional Stability Over Temp. at -40 to +85°C, ±15ppm
- Extended Automotive Grade Temp. stability at -55 to +125°C, ±25ppm
- MIL-STD-883 shock and vibration compliant
- Durable QFN Plastic Compact Packaging
- Standby or Disable Tri-state function
- Low jitter (Period jitter RMS and Phase jitter RMS)

▷ **APPLICATIONS:**
- Storage Area Networks (SATA, SAS, Fiber Channel)
- Passive Optical Networks (EPON, 10G-EPON, GPON, 10G-PON)
- Ethernet (1G, 10GBASE-T/KR/LR/SR, FCoE)
- PCI Express
- Display port

Common Key Electrical Specifications – CMOS, LVPECL, LVDS, and HCSL

Parameters		Minimum	Typical	Maximum	Units	Notes
Frequency Range	CMOS	2.3000*		170.0000	MHz	-20 ~ +70°C -40 ~ +85°C
	CMOS	3.3000*		170.0000		-40 ~ +105°C -55 ~ +125°C
	LVPECL	2.3000*		460.0000		Commercial, Industrial temp. range
	LVDS	2.3000*		460.0000		Commercial, Industrial temp. range
	HCSL	2.3000*		460.0000		Commercial, Industrial temp. range
Operating Temperature		-20		+70	°C	See options
Storage Temperature		-55		+150	°C	
Overall Frequency Stability		-50		+50	ppm	See options
Supply Voltage (Vdd)		+2.25		+3.6	V	
Startup Time				5	ms	
Enable Time				20	ns	STD (Tri-state)
				5	ms	PD option (Power Down)
Disable Time				5	ns	
Disable Current			20	22	mA	STD (Tri-state)
				0.095		PD option (Power Down)
Tri-state Function (Standby/Disable)		"1" (VIH≥0.75*Vdd) or Open: Oscillation "0" (VIL<0.25*Vdd) : Hi Z			V	40kΩ pull-up resister embedded
Aging		-5.0		+5.0	ppm	First year

Key Electrical Specifications – LVDS

Parameters		Minimum	Typical	Maximum	Units	Notes
Supply Current (I$_{dd}$)			29	32	mA	RL=100Ω
Output Offset Voltage (V$_{OS}$)		1.125		1.4	V	RL=100Ω differential
Delta Offset Voltage (ΔV$_{OS}$)				50	mV	
Peak to Peak Output Swing (V$_{pp}$)			350		mV	Single ended
Rise Time	Tr		200			RL=50Ω , CL=2pF
Fall Time	Tf		200		ps	20% to 80%
Duty Cycle		48		52	%	Differential
Integrated Phase Jitter (J$_{PH}$)			0.28	2	ps	200kHz ~ 20MHz @156.25MHz
			0.40	2		100kHz ~ 20MHz @156.25MHz
			1.70	2		12kHz ~ 20MHz @156.25MHz
Period Jitter RMS (J$_{PER}$)			2.5		ps	

Phase jitter (integrated phase noise)
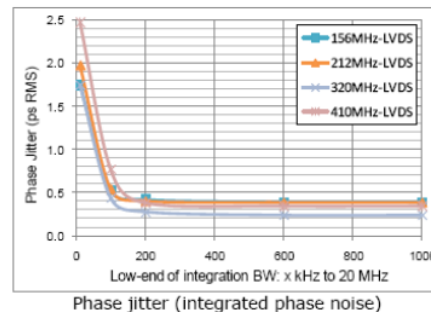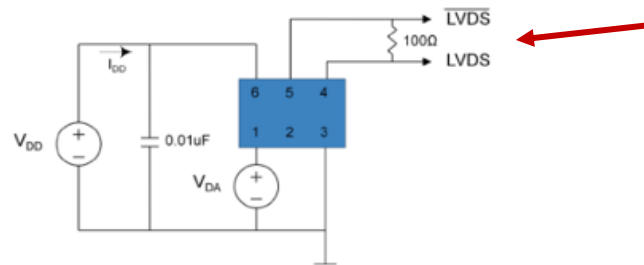
LVDS clock distribution

Texas Instruments

CDCLVD110A
SCAS841D – FEBRUARY 2007 – REVISED DECEMBER 2016

### CDCLVD110A Programmable Low-Voltage 1:10 LVDS Clock Driver

1 Features

- Low-Output Skew <30 ps (Typical) for Clock-Distribution Applications
- Distributes One Differential Clock Input to 10 LVDS Differential Clock Outputs
- V_{CC} Range: 2.5 V ±5%
- Typical Signaling Rate Capability of Up to 1.1 GHz
- Configurable Register (SI/CK) Individually Enables Disables Outputs, Selectable CLK0, $\overline{CLK0}$ or CLK1, $\overline{CLK1}$ Inputs
- Full Rail-to-Rail Common-Mode Input Range
- Receiver Input Threshold: ±100 mV
- Available in 32-Pin LQFP and VQFN Package
- Fail-Safe I/O-Pins for V_{DD} = 0 V (Power Down)

3 Description

The CDCLVD110A clock driver distributes one pair of differential LVDS clock inputs (either CLK0 or CLK1) to 10 pairs of differential clock outputs (Q0 to Q9) with minimum skew for clock distribution. The CDCLVD110A is specifically designed to drive 50-Ω transmission lines.

When the control enable is high (EN = 1), the 10 differential outputs are programmable in that each output can be individually enabled or disabled (3-stated) according to the first 10 bits loaded into the shift register. Once the shift register is loaded, the last bit selects either CLK0 or CLK1 as the clock input. However, when EN = 0, the outputs are not programmable and all outputs are enabled.

The CDCLVD110A has an improved start-up circuit that minimizes enabling time in AC- and DC-coupled systems
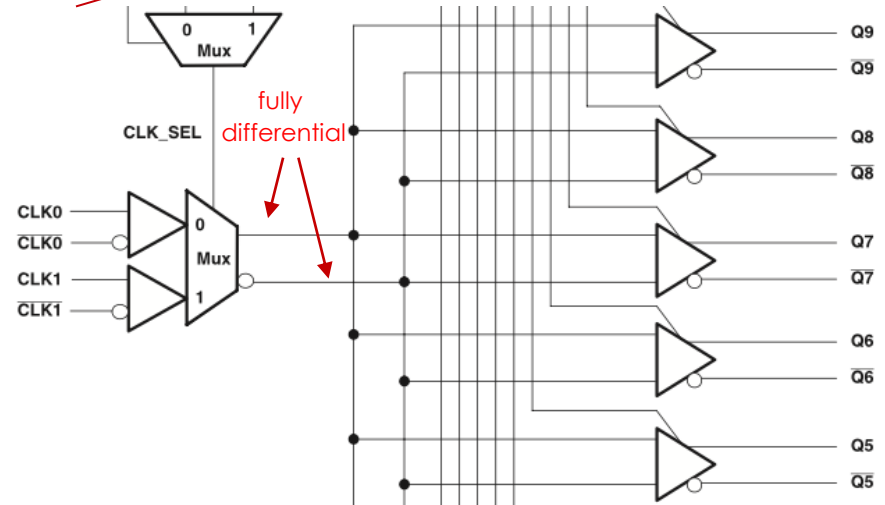
6.7 Jitter Characteristics

characterized with CDCLVD110 performance EVM, V_{DD} = 3.3 V, outputs not under test are ter
otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{jitterLVDS}$	Additive phase jitter from input to LVDS output Q3 and $\overline{Q3}$	12 kHz to 5 MHz, f_{out} = 30.72 MHz		281		fs rms
		12 kHz to 20 MHz, f_{out} = 125 MHz		111		

fully differential
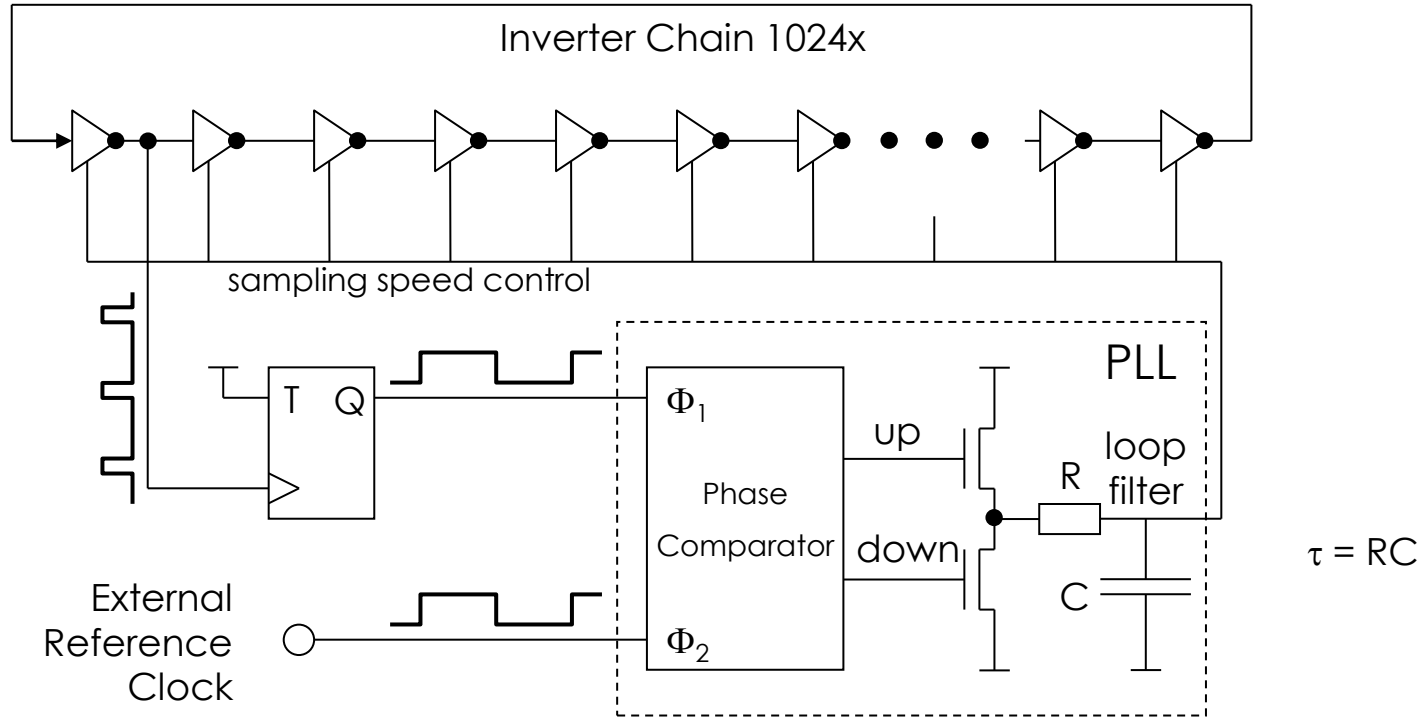
Perfect
Clock
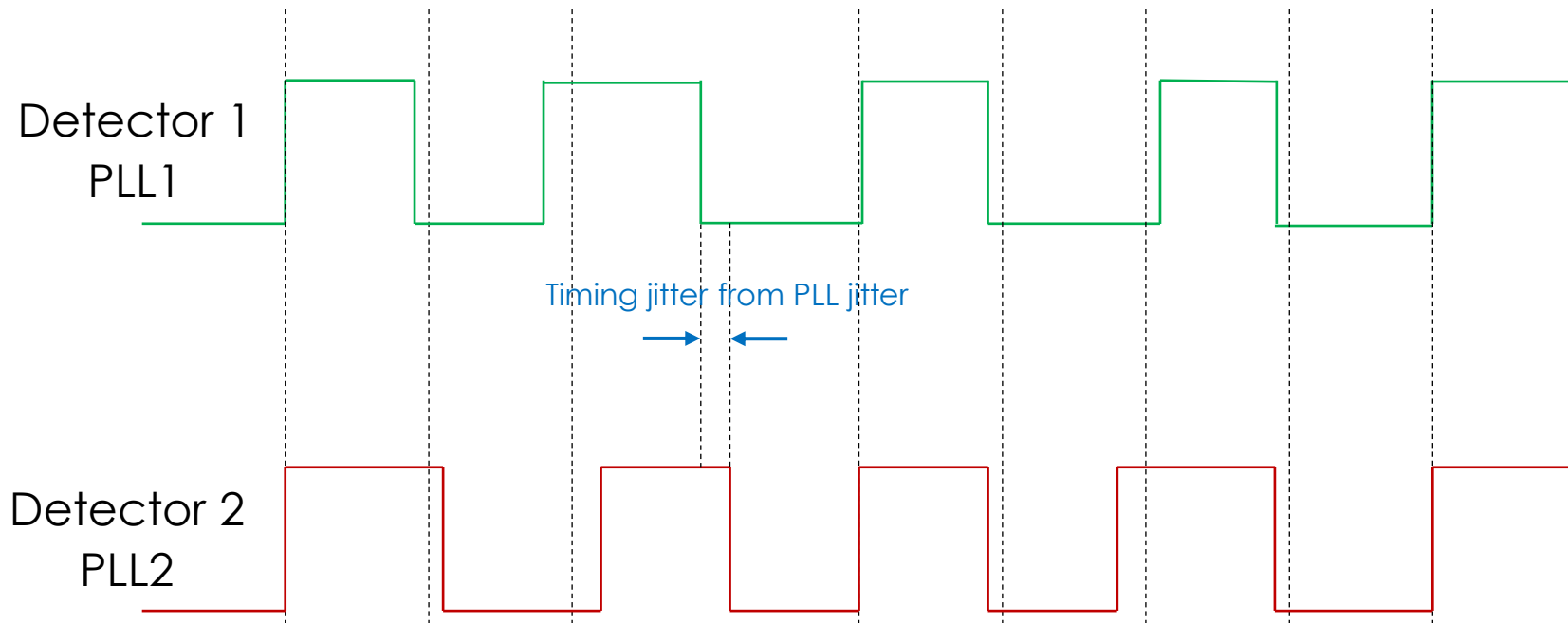
PLL
Clock

Period
Jitter

Phase
Jitter

Detector 1
PLL1

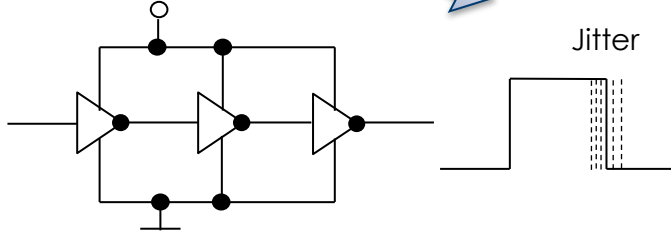Timing jitter from PLL jitter

Detector 2
PLL2
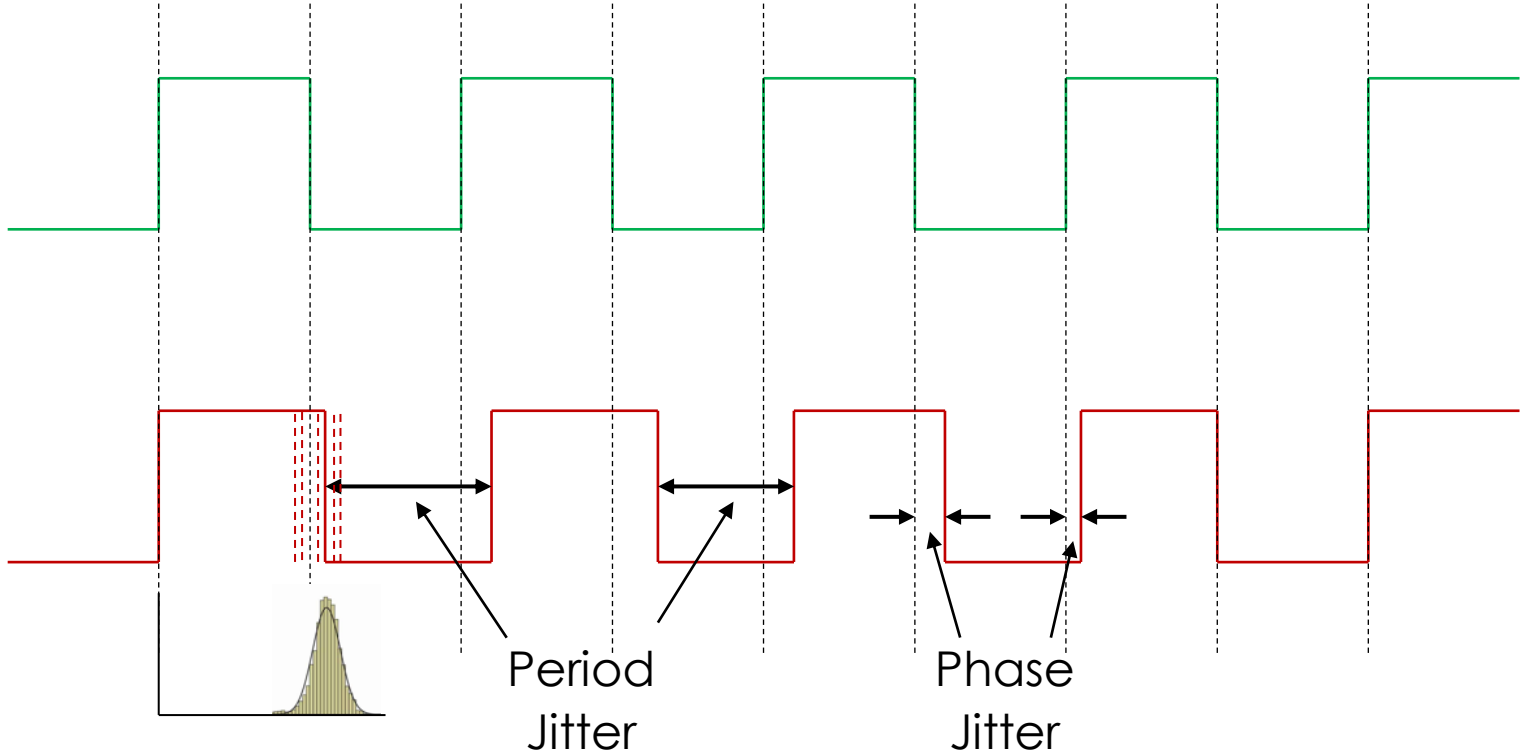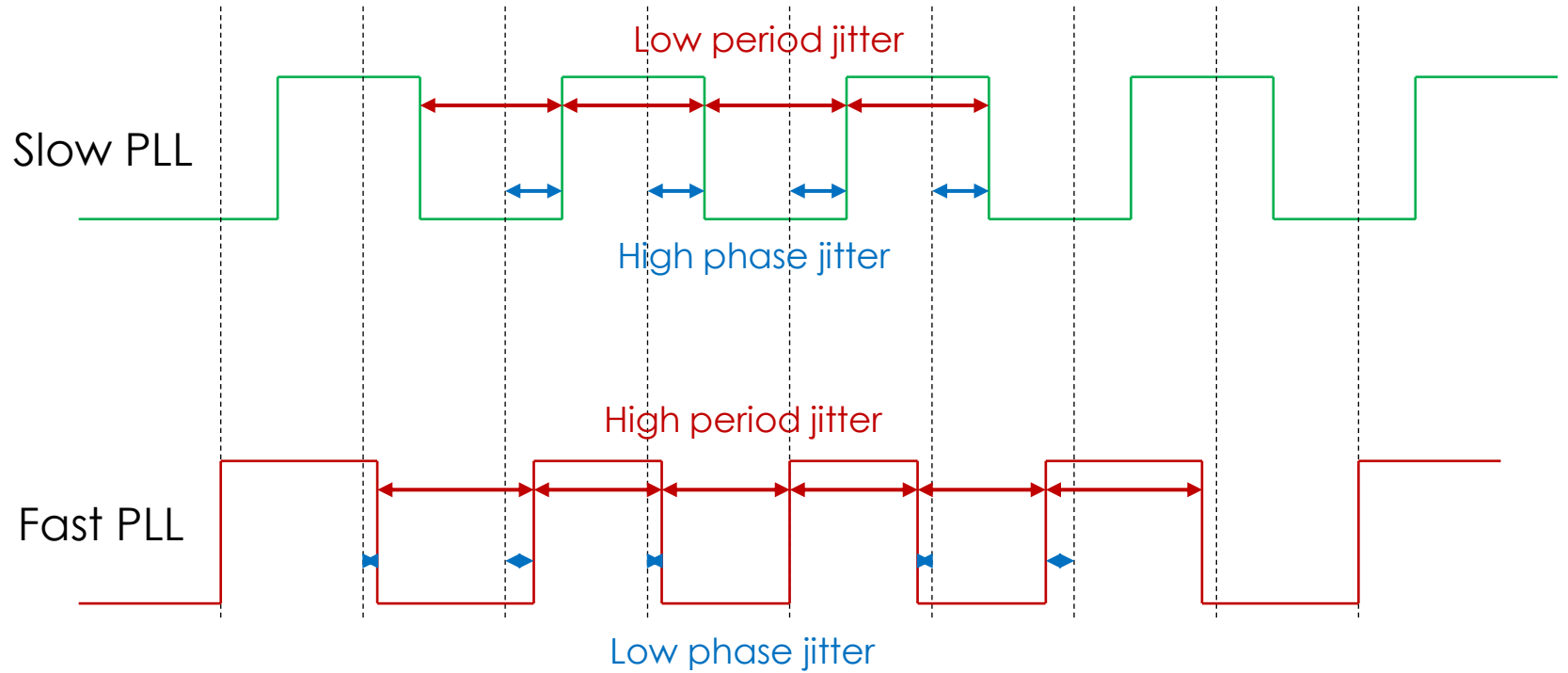
To achieve minimal timing jitter, PLL **phase jitter** must be **minimized**
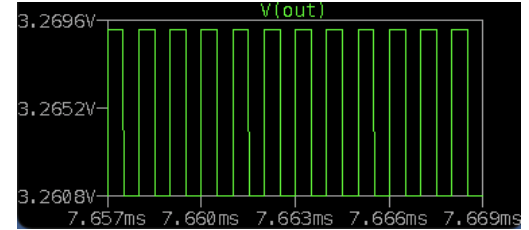
PLL jitter from power supply noise

Power Noise

VDD
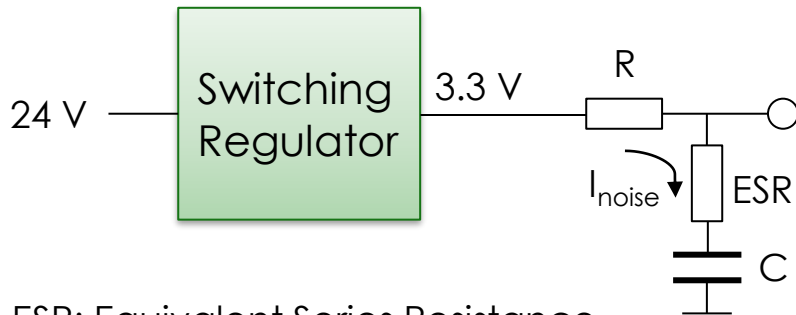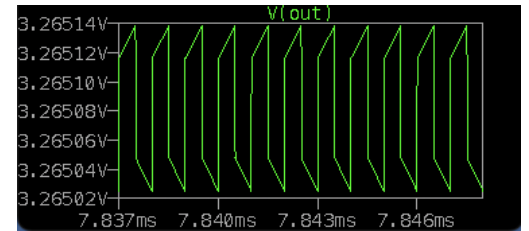
Jitter

DRS4 chip: 1 mV noise → 10 ps jitter

ESR = 1 Ohm

8 mV

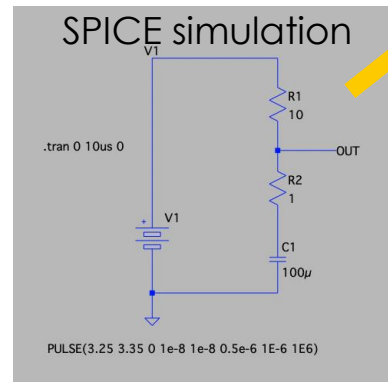ESR = 0.01 Ohm

0.1 mV

24 V — Switching Regulator — 3.3 V — R — ESR — C

I_{noise}

ESR: Equivalent Series Resistance

SPICE simulation

.tran 0 10us 0

V1
R1
10
OUT
R2
1
C1
100μ

PULSE(3.25 3.35 0 1e-8 1e-8 0.5e-6 1E-6 1E6)

Use **low-ESR** capacitors for power supply filtering

# Used filter components

Standard Ratings

Rated Voltage (V)(code)	Surge Voltage (V)	Rated Capacitance (µF)	Case Size φD × L (mm)	tan δ	Leakage Current (µA)	ESR (mΩ) (at 100kHz 20°C)	Rated Ripple (mArms)	Part Number
2.5 (0E)	2.8	390	6.3 × 6	0.12	293	10	3900	PCK0E391MCO1GS
		560	8 × 7	0.12	420	9	4500	PCK0E561MCO1GS
		680	8 × 7	0.12	510	9	4500	PCK0E681MCO1GS
		1200	10 × 8	0.12	900	9	5000	PCK0E122MCO1GS
		2200	10 × 10	0.12	1650	8	6000	PCK0E222MCO1GS

560 µF / 9 mΩ

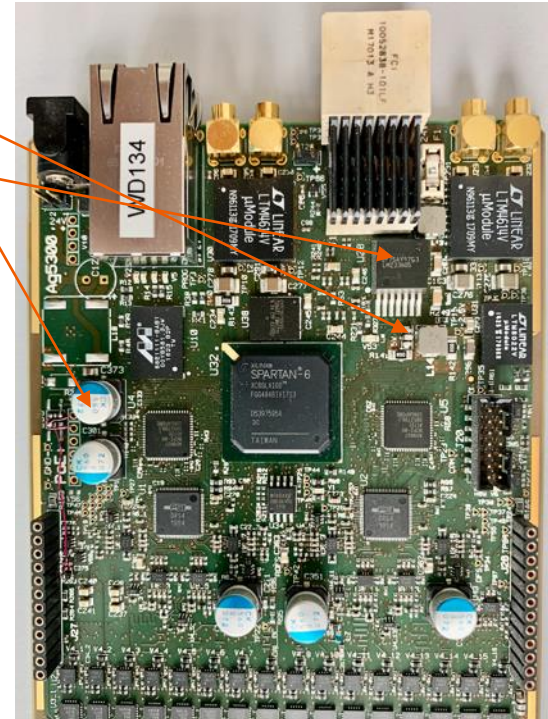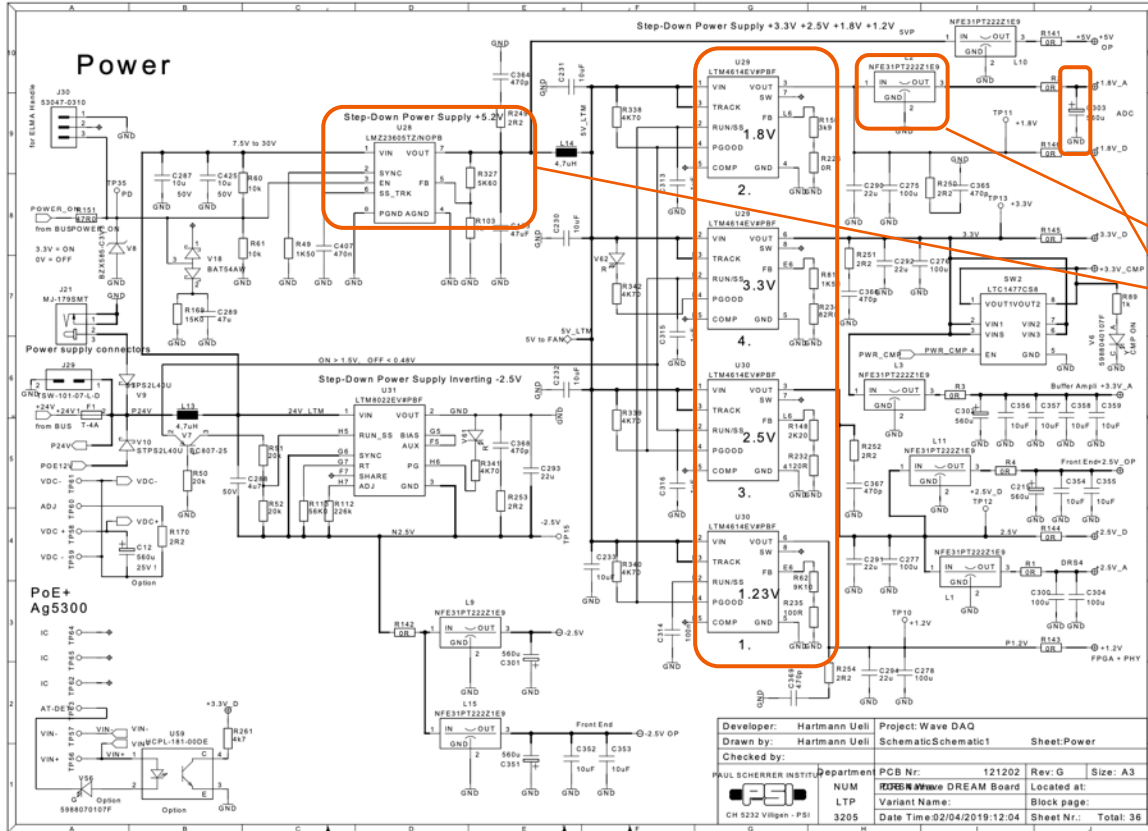## LC combines EMI Suppressor Filter NFE31PT222Z1E9
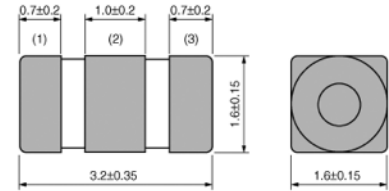
R = 100 mΩ
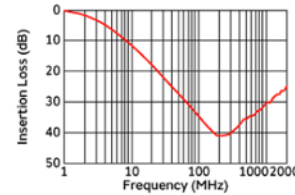
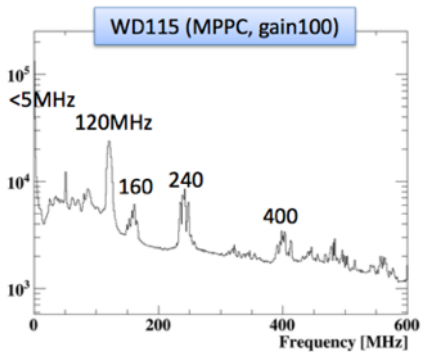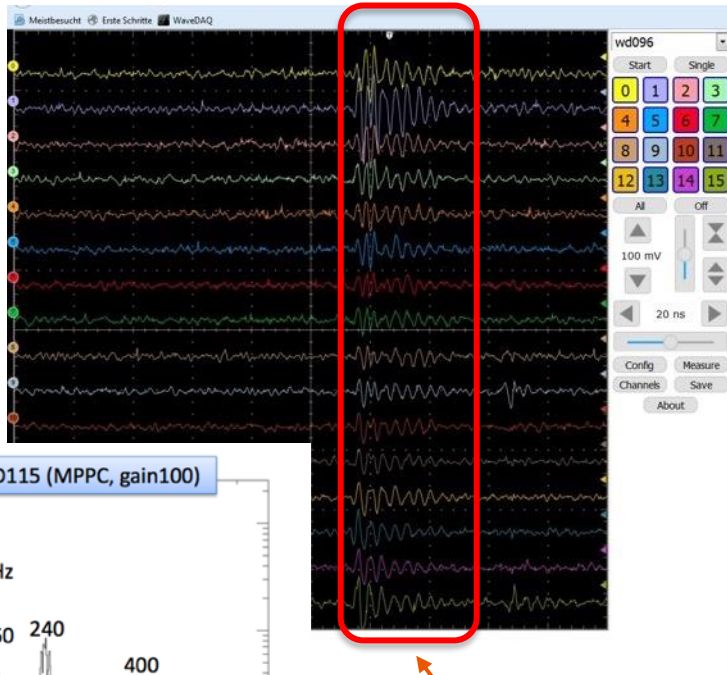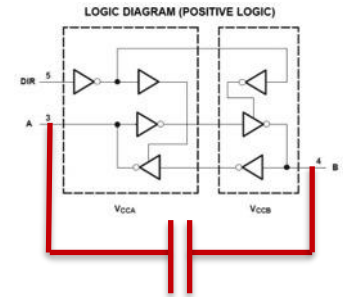Insertion Loss Characteristics   Equivalent Circuit
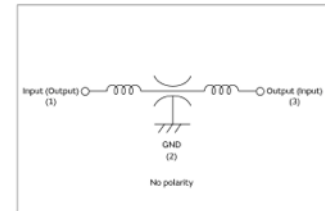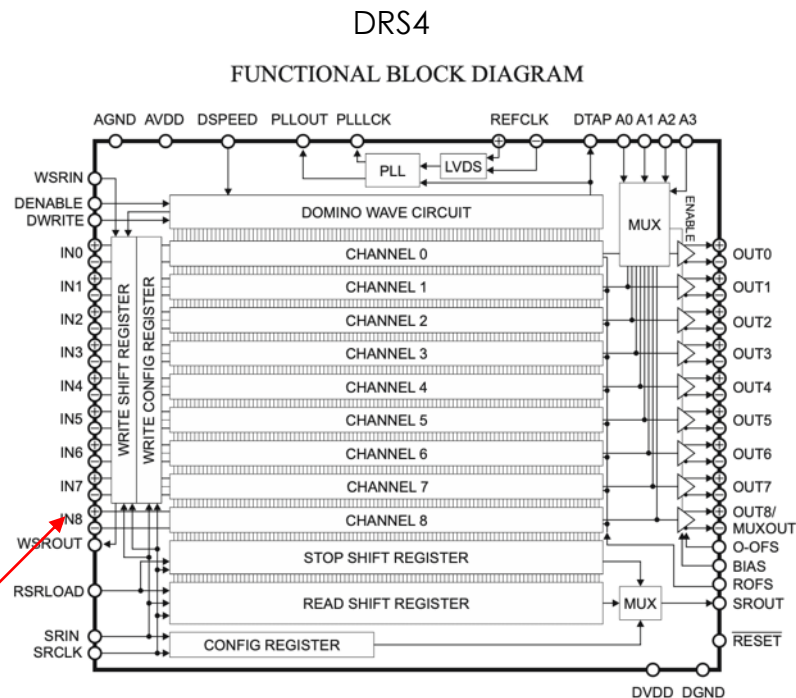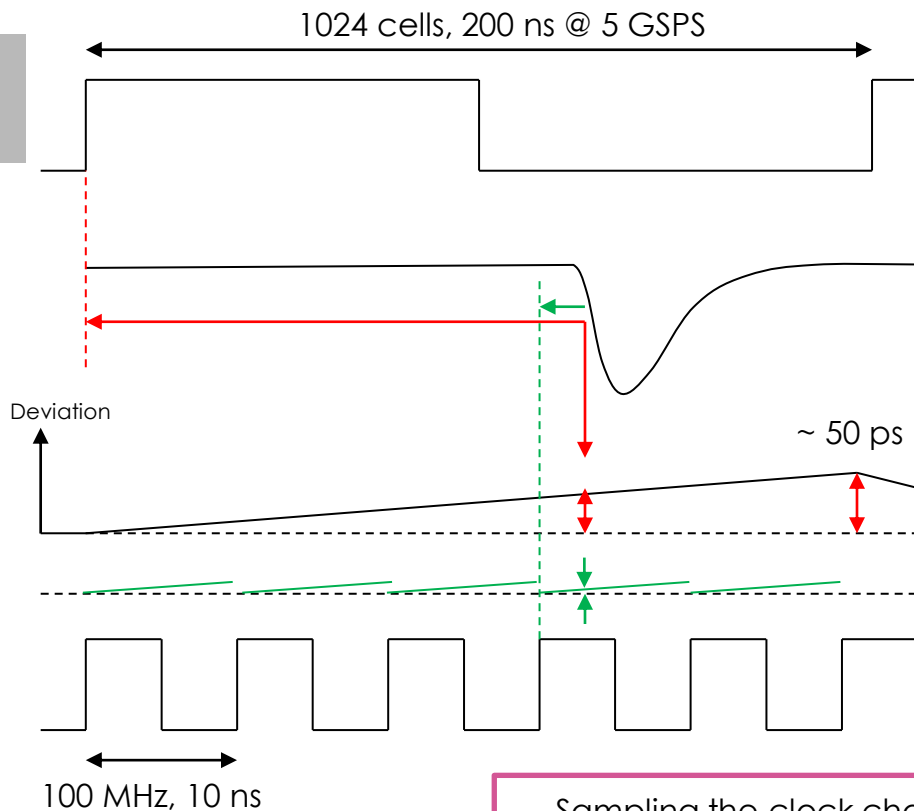
Electromagnetic Interference (EMI)

Shielding

Slew rate limiter

WD115 (MPPC, gain100)

10^5
<5MHz
120MHz
160 240
10^4
400
10^3

0   200   400   600
Frequency [MHz]

EMI pulse from switching converter

1024 cells, 200 ns @ 5 GSPS

Deviation

~ 50 ps

100 MHz, 10 ns

DRS4

FUNCTIONAL BLOCK DIAGRAM
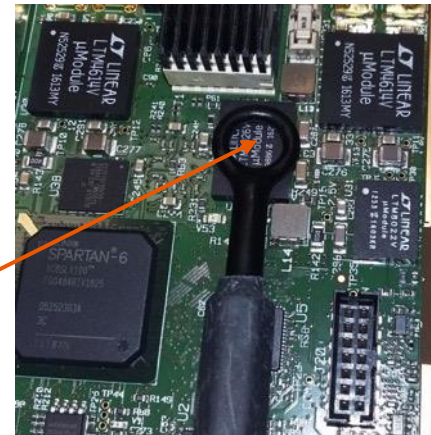
Sampling the clock channel reduces uncertainty from ~25 ps to <2 ps

The WaveDAQ system

# Custom Design "WaveDAQ"

- Standard 19" crate + **custom backplane** (no VME, no xTCA)

- Idea: Not only a solution for MEG II,
  but **more general** "crate standard"

- Features:

  – Serial bus (**SPI**) for configuration

  – **Trigger / Busy signals** in **backplane**

  – "**Dual Star**" Serial gigabit links

  – **Hot-swap** functionality

  – Low jitter (**<5 ps**) clock
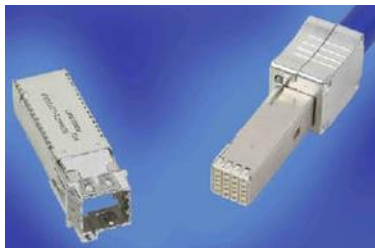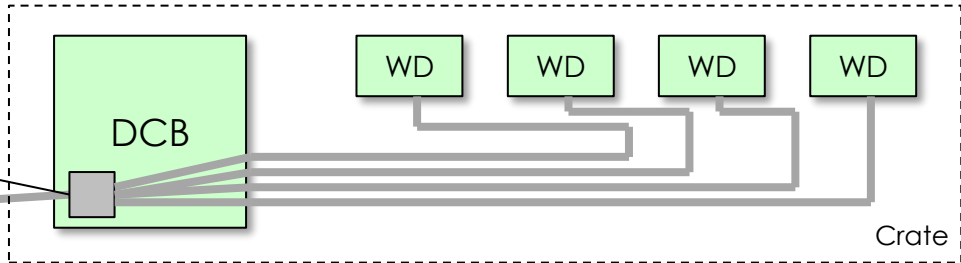
  – **Shelf management** with Ethernet and power
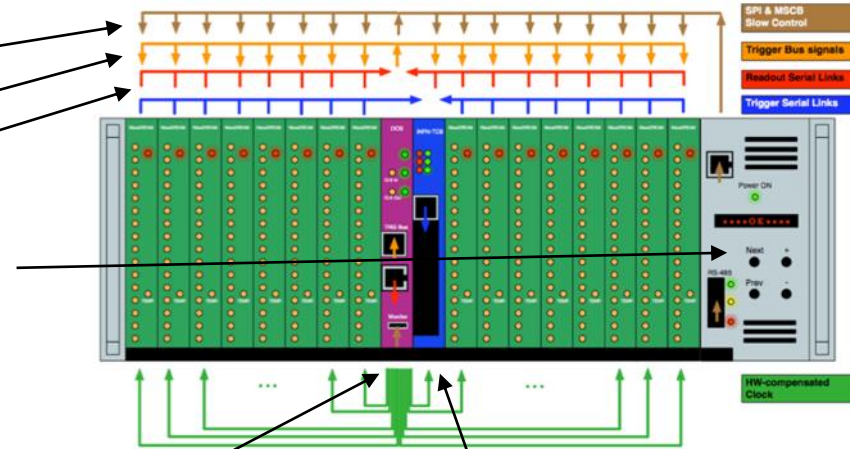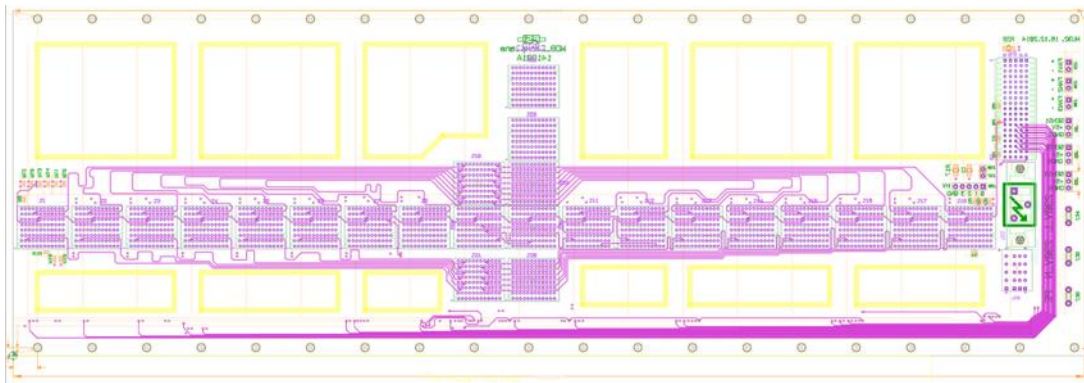
Data Concentrator Board (DCB)

Trigger Concentrator Board (TCB)

WaveDAQ Backplane
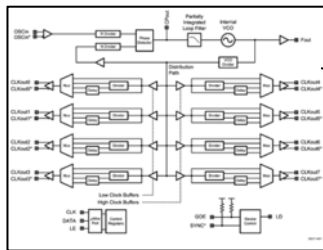
LMK03000 Jitter Cleaner
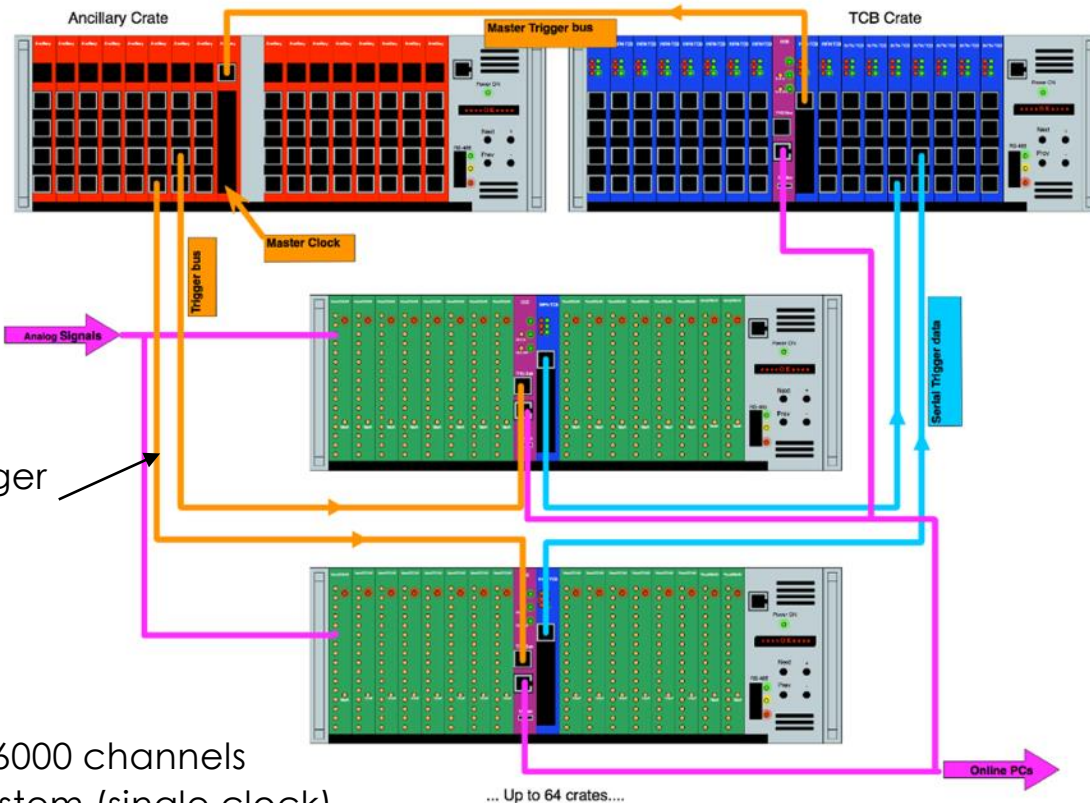
master clock

DCB

WD WD WD WD

Crate
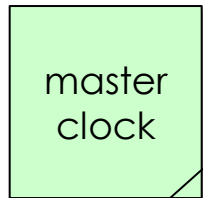
FCI Densishield Cable

Half Height Backplane
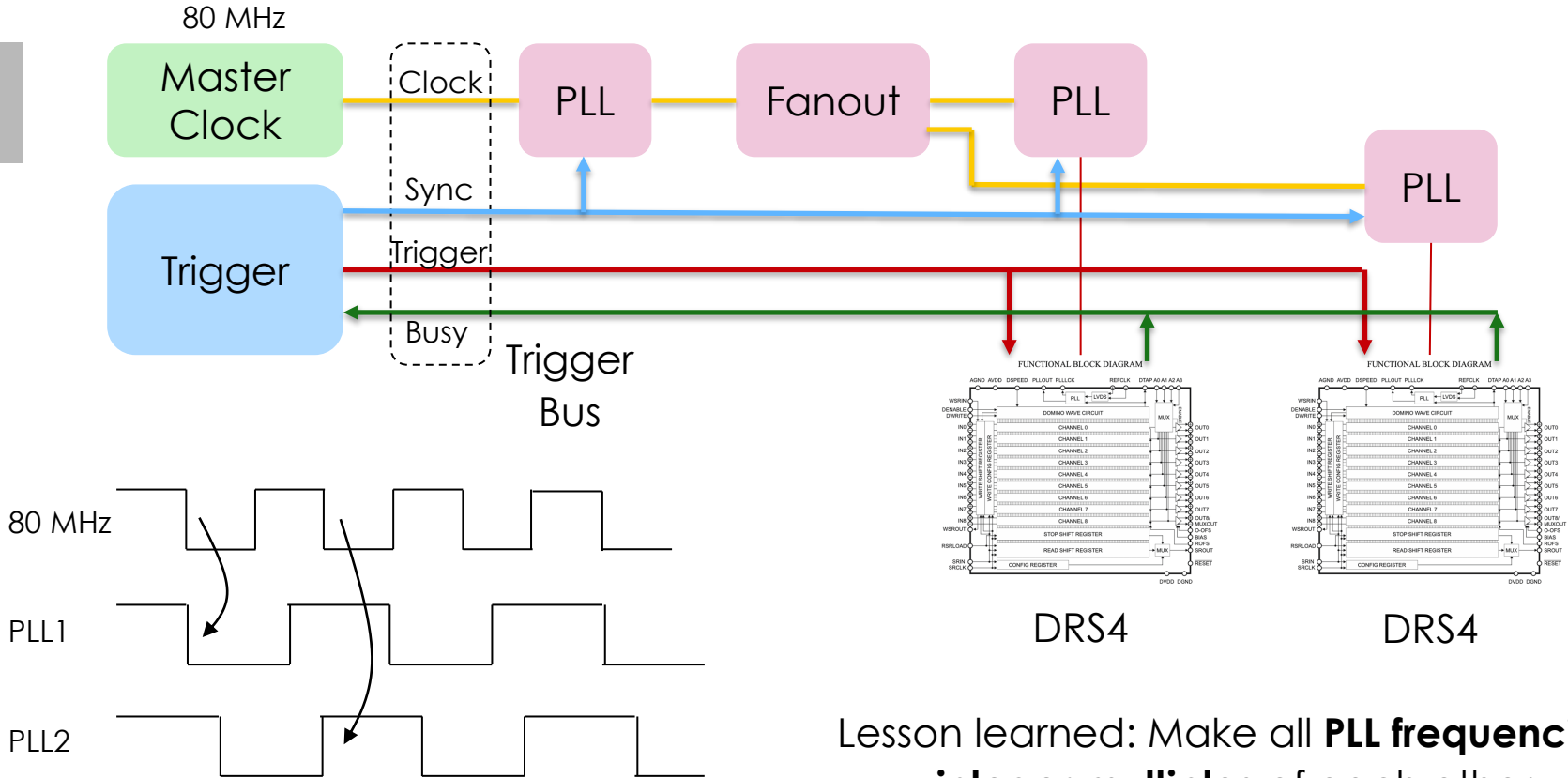
Clock and Trigger distribution

Scaling up to 16000 channels
Synchronous System (single clock)

Synchronization

80 MHz

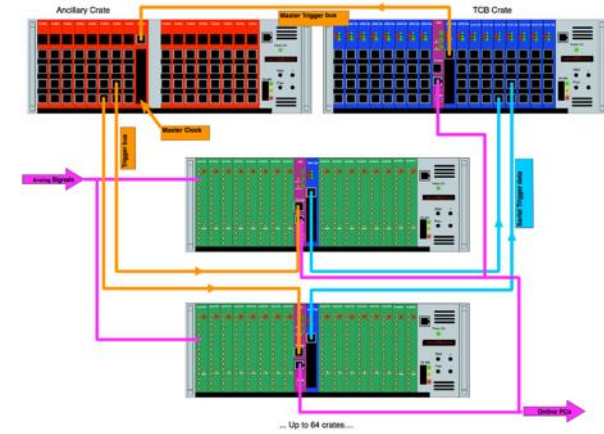Master Clock

Clock

PLL

Fanout

PLL

PLL

Sync

Trigger

Trigger

Busy

Trigger Bus

80 MHz

PLL1

PLL2

FUNCTIONAL BLOCK DIAGRAM

FUNCTIONAL BLOCK DIAGRAM

DRS4

DRS4

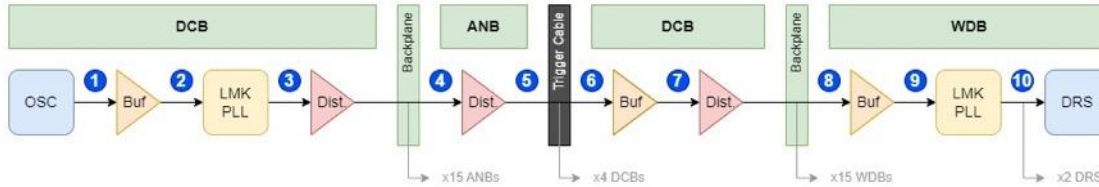Lesson learned: Make all **PLL frequencies integer multiples** of each other

Jitter measurements

courtesy E. Schmidt, PSI

Filename + ToDo	Signal Probe Location	Signal	Ref Probe Location	Ref Signal	Jitter Std Dev	Jitter Min	Jitter Max
27_4_Crate190_AnbDistIn_vs_3_DcbDistIn *Switch scope to refclk setup.*	4	ANB Distributor Input (Soldered)	3	DCB Distributor Input (Soldered)	10.8 ps	-63.7 ps	53.2 ps
28_7_Crate196_DcbDistIn_vs_Crate192_DcbDistIn *Solder 2 Probes to DCB02/DCB07 distributor input from Cable.*	7 Crate196	DCB Distributor Input (Soldered)	7 Crate192	DCB Distributor Input (Soldered)	7.3 ps	-39.7 ps	45.5 ps
29_7_Crate196_DcbDistIn_vs_ScopeRef *Switch to scope reference setup.*	7	DCB Distributor Input (Soldered)	None	Scope Constant Clock	3.9 ps	-23.4 ps	31.0 ps
30_9_Crate196_Slot15WdbLmkIn_vs_ScopeRef *Solder 2 Probes to 2 WDB280/WDB317 LMK inputs.*	9	WDB LMK Input (Soldered)	None	Scope Constant Clock	2.0 ps	-10.9 ps	12.3 ps
31_9_Crate196_Slot15WdbLmkIn_vs_Slot1WdbLmkIn *Switch scope to refclk setup.*	9 Slot15	WDB LMK Input (Soldered)	9 Slot1	WDB LMK Input (Soldered)	1.9 ps	-11.1 ps	11.8 ps
32_9_Crate196_Slot15WdbLmkIn_vs_Crate192_Slot15WdbLmkIn	9 Crate196	WDB LMK Input (Soldered)	9 Crate192	WDB LMK Input (Soldered)	3.0 ps	-16.4 ps	16.8 ps

Tektronix MSO64B
8 GHz, 50 GSPS
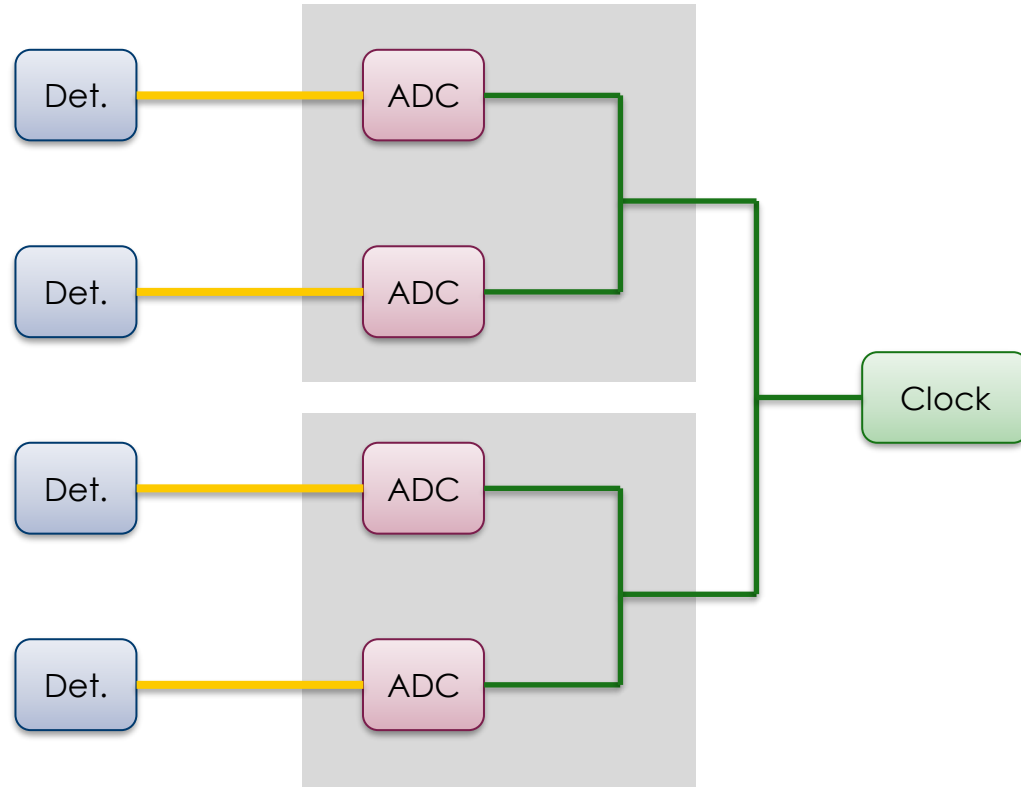**soldered diff. probes**!

σ_{jitter} = 1.9 ps
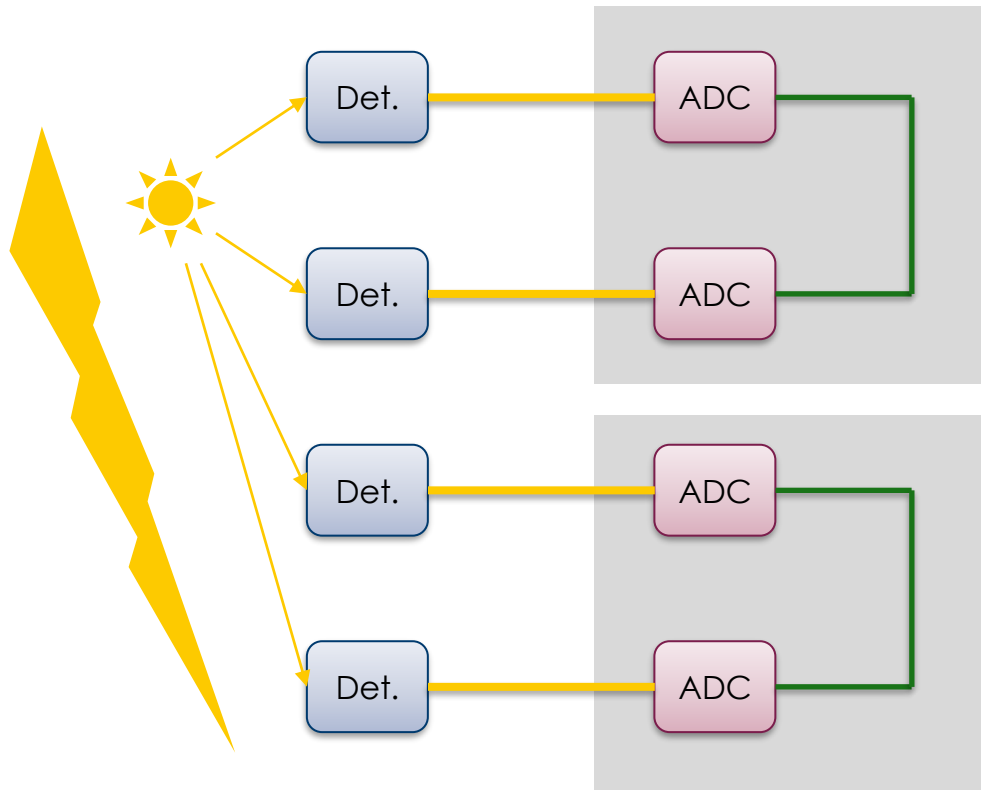
Slot - Slot

Crate - Crate
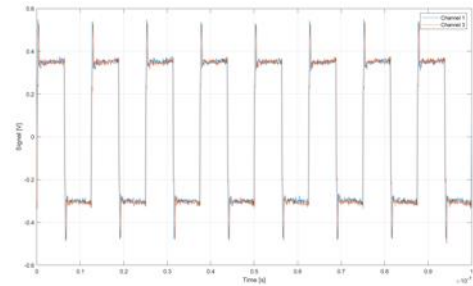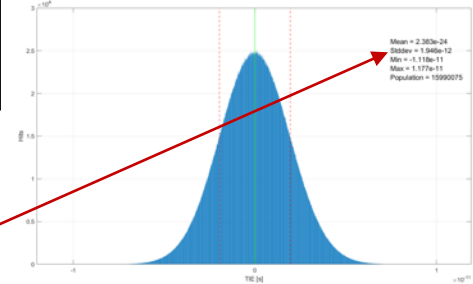
- Clock distribution is **never perfect** to the ps level

- Global sync injection at ADC does not calibrate **different cable lengths**

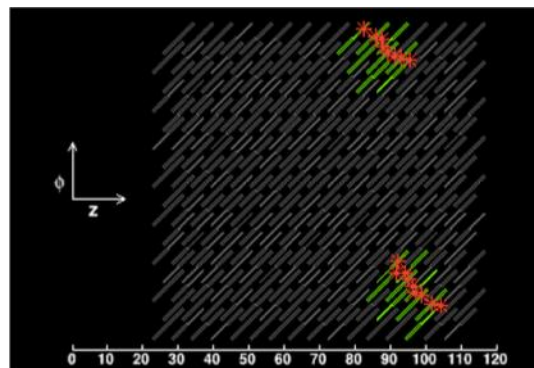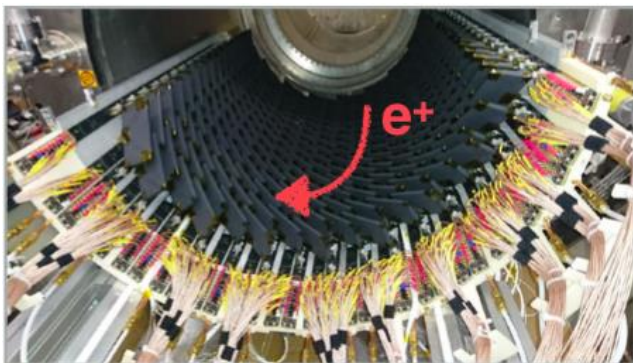- Signal **injection** at detector can be **difficult**

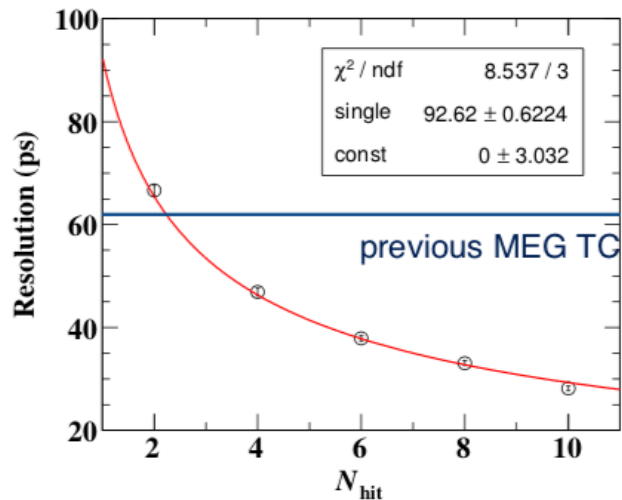**Solution**: Use a **physics event** which is seen by all detectors:

– **LED** flash in calorimeter

– **Cosmic** traversing many channels

– **Correct** for different light path

MEG II Timing Counter

- 8 x 10^8 μ/s
- 256 scintillating tiles 4x6 cm, **512 WDB chan**nels (2 crates)
- Resolution scales with sqrt(N)
- **35 ps** reached with 8 hits

χ² / ndf	8.537 / 3
single	92.62 ± 0.6224
const	0 ± 3.032

Lessons learned (so far...)

- Designing a **crate standard** is **easier** than anticipated (if no committee is involved 😉)

- Distributing a **5 ps** jitter clock is not so hard

- Doing everything **from scratch** can **simplify** things
  - **shelf manager** with 8-bit uC with few 100 lines of code
  - crate costs **~ 2k$** including power supply

- Mixed signal board with **40 μV** of noise (gain=100 !) is **tough**
  - whole project took **6 years** from first idea with ~2 FTE
  - analog front-end took **1.5 years**, FW ~2 years
  - careful selecting and shielding **DC-DC** converter, needed **4 revisions**
  - the more noise you fix, the more new sources you find
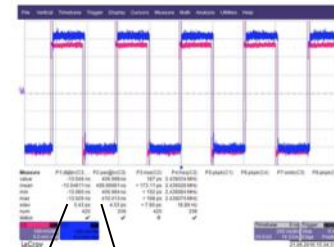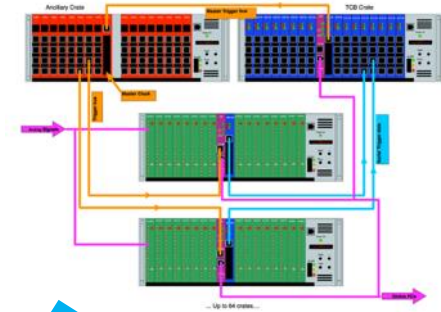 - Lots of **experience** obtained often missing in textbooks

DALL-E

- Use end-to-end **differential** clock distribution

- Careful **filter** power for all PLLs with
  low-ESR capacitors

- Identify and remove **EMI sources**

- Large systems with
  <5 ps timing can be built

- This talk:
     IEEE NPSS **Educational Video** at
        https://ieee-npss.org/videos/

5.4 ps