

Enclustra Clocking for IpGBT

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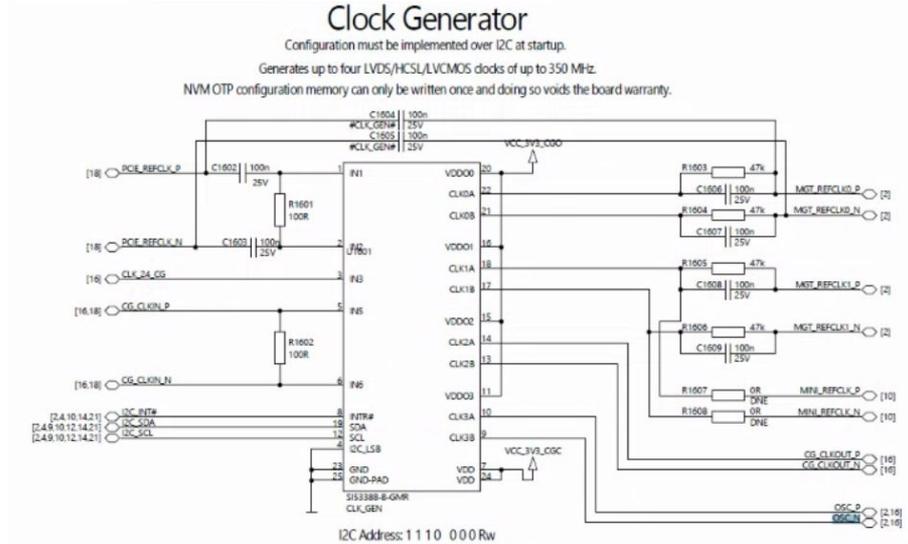
Introduction

- The Clock generator of the Enclustra board is the Si5338B
- It is an any-frequency, any-output quad clock generator
- 6 clock inputs, 4 clock outputs
- It is configurable via I2C
 - By default in Enclustra PE1 baseboard it is controlled by the system controller
 - the default values come from a NVM OTP memory (writing voids the warranty)

Clock options of Si5338B Clock generator

Inputs

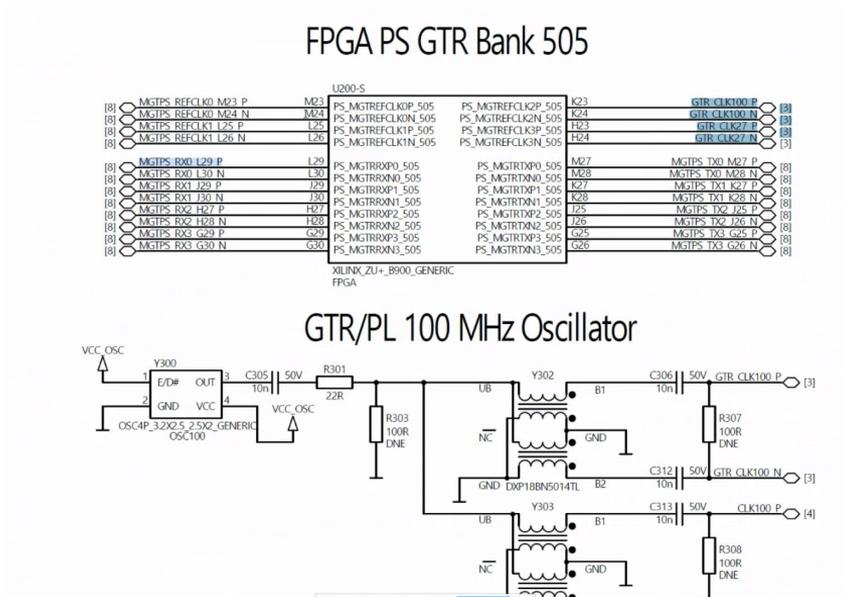
- Inputs of the Si5338B
 - Differential clock from PCIe (not to be used)
 - The board has an on-board 24MHz oscillator, the output of the oscillator passes through a multistage buffer and then fed to Si5338B chip.
 - SMA to feed a differential clock*



*Input SMA connectors shall be populated in that case

Mercury+ XU8

- We also have PS transceiver GTR
 - Connects to PCIe
 - Bank 505
 - GTR/PL 100MHz Oscillator
 - GTR can also take 27MHz (other on board oscillator)



Clocking for GTH transceivers on Mercury module

- The useful MGT ref clocks for us on the Mercury+ XU-8 SoM are those that correspond to MGT_BD_RECLK0 on carrier (Pins: D9/D10 of the Zynq)
 - The clock ends up to Bank226 of the SoC
- So we can use bank 225 as well (use the north of 225 to clock bank 226). This is done automatically from vivado
- So we can use 8 transceivers (2 quads)
 - Those of MGT bank C and MGT bank D
 - 225 => MGT Bank C => FMC DP0-DP3 (Follows VITA 57.1)
 - 226 => MGT Bank D => IOC/IOD on PMOD connector
- Configuration files for Enclustra EMP board
 - <https://gitlab.cern.ch/atlas-dcs-fpga-soc/emp-configuration>
 - Clocking generation file for the 320MHz clock on FMC
 - Any other clock needed?

Clocking for GTH transceivers on Mercury module

