ITS2 reports on Alpide temperature dependence

Marcel Rossewij

ITS2 reports on temperature dependence:

ITS2 plenary: ALPIDE Characterisation, December 12, 2016, Van Hoorne Jacobus Willem
- Beam: 6GeV/c pions from CERN's PS

https://indico.cern.ch/event/594132/contributions/2402073/attachments/1387191/2111427/ALPIDE_characterization_plenary_V2.pdf

9th ALICE ITS upgrade, MFT & O2 Asian Workshop, 26 Jun 2017, Jonghan Park
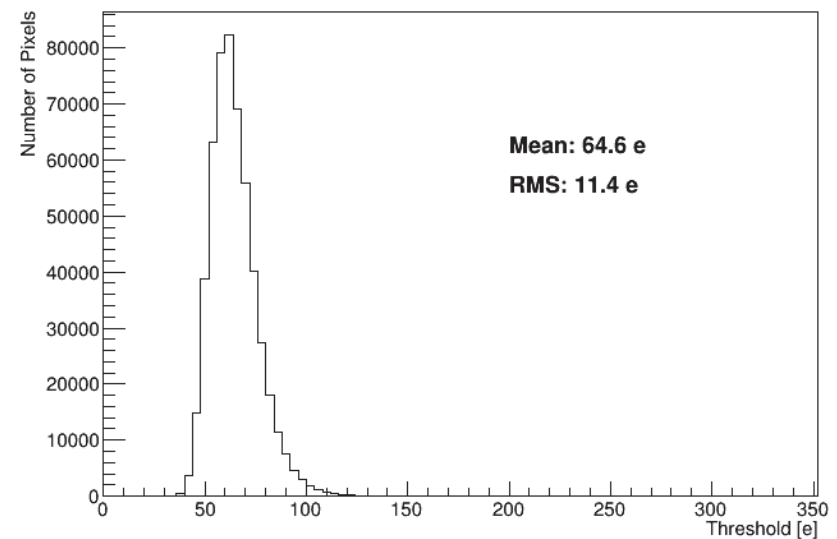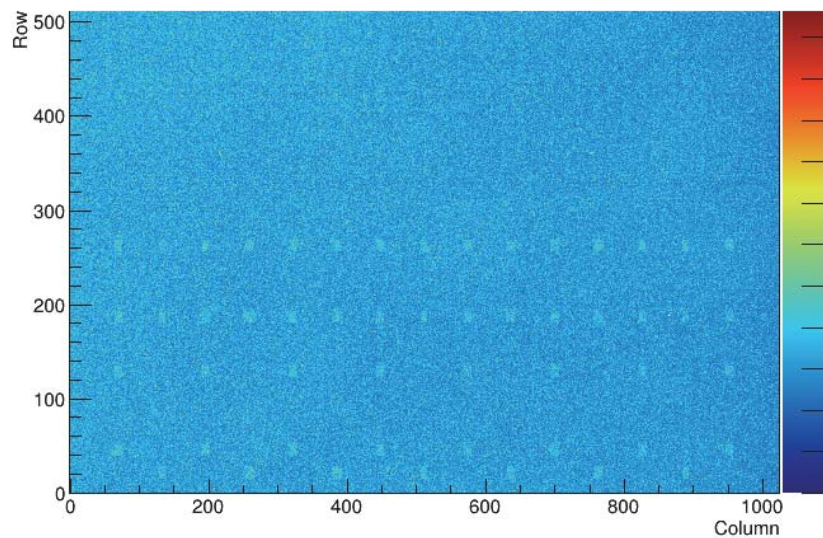- Irradiated by ^{55}FE source

https://indico.cern.ch/event/623985/contributions/2609732/

Threshold

2. Lab results

Thresholds obtained from s-curve scans with charge injections

- Homogeneous distribution of threshold
- Tail to higher thresholds, partially related to pixels below pads where higher thresholds are measured (related to lower injection capacitance C_{inj})
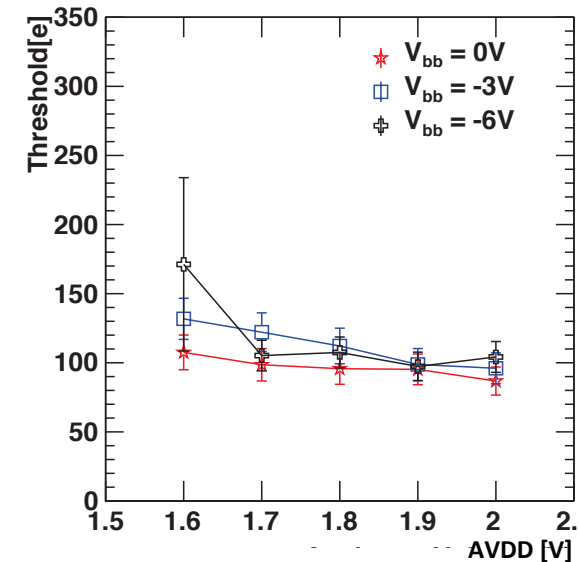
Temperature and supply voltage
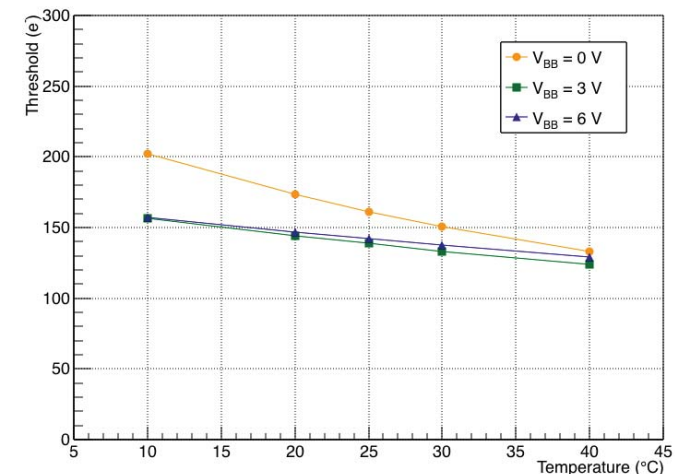
2. Lab results

Supply voltage:

- Slope of voltage and current DACs outputs changes linearly with analog supply voltage

- Similar threshold and noise values at all supply voltages if DACs are adjusted such that output currents and voltages match the original values at 1.8 V

Temperature:

- Voltage DACs independent of temperature, current DAC output increases slightly with temperature

- Threshold decreases slightly with increasing temperature; effect less pronounced with back bias

- Noise increases slightly with temperature; without back bias by ~1 e going from 10° to 40° C, much less with back bias

Threshold as function of supply voltage (top) and temperature (bottom) for different values of back bias
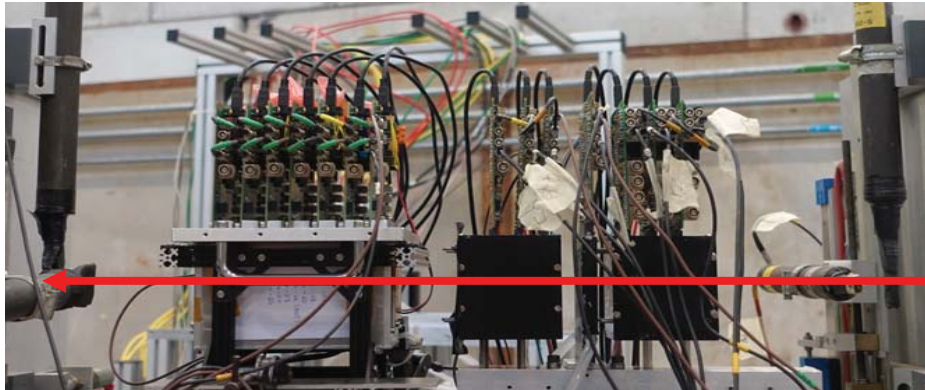
Test beam measurements

4. Test beam results

Telescope 1   Telescope 2


Beam: 6GeV/c pions from CERN's PS

- Simultaneous operation of two telescopes with 3+3 reference planes, one fully equipped with ALPIDE chips
- More than 10 chips measured:
    - Non-irradiated, NIEL, NIEL+TID
- Studied performance in terms of:
    - Detection efficiency
    - Position resolution
    - Cluster sizes and shapes

- Also performed corresponding laboratory measurements
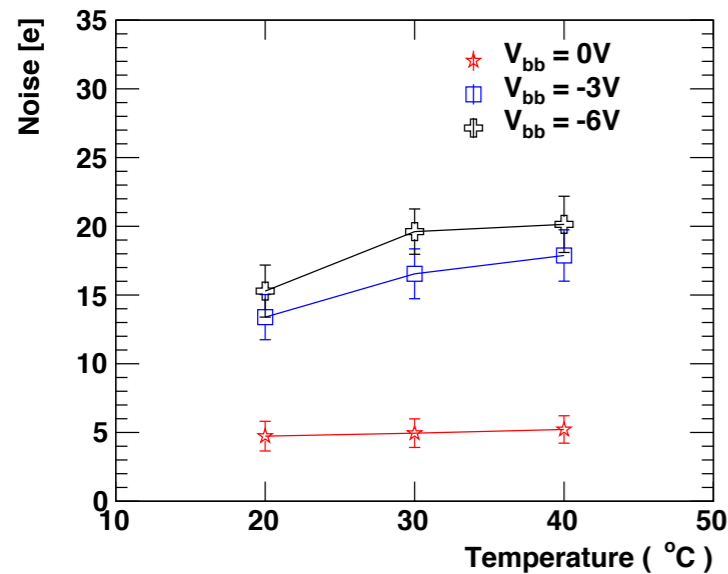   - Fake-hit rate
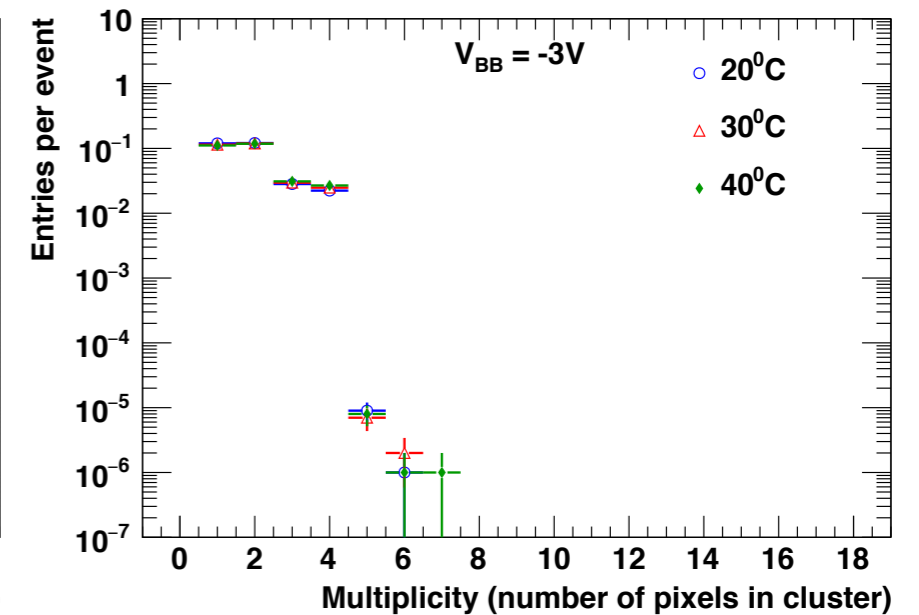   - Threshold (s-curve scan)

Temperature Dependence

4. Test beam results

Position resolution and average luster size
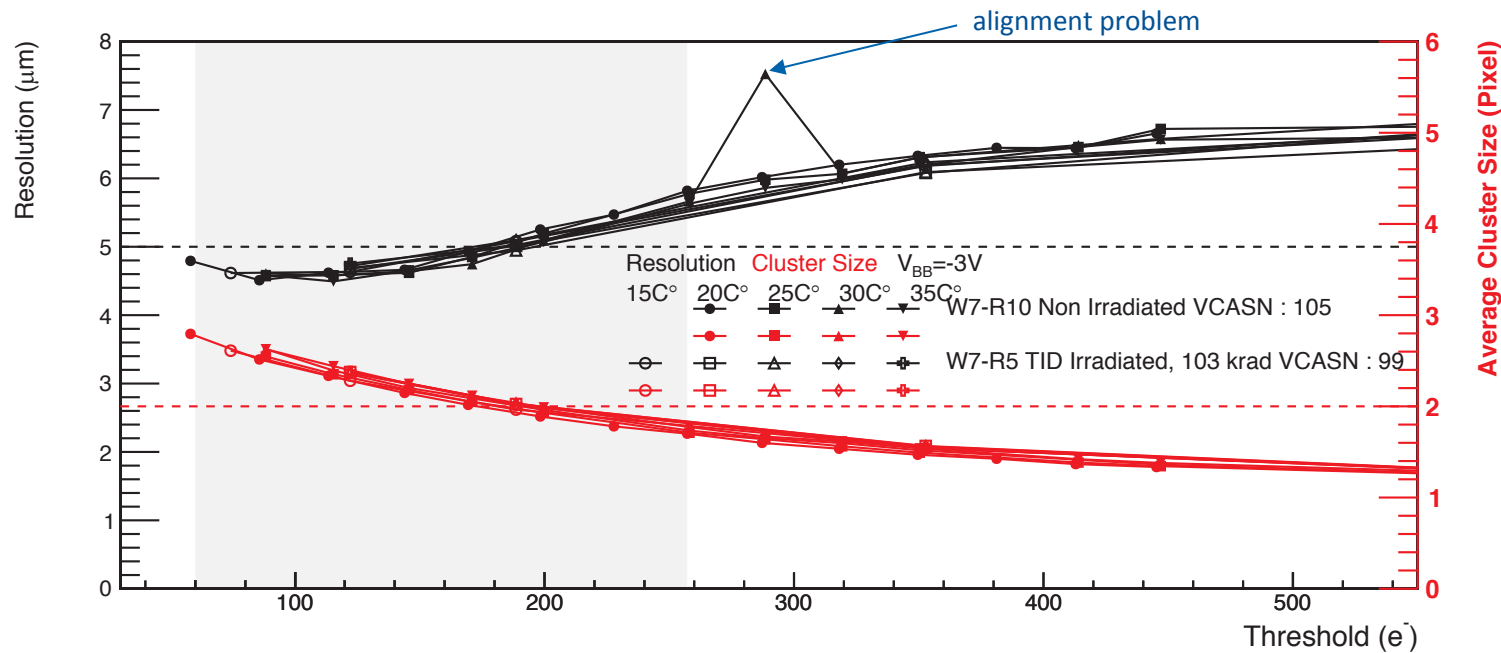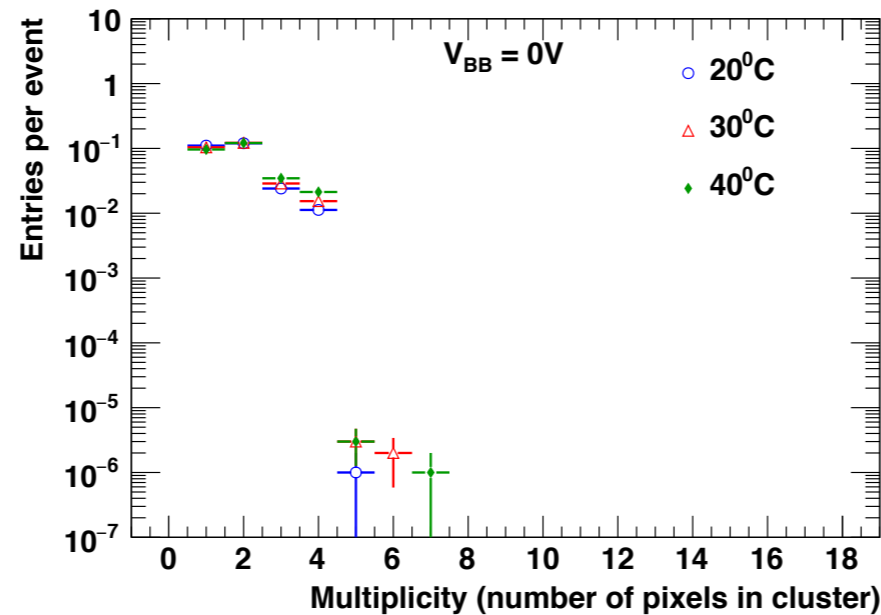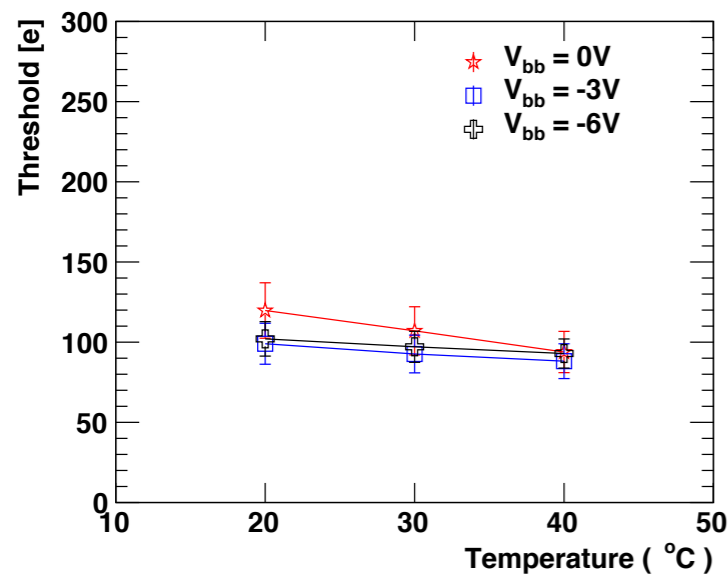

- No significant temperature dependence from 15˚C to 35˚C
- Same picture for a non-irradiated and a TID/NIEL chip

Temperature dependence study

- With back-bias voltage condition, the noise values are larger than no back-bias voltage condition → due to the creation of the additional noise signal on back-bias voltage line.

Mean Cluster Size Vs layers @5 Gev (filt)
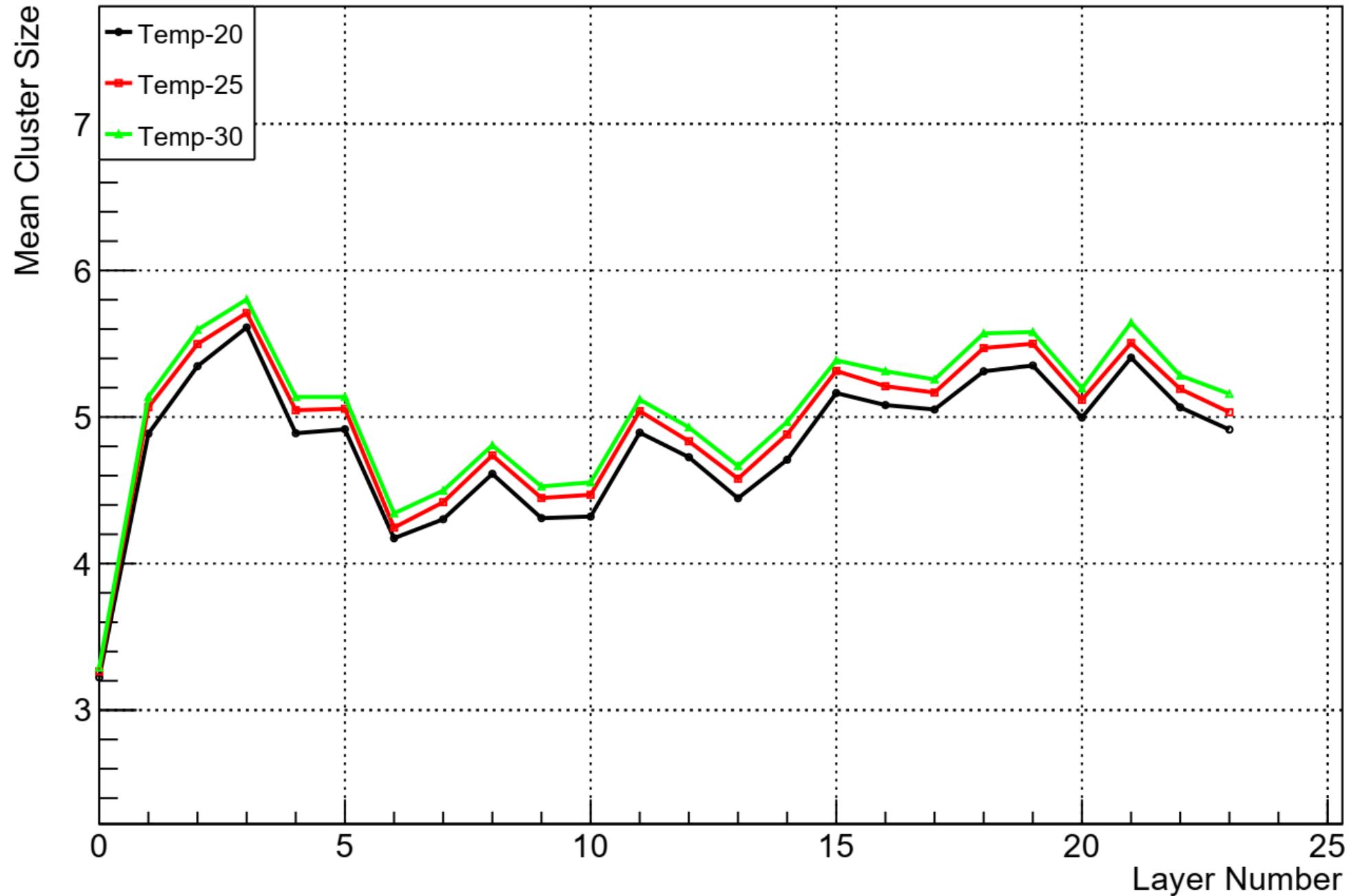
Derived conclusions

- Threshold decreases with increasing temperature

- Multiplicity shows slight increase with increasing temperature

  - More pronounced with high multiplicity events

  - Less pronounced with (-3V) back bias

ALPIDE Characterization – Pixel Matrix

ITS plenary meeting

December 12th 2016

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Table of Contents

Table of Contents

Characterization overview

1. Introduction

ALPIDE wafers produced: Two lots: T608519 ('first lot') and
T608520 ('second lot')

- in total 27 wafers (48 dies per wafer), delivered mid and
end of August, respectively

Chips on carriers from begin September, first test beam
mid September

Characterization of pixel matrix:

- Threshold and noise, pulse shape, fake-hit rate

- Detection efficiency, position resolution, cluster sizes

for different:

- Temperatures

- Supply voltages

- Reverse substrate bias (VBB)

- Readout modes: triggered and continuous

- Radiation levels: NIEL and TID

Table of Contents

Threshold

2. Lab results

Thresholds obtained from s-curve scans with charge injections

- Homogeneous distribution of threshold
- Tail to higher thresholds, partially related to pixels below pads where higher thresholds are measured (related to lower injection capacitance C_{inj})
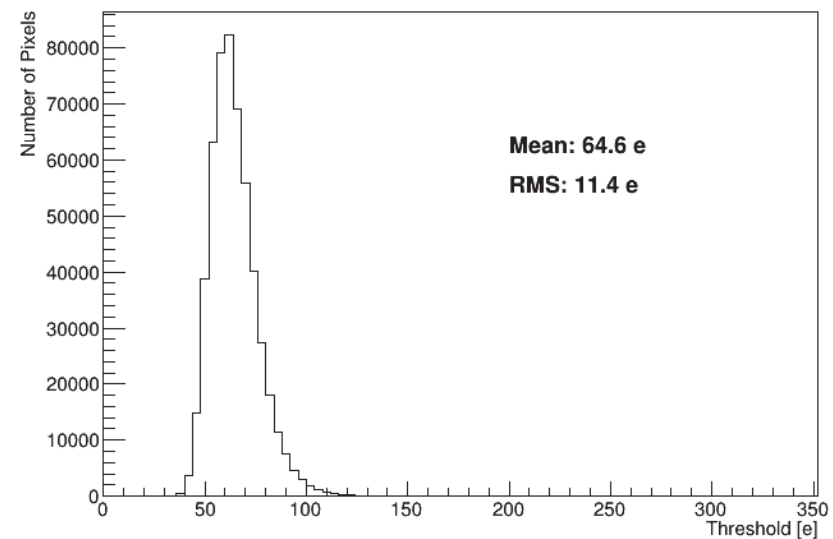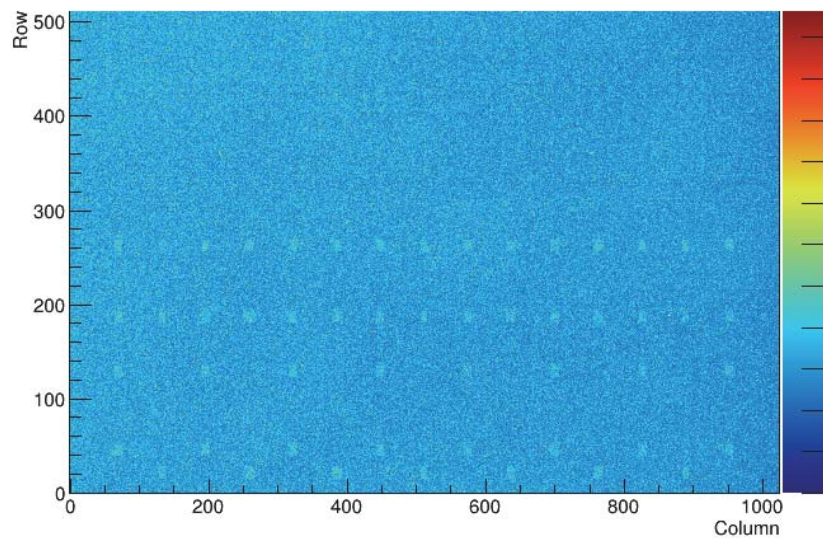
Threshold settings

2. Lab results

Threshold setting

- Threshold can be adjusted over a wide range via ITHR: nearly linear dependence
- Second handle VCASN: higher VCASN leads to lower threshold, dependency not linear

Very similar results for back bias of -3 V, with adjusted VCASN
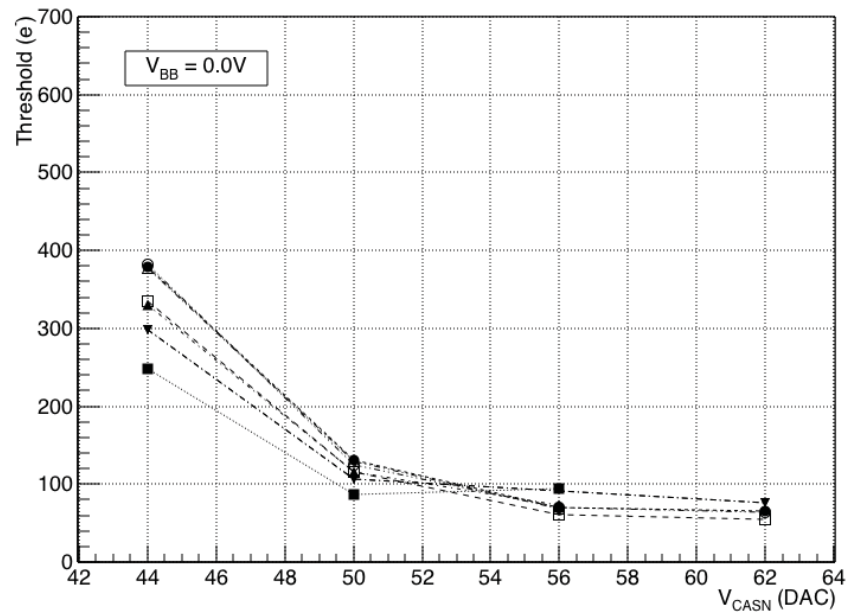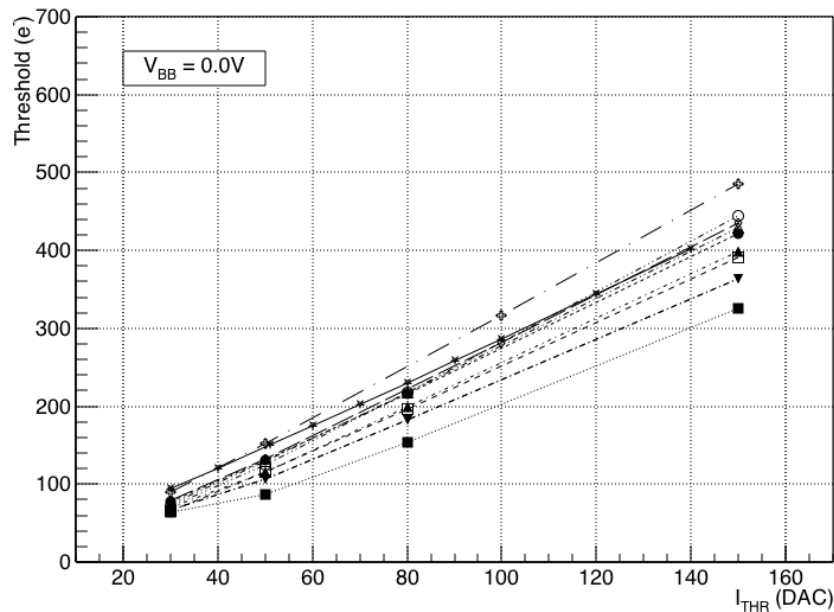
Plots show curves for sample of tested chips

Threshold RMS and noise

2. Lab results

RMS of threshold distribution – pixel-to-pixel variation of threshold

- Threshold RMS typically ~10% of average threshold, higher (15%) at low thresholds

Noise obtained form s-curve scans with charge injections

- Without back bias 5 – 6 e, with back bias 2 – 3 e
- Increase with ITHR can be explained with contribution of ITHR itself

Temperature and supply voltage

2. Lab results

Supply voltage:

- Slope of voltage and current DACs outputs changes linearly with analog supply voltage
- Similar threshold and noise values at all supply voltages if DACs are adjusted such that output currents and voltages match the original values at 1.8 V
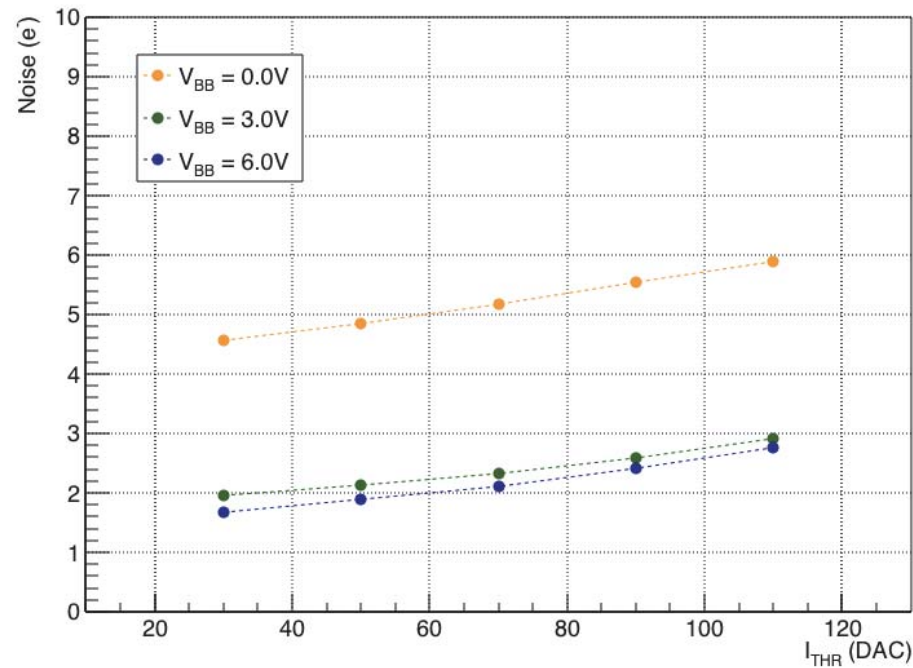
Temperature:

- Voltage DACs independent of temperature, current DAC output increases slightly with temperature
- Threshold decreases slightly with increasing temperature; effect less pronounced with back bias
- Noise increases slightly with temperature; without back bias by ~1 e going from $10°$ to $40°$ C, much less with back bias

Threshold as function of supply voltage (top) and temperature (bottom) for different values of back bias

Fake-hit rate

2. Lab results

Fake-hit rate from data taking with triggerend readout (random triggers)

- Measurements exhibit very low fake-hit rate, concentrated in only a few noisy pixels

- Even better picture for back bias voltage of -3 V
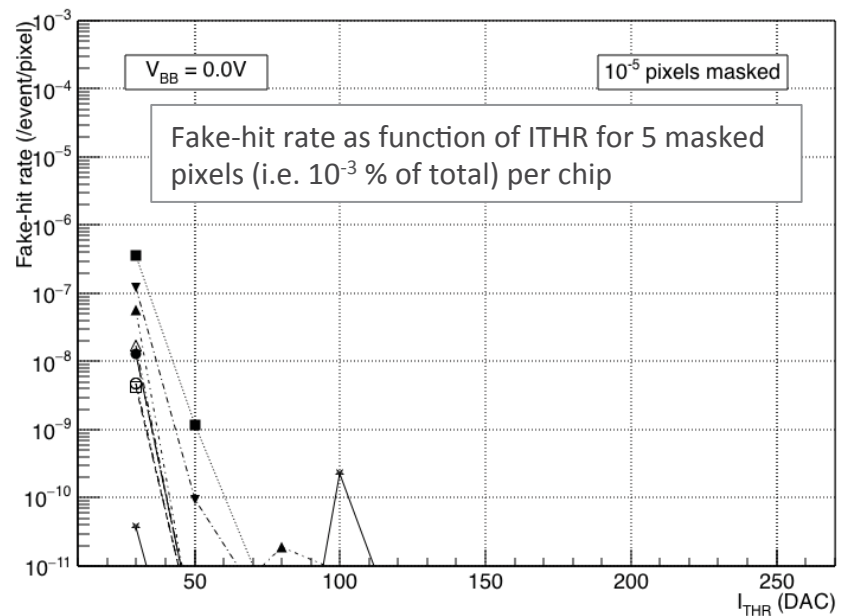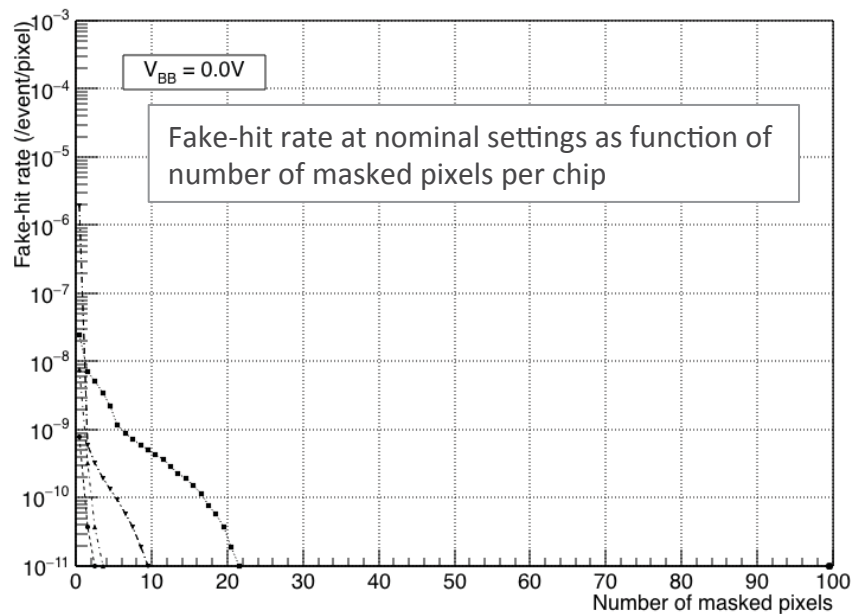
Plots show curves for sample of tested chips

Similar results obtained in measurements with continous readout with trigger rate between 20kHz and 1MHz

Pulse shape

2. Lab results

Pulse shape measurements with charge injections

- Pulse shape is measured by moving the timing of the narrow strobe (trigger) window w.r.t. the time of the charge injection ("strobe delay")
- Values extracted from 2D-measurement of injected charge vs. trigger timing: time over threshold (ToT), maximum pulse length, time walk
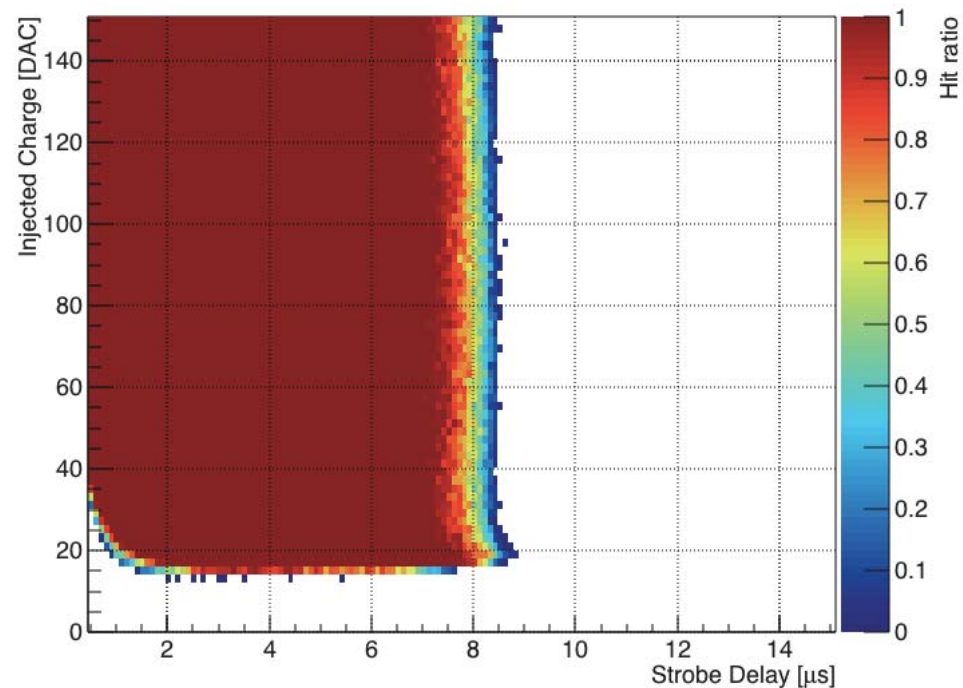
Measurement result for pulse shape for single pixel

Pulse length

2. Lab results

Measurement of Time over Threshold (ToT)

- Time over threshold nearly constant as a function of injected charge
- Very similar behavior without and with back bias of -3V

Maximum pulse length vs. ITHR

- Maximum pulse length increases slightly for decreasing ITHR (almost independent of VCASN)
- For shorter pulse lengths VCASN can be used to lower the threshold

Event time resolution determined by time walk

- Maximum time walk (for charges just above threshold) is about half of maximum pulse length
- Time walk drops quickly from maximum value, reduced by about half for charges of about 50e[-] above threshold
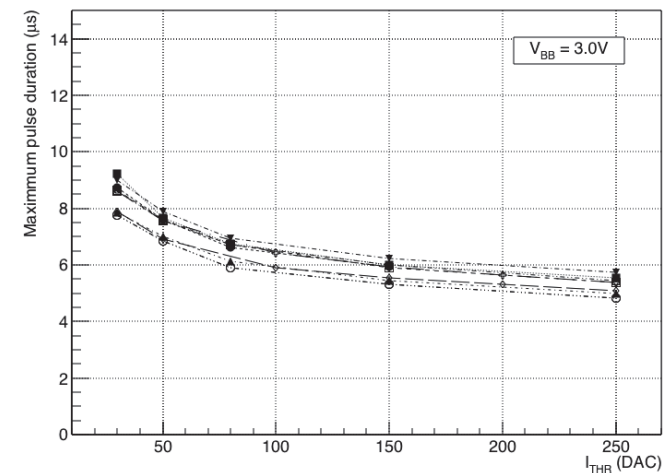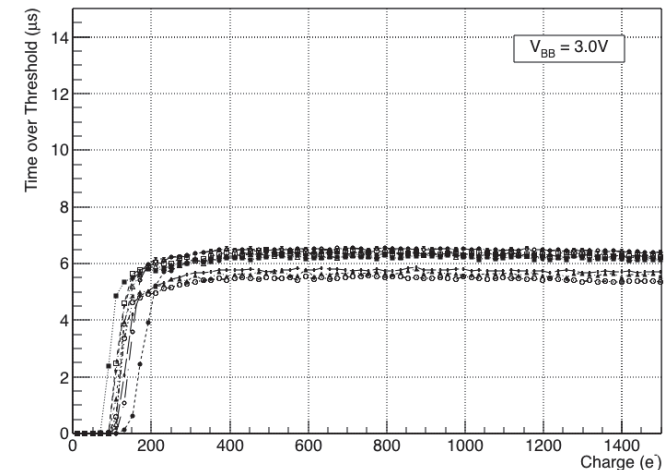
Plots show curves for sample of tested chips

Table of Contents

TID

3. Irradiation studies

Expected radiation levels in terms of TID over detector lifetime
- Inner Barrel (1.8% of detector surface): 273 krad at L0; maximum dose rate at L0 expected <0.1 krad/h ≈ 1.7 rad/min
- Outer Barrel (98.2% of detector surface): 10 krad at L4

Extensive test program performed on sample with >10 chips, with both protons and X-Rays, at various dose rates, going to various doses (currently up to 500 krad)
- Program started with aim to validate sufficient radiation tolerance for Outer Barrel (98.2% of detector surface), since then going to increasingly larger doses

- DACs and supply currents: at dose rates ≈20 times larger than max expected in experiment (34rad/min), no effect of TID observed up to 320krad

- Threshold: decreases with increasing dose (by about 50% at 300krad)
  - Can be efficiently readjusted by according DAC settings (VCASN, ITHR)
  - Fake-hit rate remains almost unchanged after up to 500krad with readjusted thresholds

- Timing: no significant change of the pulse shape

At doses up to 500 krad the chip remains fully functional without a degradation of peformance
- Safety factor ≥50 for Outer Barrel, factor ≥1.8 for Inner Barrel

TID - thresholds

3. Irradiation studies

Readjustment of threshold: expample for chip W8R21 (320krad)
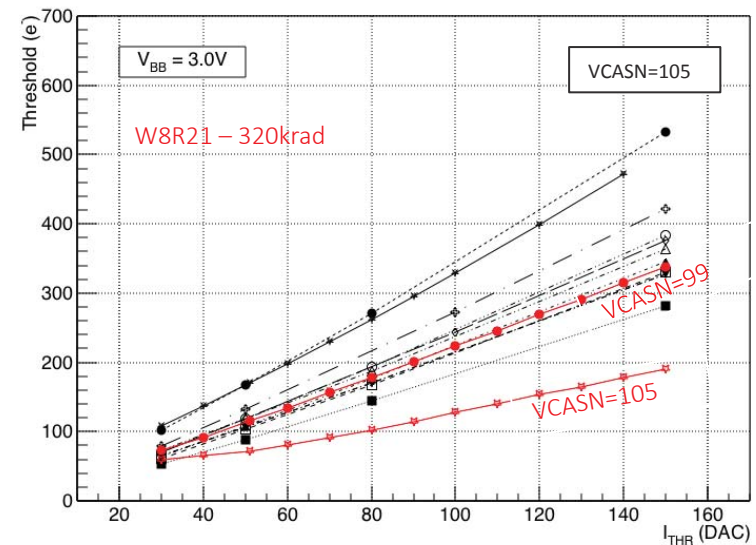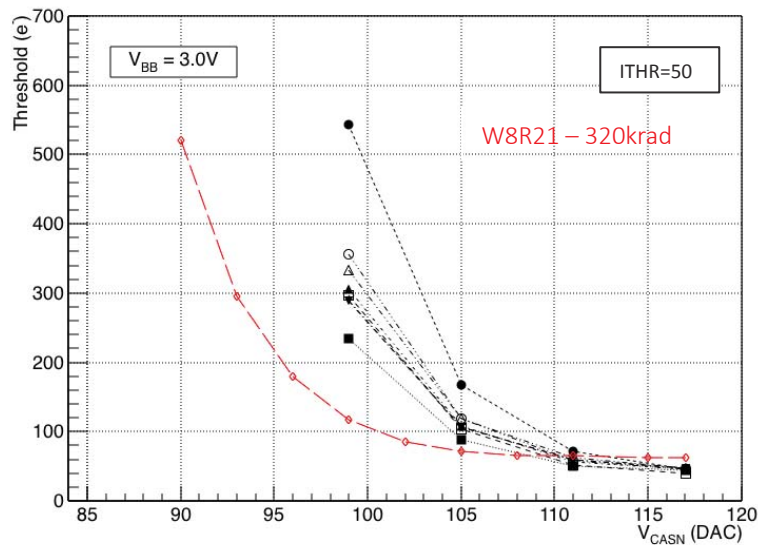
Threshold increase can best be radjusted by decreasing VCASN
- with readjusted VCASN, slope of threshold as function of ITHR is exactly the same as before irradiation

Table of Contents

Test beam measurements

4. Test beam results

Telescope 1   Telescope 2

Beam: 6GeV/c pions from CERN's PS

- Simultaneous operation of two telescopes with 3+3 reference planes, one fully equipped with ALPIDE chips
- More than 10 chips measured:
  - Non-irradiated, NIEL, NIEL+TID
- Studied performance in terms of:
  - Detection efficiency
  - Position resolution
  - Cluster sizes and shapes

- Also performed corresponding laboratory measurements
  - Fake-hit rate
  - Threshold (s-curve scan)

Measurement list

4. Test beam results

- **Operational margin**
    - Detection efficiency, fake-hit rate and position resolution as function of threshold

- **Irradiation study**
    - Large operational margin sustained after the expected lifetime

- **Reverse substrate (back) bias dependence** (0V, -1V, -2V, -3V, -4V, -5V, -6V)
    - Clear ordering with higher reverse-substrate bias leading to better performance
    - -3V sufficient for substantial improvement

- **Supply voltage study** (1.62V, 1.8V, 1.98V)
    - Same performance achievable also for +/-10% of the nominal supply voltage with adjusted DAC settings

- **Temperature dependence** (15˚C, 20˚C, 25˚C, 30˚C, 35˚C)
    - No significant dependence measured

- **Different operation modes** (triggered, continuous integration)
    - Both modes show similar performance

NIEL and TID

4. Irradiation studies

Expected radiation levels in L0 in terms of NIEL over detector lifetime: 1.7×10^{12} 1MeV n/cm^2

- Test beam results: detection efficiency and fake-hit rate
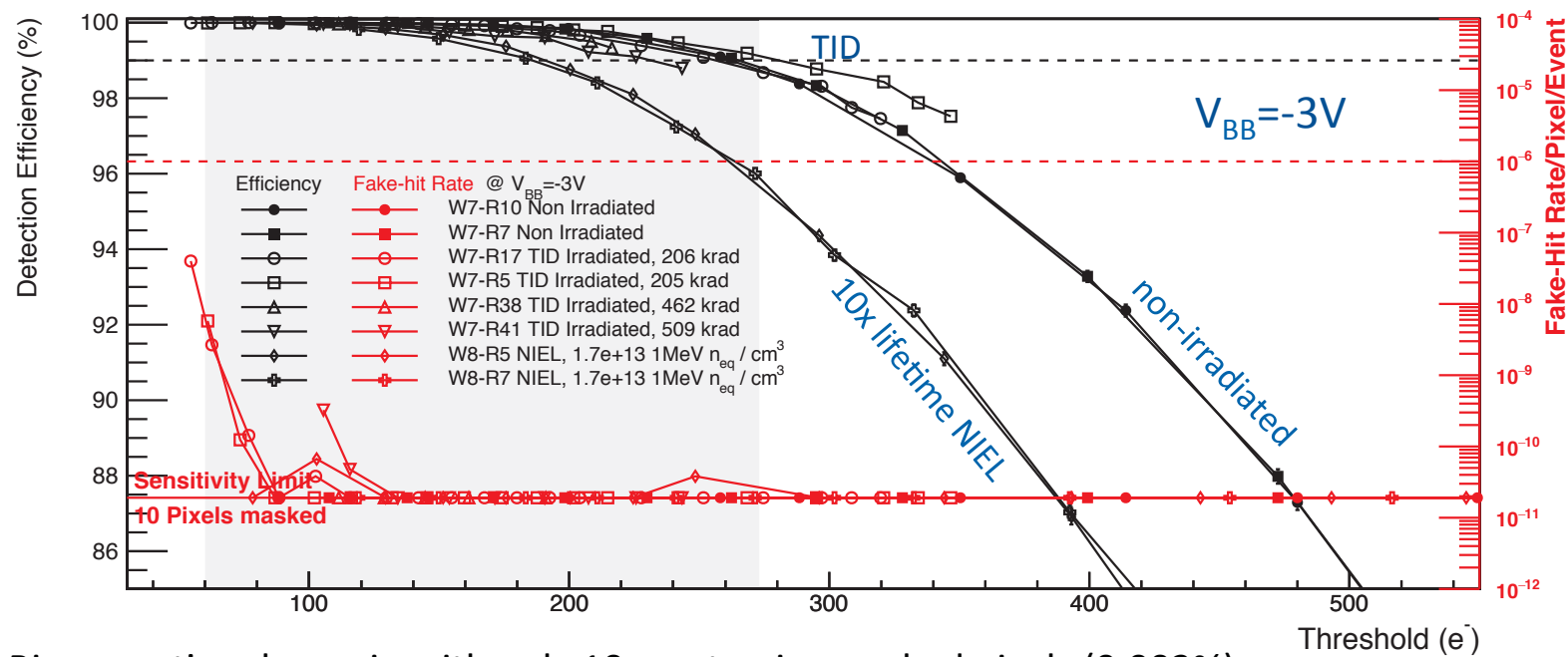
- Big operational margin with only 10 most noisy masked pixels (0.002%)
- Chip-to-chip fluctuations negligible
- Non-irradiated and TID chips show similar performance
- Sufficient operational margin after 10x lifetime NIEL dose

For proton-irradiated samples:
about 10^{12} 1MeV n/cm2 (NIEL) per 100krad (TID)

NIEL and TID

4. Irradiation studies

- Test beam results: resolution and cluster size

V_{BB}=-3V

Legend:
Resolution | Cluster Size @ V_{BB}=-3V
- W7-R10 Non Irradiated
- W7-R7 Non Irradiated
- W7-R17 TID Irradiated, 206 krad
- W7-R5 TID Irradiated, 205 krad
- W7-R38 TID Irradiated, 462 krad
- W7-R41 TID Irradiated, 509 krad
- W8-R5 NIEL, 1.7e+13 1MeV n_{eq} / cm^3
- W8-R7 NIEL, 1.7e+13 1MeV n_{eq} / cm^3

- Chip-to-chip fluctuations negligible

- Resolution of about 5µm at thresholds where detection efficiency >99%

- Non-irradiated and TID chips show similar performance

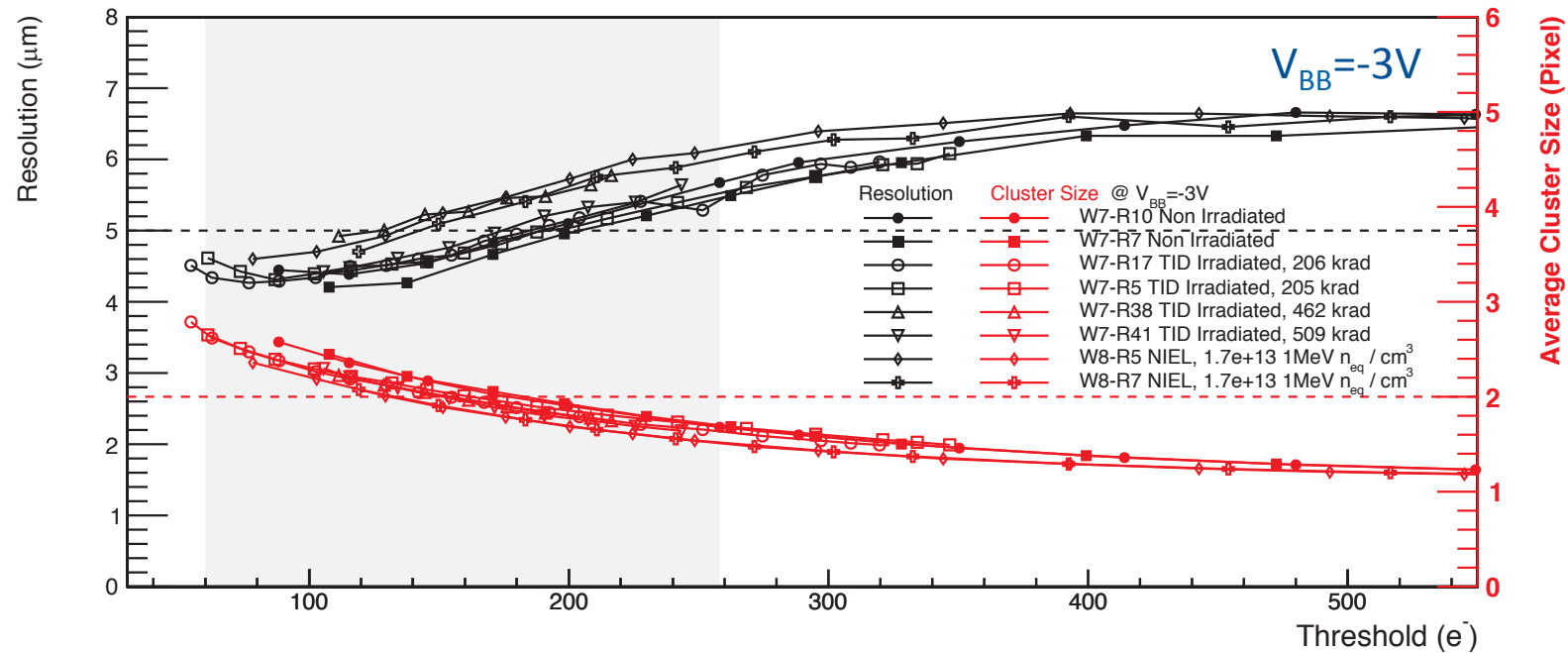- Sufficient operational margin even after 10x lifetime NIEL dose

For proton-irradiated samples: about 10^{12} 1MeV n/cm2 (NIEL) per 100krad (TID)

Reverse substrate bias dependence

4. Test beam results

Detection efficiency and fake-hit rate (non-Irradiated)
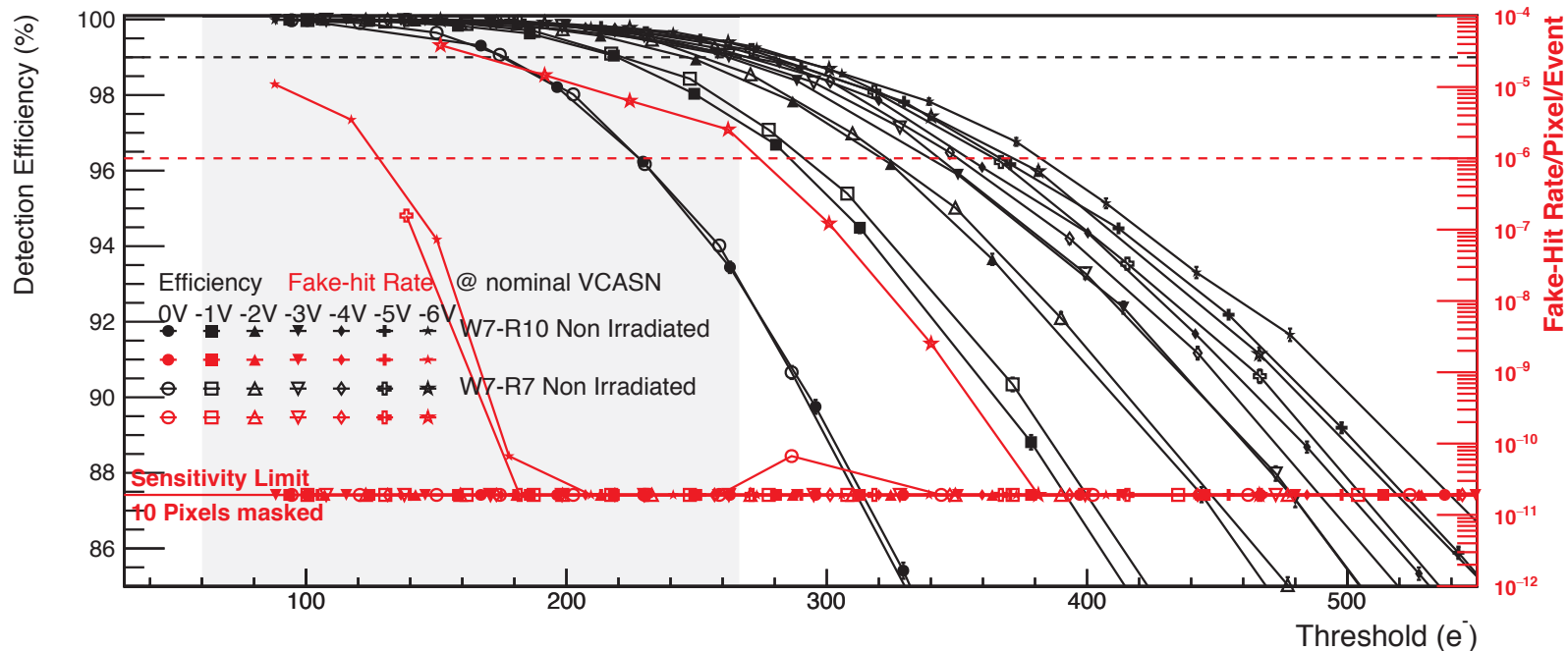
- Both chips show clear ordering with increasing performance with larger reverse substrate bias

- Already significant improvement from 0V to -1V

- Gain from -3V to -6V marginal

Reverse substrate bias dependence

4. Test beam results

Position resolution and cluster size (non-Irradiated)
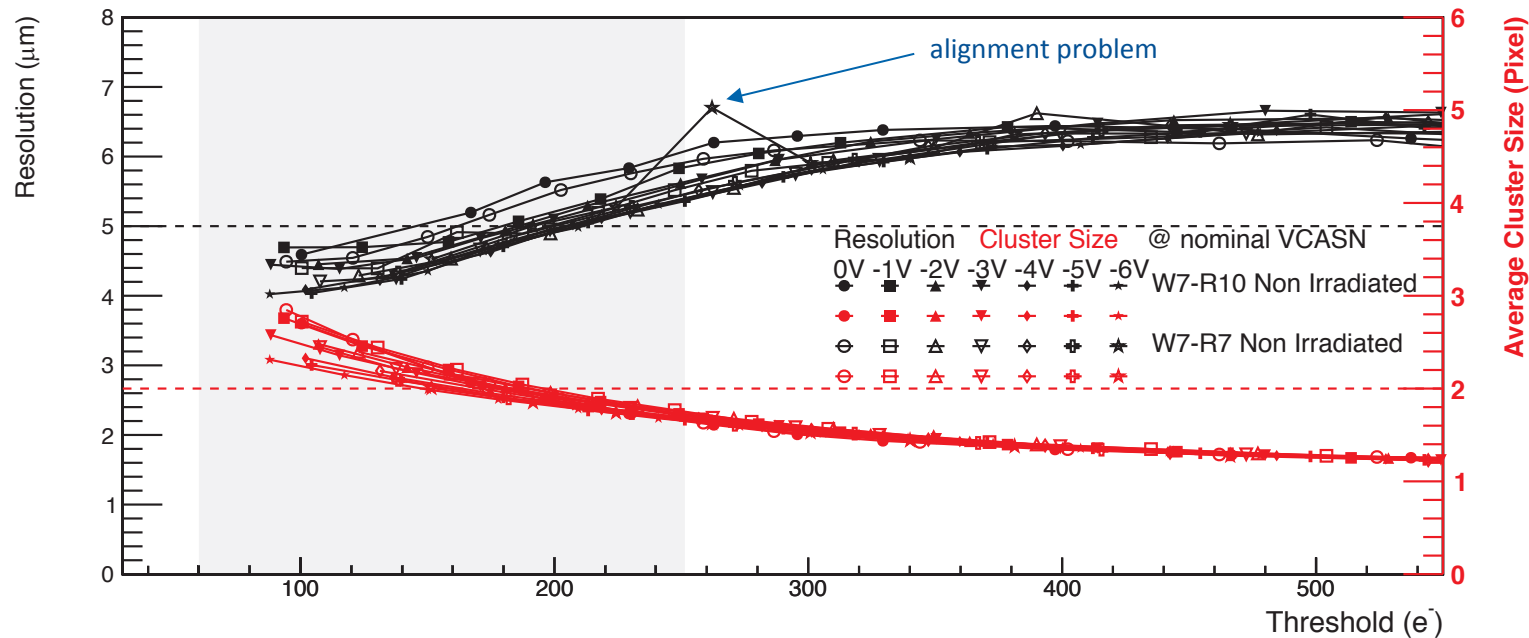
- Biggest improvement from 0V to -1V
- Little dependence of resolution and cluster size on reverse substrate bias from -2V to -6V

Temperature dependence

4. Test beam results

Detection efficiency and fake-hit rate
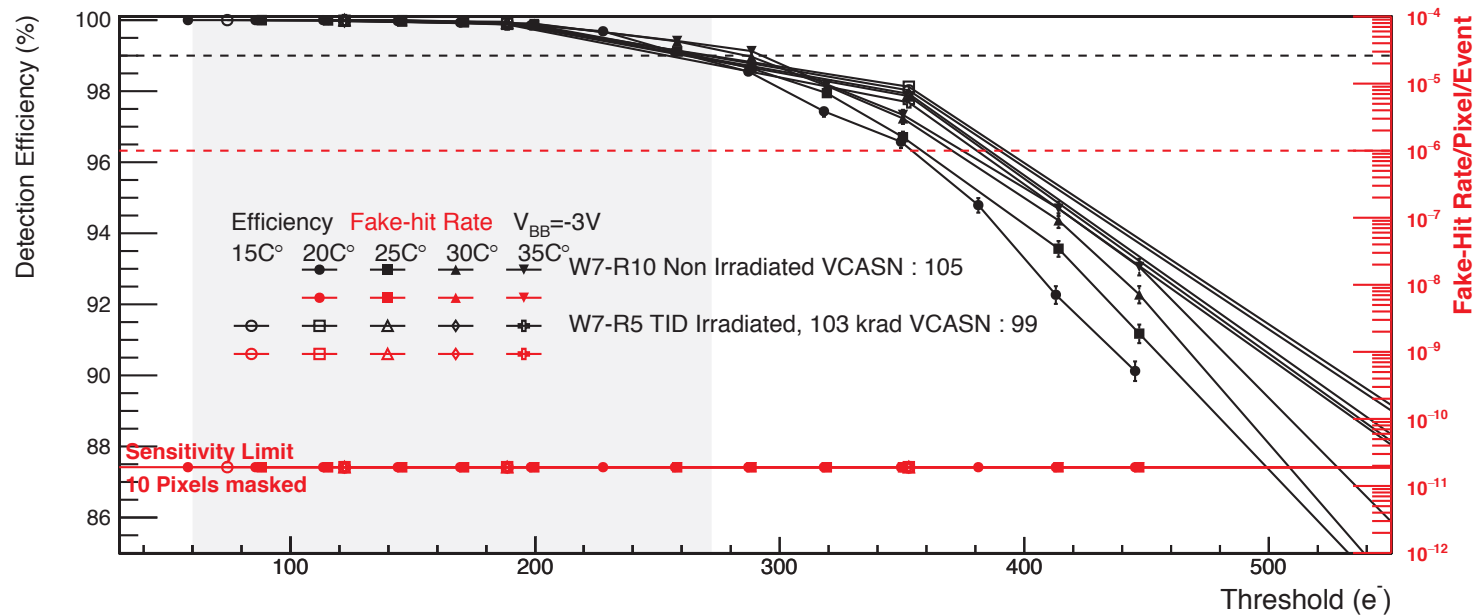
- No temperature dependence of the operational margin in the temperature range from 15˚C to 35˚C

- Same picture for a non-irradiated and a TID/NIEL chip

Temperature Dependence

4. Test beam results

Position resolution and average luster size

- No significant temperature dependence from 15°C to 35°C
- Same picture for a non-irradiated and a TID/NIEL chip

Supply voltage dependence

4. Test beam results

Detection efficiency and fake-hit rate (V_{BB}=-3V)
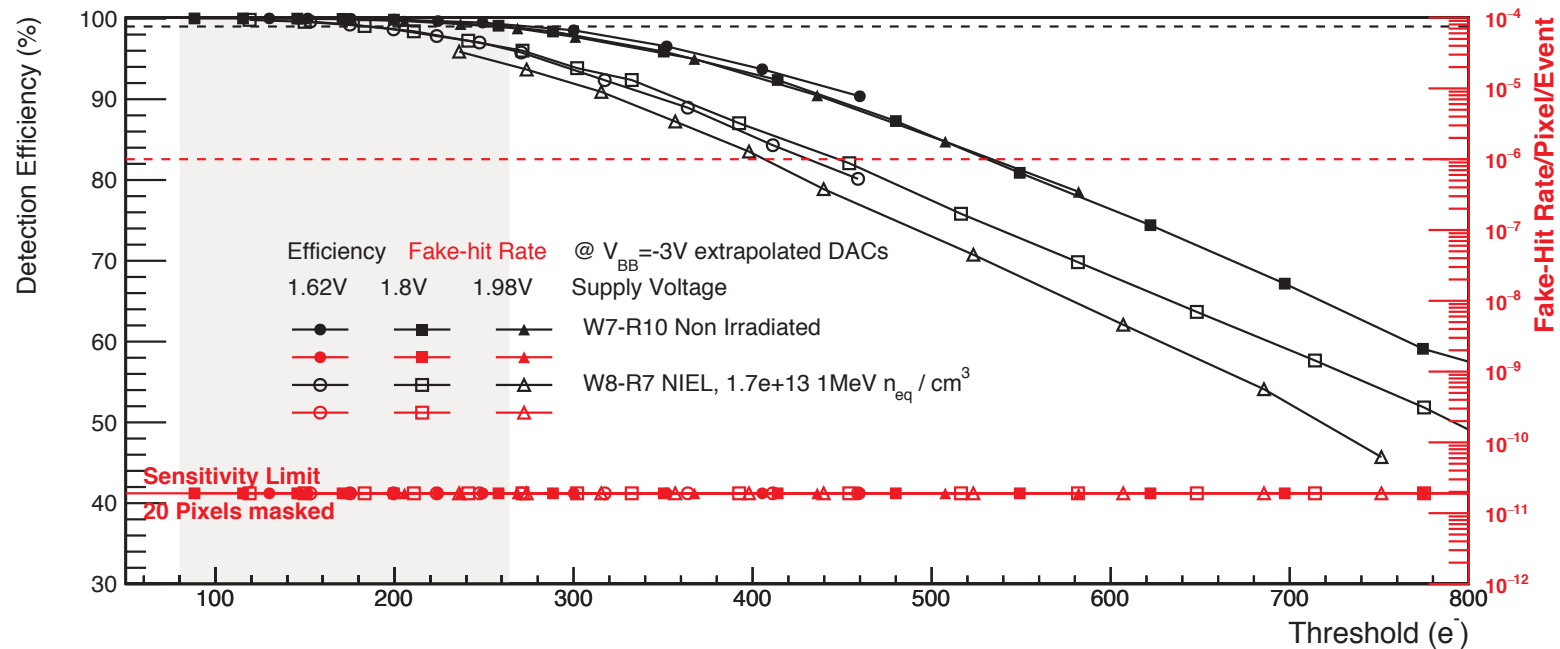
- All three voltages are superimposed → DAC settings tuning works
- Same picture for a non-irradiated and a 10x lifetime dose NIEL chip

Supply voltage dependence

4. Test beam results

Position resolution and average cluster size (V_{BB}=-3V)
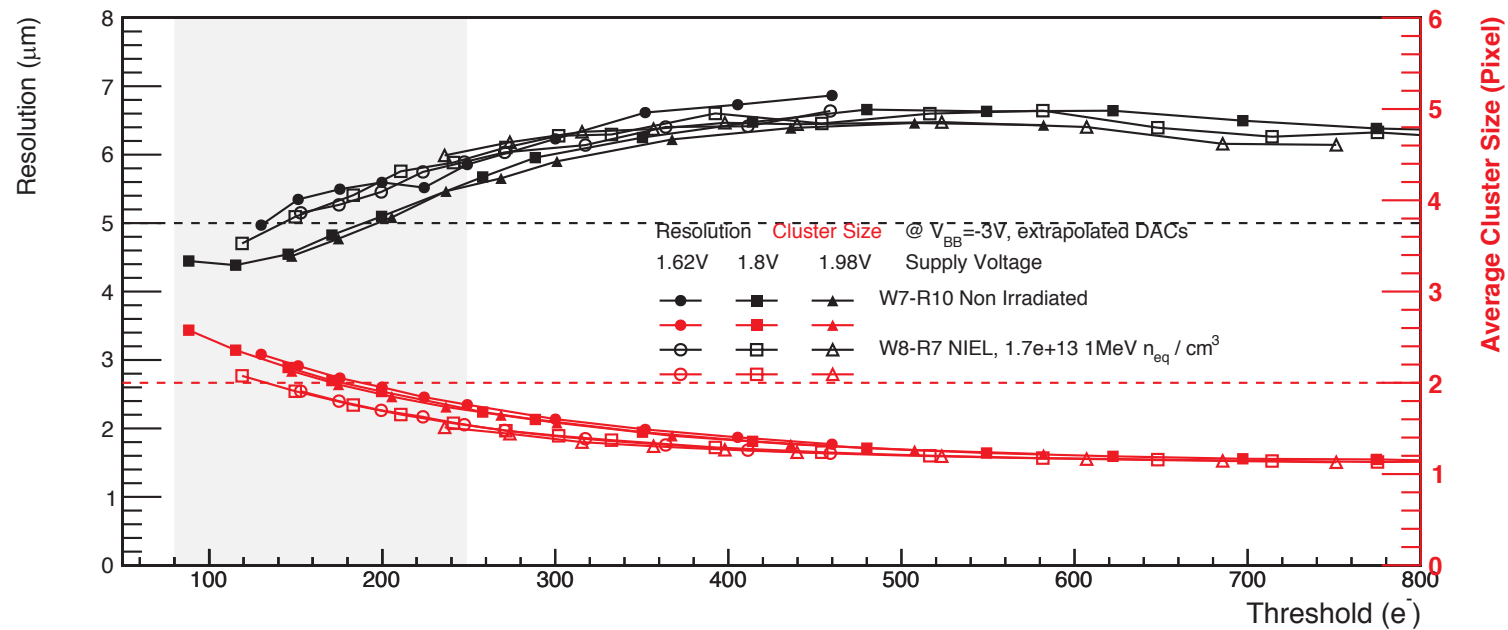
- Cluster sizes nicely matching for different supply voltages

Continuous integration

4. Test beam results

Continuous integration mode: strobe continuously asserted, only de-asserted after integration time to switch to the next in-pixel memory (250ns gap)
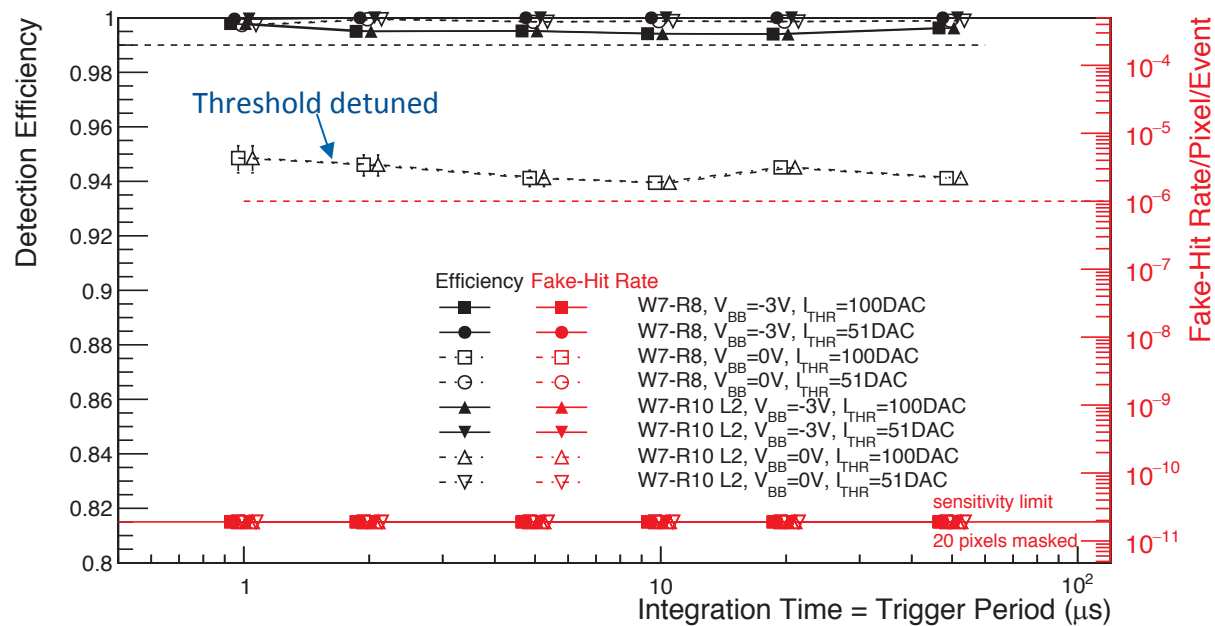
- No significant dependence on the trigger period
- Fake-hit rate rests very low also at 50μs strobe duration
- No chip-to-chip fluctuations visible
- No effect even at a deliberately detuned threshold

Table of Contents

Summary

- Thorough characterization of pixel matrix with large sample of chips under various conditions in lab and test beam, before and after irradiation, with excellent results

  - Large operational margin at V_{BB} =-3V
  - No significant reduction of the operation margin after the lifetime NIEL and TID dose
  - No significant chip-to-chip fluctuations visible
  - Chip successfully operated with +/-10% of the nominal supply voltage
  - No temperature dependence of the performance
  - Continuous integration and triggered operation possible

- Results were presented in the Production Readiness Review (PRR) held on November 25th

REFERENCE MATERIAL

Chips measured in test beam

Name	TID Dose	NIEL Dose
W7-R10	-	-
W7-R7 (2nd lot)	-	-
W7-R5	206 krad (75%)*	2.2×10^{12} 1MeV n_{eq}/cm^2 (130%)*
W7-R17	205 krad (75%)*	2.2×10^{12} 1MeV n_{eq}/cm^2 (130%)*
W7-R38	462 krad (170%)*	5.5×10^{12} 1MeV n_{eq}/cm^2 (320%)*
W7-R41	509 krad (190%)*	5.5×10^{12} 1MeV n_{eq}/cm^2 (320%)*
W8-R5	-	1.7×10^{13} 1MeV n_{eq}/cm^2 (1000%)*
W8-R7	-	1.7×10^{13} 1MeV n_{eq}/cm^2 (1000%)*

* Percentage is relative to the lifetime dose

Continuous integration

- Strobe continuously asserted, only de-asserted to switch to the next in-pixel memory (250ns gap)

- Triggering of trains of 100 consecutive events

- Tested different frequencies:
  20kHz (50μs), 50kHz (20μs), 100kHz (10μs),
  200kHz (5μs), 500kHz (2μs), 1MHz (1μs)

- Analysis peculiarities
  - Requirement of 10 previous to have the nominal time distance
  - Subtraction of all hits found in the previous 10 events
  - Merging the previous (i-1) and the following event (i+1) with the current event (i) in the DUT

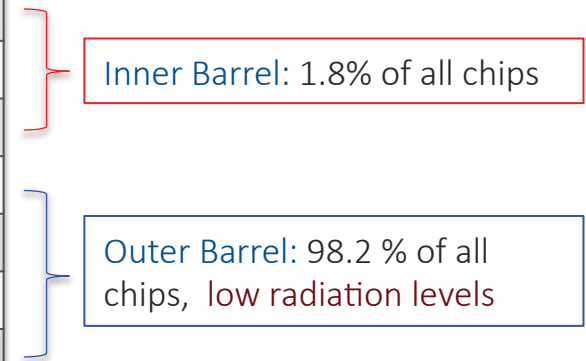| Tracking	i-10	i-9	i-8	i-7	i-6	i-5	i-4	i-3	i-2	i-1	i	i+1
DUT	i-10	i-9	i-8	i-7	i-6	i-5	i-4	i-3	i-2	i-1	i	i+1

Radiation levels in experiment

Expected radiation levels in experiment

Expected radiation levels in ALICE based on physics program after LS2:

- IP collisions: $13nb^{-1}$ Pb-Pb + $50nb^{-1}$ p-Pb + $6pb^{-1}$ pp
- Beam-gas interactions: scales with vacuum pressure

Element	Radius [cm]	TID [krad]	NIEL [1Mev n/cm^2]	Number of chips
L0	2.2	273	1.7×10^{12}	108
L1	2.8	221	1.2×10^{12}	144
L2	3.6	134	8.0×10^{11}	180
L3	20	10	1.0×10^{11}	2688
L4	22	10	1.0×10^{11}	3360
L5	41	2.4	8.3×10^{10}	8232
L6	43	2	8.1×10^{10}	9408

Inner Barrel: 1.8% of all chips

Outer Barrel: 98.2 % of all chips, low radiation levels

- For details see: *Radiation Dose and Fluence in ALICE after LS2*, W. Riegler et al., ALICE internal note (PUB-2443)

- Max dose rate at L0 expected <0.1 krad/h ≈ 1.7 rad/min

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TID-irradiated Chips

Available samples

- Samples irradiated in X-Ray machine and with 30MeV protons at NPI Cyclotron, Rez (Prague)

	Chip ID	Dose rate [krad/min]	Integrated dose [krad]	NIEL [1MeV n/cm^2]	Irradiation dates
X-Rays	W8R21	0.034	310	0	7.10 - 14.10
	W7R12	0.034	320	0	15.10 - 23.10
Protons	W7R5	1.89	100	1.1e12	23/24.9
		1.89	200	2.2e12	14/15.10
	W7R16	1.73	100	1.1e12	23/24.9
		1.73	200	2.2e12	14/15.10
	W7R17	1.92	100	1.1e12	23/24.9
		1.92	200	2.2e12	14/15.10
	W7R19	3.1	100	1.1e12	23/24.9
		3.1	200	2.2e12	14/15.10
	W7R42	3.1	100	1.1e12	23/24.9
		3.1	200	2.2e12	14/15.10
	W7R38	4.4	342	3.7e12	23/24.9
		3.9	464	4.9e12	14/15.10
	W7R41	0.7	180	3.7e12	23/24.9
		3	338		
		4.1	509	5.6e12	14/15.10
	W8R23	0.071	23.7	2.5e11	14/15.10
	W8R28	0.086	22.9	2.5e11	14/15.10

'Low' dose rate
Factor >20 larger
than for 50kHz Pb-Pb

'High' dose rate
Factor >400-2000
larger than for 50kHz
Pb-Pb

Chips irradiated in two steps:
- 100krad + 100krad
- ~340krad + ~120(170)krad

'Low' dose rate
Factor >40 larger
than for 50kHz Pb-Pb

- All samples irradiated at VBB = -3V and room temperate, also annealing at room temperature

TID

Effects on threshold

After slight increase of threshold within first 10-20krad threshold decreases gradually

- At ≈300 krad threshold is reduced by about 50%

- No effect of dose rate observed

- At room temperature, thresholds only increase again very slowly with annealing time

- Thresholds can simply be readjusted by according DAC settings (VCASN, ITHR)
  - Shown very convincingly in test beam results

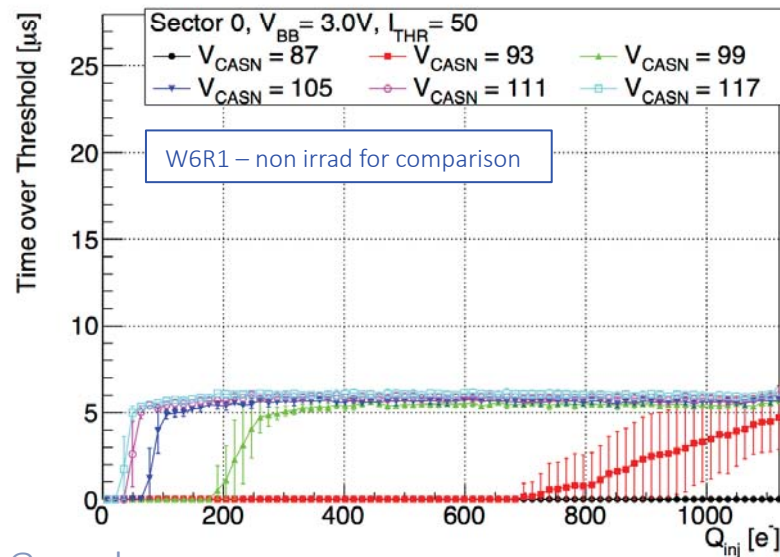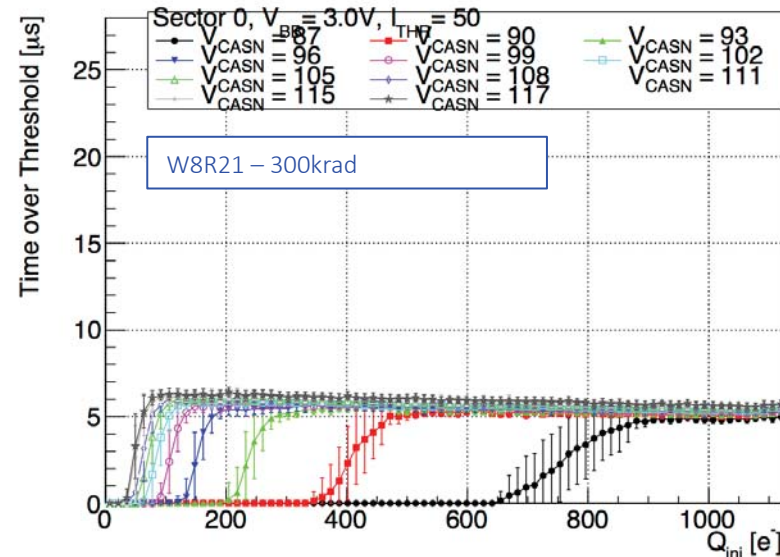Threshold and noise plotted as function of dose for various samples
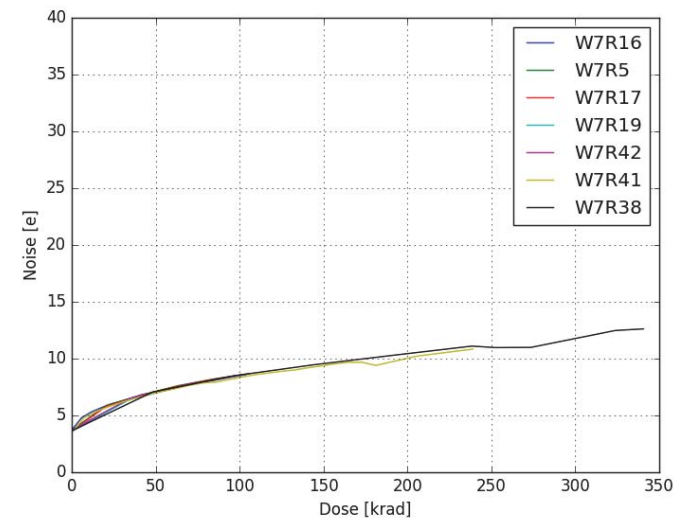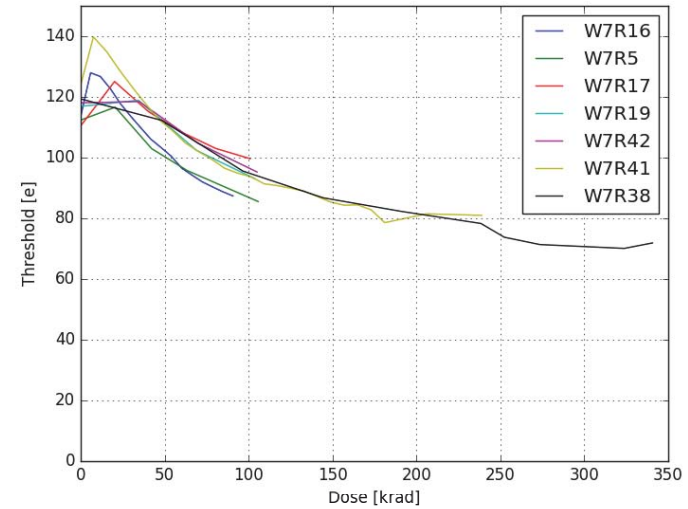
Pulse duration

Max pulse duration as function of ITHR: example of W8R21
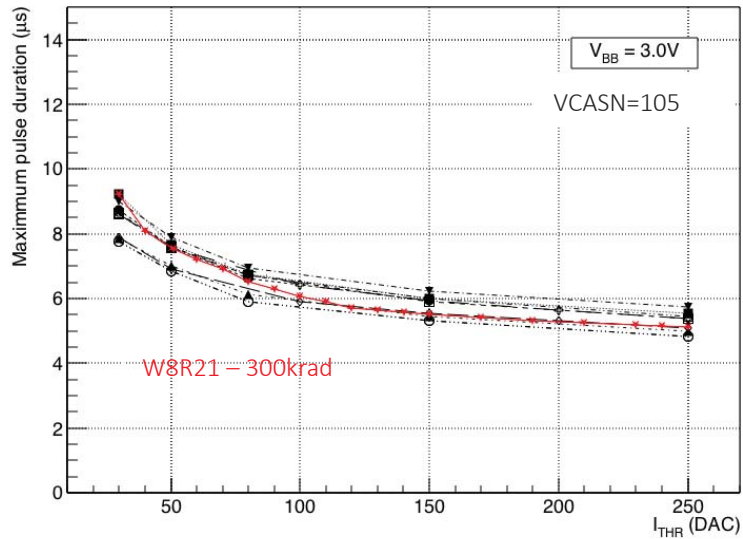
- Max pulse duration unchanged after irradiation

- ToT slightly reduced at higher values of injected charge

- Also visible in plots on the right: VCASN has no influence on ToT, only on threshold

Characterization of ALPIDE at INHA

The 9th ALICE ITS, MFT and O2 Asian Workshop

26 June 2017

Jonghan PARK
Nirbhay Kummar Behera, Hyesun Bang, Minjung Kweon*, Jinhee Yoon*

Contents

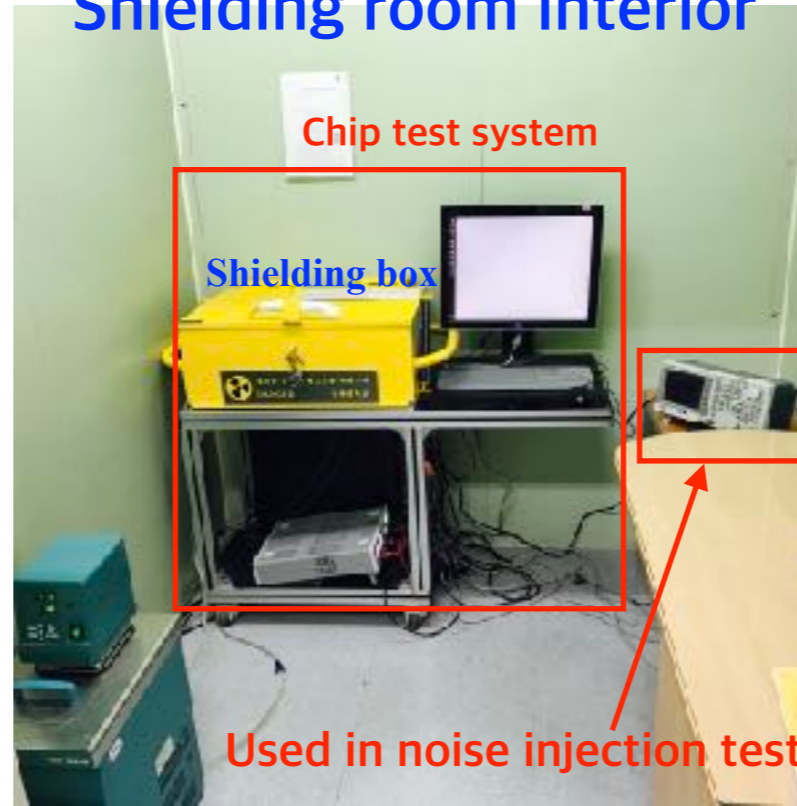- **Introduction.**

  - Chip test system at INHA.
  - Reminder of the last ITS Asian workshop.

- **Chip charaterization test for ALPIDE.**

  - Noise injection study.
  - Other activities for chip characterization test at INHA.

- **Summary and outlook**

Overall chip test system in INHA
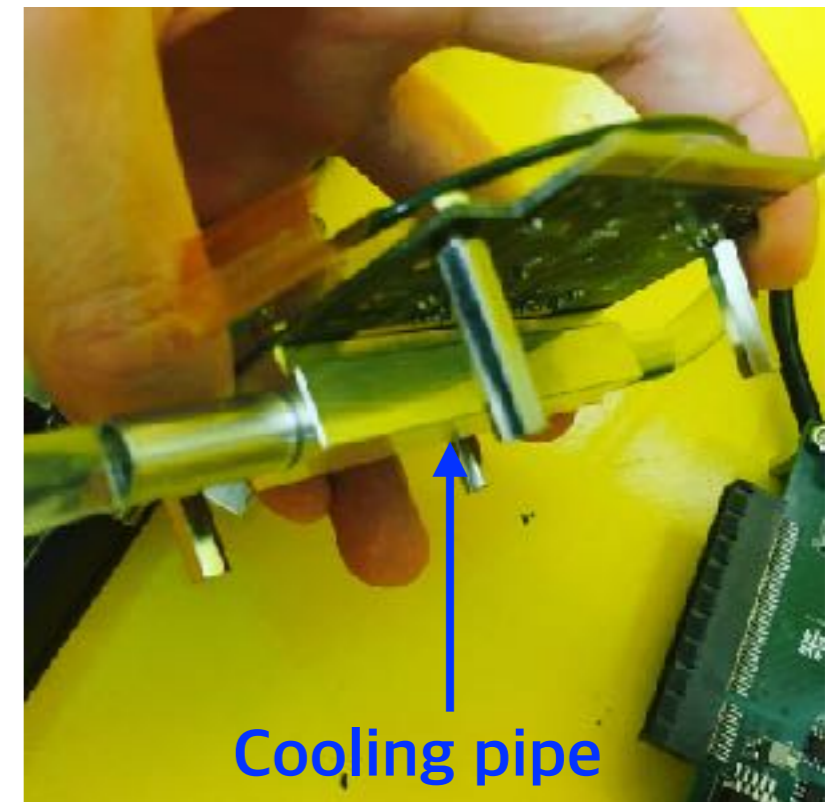
Shielding room

Shielding room interior

Chip test system

Shielding box

Used in noise injection test

Shielding box interior

Chip & DAQ borad

Cooling system

Cooling pipe

Reminder of the last workshop

Study	Test condition	VBB	Test list
Temperature dependence	20, 30, 40 ℃	0, -3, -6 V	SCANDACS, Threshold scan, Source scan using ^{55}Fe
Supply voltage dependence	Analog supply voltage 1.6, 1.7, 1.8, 1.9, 2.0 V	0, -3, -6 V	SCANDACS, Threshold scan, Source scan using ^{55}Fe

Temperature dependence study
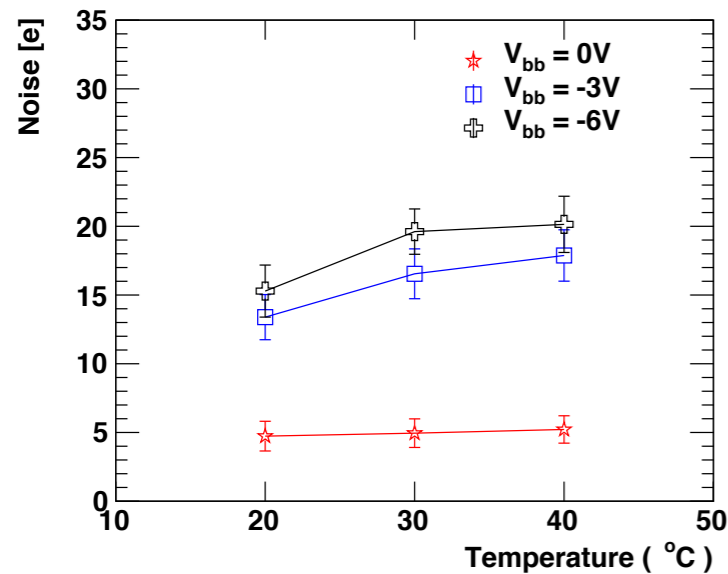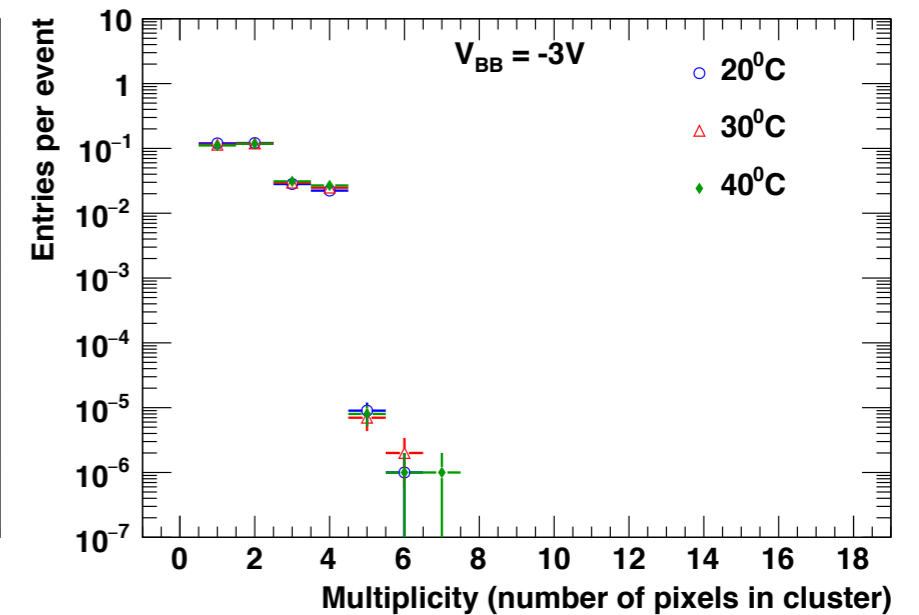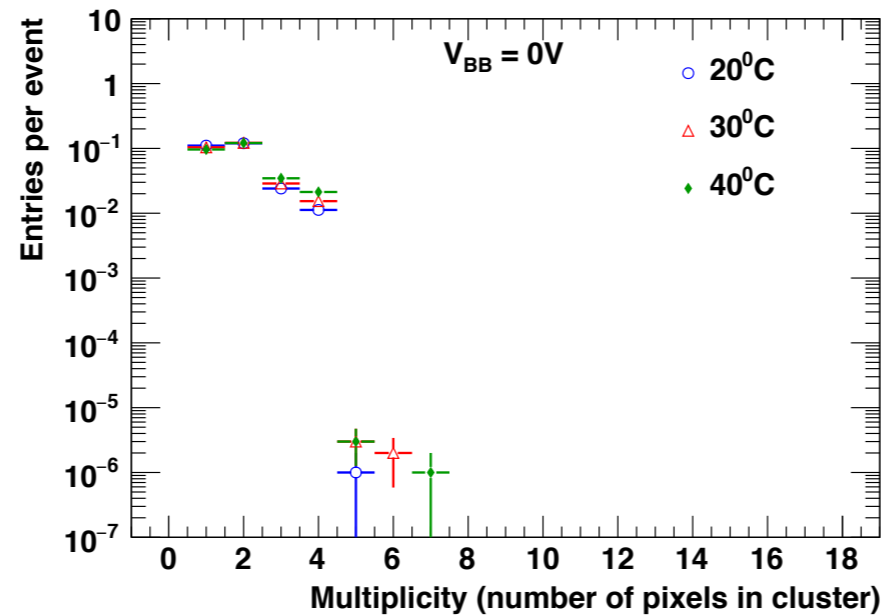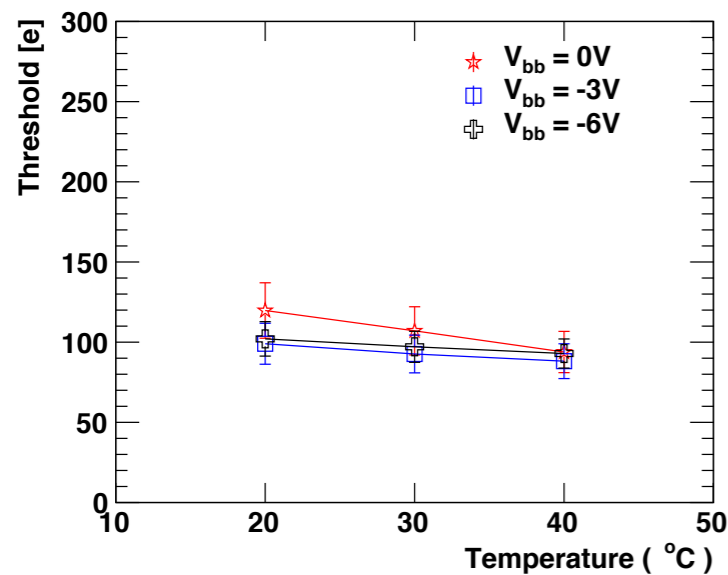
- With back-bias voltage condition, the noise values are larger than no back-bias voltage condition → due to the creation of the additional noise signal on back-bias voltage line.

Supply voltage dependence study
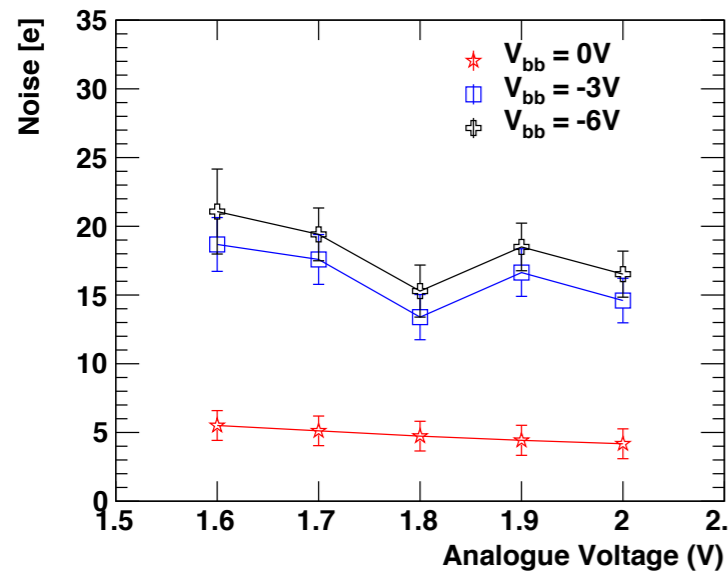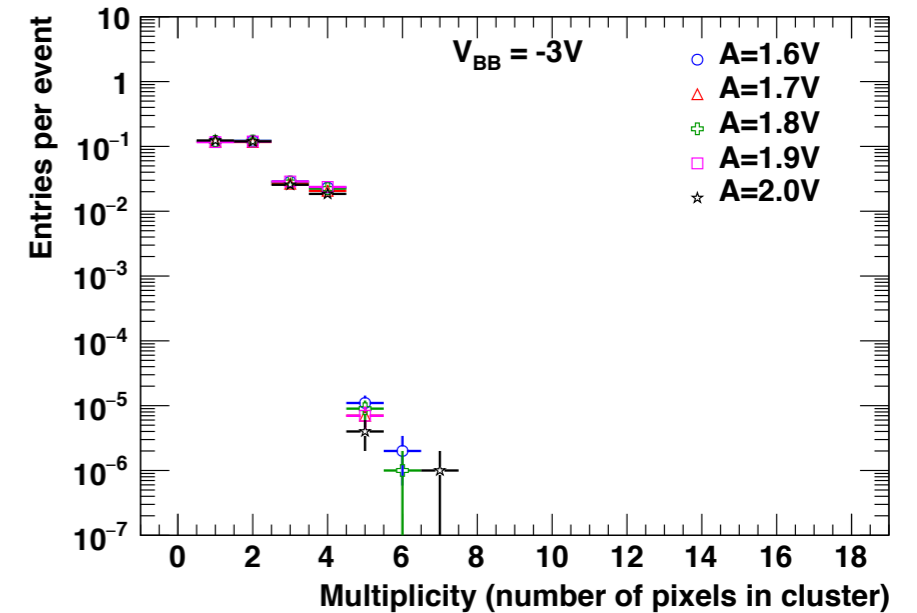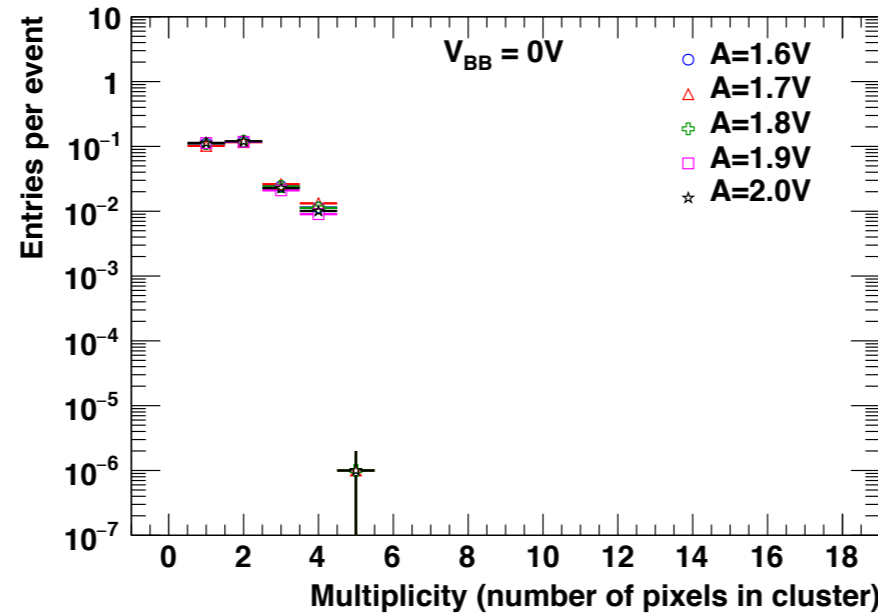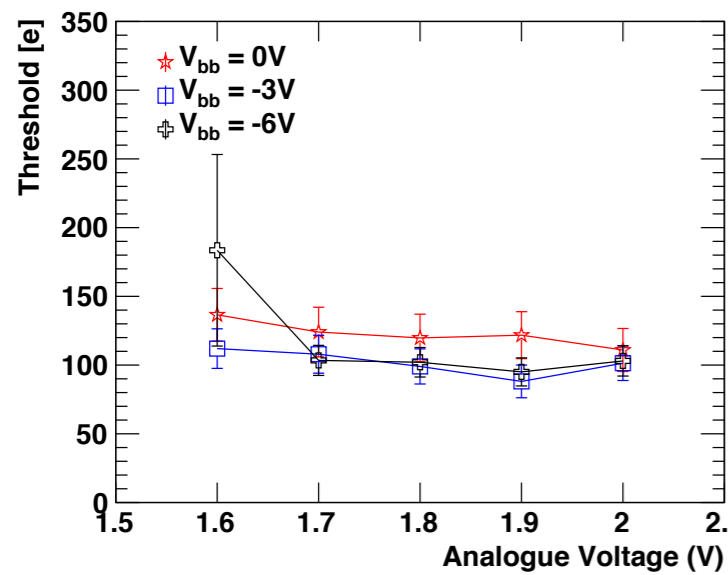
- After DAC tunning, the threshold and noise values are placed in nominal range.
    - → threshold : around 100-150[e].
    - → noise : around 5[e] without VBB.
      around 15-20[e] with VBB.

Reminder of the last workshop

| Study	Test condition	VBB	Test list
Temperature dependence	20, 30, 40 ℃	0, -3, -6 V	SCANDACS, Threshold scan, Source scan using ^{55}Fe
Supply voltage dependence	Analog supply voltage 1.6, 1.7, 1.8, 1.9, 2.0 V	0, -3, -6 V	SCANDACS, Threshold scan, Source scan using ^{55}Fe

Summary

▸ Temperature dependence study : DACs slope is slightly changed then the threshold and noise values slightly changed. However, the chip response was not changed → Cluster multiplicity is temperature independent.

▸ Supply voltage dependence study : By tunning DAC values, threshold and noise values have almost same values with default setting and all analog supply voltage conditions show almost same cluster multiplicity. Analog supply voltage variation can be mostly compensated with DAC tunning.

Chip characterization test for ALPIDE

Noise injection study

- Studied how the chip response varies with external noise signal.
- Chip test condition.

  - **Chip :** ALPIDE(W6R8, W7R14)
  - **Digital supply voltage :** 1.8V
  - **Analog supply voltage :** 1.8V
  - **Chip temperature :** 20℃
  - **Back-bias voltage :** 0V, -3V, -6V
  - **Performed test :** threshold scan
  - **Function generator :** Tectronix AFG3251
  - **External noise form :** sine wave
  - **External signal amplitude :** 200mV, 400mV, 600mV
  - **External signal frequency :** 15kHz - 400kHz
  - Noise ratio = (noise value with external signal)/(noise value without external signal)

carrier board & chip

DAQ board

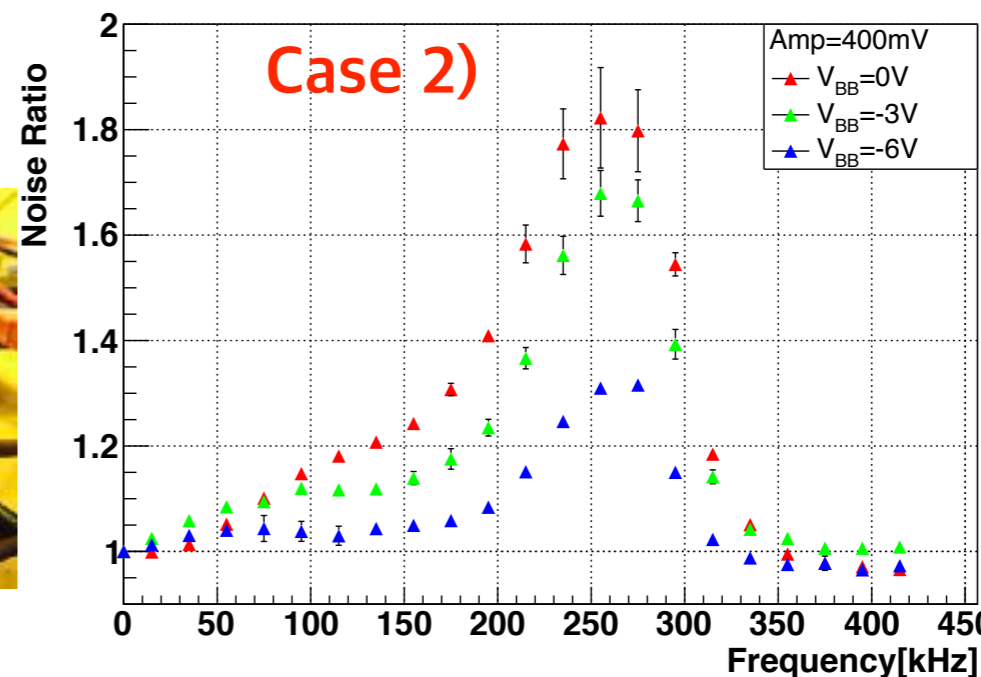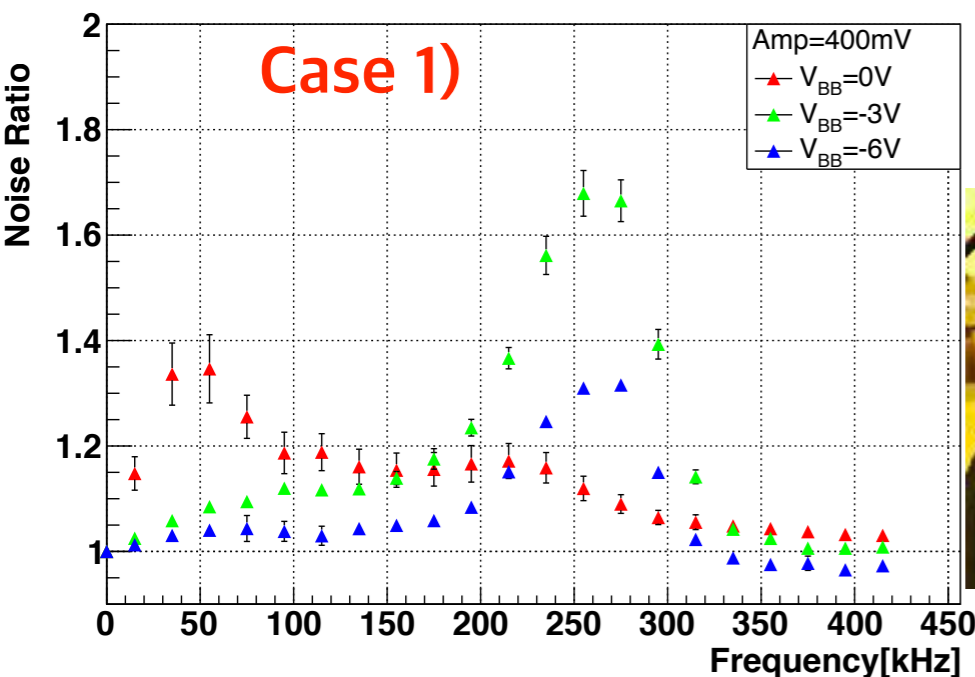# Chip characterization test for ALPIDE
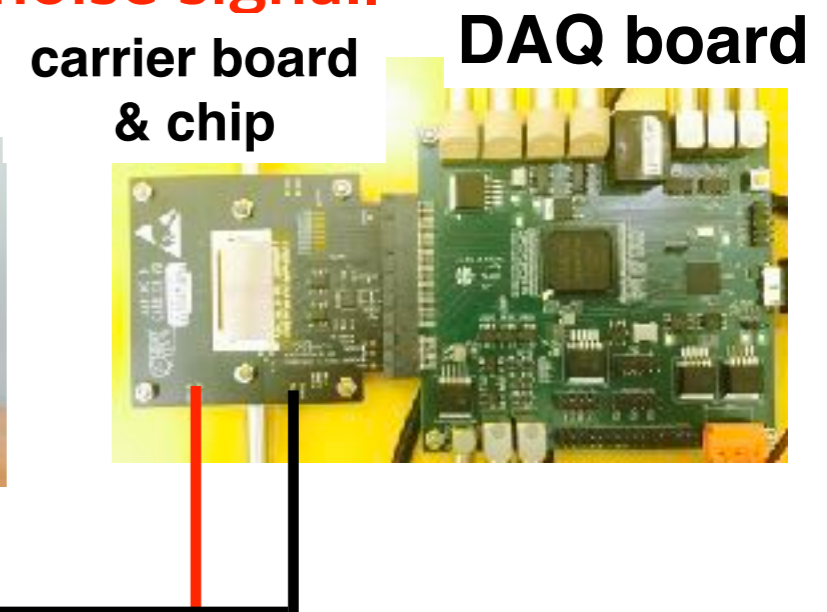
Amplitude dependence study (Noise ratio vs Frequency).

- The noise ratio is increased with increasing external signal amplitude for all back-bias voltage conditions.

- It seems the sensitive region in frequency is shifted with back-bias voltage.

Back-bias voltage dependence study (Noise ratio vs Frequency).

- Case 1) In V_{BB}=0V, connected 0Ω terminator to the back-bias voltage line.
  - It avoids the additional noise signal which is created in back-bias voltage line.
  - In this case, the sensitive region in V_{BB}=0V is around 50kHz.

- Case 2) Connected a cable which is connected to the power supply and set the power supply voltage as 0V.
  - Power supply create the current even if the V_{BB} is set to 0V.
  - In this case, the sensitive region is around 250kHz.

- The sensitive region is affected by the current which flows on back-bias voltage line from power supply.

- There are still noise effects but solved by filter.

Other activities

• Participate beam test at Gyeongju.
  (Minjung Kim, Hyesun Bang)
  - Beam test setup.
  - Data taking shift.

• HIC OB module assembly training
  during end of Feb. (Jonghan park,
  Hyesun Bang)
  - How to make OB HIC module.
  - Module test.

Summary and outlook

- Performed the chip characterization test for ALPIDE.
  - Noise injection study.
    - External signal amplitude dependence study and back-bias voltage dependence study.
    - Studied the noise ratio with changing external signal frequency.
    - Noise ratio is increased with increasing external signal amplitude.
    - For V_{BB}=0V, the sensitive region is different with 0Ω terminator from other cases.
    - The sensitive region is changed by additional signal which flows on back-bias voltage line.
    - The noise effects was solved by filter.
- Participated beam test for ALPIDE at Gyeongju.
- Participated OB HIC module assembly training.
- Inha and PNU are preparing the MCT and OB HIC module assembly.