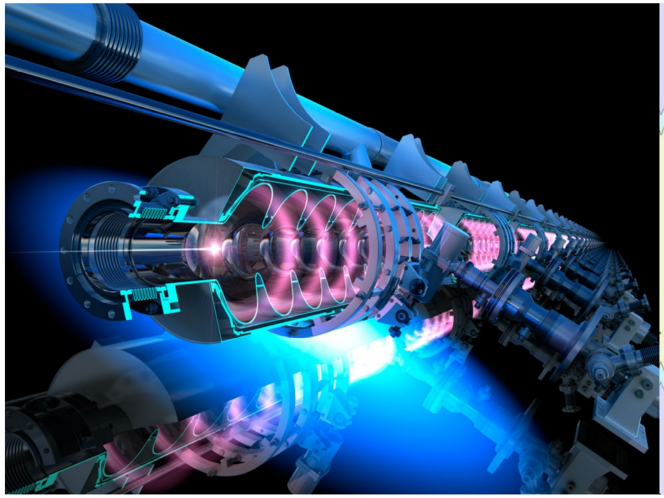
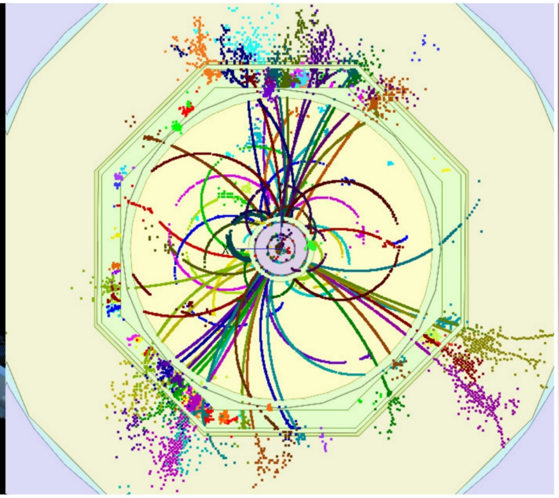
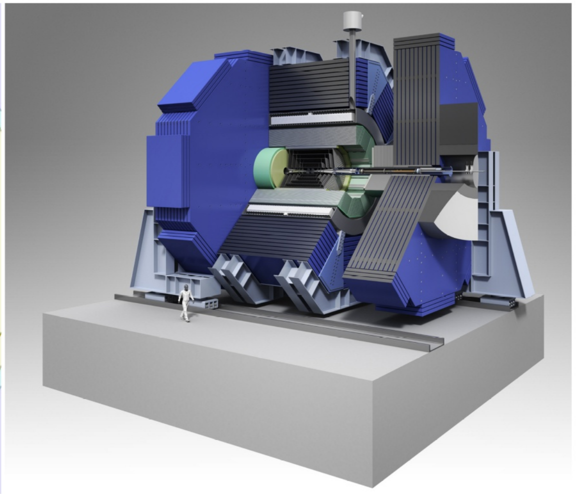
# ILC Detector Designs

## Overview, Status & Perspectives

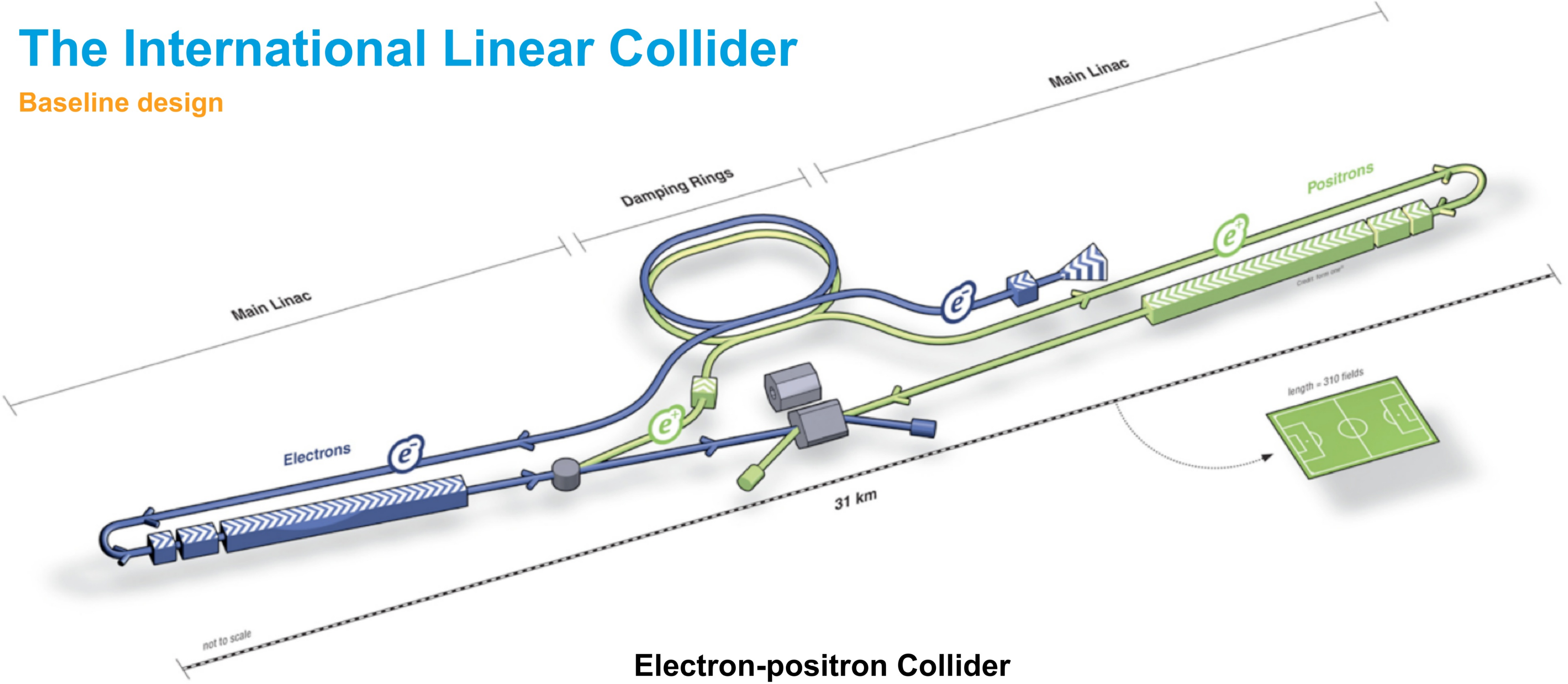




Marcel Stanitzki
LCUK 18/September/2020

# Introduction

# The International Linear Collider

## Baseline design




### Electron-positron Collider

- Center-of-mass energy 250 GeV (Higgs factory)
  Extendable to higher energies (1 TeV)
- Based on superconducting RF niobium cavities
- Polarized beams
- One interaction region, two detectors

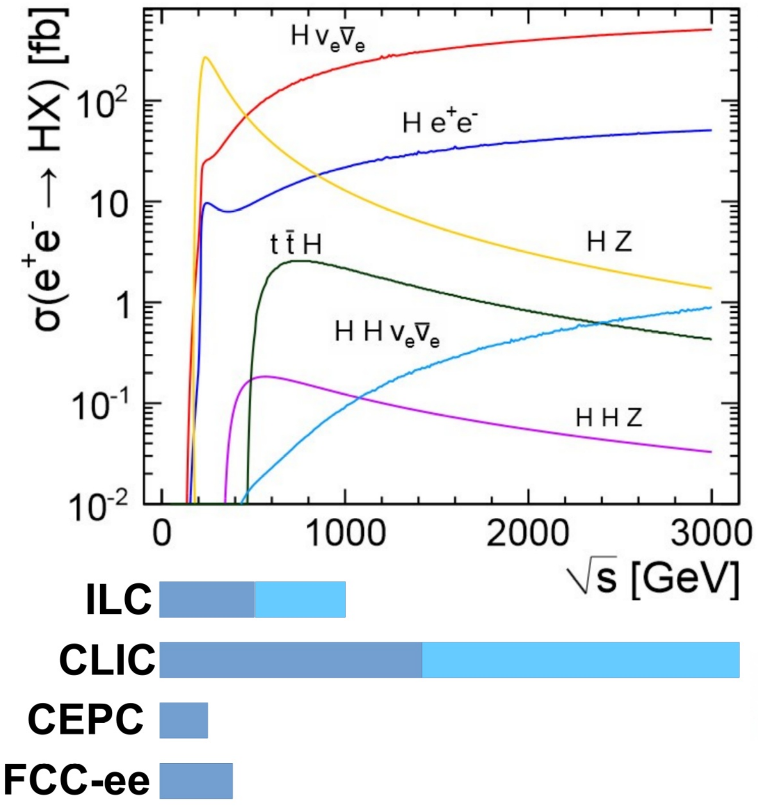
# The ILC Physics Case

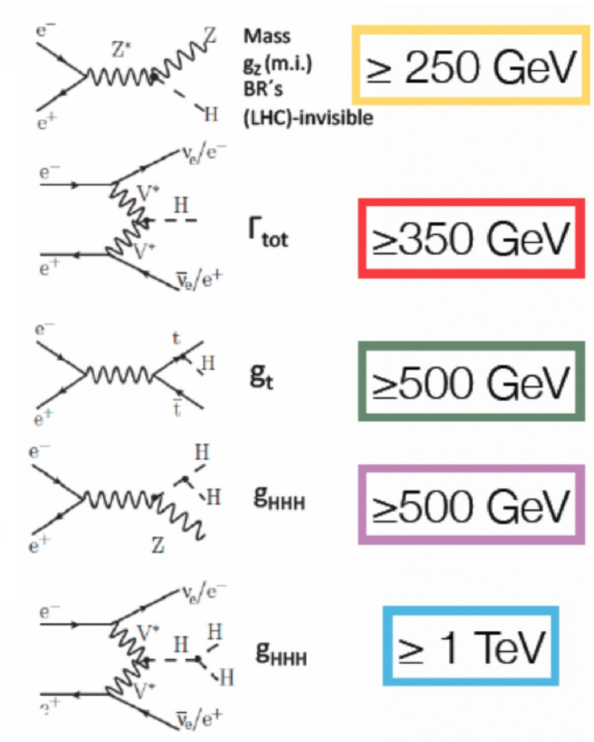
## Higgs, Top, BSM

**ILC: a rich physics program @ 250Gev - 1TeV**
Higgs precision physics, top-quark physics, physics beyond the standard model

**Discovery of a Higgs boson in 2012**
Higgs as new window into physics beyond the Standard Model

**So far absence of new physics at the LHC**
➔ precision is key to BSM physics; deviations of e.g. SM Higgs couplings are O(%)



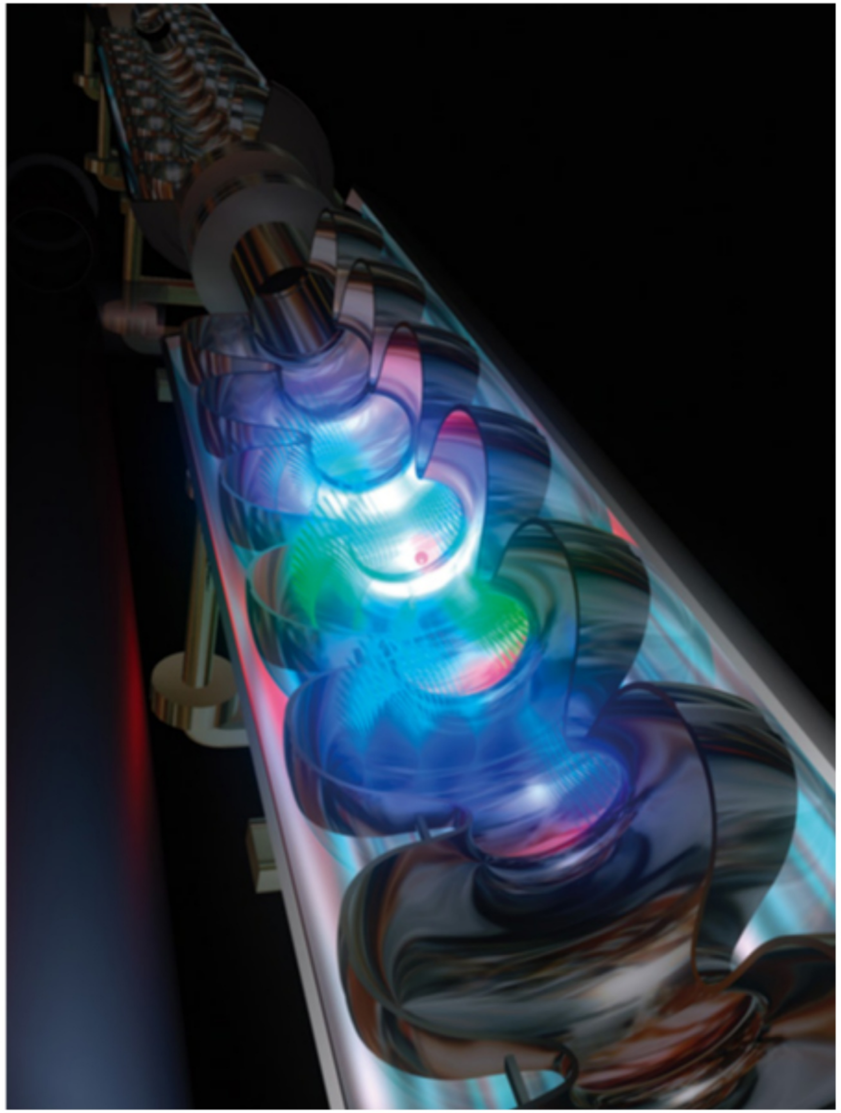




**The ILC is a Higgs factory at all energies!**
At 250 GeV: Very clean and easy to reconstruct HZ final state. Precision access to many Higgs properties

# ILC Machine Parameters - Reminder

## Baseline Configuration

| Quantity | Unit | ILC250 | ILC500 | ILC1000 |
|---|---|---|---|---|
| Centre-of-mass energy | GeV | 250 | 500 | 1000 |
| Luminosity | $10^{34}cm^{-2}s^{-1}$ | 1.35 | 1.8 | 4.9 |
| Repetition frequency | Hz | 5 | 5 | 4 |
| Bunches per pulse | 1 | 1312 | 1312 | 2450 |
| Bunch population | $10^{10}$ e- | 2 | 2 | 1.74 |
| Linac bunch interval | ns | 554 | 554 | 366 |
| Beam current in pulse | mA | 5.8 | 5.8 | 7.6 |
| Beam pulse duration | s | 727 | 727 | 897 |
| Average beam power | MW | 5.3 | 10.5 | 27.2 |
| Norm. hor. emitt. at IP | μm | 5 | 10 | 10 |
| Norm. vert. emitt. at IP | nm | 35 | 35 | 35 |
| RMS hor. beam size at IP | nm | 516 | 474 | 335 |
| RMS vert. beam size at IP | nm | 7.7 | 5.9 | 2.7 |
| Site AC power | MW | 129 | 163 | 300 |
| Site length | km | 20.5 | 31 | 40 |



**Luminosity Upgrades by doubling the number of bunches**

# Extendability built-in

## Going fom 250 GeV to 1 TeV

### ILC Site & Infrastructure

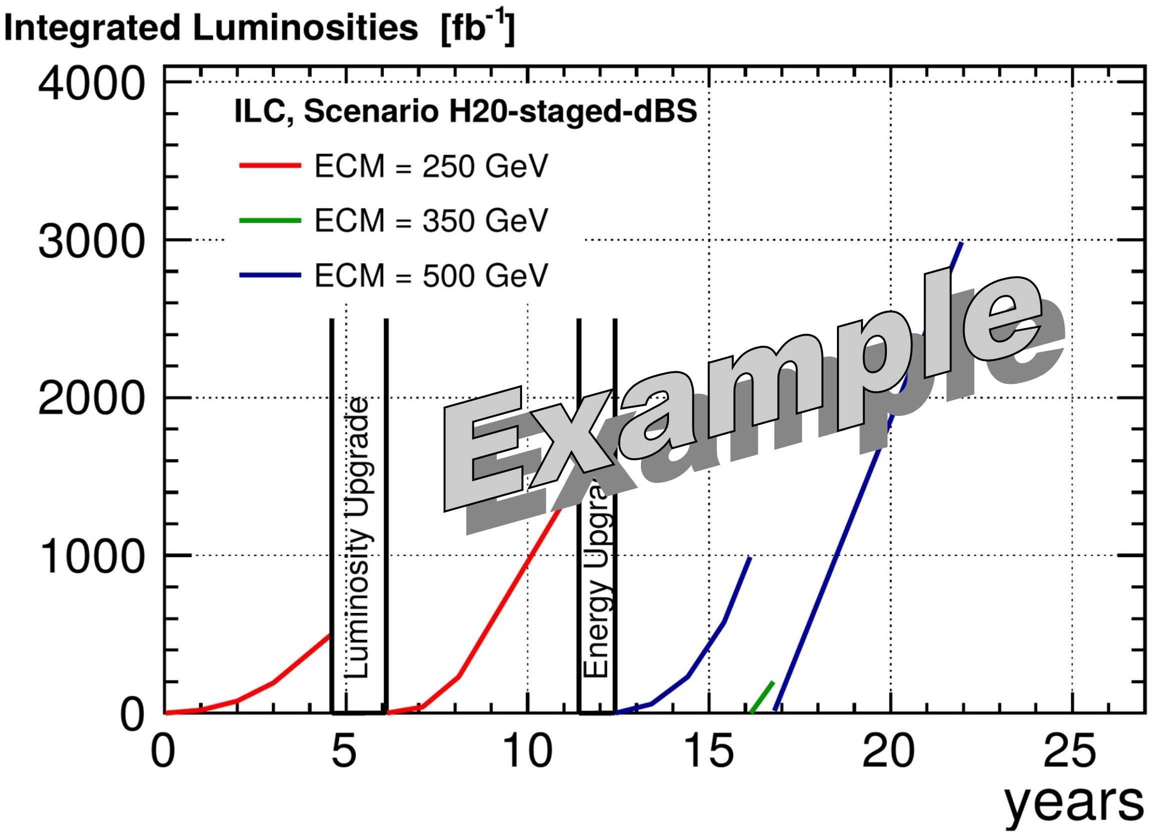
- 67 km maximal length of tunnel
- Beam dumps, etc designed for 1 TeV operation
- Overall recommended ILC power limit for the 1 TeV ILC : 300 MW

### Luminosity upgrades

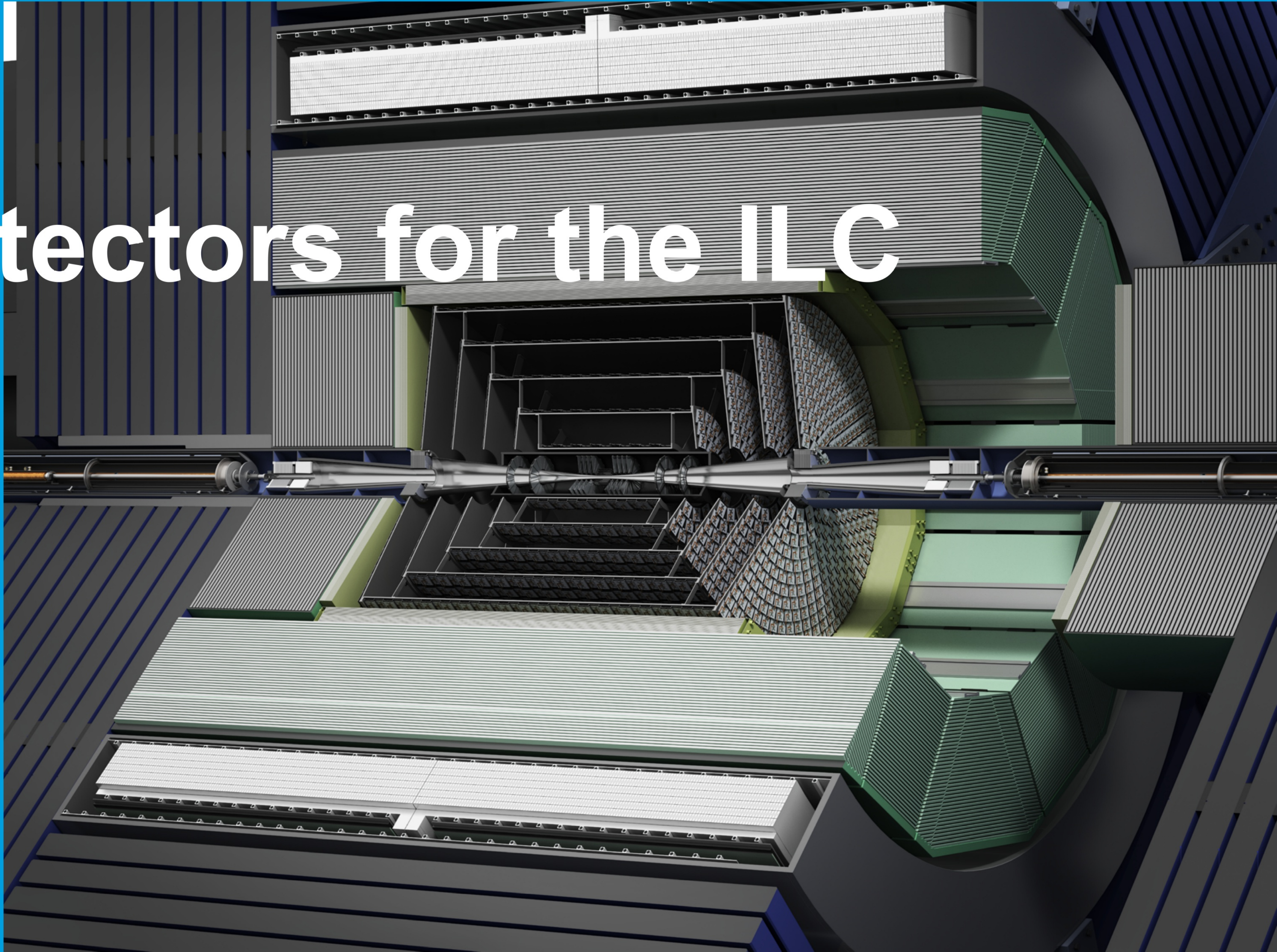
- Straightforward: Increasing the number of bunches from 1312 to 2624
- Power Increase 129 MW → 164 MW

### Energy upgrades

- Energy upgrades to 350 GeV ($t\bar{t}$ threshold) and ~500 GeV being discussed
- 1 TeV for longer-term plan



# The Detectors for the ILC

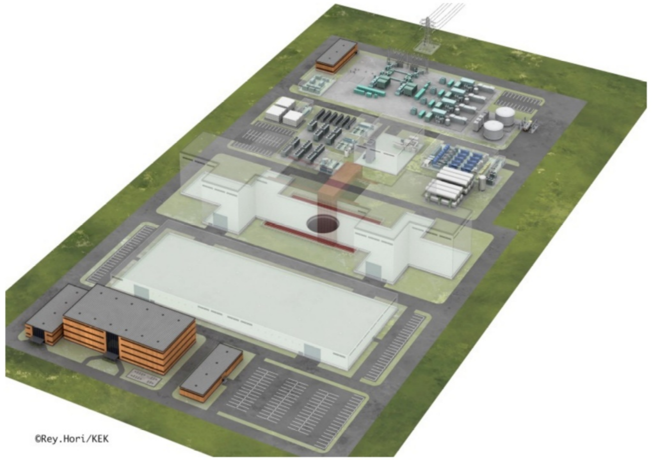


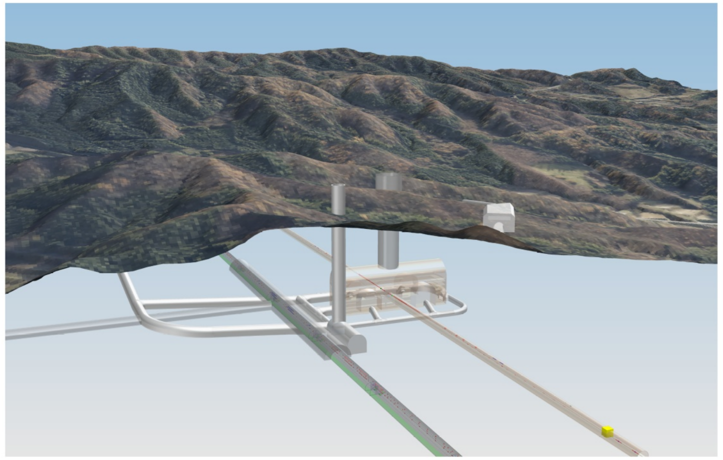
# ILC Interaction Region

## Kitakami Mountain

### Interaction Region Campus

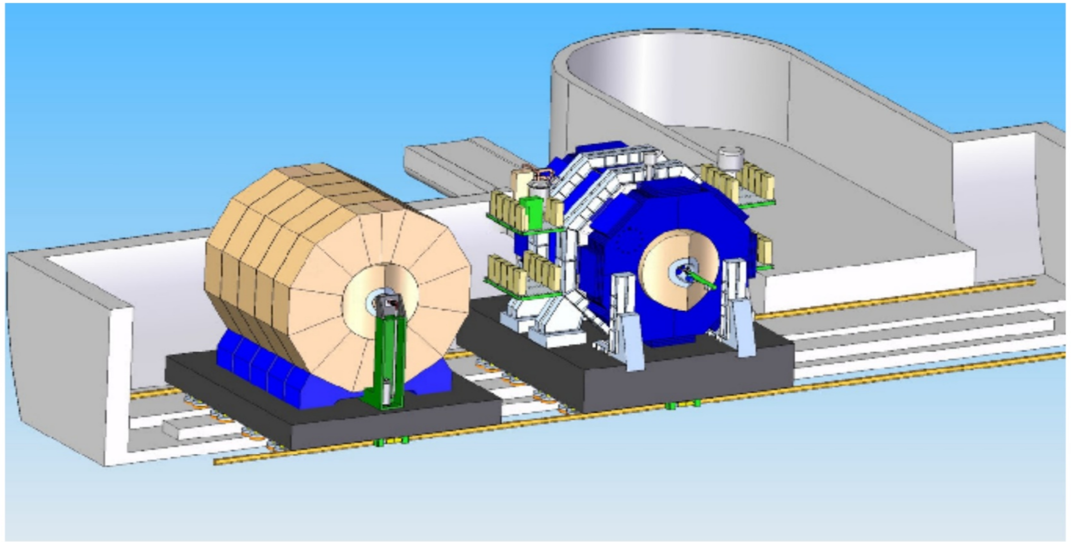
- Campus located in the Kitakami mountains
- Assembly hall, service buildings
- Access to IP using vertical shafts



### 1 IP - 2 Detectors

- The ILC has only one interaction region
- Two detectors share the IP in a push-pull configuration
  - Detectors on platforms
  - Swap-over in 48-72 hours

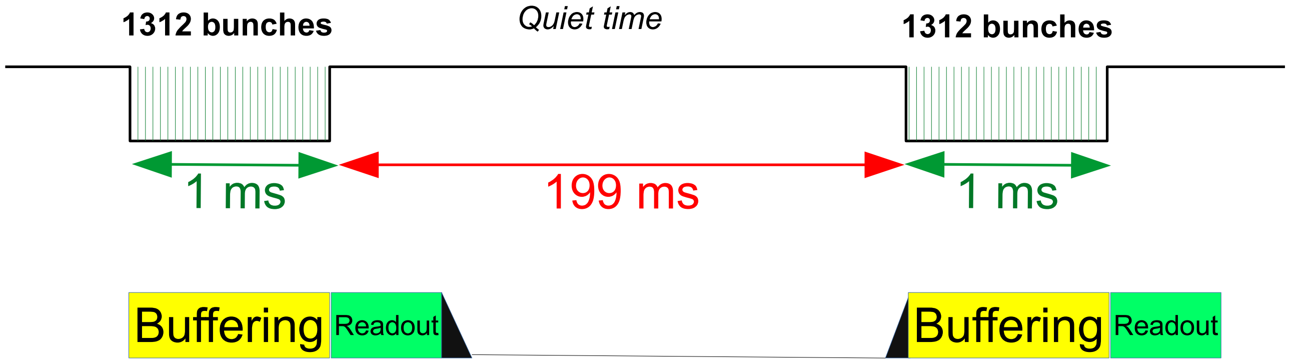


# ILC Bunch Train Structure

## Bunches, Bunch trains & Power Pulsing

### ILC Timing

- Bunch Structure at the ILC is very different compared to a synchrotron e.g. LHC
  - Bunch spacing of 554 ns
  - 1 Train has 1312 bunches in ~ 1 ms
  - Then 199 ms quiet time until the next train
- Huge Impact on the Detector design
  - Occupancy dominated by beam background & noise
  - Trigger-less Readout
  - Buffering on front-end &Readout after the last bunch
  - Powering off the front-ends during the quiet time
  - Power saving of a Factor 100 → No Active cooling



# Particle Flow Paradigm

## Driver for ILC Detector Design

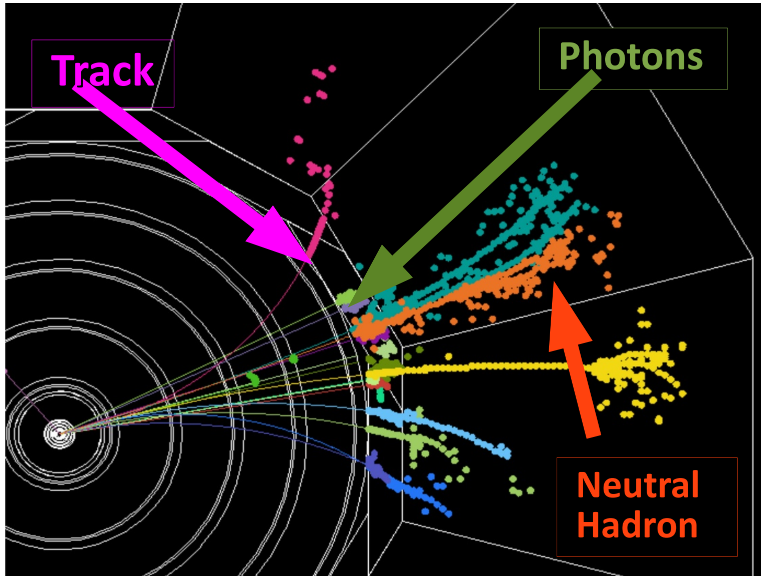
### Particle Flow Algorithms

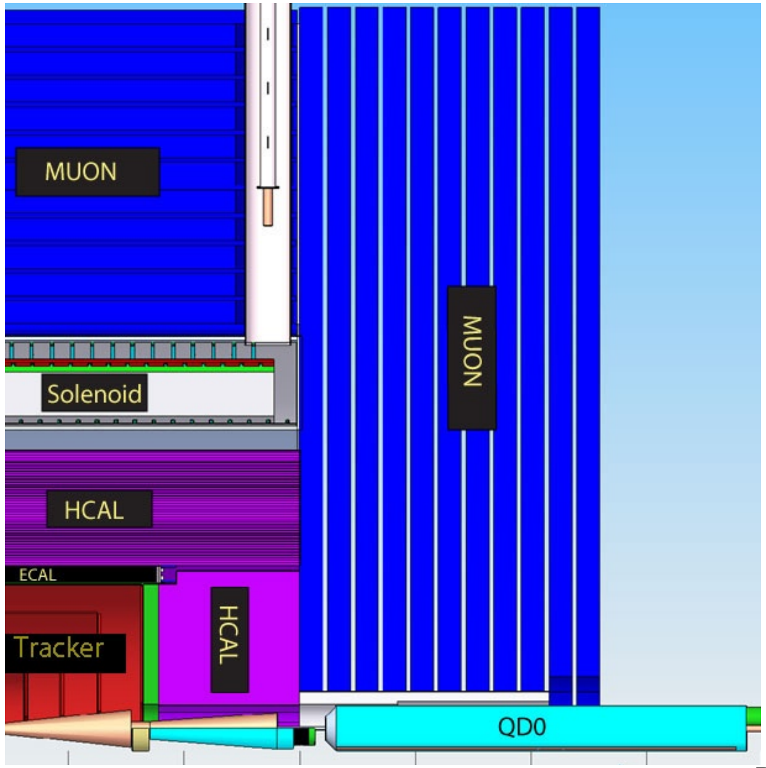
- PFA has been used before at LEP, HERA and LHC
- Novel Approach at the ILC→ PFA drives design of the detector

### Impact on the detector design

- Highly granular calorimetry
- Low-mass tracking
- Calorimetry inside the superconducting solenoid

**The combination of these requirements already exclude certain technological options**



# Detector Requirements

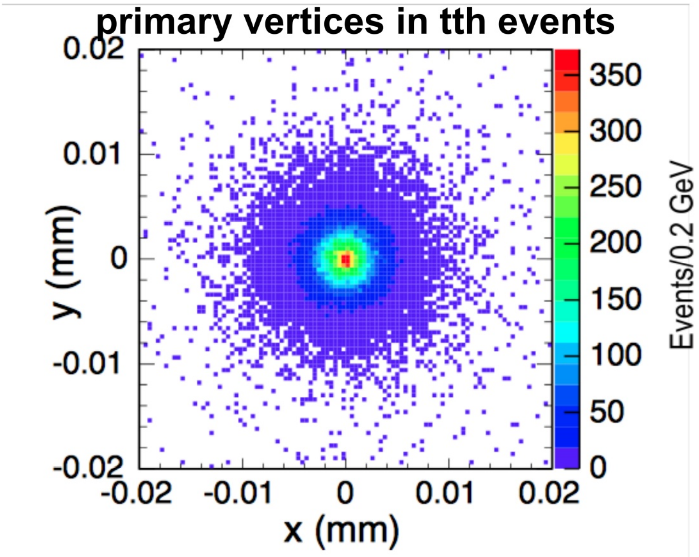
## ILC requires precision detectors

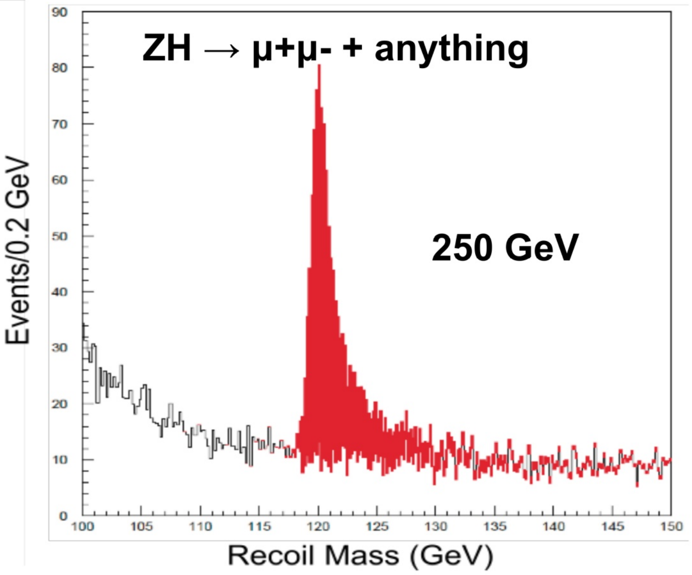
### ILC detector design cornerstones

- Particle Flow
- Power Pulsing

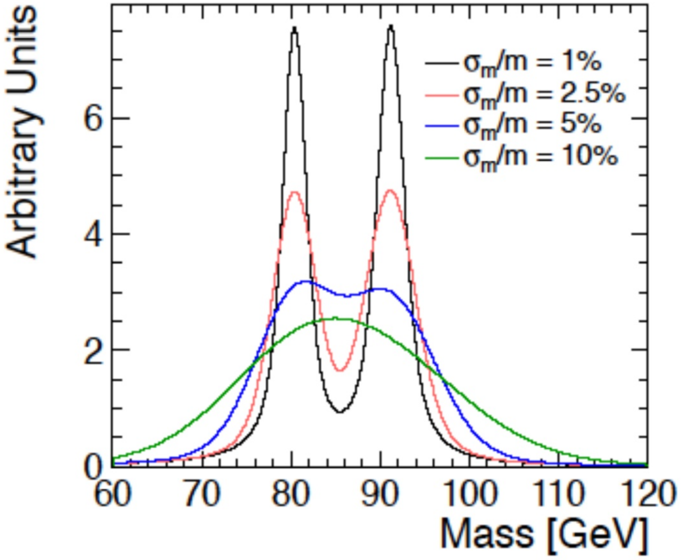
### Performance Requirements

- Time stamping
  - Single Bunch resolution
- Vertex detector
  - < 4 μm precision
  - $\sigma_{r\phi} \approx 5 \ \mu m \oplus 10 \ \mu m / p \sin^{\left(\frac{3}{2}\right)}(\theta)$
- Tracker
  - $\sigma(1/p) \sim 2.5 \times 10^{-5}$
- Calorimeter
  - $\frac{\sigma_{E_{Jet}}}{E_{Jet}} = 3-4\%, E_{Jet} > 100 \ GeV$



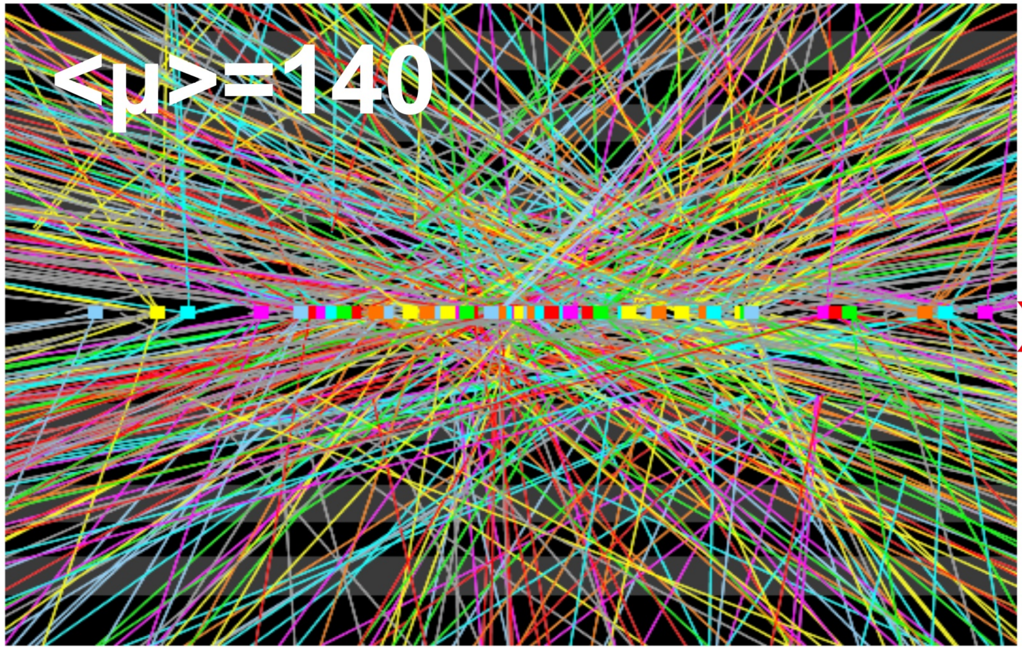



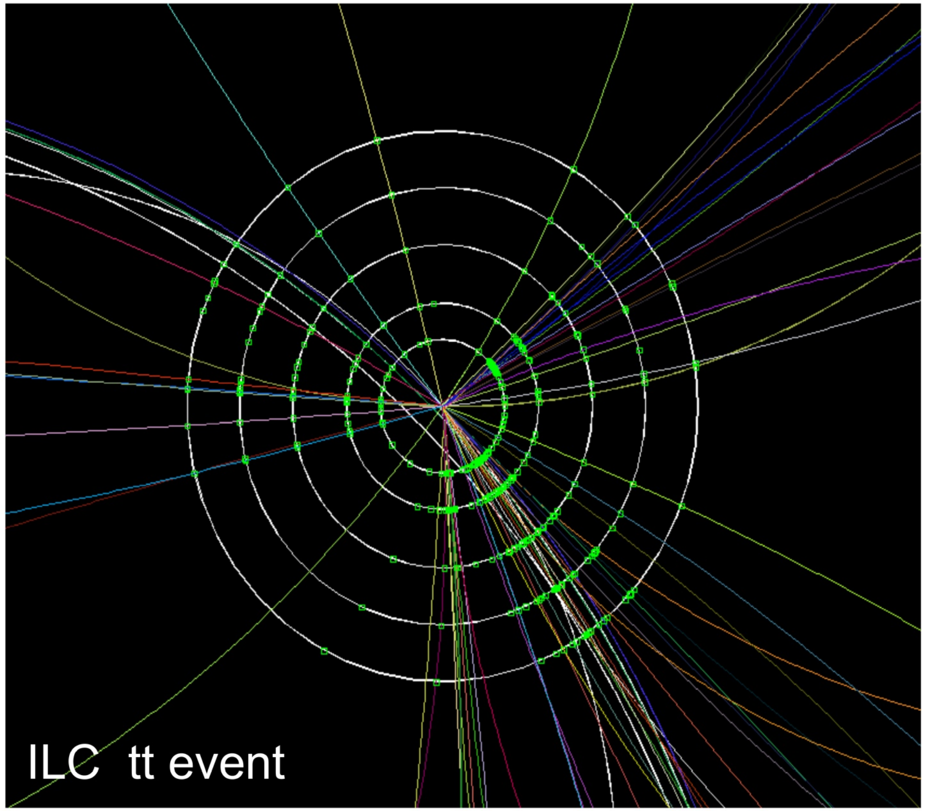

W-Z separation



# A bit of perspective – Going from HL-LHC to ILC

## It's a different ball game




Moving from 140 interactions per crossing to ~1 event/train

# Reducing the Material

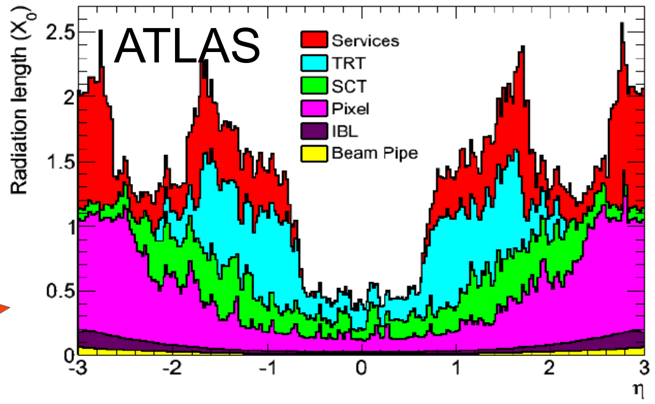
## From HL-LHC to ILC

### The HL-LHC

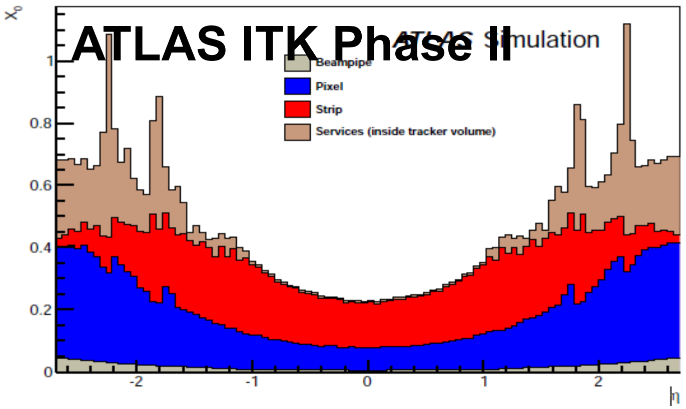
- Lots of work on power distribution, cooling, material

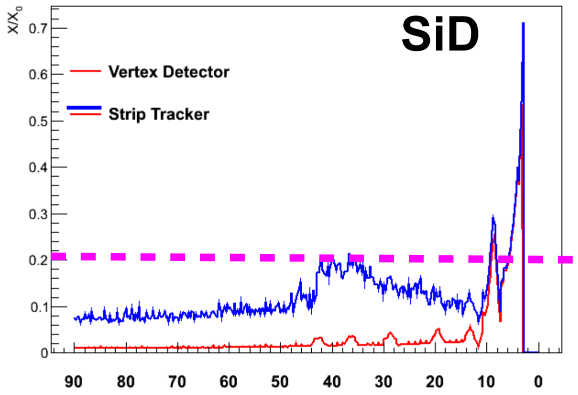
### For an ILC detector

- No cooling at -30 due to radiation damage
- Power pulsing reduced power consumption by a factor O(100)
- Moving to air-cooling ...




R&D on Services, Mechanics, Cooling



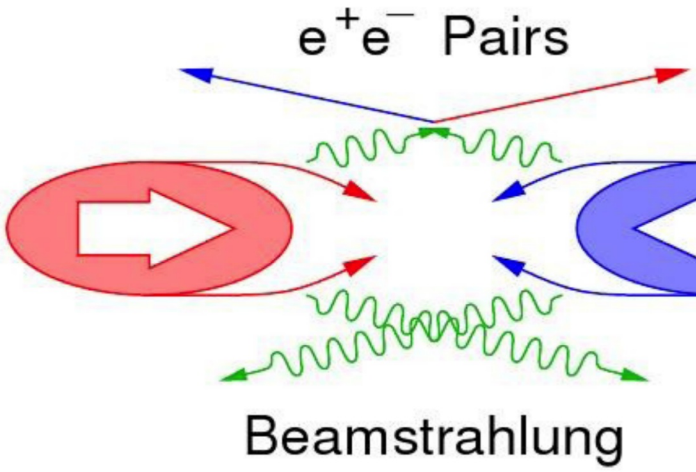



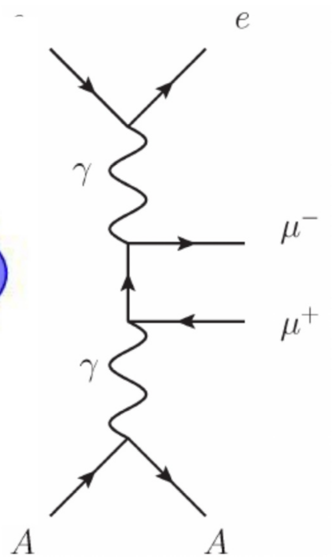

Power pulsing Air cooling

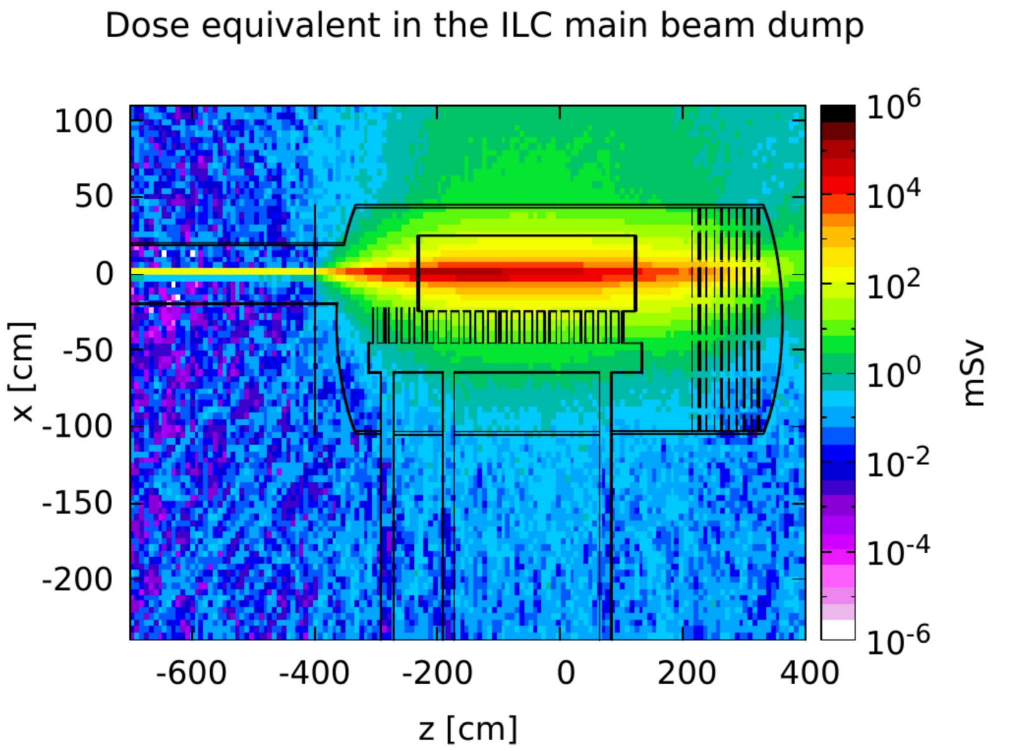
# ILC Backgrounds and Impact

## From beamstrahlung to neutrons

- e+e- Pairs
  - Caused by beam beam interactions
  - High cross-section
- Muons from the spoilers
  - Interaction of beam halo with final focus system
- Neutrons from the the main beam dump
  - At the ILC the dump is a really hot object
- Performance
  - The closer to the IP, the better your tagging ...
- Radiation damage
  - It's not an LHC-scale problem
  - But needs to be understood and comes with certain trade-offs



# SiD and ILD

## Detector concepts for the ILC

**Common Aspects**

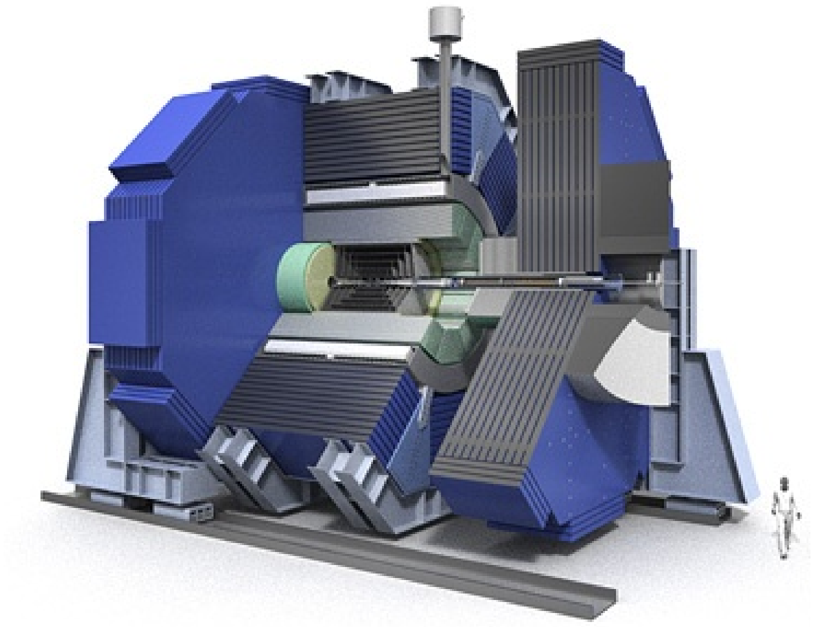
- Designed for Particle Flow
- Highly granular calorimetry
- Designed for easy Push-Pull operation

**SiD**

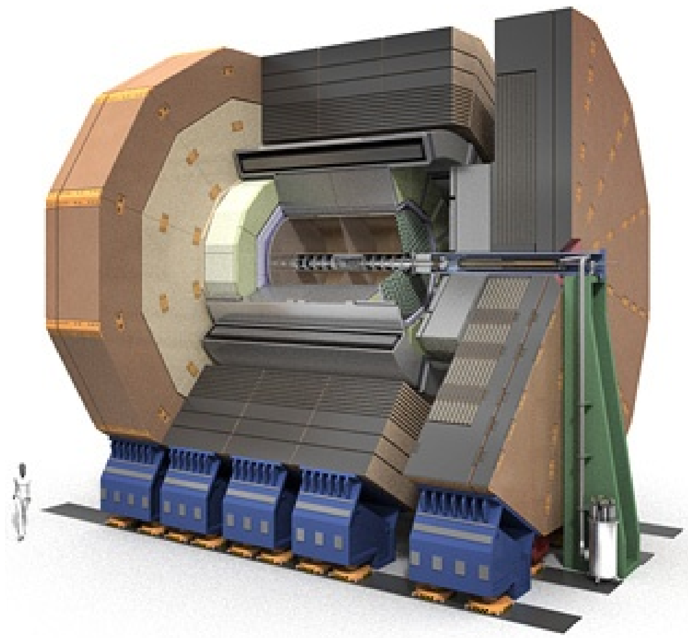
- Compact high-field design
- All-Silicon tracking
- B Field 5 T, $r_{ECAL}$=1.25 m

**ILD**

- Large medium-field design
- TPC as main tracking device
- B Field 3.5 T, $r_{ECAL}$=1.7 m



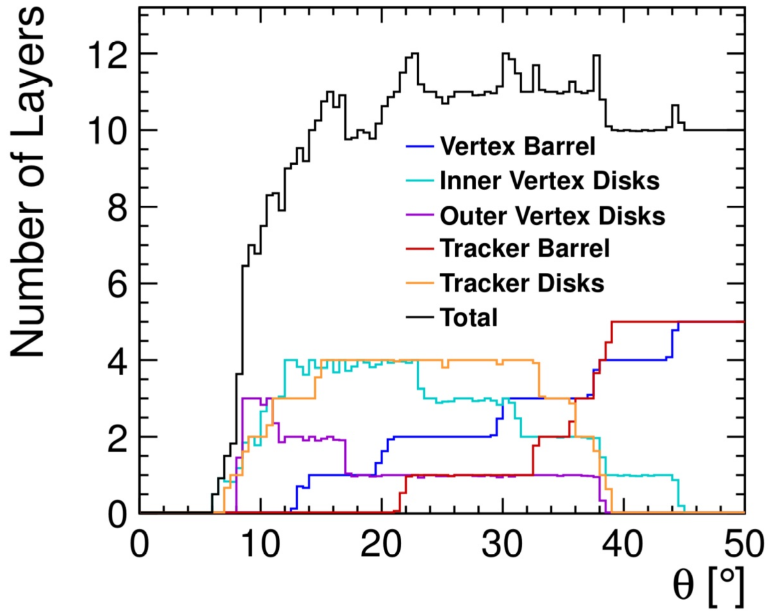
SiD

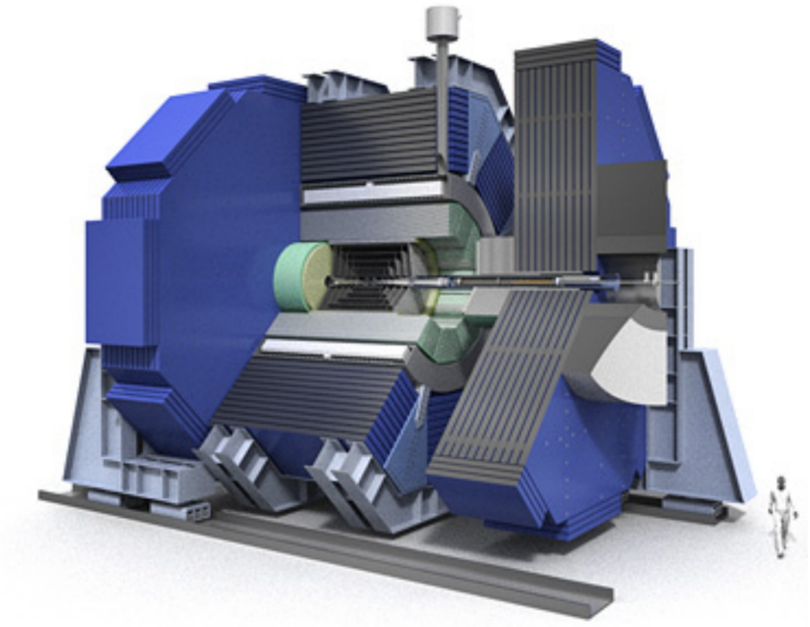


ILD

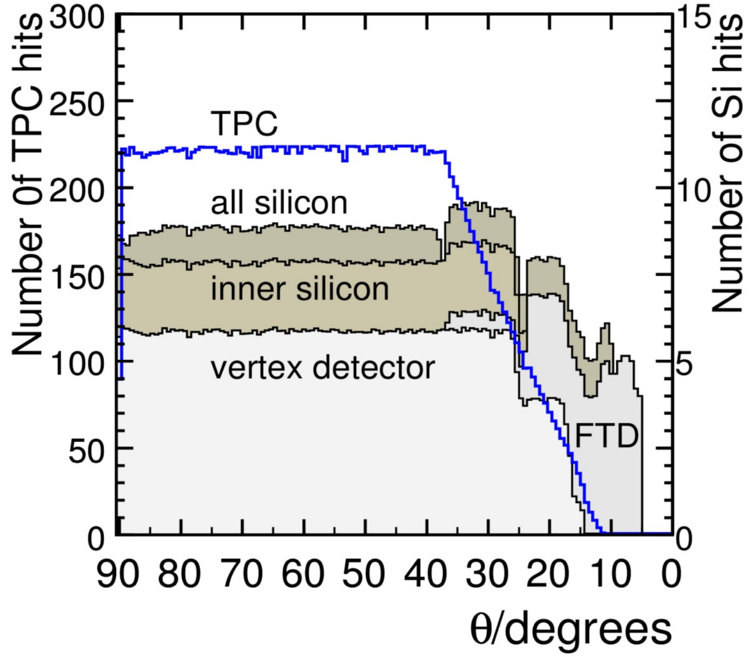
# SiD and ILD

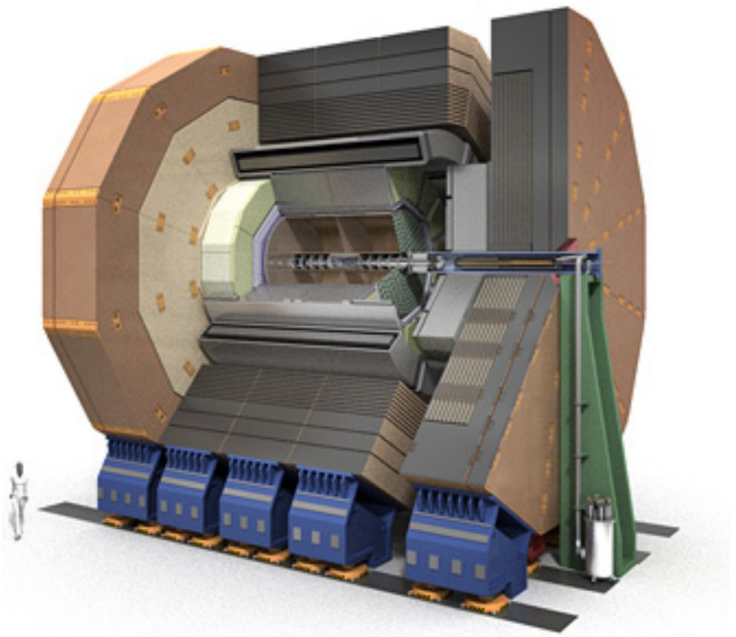
## Differences



SiD

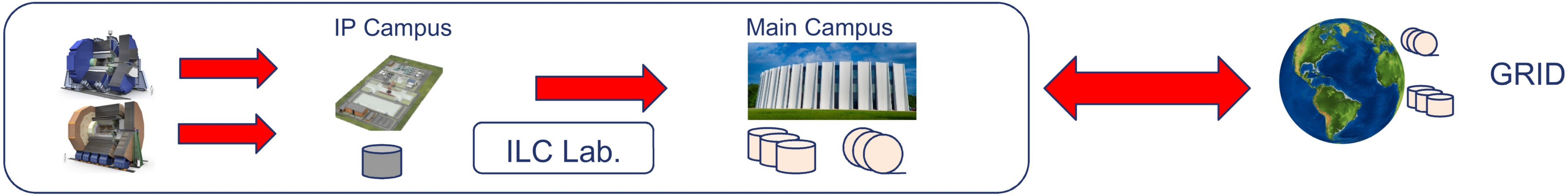


ILD

# ILC Computing

## Overall Concept




**Role of each facility**

IP Campus: Event building & Monitoring

- Main Campus: Data storage, Event(BX) selection,
- GRID Computing: Data Analysis &Simulation

**Challenges**

- Trigger less readout. O(1000) BXs per 1 train of 5 Hz.
- Efficient event selection using full reconstruction
- GRID infrastructure for data and CPU sharing

**Resource Requirements**

- Raw data rate ~ 1.5GB/s. Annually 10~15 PB
- CPU : 200 ~ 300kHepSpec06 for simulation, reconstruction and analysis
- Resources ~ 1 order of magnitude less than LHC requirements

# Detector R&D for the ILC

## The LCC Detector R&D Report

Summarizing the state of detector R&D relevant for linear collider detectors

- Current version Summer 2020 (living document)

- You can download the latest version from
  - [http://www.linearcollider.org/P-D/Working-groups/Detector-R-D-liaison](http://www.linearcollider.org/P-D/Working-groups/Detector-R-D-liaison)

LINEAR COLLIDER COLLABORATION

**Detector R&D Report**

VERSION 2018.2

Editors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LINEAR COLLIDER COLLABORATION
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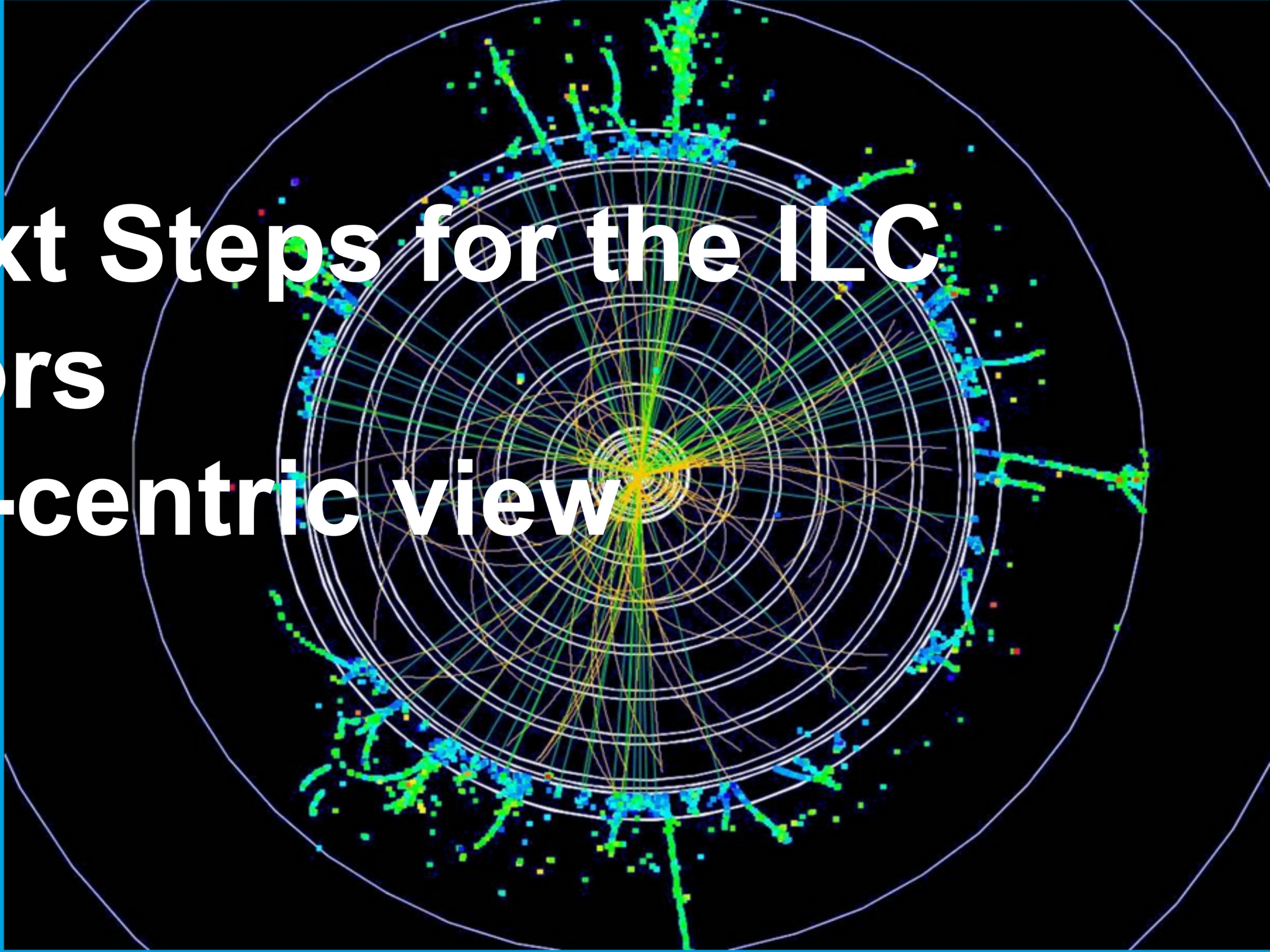
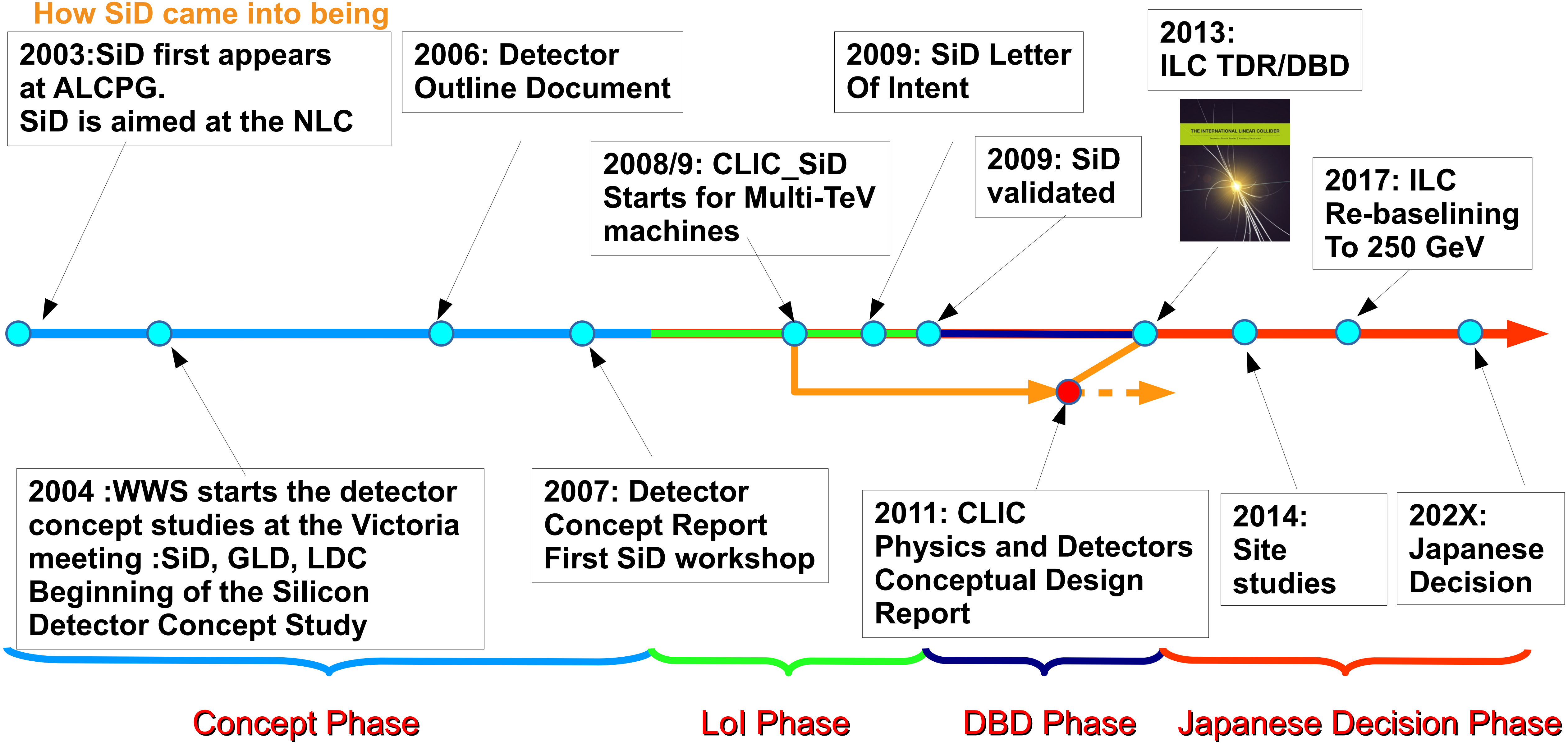
# The next Steps for the ILC detectors An SiD-centric view



# SiD – A bit of history

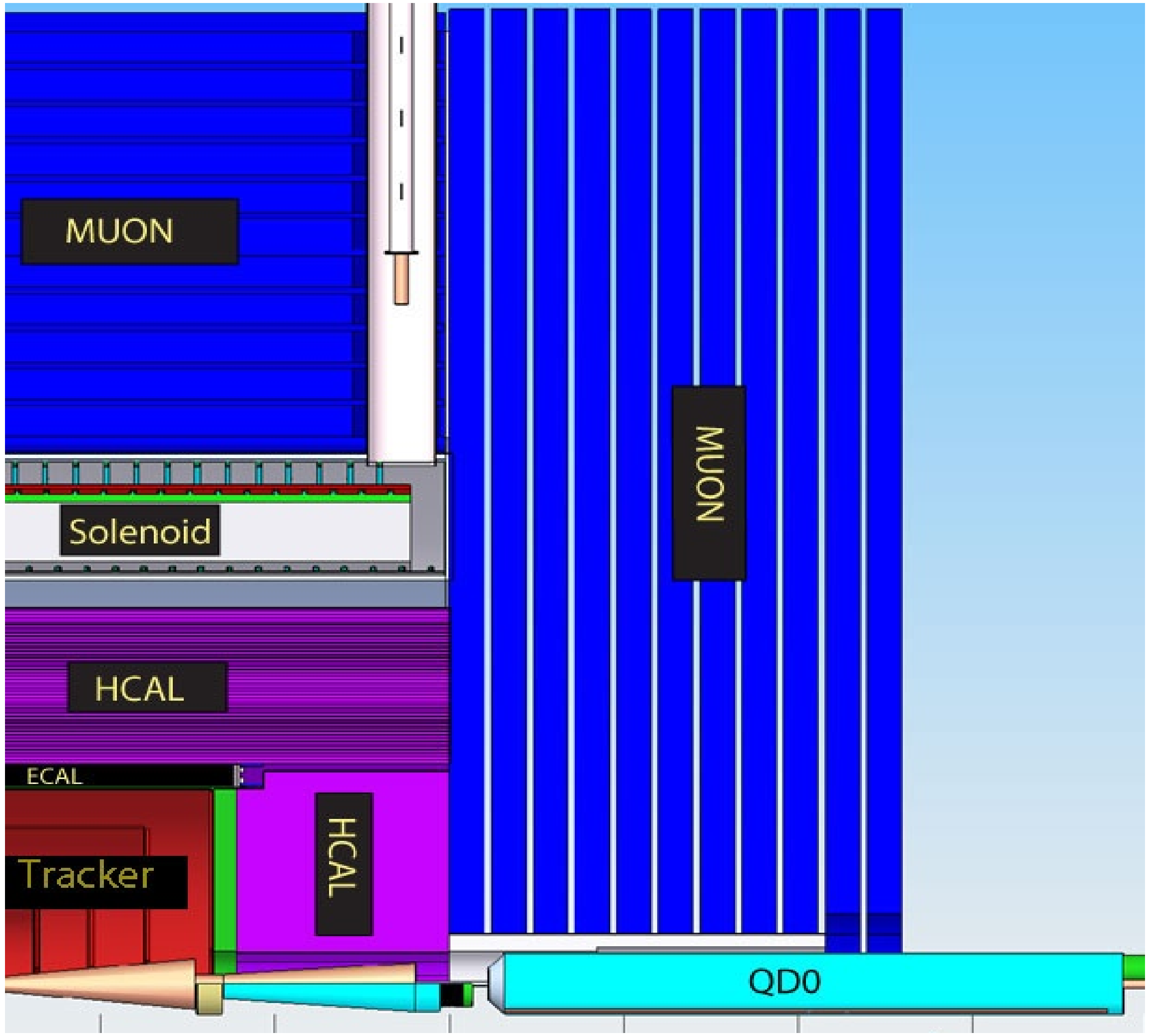
## How SiD came into being



# SiD – Compact Silicon Detector

## Baseline Technologies

- The DBD was finalized 2012/13
  - Clearly technology has made huge progress since then
  - HL-LHC as technology driver
- But overall assessment
  - Basic concept of a compact all-silicon detector is sound
  - This idea also migrated into other Higgs factories
- Decisions already taken
  - Move from DHCAL (RPC-based) to SiPM-AHCAL
- A lot of obvious points to take advantage of new technology
- And we need to get more serious about DAQ and powering schemes



# SiD – Detector design choices

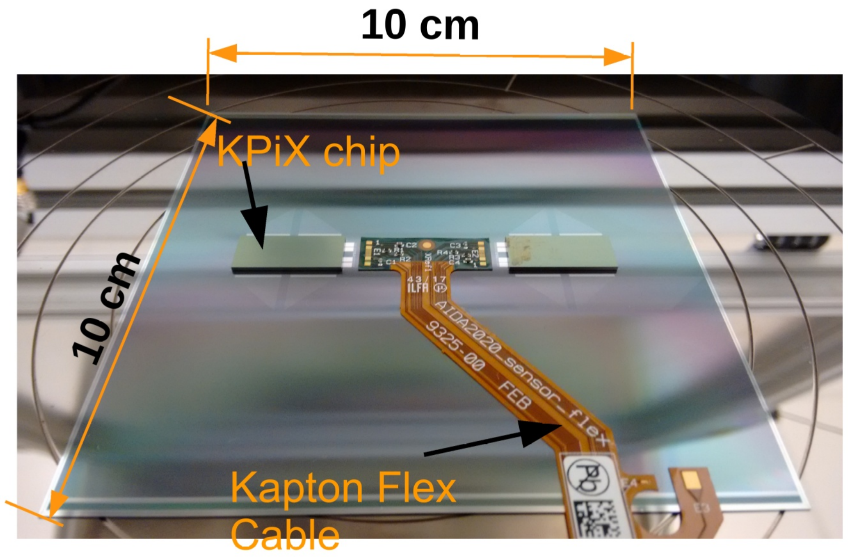
## Which we should re-visit

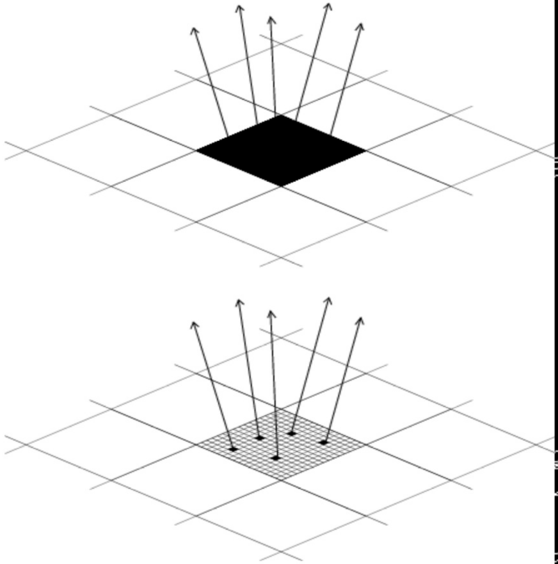
**Silicon-Strip Tracker**

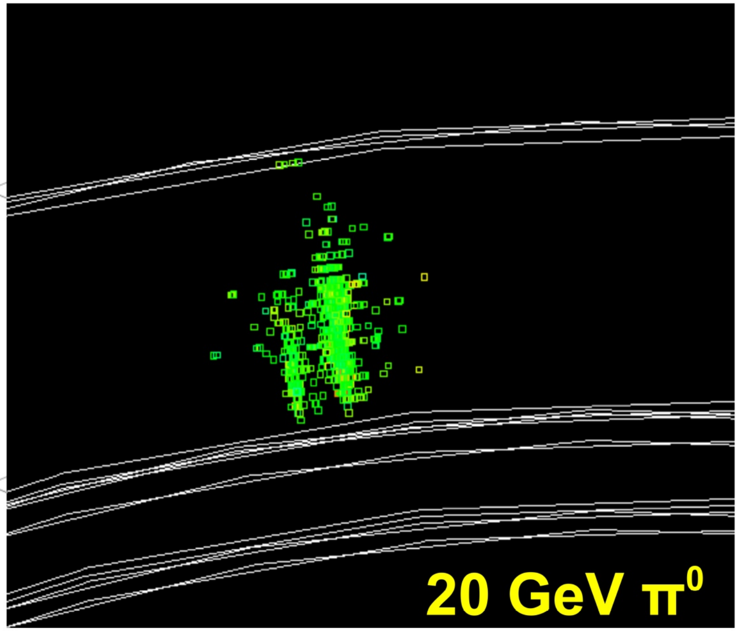
- Concepts works well
  - Demonstrated 6.2 micron resolution
- But comes with a delicate assembly process
  - Bump-bonding, gluing …
- An all-pixel solution is the obvious choice
  - Get highly precise x and y coordinate
  - Get rid of bump-bonded ASIC

**Silicon-W ECAL**

- Concepts works well – but requires again a lot of bump-bonding
- But a MAPS-based ECAL would open a lot more possibilities→ Ultimate DECAL ?



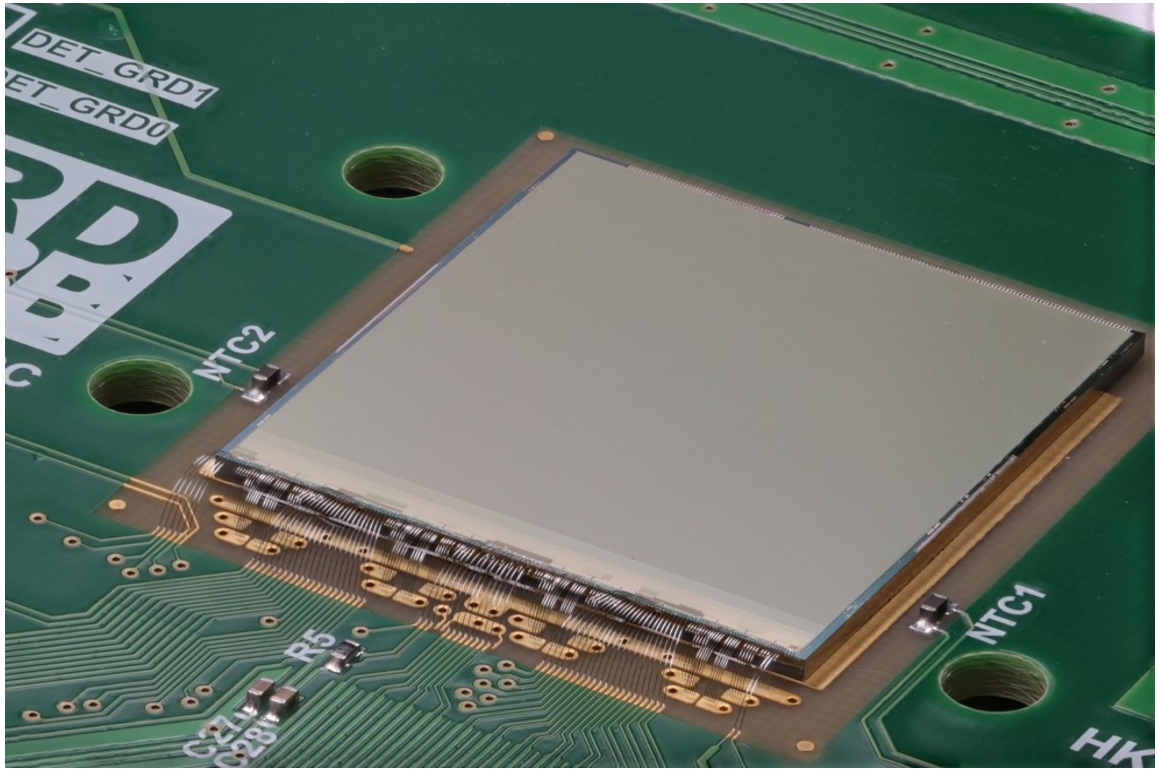





# New Technologies

## The raise of the 65 nm CMOS

- On the DBD Timescale 250 nm and 180 nm were the workhorse processes
- HL-LHC has driven use of 65 nm ASIC processes forward
  - Power savings for e.g the lpGBT high-speed link or the RD53 Pixel ASIC are compelling
  - We're talking factors of five ..
- What can this do for ILC Detectors ?
  - New ideas welcome …
- MAPS is moving along
  - ALPIDE fittingly was kind of the pinnacle of a 180 nm MAPS
  - What are the possibilities of MAPS in 65 nm ?
  - This will come exactly at the right time for ILC



# Timing, 4D and all that

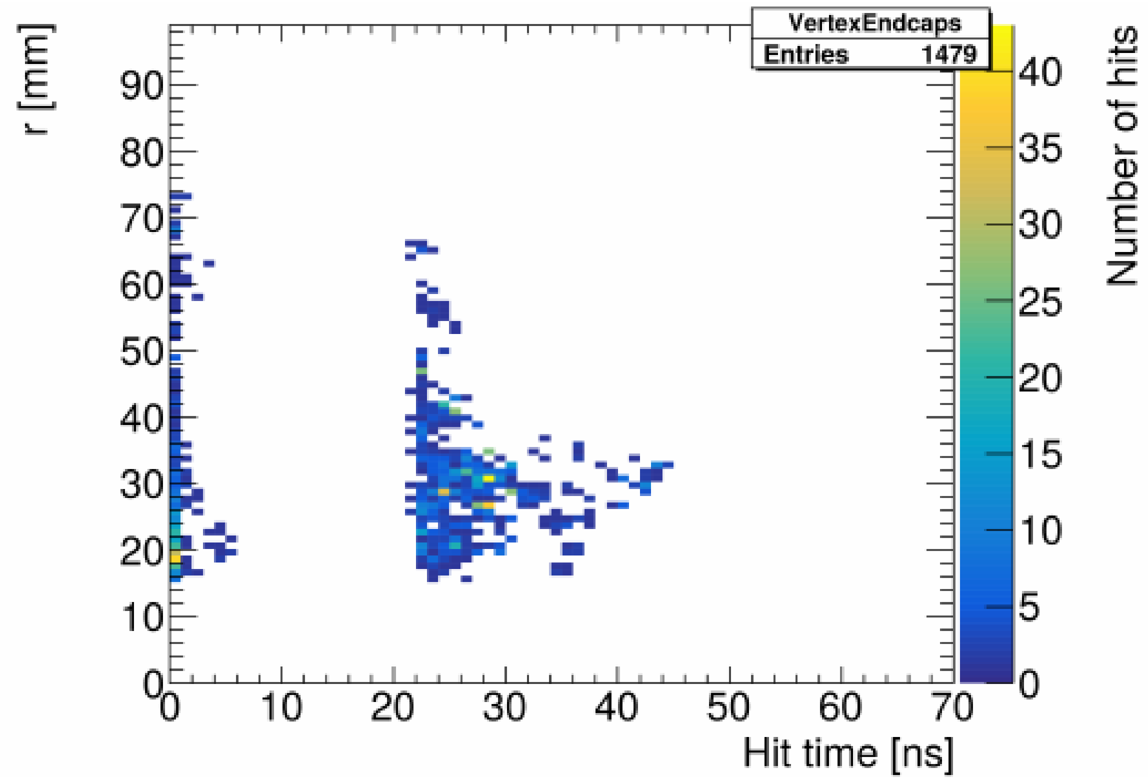
## What we really have not explored in detail

**Integrated time-stamping**

- e.g. Background rejection in the Vertex Detector and others
- ns level resolution

**Dedicated Timing Layers**

- Time-of-flight systems
- Full 4D Tracking
- Here we talking 10 ps resolution
- What can be done with LGAD, etc
- Lots of room for new ideas
  - From technology to physics impact




(b) *SiD vertex detector endcaps*

# Summary

## International Linear Collider Detectors

**The ILC is ready to go**

- Physics case well established
- Accelerator technology proven and ready
- Detector designs are very advanced

**ILC Detectors**

- There will be increased activity in the upcoming years
- Now is the ideal time to come with new ideas
- And incorporate R&D and experience from HL-LHC
- UK expertise in pixels, calorimetry and DAQ crucial and very welcome
- MDI expertise provides direct link to the accelerator activities

# Thank you